TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7WB66FK

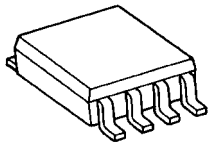
Dual Bus Switch

The TC7WB66FK is a low on-resistance, high-speed CMOS2-bit bus switch. This bus switch allows the connections or disconnections to be made with minimal propagation delay while maintaining Low power dissipation which is the feature of CMOS.

When output enable (OE) is at High level, the switch is on; when at Low level, the switch is off.

P-MOS and N-MOS channel block means the device is suitable for analog signal transmission.

All inputs are equipped with protector circuits to protect the device from static discharge.



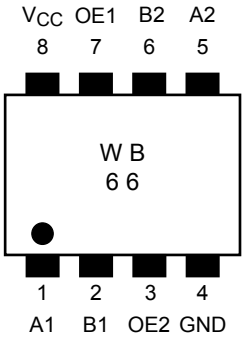
SSOP8-P-0.50A

Weight: 0.01 g (typ.)

Features

- Operating voltage: V_{CC} = 2~5.5 V
- High speed operation: t_{pd} = 0.25 ns (max)
- Ultra-low on resistance: R_{ON} = 5 Ω (typ.)
- ESD performance: Machine model ≥ ±200 V
  Human body model ≥ ±2000 V
- High noise margin: V_{NIL} = V_{NIH} = 28% V_{CC} (min)
- Power-down protection for inputs (control inputs only)
- Package: US8

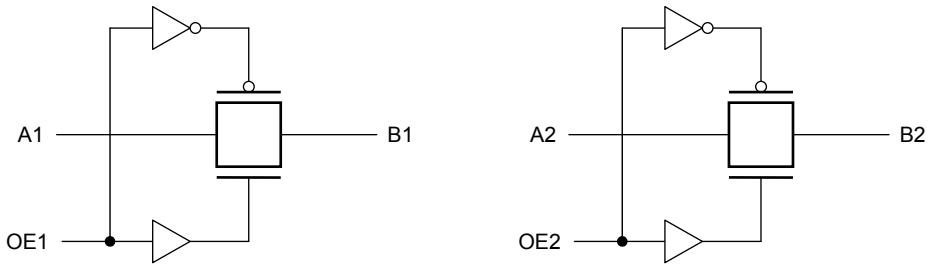
Pin Assignment (top view)



Truth Table

Inputs	Function
OE	
H	A port = B port
L	Disconnect

System Diagram



Absolute Maximum Ratings (Note)

Characteristics		Symbol	Rating	Unit
Power supply voltage		V_{CC}	−0.5~7.0	V
Control pin input voltage		V_{IN}	−0.5~7.0	V
Switch terminal I/O voltage		V_S	−0.5~V_{CC} + 0.5	V
Clump diode current	Control input pin	I_{IK}	−50	mA
	Switch terminal		±50	
Switch I/O current		I_S	128	mA
Power dissipation		P_D	200	mW
DC V_{CC}/GND current		I_{CC}/I_{GND}	±100	mA
Storage temperature		T_{stg}	−65~150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	2.0~5.5	V
Control pin input voltage	V_{IN}	0~5.5	V
Switch I/O voltage	V_S	0~V_{CC}	V
Operating temperature	T_{opr}	−40~85	°C
Control pin input rise/fall time	dt/dv	0~10	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics (Ta = –40~85°C)

Characteristics		Symbol	Test Condition	V_{CC} (V)	Min	Typ. (Note 1)	Max	Unit
Control pin input voltage	"H" level	V_{IH}	—	2.0~5.5	0.7 × V_{CC}	—	—	V
	"L" level	V_{IL}	—	2.0~5.5	—	—	0.3 × V_{CC}	
Control pin input leakage current		I_{IN}	V_{IN} = 0~5.5 V	2.0~5.5	—	—	±1.0	μA
Off-state leakage current (switch off)		I_{SZ}	A, B = 0~V_{CC}, OE = GND	2.0~5.5	—	—	±1.0	μA
ON resistance (Note 2)		R_{ON}	V_{IS} = 0 V, I_{IS} = 30 mA	4.5	—	3	7	Ω
			V_{IS} = 4.5 V, I_{IS} = 30 mA	4.5	—	5	15	
			V_{IS} = 2.4 V, I_{IS} = 15 mA	4.5	—	6	12	
			V_{IS} = 0 V, I_{IS} = 24 mA	3.0	—	4	9	
			V_{IS} = 3 V, I_{IS} = 24 mA	3.0	—	7	20	
			V_{IS} = 0 V, I_{IS} = 8 mA	2.0	—	6	12	
			V_{IS} = 2 V, I_{IS} = 8 mA	2.0	—	10	30	
Quiescent supply current		I_{CC}	V_{IN} = V_{CC} or GND, I_{OUT} = 0	5.5	—	—	10	μA

Note 1: The typical values are at Ta = 25°C.

Note 2: Apply the specified current to the switch, then measure the voltages on pins A and B. The on-resistance is the lower of the two.

AC Characteristics (Ta = –40~85°C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit
Propagation delay time (bus to bus)	t_{pLH} t_{pHL}	Figure 1, Figure 2 (Note)	2.0	—	0.5	ns
			3.3 ± 0.3	—	0.35	
			5.0 ± 0.5	—	0.25	
Output enable time	t_{pZL} t_{pZH}	Figure 1, Figure 3	2.0	—	11.5	ns
			3.3 ± 0.3	—	6	
			5.0 ± 0.5	—	4.5	
Output disable time	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	2.0	—	11.5	ns
			3.3 ± 0.3	—	6.5	
			5.0 ± 0.5	—	5	

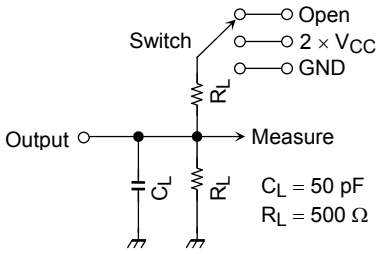
Note: The propagation delay time is calculated by the RC (on-resistance and load capacitance) time constant.

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Unit
Control pin input capacitance	C_{IN}	(Note)	5.0	3	pF
Switch terminal capacitance	$C_{I/O}$	OE = GND (Note)	5.0	10	pF

Note: Guaranteed by design.

AC Test Circuit



Parameter	Switch
t_{pLH}, t_{pHL}	Open
t_{pLZ}, t_{pZL}	2 × V_{CC}
t_{pHZ}, t_{pZH}	GND

Figure 1

AC Waveform

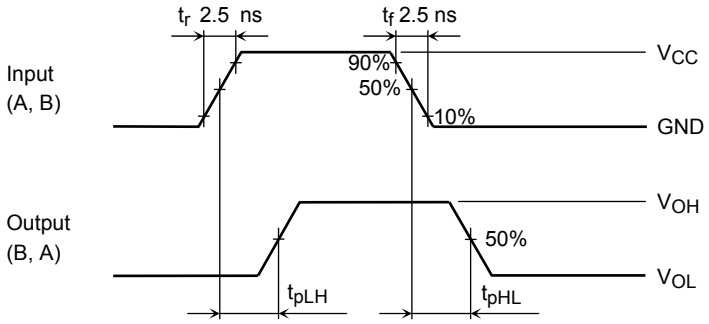


Figure 2 t_{pLH}, t_{pHL}

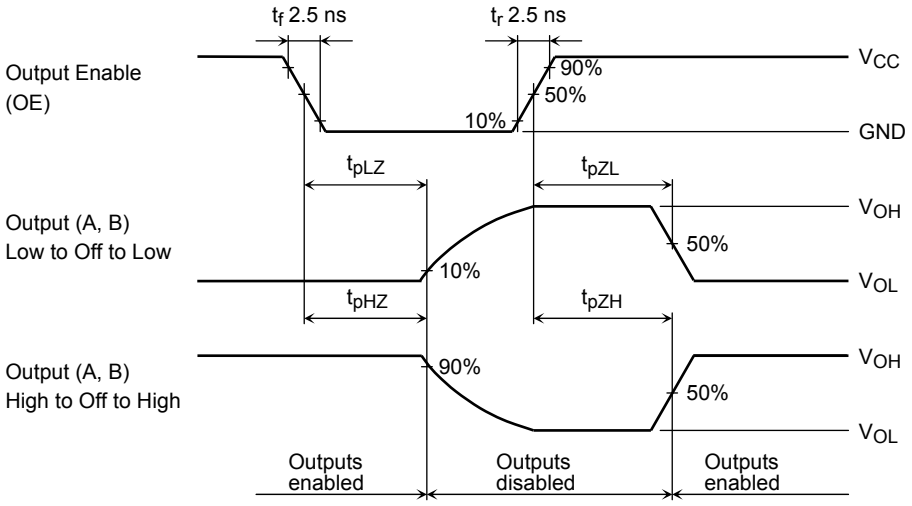
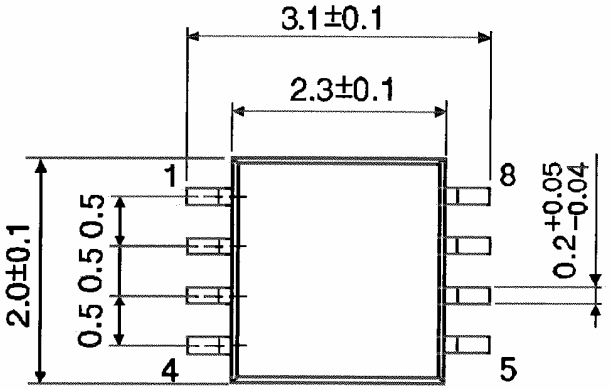
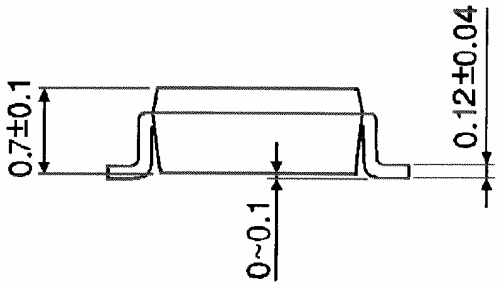


Figure 3 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

Package Dimensions

SSOP8-P-0.50A Unit : mm





Weight: 0.01 g (typ.)

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20070701-EN GENERAL

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