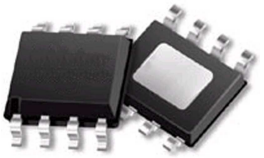
Preliminary

# SPA-2318

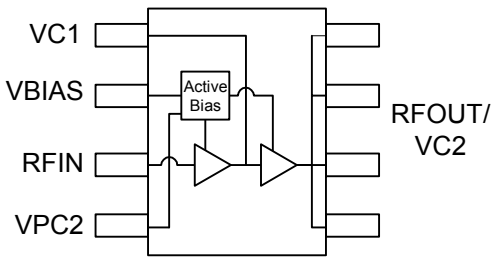
## 2150 MHz 1 Watt Power Amplifier with Active Bias



## Product Description

Stanford Microdevices' SPA-2318 is a high efficiency GaAs Heterojunction Bipolar Transistor (HBT) amplifier housed in a low-cost surface-mountable plastic package. These HBT amplifiers are fabricated using molecular beam epitaxial growth technology which produces reliable and consistent performance from wafer to wafer and lot to lot.

This product is specifically designed for use as a driver amplifier for infrastructure equipment in the 2150 MHz PCS band. Its high linearity makes it an ideal choice for multi-carrier and digital applications.




## Product Features

- **High Linearity Performance:**
  **+47 dBm Typ. OIP3 at 2140 MHz**
  **+21.7 dBm W-CDMA Channel Power at -45 dBc ACP**
- **On-chip Active Bias Control**
- **High Gain: 23 dB Typ.**
- **Patented High Reliability GaAsHBT Technology**
- **Surface-Mountable Plastic Package**

## Applications

- **W-CDMA Systems**
- **Multi-Carrier Applications**

| Symbol | Parameters: Test Conditions: $Z_0$ = 50 Ohms Temp = 25°C, Vcc=5.0V | Units | Min. | Typ. | Max. |
|---|---|---|---|---|---|
| $f_0$ | Frequency of Operation | MHz | 2110 | 2140 | 2170 |
| $P_{1dB}$ | Output Power at 1dB Compression | dBm | | 28 | |
| $S_{21}$ | Small Signal Gain | dB | | 23 | |
| VSWR | Input VSWR | - | | 1.5:1 | |
| $OIP_3$ | Output Third Order Intercept Point<br>Power out per tone = +14dBm | dBm | | 47 | |
| NF | Noise Figure | dB | | 5.0 | |
| Icc | Device Current<br>**Ibias** = 10mA, **Ic1** = 70mA, **Ic2** = 320 mA | mA | | 400 | |
| $R_{th\ j\text{-}l}$ | Thermal Resistance (junction - lead) | °C/W | | 32 | |



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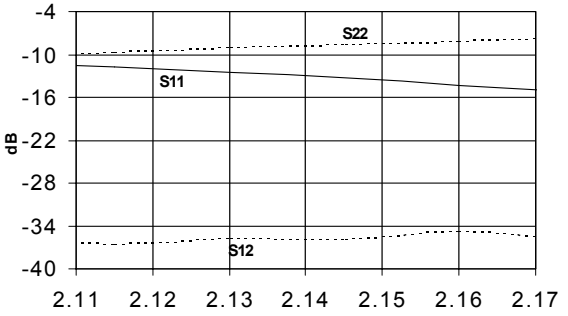
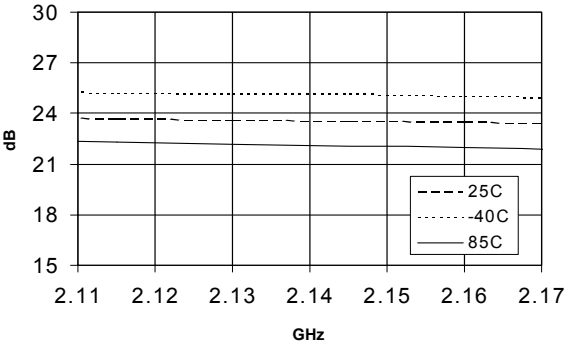
## 2140 MHz Application Circuit Data, Icc=400mA, T=+25C, Vcc=5V

Note: Tuned for Output IP3

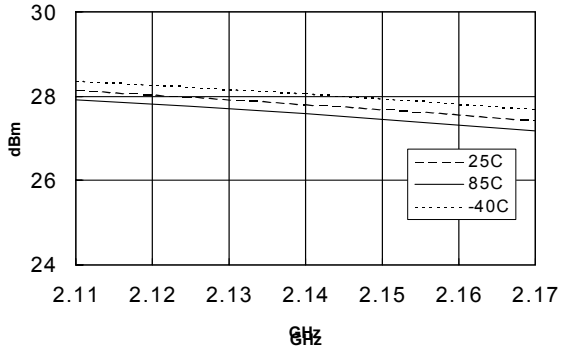
**Input/Output Return Loss, Isolation vs Frequency**



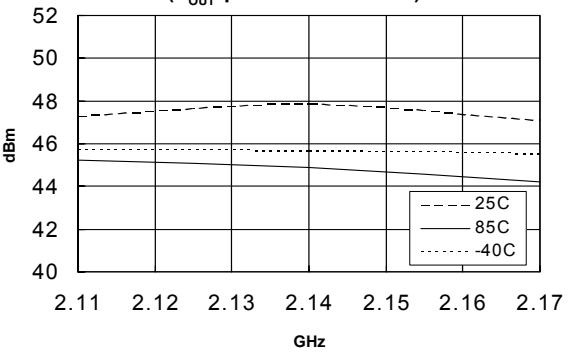

**Gain vs. Frequency**



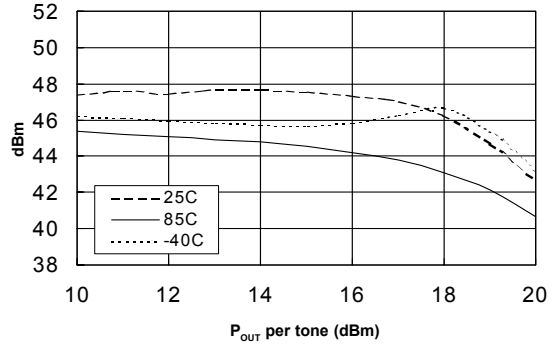

**P1dB vs Frequency**



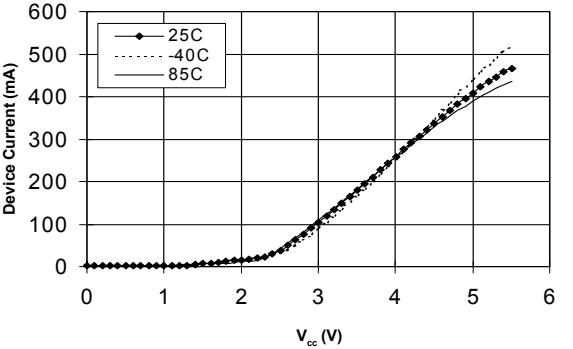

**Output Third Order Intercept vs. Frequency ($P_{OUT}$ per tone = 14dBm)**




**Output Third Order Intercept vs. Tone Power 2.14GHz**



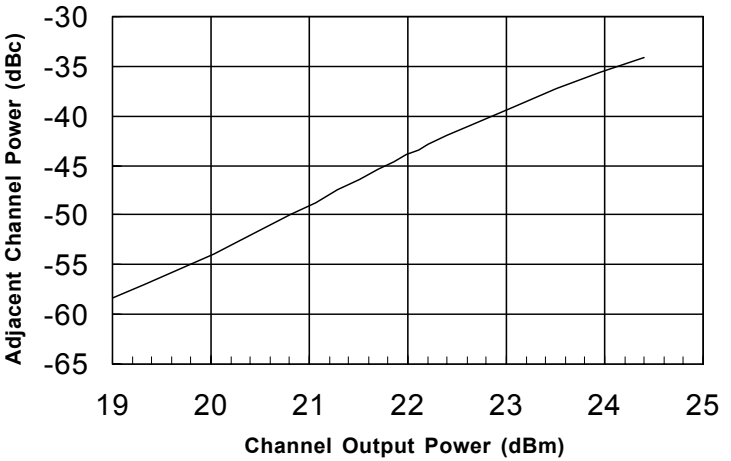

**Device Current vs. Source Voltage**



## 2140 MHz Application Circuit Data, Icc=400mA, T=+25C, Vcc=5V

**The W-CDMA setup is PCCPCH+PSCH+SSCH+CPICH+PICH+64 DPCH**

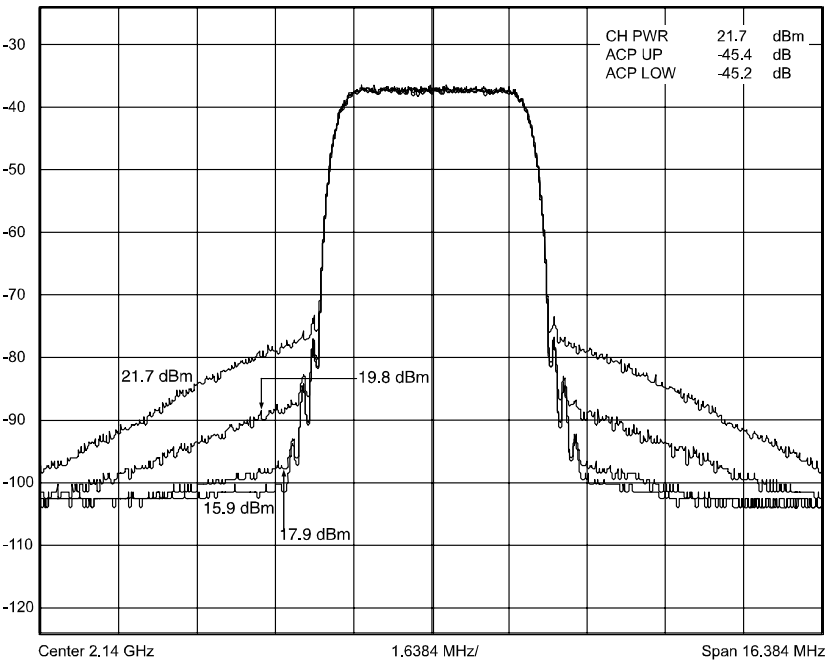
### W-CDMA at 2.14 GHz Adjacent Channel Power vs. Channel Output Power



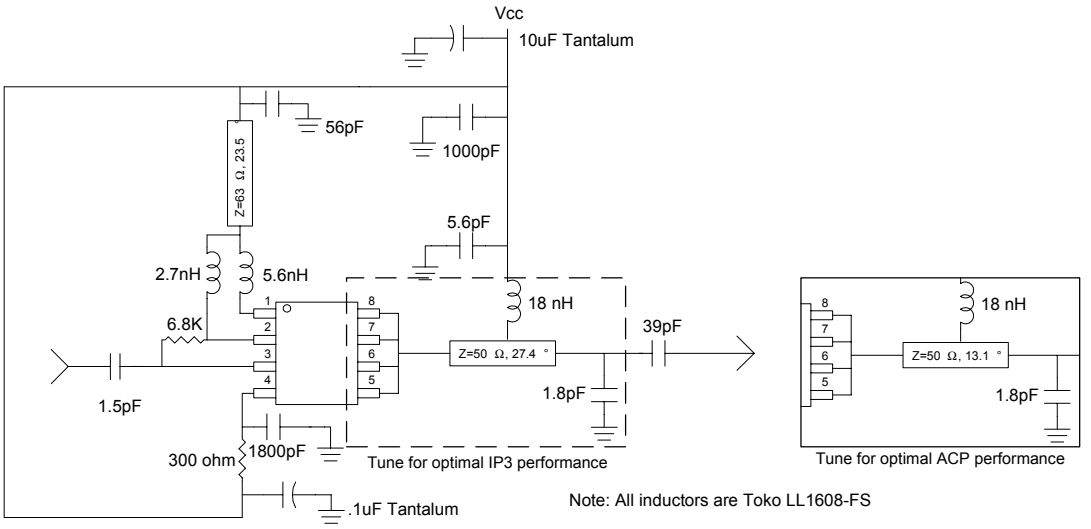

| Frequency | 2140 MHz |
|---|---|
| Small Signal Gain (dB) | 23.4 |
| Ch. Pwr. (dBm) @ -45 dBc ACP | 21.7 |
| Output IP3 (dBm) | 45.4* |
| P1dB (dBm) | 29.9 |

***Note:** IP3 performance degraded due to Device being tuned for optimal ACP performance

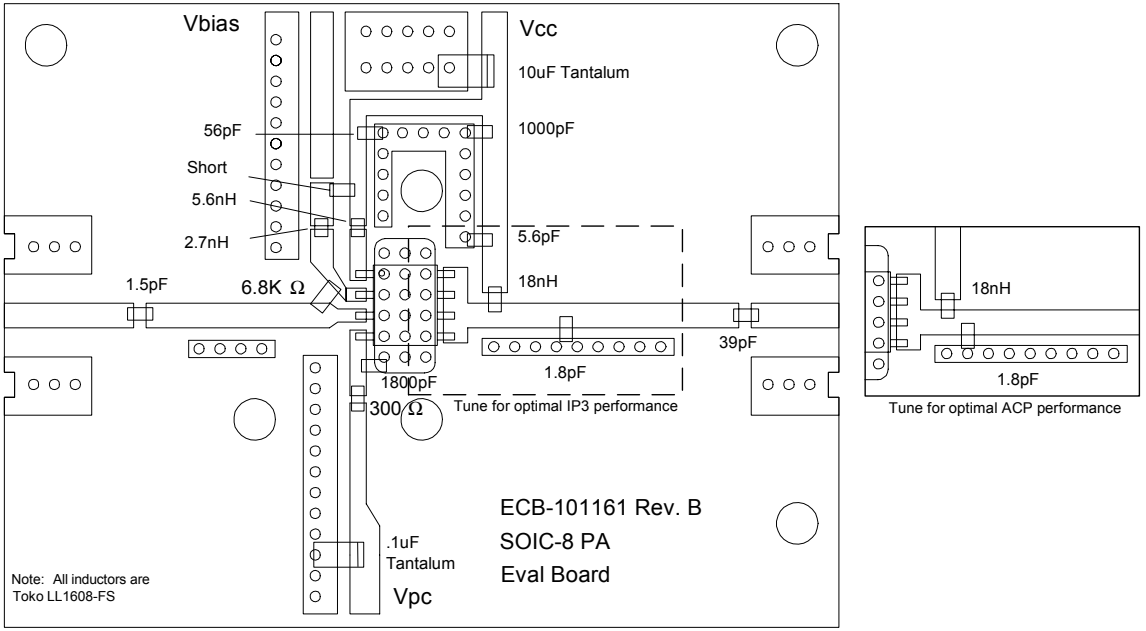
### W-CDMA at 2.14 GHz



## 2110 - 2170 MHz Schematic

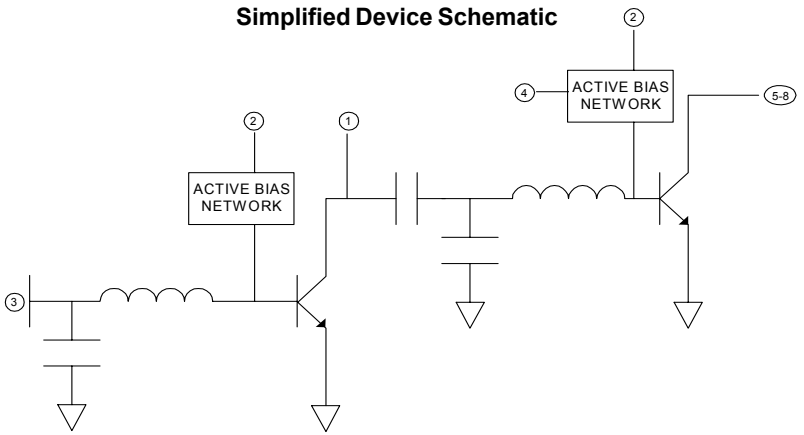



## 2110 - 2170 MHz Evaluation Board Layout



| Pin # | Function | Description |
|---|---|---|
| **1** | VC1 | VC1 is the supply voltage for the first stage transistor. The configuration as shown on application schematic is required for optimum RF performance. |
| **2** | Vbias | Vbias is the bias control pin for the active bias network. Recommended configuration is shown in the Application Schematic. |
| **3** | RF In | RF input pin. This pin requires the use of an external DC blocking capacitor as shown in the Application Schematic. |
| **4** | VPC2 | VPC2 is the bias control pin for the active bias network for the second stage. The recommended configuration is shown in the Application Schematic. |
| **5, 6, 7, 8** | RF Out/VC2 | RF output and bias pin. Bias should be supplied to this pin through an external RF choke. Because DC biasing is present on this pin, a DC blocking capacitor should be used in most applications (see application schematic). The supply side of the bias network should be well bypassed. An output matching network is necessary for optimum performance. |
| **EPAD** | Gnd | Exposed area on the bottom side of the package needs to be soldered to the ground plane of the board for optimum thermal and RF performance. Several vias should be located under the EPAD as shown in the recommended land pattern (page 6). |

**Simplified Device Schematic**




## Absolute Maximum Ratings

Operation of this device above any one of these parameters may cause permanent damage.

Bias Conditions should also satisfy the following expression: $I_D V_D$ (max) < $(T_J - T_L)/R_{th,j-l}$

**Caution: ESD sensitive**
Appropriate precautions in handling, packaging and testing devices must be observed.

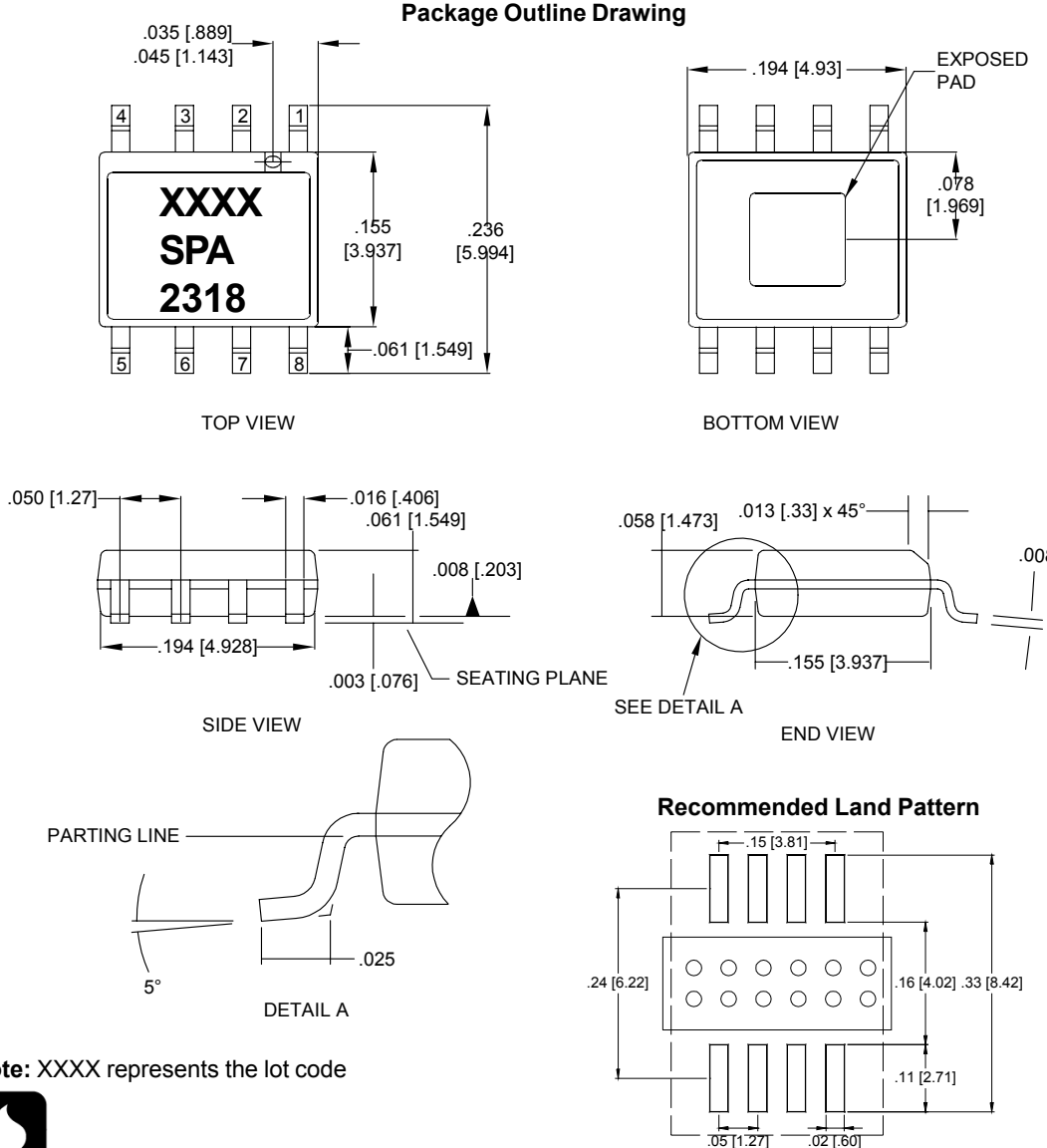
| Parameter | Value | Unit |
|---|---|---|
| Supply Current ($V_{C1}$) | 150 | mA |
| Supply Current ($V_{C2}$) | 750 | mA |
| Device Voltage ($V_D$) | 6.0 | V |
| Power Dissipation | 4.0 | W |
| Operating Lead Temperature ($T_L$) | -40 to +85 | °C |
| RF Input Power | +40 | mW |
| Storage Temperature Range | -40 to +150 | °C |
| Operating Junction Temperature ($T_J$) | +150 | °C |

# SPA-2318 2150 MHz 1 Watt Power Amp

## Part Number Ordering Information

| Part Number | Devices Per Reel | Reel Size |
|---|---|---|
| SPA-2318 | 500 | 7" |

## Package Outline Drawing




## Recommended Land Pattern




**Note:** XXXX represents the lot code

**Note:** Parts need to be baked prior to use as discussed in application note AN-029 (Special handling information for Exposed Pad ™ SOIC-8 products) to ensure no moisture is trapped in the encapsulated package. In production, this baking procedure is not necessary if parts are used within 48 hours of opening the sealed shipping materials.