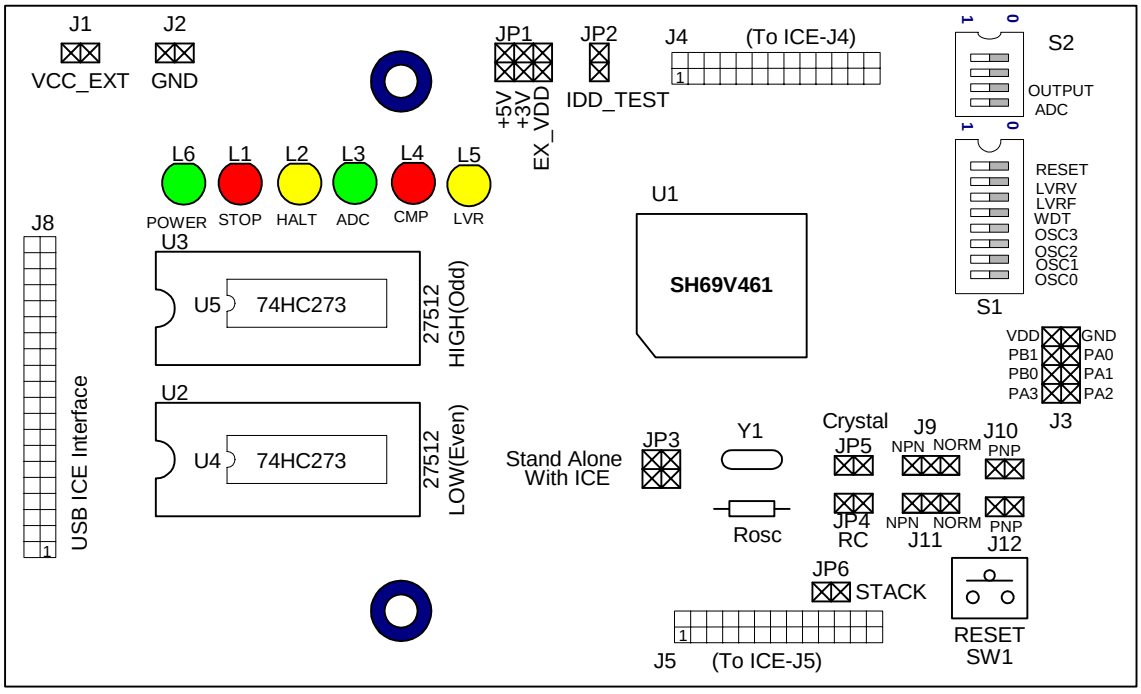
SH69P461/P862/P842/P822/P802/P801 EVB

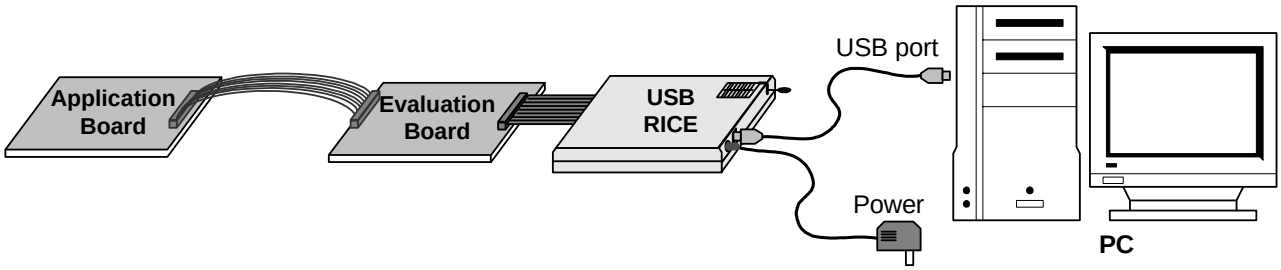
Application Notes for SH69P461/P862/P842/P822/P802/P801 EVB

SH69P461/P862/P842/P822/P802/P801 Evaluation board (EVB)

The SH69P461/P862/P842/P822/P802/P801 EVB is used to evaluate the SH69P461/P862/P842/P822/P802/P801 chip's function for the development of application program. It contains of an SH69V461 chip to evaluate the functions of SH69P461/P862/P842/P822/P802/P801. The following figure shows the placement diagram of SH69P461/P862/P842/P822/P802/P801 EVB.

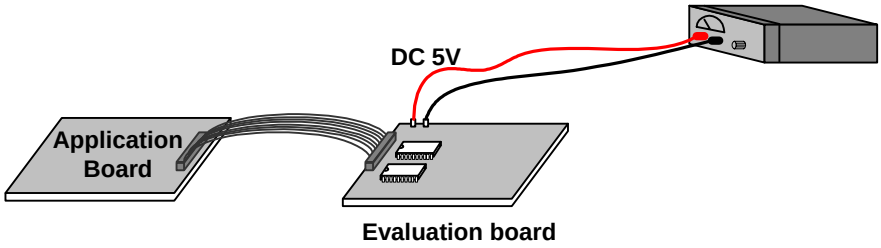


There are two configurations of SH69P461/P862/P842/P822/P802/P801 EVB in application development: ICE mode and stand-alone mode. In ICE mode, the ICE (motherboard) is connected to the EVB by the ICE interface.



(a) ICE mode

In standalone mode, the EVB is no longer connected to the motherboard, but the Flash (or EPROM) must be inserted to the socket that stored the application program.



(b) Stand-alone mode

The process of program's evaluation on SH69P461/P862/P842/P822/P802/P801 EVB

User can use **Sino Wealth Rice66 Integrated Development Environment (IDE)** to emulate the program and produce the obj file. Rice66 IDE is a real-time in-circuit emulator program. It provides real-time and transparent emulation support for the SH6X series 4-bit micro-controller. And integrate assembler can create binary (*.obj) file and the other files.

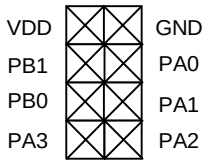
Use Flash (or EPROM) In standalone mode

Rice66 IDE is built-in with an object file depart function. The command "Split object file" can separate the one 16 bits object file into two 8 bits files, which contain the high and low bytes respectively.

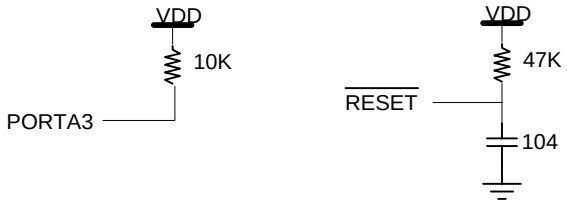
Write the high/low byte obj file to Flash (or EPROM) and insert them to EVB (ROMH and ROML). Then, user can evaluate the program in standalone mode.

SH69P461/P862/P842/P822/P802/P801 interface connector: (Top View from EVB)

IO port interface: J3



Note: The port 'PA3' is functioned as both 'PORTA3' port and 'RESET' port selected by option. The different port function needs correspondent peripheral connection. See the following diagram:



External VCC input for stand alone mode:
J1, J2 -The external power input when the EVB worked in stand-alone mode. The voltage of Vcc must be 5V±5%.

Interface to ICE:
J4, J5 -connect to RICE66 2.0, or connect to RICE66 3.0 with a transition board.
J8 -connect to RICE66 3.0 directly.

Interface to test the EV chip operating current
JP2 - User can test the EV chip current through JP2

Note: In ICE mode, the current value is correct only when the RICE66 runs in external clock from EVB mode. (Select the "external clock from EVB" in OSC Frequency Configure manual.)

Switch setting:

S1:

Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Remarks
RESET	LVRV	LVRF	WDT	OSC3	OSC2	OSC1	OSC0	
X	X	X	X	X	Off	Off	Off	Select external clock as OSC clock
X	X	X	X	X	Off	On	On	Select internal RC oscillator as OSC clock
X	X	X	X	X	On	Off	Off	Select external RC oscillator as OSC clock
X	X	X	X	X	On	Off	On	Select ceramic oscillator as OSC clock
X	X	X	X	X	On	On	Off	Select crystal oscillator as OSC clock
X	X	X	X	X	On	On	On	Select 32.768k crystal as OSC clock
X	X	X	X	Off	X	X	X	Select 30kHz - 2MHz oscillator range
X	X	X	X	On	X	X	X	Select 2MHz - 10MHz oscillator range
X	X	X	Off	X	X	X	X	Disable the Watch Dog Timer
X	X	X	On	X	X	X	X	Enable the Watch Dog Timer
X	X	Off	X	X	X	X	X	Disable the Low Voltage Reset
X	X	On	X	X	X	X	X	Enable the Low Voltage Reset
X	Off	X	X	X	X	X	X	Select low LVR voltage
X	On	X	X	X	X	X	X	Select high LVR voltage
Off	X	X	X	X	X	X	X	Enable chip pin reset input
On	X	X	X	X	X	X	X	Disable chip pin reset input

S2:

Bit 4	Bit 3	Bit 2	Bit 1	Remarks
-	-	OUTPUT	ADC	
-	-	X	Off	Select ADC off (for SH69P461/P862/P822)
-	-	X	On	Select ADC on (for SH69P461/P862/P822)
-	-	Off	X	Select normal output for PB0 and PB1
-	-	On	X	Reserved

Jumper setting:

JP1	EV chip power supply select
Short at 3V position	The power of EV chip is set as internal 3V power source.
Short at 5V position	The power of EV chip is set as internal 5V power source.
Short at EXT position	The EV chip use external power supply that was input from EXT_VDD pin.

JP3	EVB ICE/Stand-alone mode select
Short at Stand-alone position	Select stand-alone mode. (The system clock is provided by the on board oscillator.)
Short at With-ICE position	Select with-ICE mode. (The system clock is provided by the ICE.)

JP4	External RC select
Short	The external RC on board will be selected as OSC clock source.
Open	The external RC on board will not be selected as OSC clock source.

JP5	Ceramic or Crystal select
Short	The external ceramic or crystal will be selected as the OSC clock source.
Open	The external ceramic or crystal will not be selected as the OSC clock source.

JP6	Stack Overflow select
Short	The stack overflow function in ICE mode will be enabled.
Open	The stack overflow function in ICE mode will be disabled.

J9	PB1 output mode select
Short NORM	PB1 will output normally.
The others	Reserved

J10	PB1 output mode select
Short	Reserved
Open	PB1 will output normally.

J11	PB0 output mode select
Short NORM	PB0 will output normally.
The others	Reserved

J12	PB0 output mode select
Short	Reserved
Open	PB0 will output normally.

SW1:

Reset the whole system by pressing the button.

Diagnostic LED:

Power LED: The LED will be turned on when the EVB is powered.

HALT LED: The LED will be turned on when the system is in HALT mode.

STOP LED: The LED will be turned on when the system is in STOP mode.

ADC LED: The LED will be turned on when the ADCON bit is set as 1. (For SH69P461/P862/P822)

CMP LED: The LED will be turned on when the comparator is enabled. (For SH69P461/P862/P842)

LVR LED: The LED will be turned on when the VDD is lower than LVR voltage.

Oscillator setting:

JP4:

- If short the JP4 and set S1 to select external RC oscillator, the on board RC oscillator will be selected as OSC clock. User must put a resistor(R_{OSC}=8.2kΩ/F_{OSC}=8MHz, for reference only) on the ROSC position.
- If JP4 is open, the on board RC oscillator will not be selected as OSC clock.

JP5:

- If short the JP5 and set S1 to select ceramic or crystal oscillator, the on board ceramic or crystal will be selected as OSC clock. User must put a crystal oscillator or ceramic resonator on the Y1 position.
- If JP5 is open, the on board ceramic or crystal will not be selected as OSC clock.

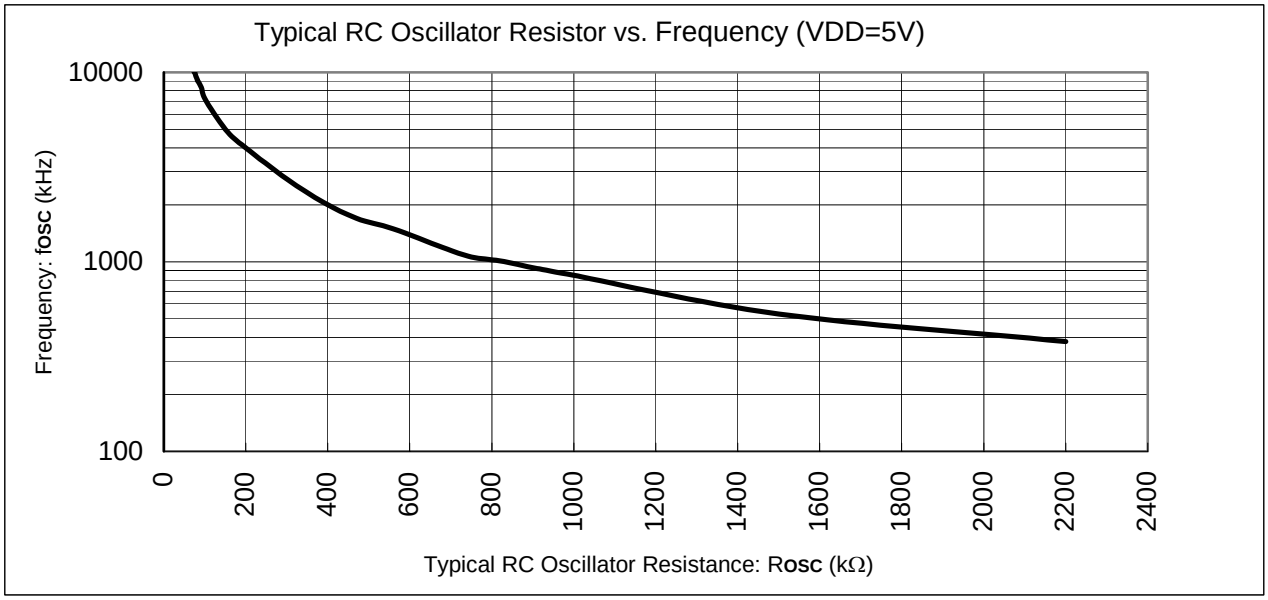
Capacitor selection for oscillator

Ceramic Resonators		
Frequency	**C1**	**C2**
455kHz	47~100pF	47~100pF
3.58MHz	-	-
4MHz	-	-

*- The specified ceramic resonator has internal built-in load capacity

Crystal Oscillator		
Frequency	**C1**	**C2**
32.768kHz	5~12.5pF	5~12.5pF
4MHz	8~15pF	8~15pF
8MHz	8~15pF	8~15pF

RC oscillator Characteristics Graphs (for reference only)



Notes:

1 Application notes:

1.1 After entering into the RICE66 and successfully downloaded the user program, use the F5 key on the PC keyboard to reset the EVB before running the program. If abnormal response occurs, the user must switch off the ICE power and quit RICE66, then wait for a few seconds before restarting.

1.2 When running the RICE66 for the first time, the user needs to select the correct MCU type, clock frequency, then save the settings and restart RICE66 again.

1.3 Can't Step (F8) or Over (F9) a HALT and STOP instruction.

1.4 Can't emulate the interrupt function in Step (F8) operating mode.

1.5 When you want to escape from HALT or STOP (in ICE mode), please press F5 key on the PC keyboard twice.

1.6 The maximum current limit supplied from EVB to the target is 100mA. When the current in the target is over 100mA, please use external power supply.

2 Programming notes:

2.1 Clear the data RAM and initialize all system registers during the initial programming.

2.2 Never use the reserved registers.

2.3 Do not execute arithmetic operation with those registers that only have 1, 2 or 3 bits. This kind of operation may not produce the result you expected.

2.4 To add "p=69P461" ("p=69P862","p=69P842","p=69P822","p=69P802") and "romsize=2048" (or add "p=69P801" and "romsize=1024") at the beginning of a program. If any problem occurs during the compilation of the program, check the device and set if it was set correctly.

2.5 Both index register DPH and DPM have three bits; so pay attention to the destination address when using them.

2.6 It takes more than 0.3 second to wake up from STOP mode when using 32.768kHz crystal. So, if the system is awake when the key is pressed, the key may have been released when the program starts to read the Key value.

2.7 Notes for interrupt:

2.7.1 Please make sure that the IE flag is enabled before entering into a "HALT" or a "STOP mode. It means that the "HALT" or "STOP" instruction must follow the set "IE" instruction closely.

2.7.2 After the CPU had responded to an interrupt, IRQ should be cleared before resetting IE in order to avoid multi-responses.

2.7.3 Interrupt Enable instruction will be automatically cleared after entering into the interrupt-processing subroutine. If setting IE is too early, it is possible to reenter into the interrupt. So the Interrupt Enable instruction should be placed at the last 3 instructions of the subroutine.

2.7.4 CPU will not respond to any interrupt during the next two instructions after the Interrupt Enable flag be set from 0 to 1.

2.7.5 After CPU has responded to an interrupt, IE will be cleared by the hardware. It is recommended to clear the IRQ at the end of interrupt subroutine.

2.7.6 The stack has eight levels. If an interrupt is enabled, there will be only seven levels that can be used.

2.7.7 It is recommended that the last line of program is "END".

Examples:

1> Description: CPU can not wakeup after executing the "HALT" or "STOP" instruction.

Program: Interrupt Enable instruction is set outside the interrupt subroutine

<Wrong example>	**<Correct example >**
……	……
LDI IE, 0FH ;enable interrupt	LDI IE, 0FH ;enable interrupt
NOP	~~NOP~~
NOP	~~NOP~~
HALT	HALT

Analysis: After two "NOP" instructions, if an interrupt request comes or IRQ is non-zero during the third instruction cycle, CPU will respond to the interrupt and IE will be cleared. Then when returning to main program, CPU starts to execute "HALT" or "STOP" and will not be activated, because IE is cleared to zero and all interrupts are disabled.

Solution: "HALT" or "STOP" are being followed closely by the "LDI IE, 0FH"

2> Description: CPU responds to one interrupt several times.

Program: Interrupt Enable instruction is placed outside the interrupt subroutine.

```
L1:
    ……
    LDI     IE, 0FH          ; enable interrupts
    NOP
    NOP
    JUMP    L1
```

Analysis: After executing this two "NOP" instructions, and IRQ is not cleared in time, CPU will respond to the interrupt again when it executes the two instructions followed by "LDI IE, 0FH". This will happen again and again. So CPU responds to one interrupt several times.

Solution: The relative IRQ flag is cleared in time after responding to the interrupt.

3> Description: CPU is running dead in the interrupt-processing program.

Program: an interrupt subroutine.

```
ENTERINT:
    ……
    LDI    IE, 0FH
    NOP
    LDA STACK, 0
    RTNI
```

Analysis: After executing "LDI IE, 0FH" and the following two instructions, an interrupt request comes or the last relative IRQ flag is not cleared in time, then CPU will respond to the interrupt again, so the interrupt is nesting again. When the stack is beyond 8 levels, it will run into a dead loop.

Solution: Make sure that the CPU can quit from interrupt subroutine within two instruction cycles after interrupt is enabled; After the interrupt is responded, the relative IRQ flag should be cleared before enabling the interrupt.

2.8 Notes for TIMER

2.8.1 When setting the Timer Counter, write first T0L, then T0H.

2.8.2 After setting TM0, T0L, T0H, there is no need to rewrite after the Timer counts overflow, otherwise it will cause a time error every time. The timer is interrupted by the reload register that was set in different time.

2.9 Notes for I/O

2.9.1 Never do the logical operation with the I/O ports. Especially when the I/O ports are connected with the other components externally.

2.9.2 When the internal pull-up resistor is turned on, "1" must be written to I/O Port before Reading.

2.9.3 In "STOP" mode, if the Open Drain output register is set to "1", it will cause current leakage from tens to hundreds micro-ampere. To prevent I/O floating , pull-high or pull-low resistors to the resistance from 1 to 2 MΩ must be connected.

2.9.4 When counting external pulse, please directly read the PORT status to make sure that the counted number is correct.

2.9.5 When scanning key value, writing and reading operation to the PORT should be separated by 2 or 3 "NOP" instructions.

2.9.6 The Key De-bounce time is recommended to be 50ms. But in the Rubber Key application, it is best to test Rubber Key's De-bounce time.

Application notes Revision History

Revision No.	History	Date
1.1	Change on and off definition in switch setting. (Page 4)	Feb.2006
1.0	Original	Mar.2005