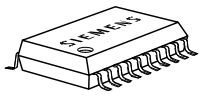
SIEMENS

## 5-V Low Drop Voltage Regulator — TLE 4262

**Bipolar IC**

### Features

- Output voltage tolerance ≤ ± 2 %
- Low-drop voltage
- Very low standby current consumption
- Overtemperature protection
- Reverse polarity protection
- Short-circuit proof
- Settable reset threshold
- Wide temperature range
- Suitable for use in automotive electronics



**P-DSO-20-6**

**P-DSO-14-4**

| Type | Ordering Code | Package |
|---|---|---|
| TLE 4262 G | Q67006-A9068 | P-DSO-20-6 (SMD) |
| ▼ TLE 4262 GM | Q67006-A9356 | P-DSO-14-4 (SMD) |

▼ New type

### Functional Description

TLE 4262 G is a 5-V low-drop voltage regulator in a P-DSO-20-6 SMD package. The maximum input voltage is 45 V. The maximum output current is more than 200 mA. The IC is short-circuit proof and incorporates temperature protection that disables the IC at overtemperature.

The IC regulates an input voltage $V_I$ in the range of 6 V < $V_I$ < 45 V to $V_{Qrated}$ = 5.0 V. A reset signal is generated for an output voltage of $V_Q$ < 4.5 V. This voltage threshold can be decreased to 3.5 V by external connection. The reset delay can be set externally with a capacitor. The IC can be switched off via the inhibit input, which causes the current consumption to drop from 720 µA to < 50 µA.

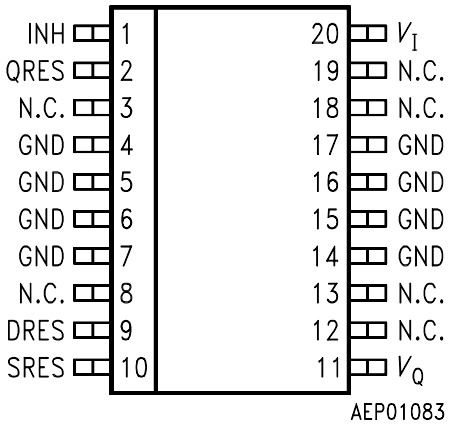
### Dimensioning Information on External Components

The input capacitor $C_I$ is necessary for compensating line influences. Using a resistor of approx. 1 Ω in series with $C_I$, the oscillating circuit consisting of input inductivity and input capacitance can be damped. The output capacitor is necessary for the stability of the regulating circuit. Stability is guaranteed at values ≥ 22 µF and an ESR of ≤ 3 Ω within the operating temperature range. For small tolerances of the reset delay, the spread of the capacitance of the dalay capacitor and its temperature coefficient should be noted.

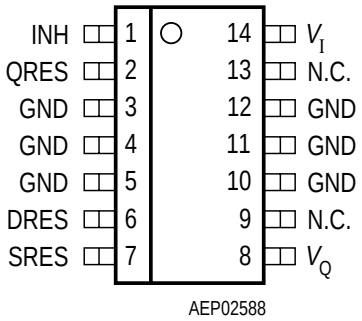
### Pin Configuration

(top view)

**TLE 4262 G**




**TLE 4262 GM**



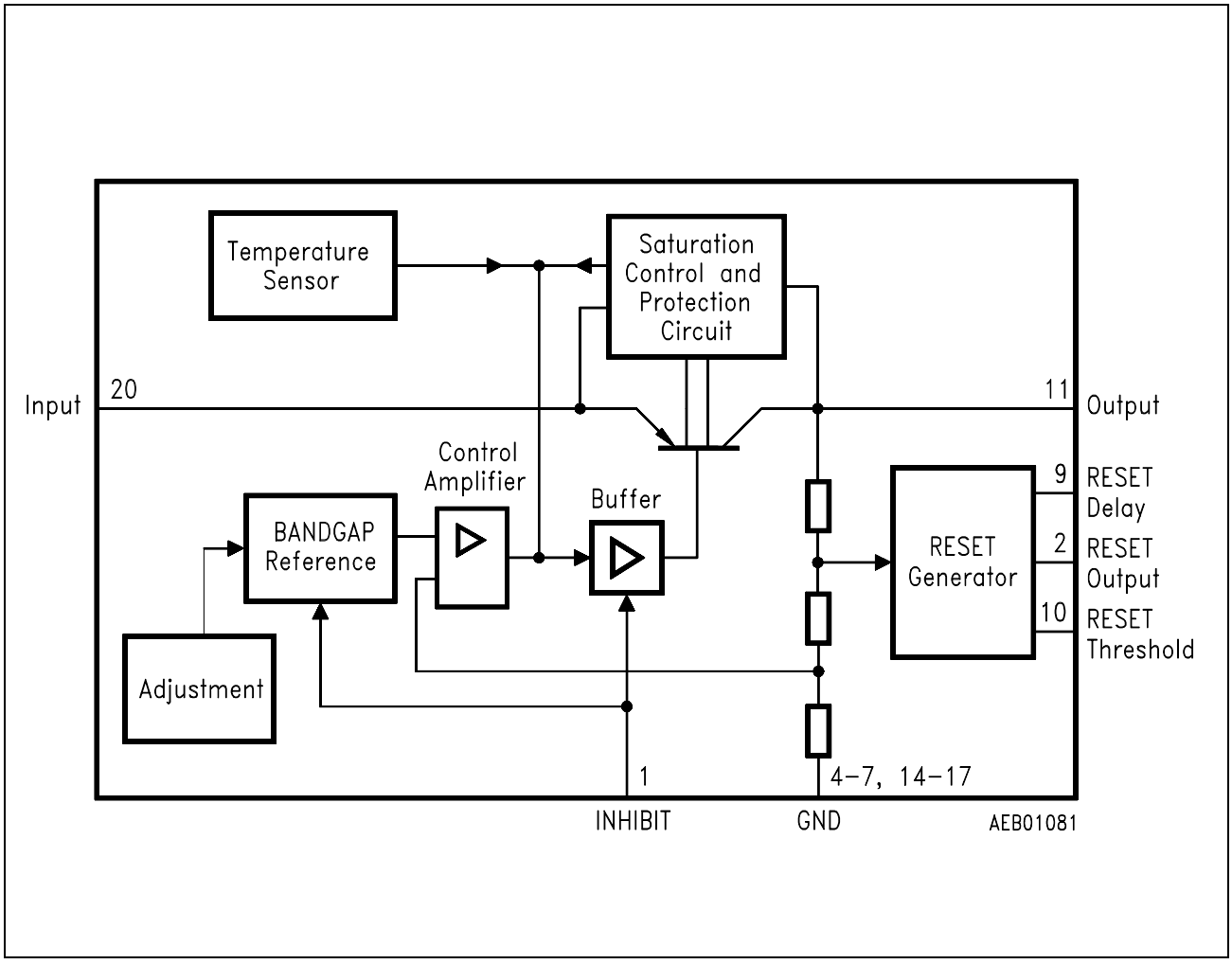
**Pin Definitions and Functions**

| Pin | Symbol | Function |
|---|---|---|
| 1 | INH | **Inhibit;** TTL-compatible, low-active input |
| 2 | QRES | **Reset output;** open-collector output internally connected to the output via a resistor of 30 kΩ. |
| 4-7, 14-17 | GND | **Ground** |
| 9 | DRES | **Reset delay;** connected to ground by a capacitor |
| 10 | SRES | **Reset threshold;** for setting the switching threshold connect by a voltage divider from output to ground. If this input is connected to GND, reset is triggered at an output voltage of 4.5 V. |
| 11 | $V_Q$ | **5-V output voltage;** block to ground by a 22–µF capacitor. |
| 20 | $V_I$ | **Input voltage;** block to ground directly at the IC by a ceramic capacitor. |
| 3, 8, 12, 13, 18, 19 | N.C. | Not connected |

## Circuit Description

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element. If the externally scaled down output voltage at the reset threshold input drops below 1.35 V, the external reset delay capacitor is discharged by the reset generator. If the voltage on the capacitor reaches the lower threshold $V_{ST}$, a reset signal is issued on the reset output and not cancelled again until the upper threshold $V_{dT}$ is exceeded. If the reset threshold input is connected to GND, reset is triggered at an output voltage of 4.5 V. The IC can be switched at the TTL-compatible, low-active inhibit input. It also incorporates a number of internal circuits for protection against:

- Overload
- Overtemperature
- Reverse polarity




**Block Diagram**

## Absolute Maximum Ratings

| Parameter | Symbol | Limit Values | | Unit | Remarks |
|---|---|---|---|---|---|
| | | min. | max. | | |
| **Input** | | | | | |
| Input voltage | $V_I$ | – 42 | 45 | V | – |
| Input current | $I_I$ | – | – | – | internally limited |
| **Reset Output** | | | | | |
| Voltage | $V_R$ | – 0.3 | 42 | V | – |
| Current | $I_R$ | – | – | – | internally limited |
| **Reset Input** | | | | | |
| Reset threshold | $V_{RE}$ | – 0.3 | 6 | V | – |
| **Reset Delay** | | | | | |
| Voltage | $V_d$ | – 0.3 | 42 | V | – |
| Current | $I_d$ | – | – | – | internally limited |
| **Output** | | | | | |
| Voltage | $V_Q$ | – 5.25 | $V_I$ | V | – |
| Current | $I_Q$ | – | – | – | internally limited |
| **Inhibit** | | | | | |
| Voltage | $V_e$ | – 42 | 45 | V | – |
| **Ground** | | | | | |
| Current | $I_{GND}$ | – 0.5 | – | A | – |

**Absolute Maximum Ratings** (cont'd)

| Parameter | Symbol | Limit Values | | Unit | Remarks |
|---|---|---|---|---|---|
| | | min. | max. | | |
| **Temperature** | | | | | |
| Junction temperature | $T_j$ | – | 150 | °C | – |
| Storage temperature | $T_{stg}$ | – 50 | 150 | °C | – |
| **Operating Range** | | | | | |
| Input voltage | $V_I$ | 5.2 | 45 | V | *) |
| Junction temperature | $T_j$ | – 40 | 150 | °C | – |
| Thermal resistance | | | | | |
| junction-ambient | $R_{th\ JA}$ | – | 70 | K/W | soldered |
| junction-case | $R_{th\ JC}$ | – | 25 | K/W | – |

*) Corresponds with characteristics of drop voltage, output current and power description (**see diagrams**).

## Characteristics

$V_I$ = 13.5 V; $T_j$ = 25 °C; $V_e$ > 3.5 V; (unless specified otherwise)

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| **Normal Operation** | | | | | | |
| Output voltage | $V_Q$ | 4.9 | 5.00 | 5.10 | V | 5 mA ≤ $I_Q$ ≤ 150 mA;<br>6 V ≤ $V_I$ ≤ 28 V;<br>– 40 °C ≤ $T_j$ ≤ 125 °C |
| Output voltage | $V_Q$ | 4.95 | 5.00 | 5.05 | V | 6 V ≤ $V_I$ ≤ 32 V;<br>$I_Q$ = 100 mA<br>$T_j$ > 100 °C |
| Output current limiting | $I_Q$ | 200 | 250 | | mA | – |
| Current consumption;<br>$I_q = I_i - I_Q$ | $I_q$ | – | – | 50 | µA | $V_e$ < 0.8 V |
| | $I_q$ | – | 720 | – | µA | $I_Q$ = 0 mA |
| | $I_q$ | – | 10 | 15 | mA | $I_Q$ = 150 mA |
| | $I_q$ | – | 15 | 20 | mA | $I_Q$ = 150 mA; $V_i$ = 4.5 V |
| Drop voltage | $V_{Dr}$ | – | 0.35 | 0.6 | V | $I_Q$ = 150 mA *) |
| Load regulation | $\Delta V_Q$ | – | – | 25 | mV | $I_Q$ = 5 mA to 150 mA |
| Supply-voltage regulation | $\Delta V_Q$ | – | 15 | 25 | mV | $V_I$ = 6 V to 28 V;<br>$I_Q$ = 150 mA |
| Ripple rejection | $SVR$ | – | 54 | – | dB | $f_r$ = 100 Hz;<br>$V_r$ = 0.5 Vpp |
| **Reset Generator** | | | | | | |
| Switching threshold | $V_{RT}$ | 4.2 | 4.5 | 4.8 | V | $V_{RE}$ = 0 V |
| Switching voltage | $V_{RE}$ | 1.28 | 1.35 | 1.42 | V | $V_Q$ > 3.5 V |
| Saturation voltage | $V_R$ | – | 0.10 | 0.40 | V | $I_R$ = 1 mA |

*) Drop voltage $V_I \geq$ 4.5 V; drop voltage = $V_I - V_Q$ (below regulating range)

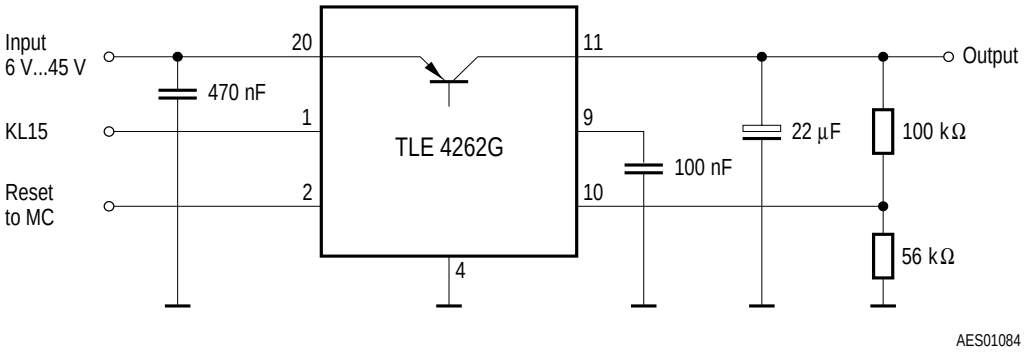
**Note:** The reset output is low within the range $V_Q$ = 1 V to $V_{RT}$.

**Characteristics** (cont'd)

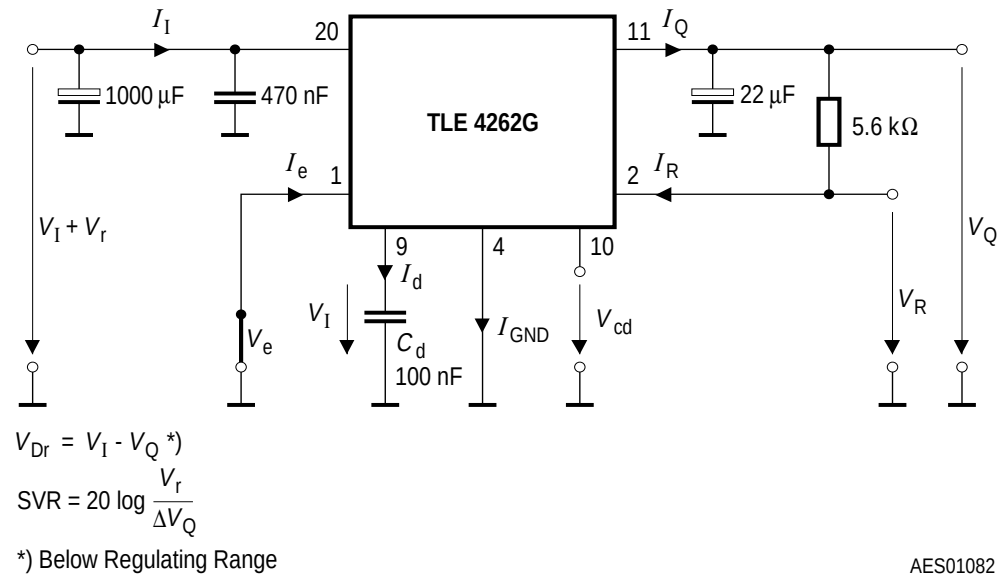
$V_I$ = 13.5 V; $T_j$ = 25 °C; $V_e$ > 3.5 V; (unless specified otherwise)

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Saturation voltage | $V_C$ | – | 50 | 100 | mV | $V_Q < V_{RT}$ |
| Charge current | $I_d$ | 7 | 10 | 14 | µA | – |
| Delay switching threshold | $V_{dT}$ | 1.5 | 1.7 | 2.1 | V | – |
| Switching threshold | $V_{ST}$ | 0.2 | 0.35 | 0.55 | V | – |
| Delay time | $t_D$ | – | 17 | – | ms | $C_d$ = 100 nF |
| Delay time | $t_t$ | – | 2 | – | µs | $C_d$ = 100 nF |
| **Inhibit** | | | | | | |
| Switch-ON voltage | $V_{e\ ON}$ | 3.5 | – | – | V | IC turned on |
| Switch-OFF voltage | $V_{e\ OFF}$ | – | – | 0.8 | V | IC turned off |
| Input current | $I_e$ | 5 | 10 | 15 | µA | $V_e$ = 5 V |

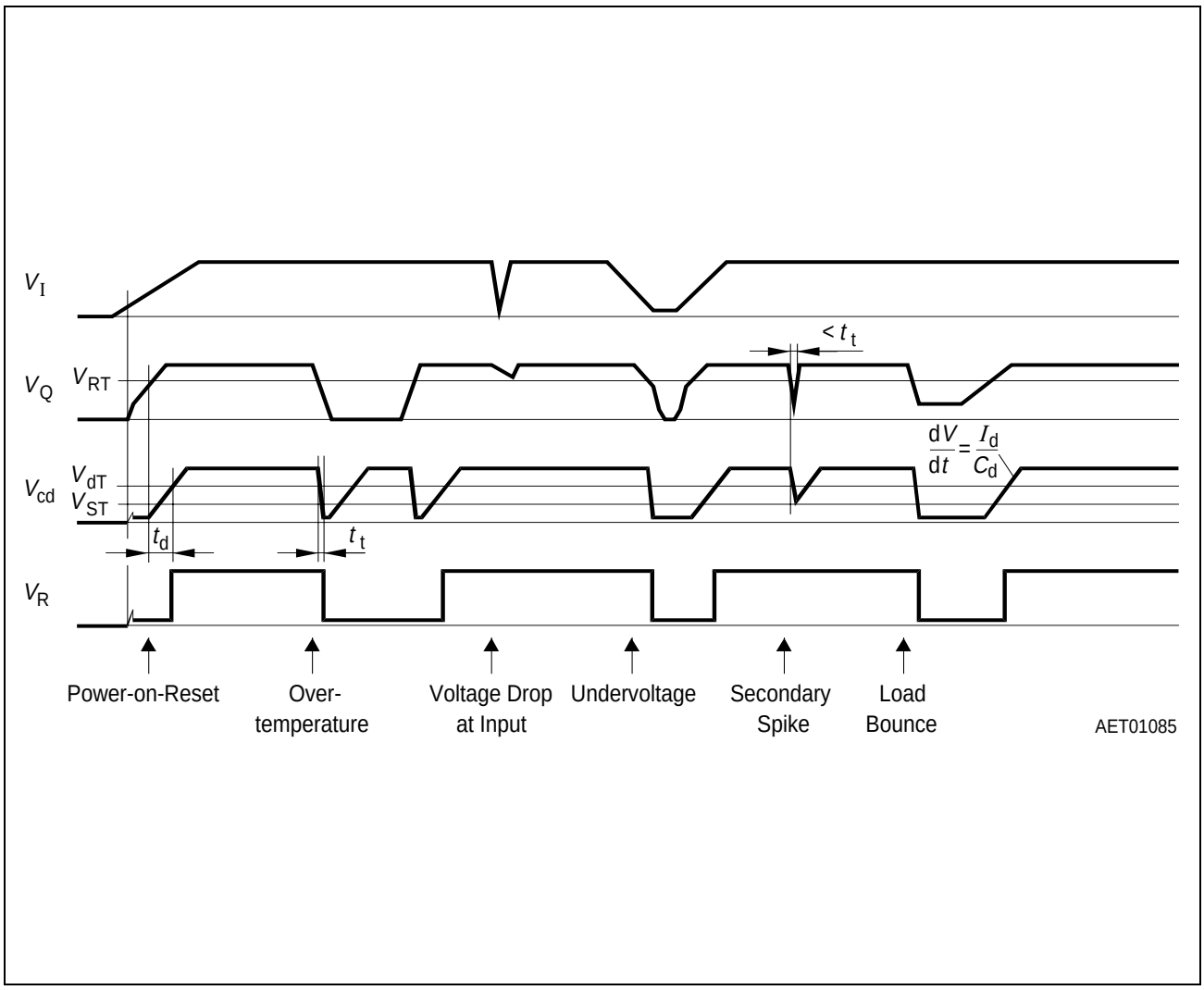
**Note:** The reset output is low within the range $V_Q$ = 1 V to $V_{RT}$.




**Application Circuit**

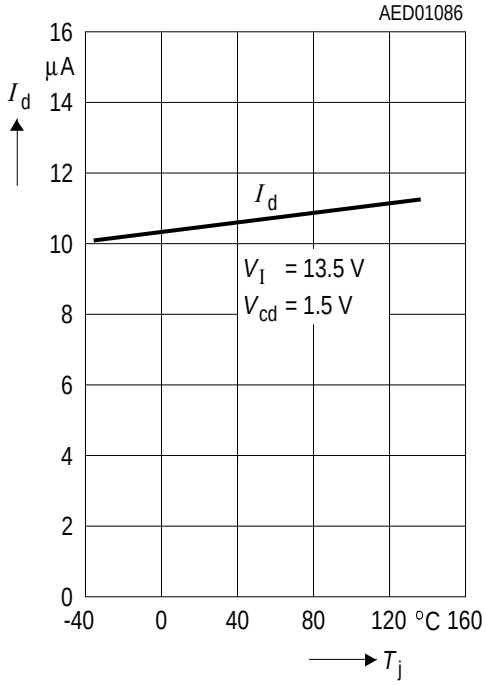



**Test Circuit**

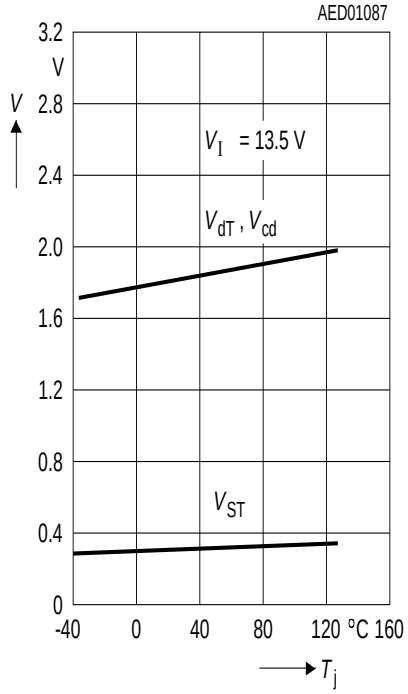



**Time Response**

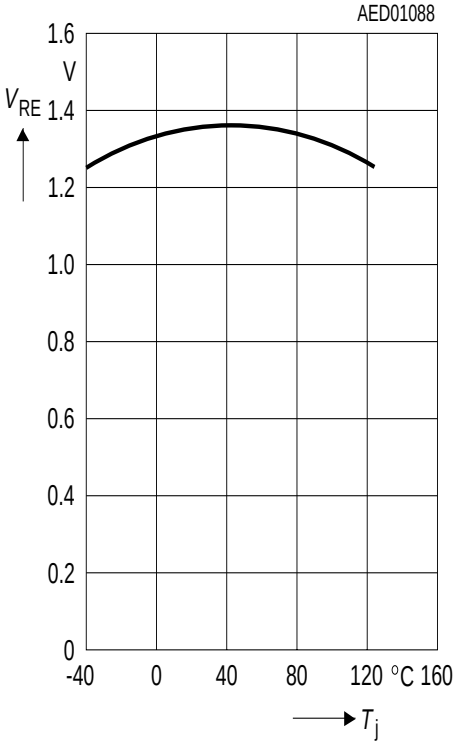
### Charge Current versus Temperature



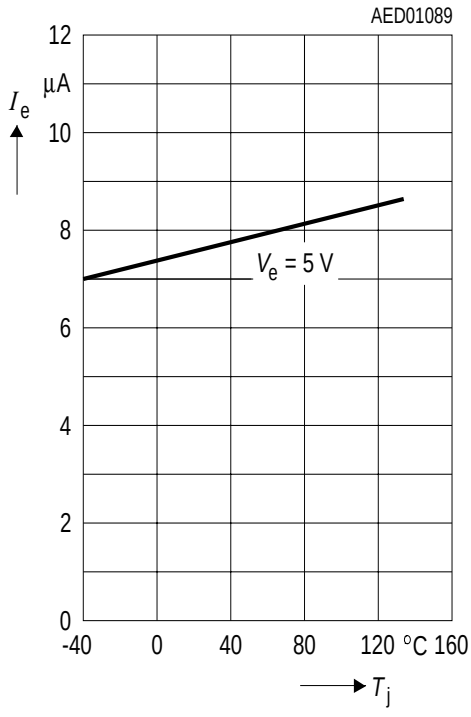

### Switching Voltage $V_{dT}$ and $V_{ST}$ versus Temperature



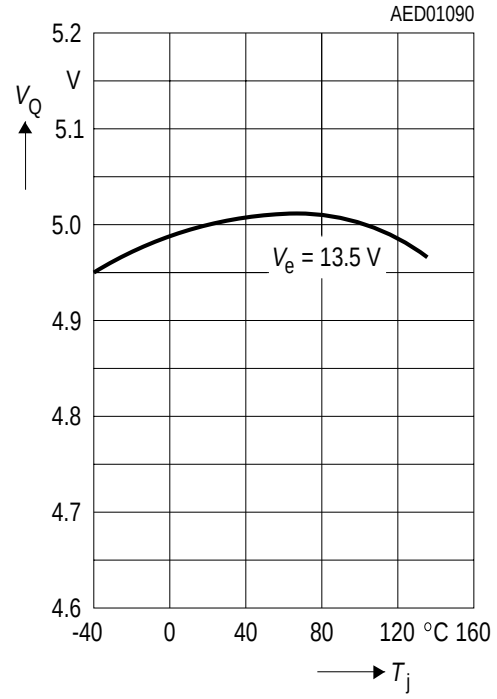

### Reset Switching Threshold versus Temperature



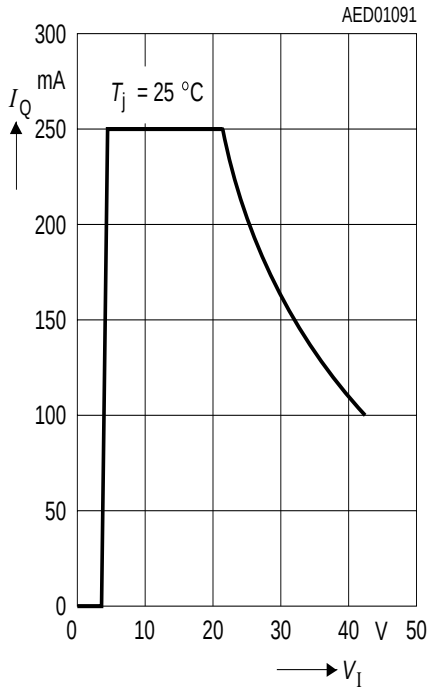

### Current Consumption of Inhibit versus Temperature Output Current



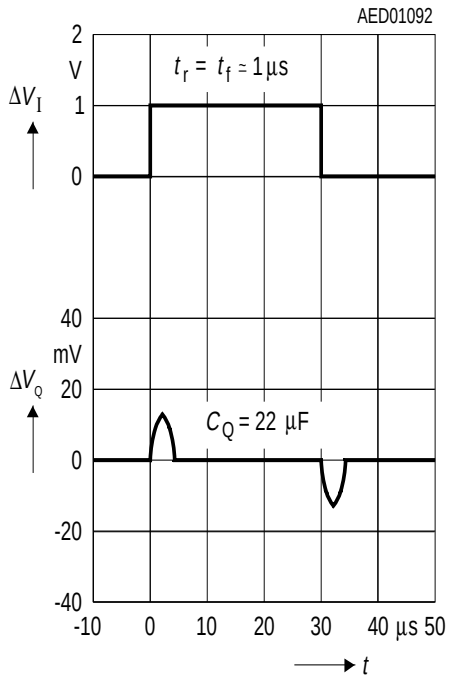
### Output Voltage versus Temperature



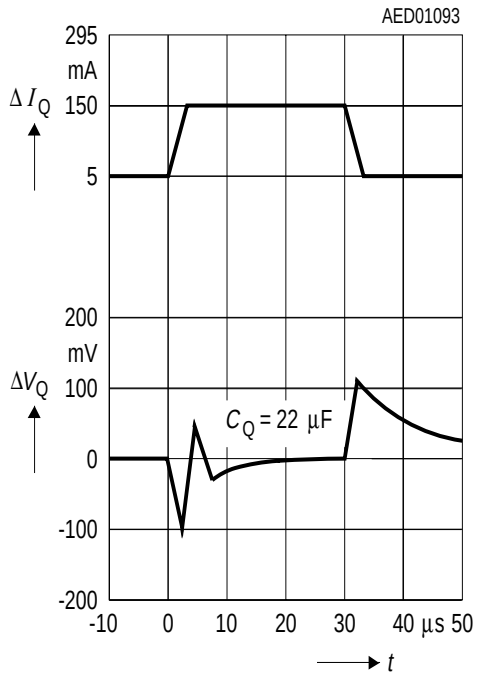

### Output Current versus Input Voltage



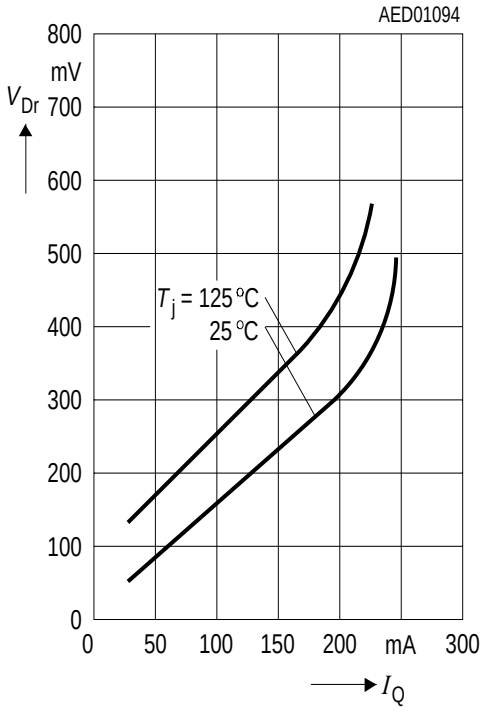

### Input Response



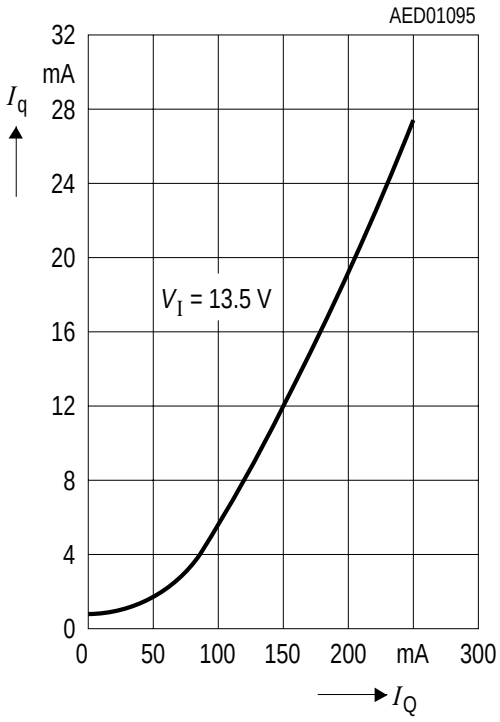

### Load Response



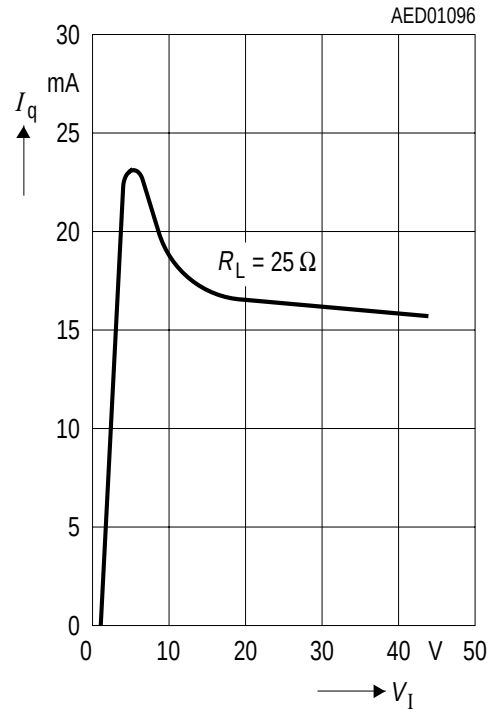
### Drop Voltage versus Output Current



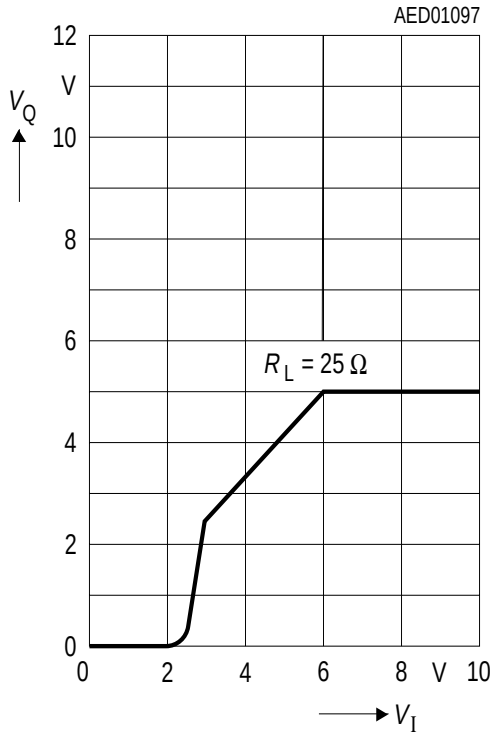

### Current Consumption versus Output Current




### Current Consumption versus Input Voltage

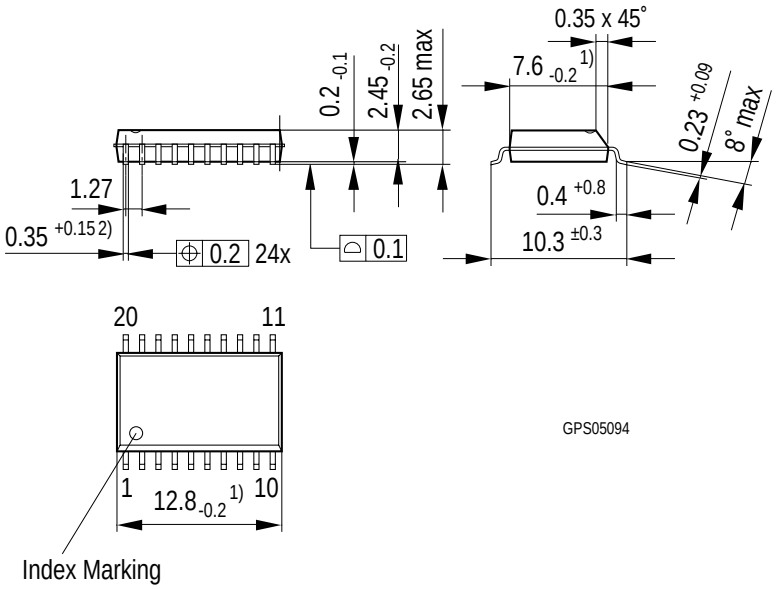



### Output Voltage versus Input Voltage



## Package Outlines

**P-DSO-20-6**
(Plastic Dual Small Outline)



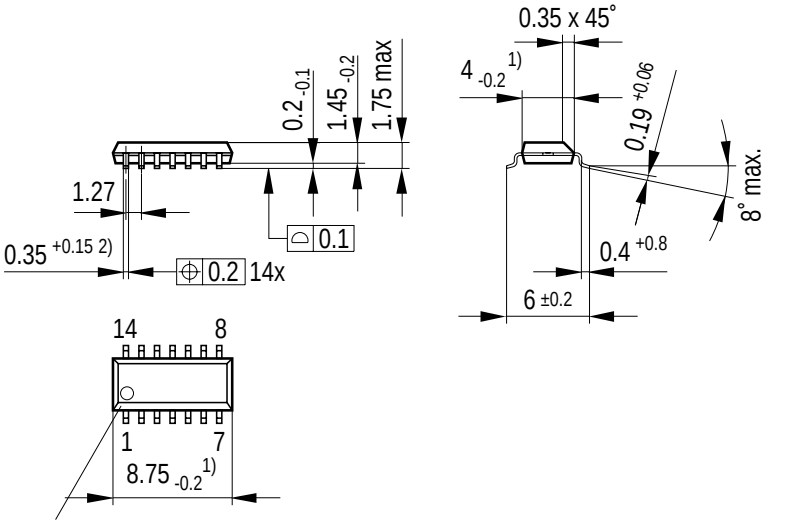

1) Does not include plastic or metal protrusions of 0.15 max per side
2) Does not include dambar protrusion of 0.05 max per side

Weight approx. 0.6 g

**Sorts of Packing**
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm

**P-DSO-14-4**
(Plastic Dual Small Outline)




1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.05 max. per side

GPS05093

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