1 PRODUCT OVERVIEW

OVERVIEW

The S3C7281 is a SAM48 core-based 4-bit CMOS single-chip microcontroller. It is built around the SAM48 core CPU and contains ROM, RAM. 14 I/O lines, buzzer and inverted buzzer output, and LCD driver/controller with an up-to-64-dot.

The S3C7281 can be used for dedicated control functions in a variety of applications, and is especially designed for LCD general purpose.

FEATURES

Memory

- 1024 x 8 bit program memory
- 64 x 4 bit data memory
  (Including stack and excluding LCD RAM)

14 I/O Pins

- I/O: 6 pins
- Output: 8 pins(Sharing with segment outputs)

8-Bit Basic Timer

- 4 clock source(0.26, 2.1, 8.2, 32.8ms at 1MHz)
- Watch-dog timer

Watch Timer

- Quasi interrupt(stand by release mode only)
- Time divider:
  3.91, 32, 125, 500ms at fw=32.8kHz
- BUZ, BUZ output(0.5, 1, 2, 4kHz at
  1MHz<main>, 32.8kHz<sub>)

Key Interrupt input(Quasi-interrupt)

- Falling edge detection(KS0, KS1)
- Stand by mode(idle, stop) release

Power on RESET (Program ROM MASK option)

- Initial power on RESET
- Reset operation under 2.0V

LCD Display

- 16 segments and 4 common pins
- 2, 3, and 4 common selectable
- Internal resistor for LCD bias(170 KΩ)

Memory Mapped I/O Structure

- Data memory bank 15

Power-Down Modes

- Idle: only CPU clock stops
- Stop: Main System clock and CPU clock stops
- Subsystem clock stop mode

Oscillation Sources

- Main: Internal RC OSC(1MHz)
- Sub: External 32.8kHz crystal only

Instruction Execution Times

- Main system clocks:4, 8, 64μs at 1MHz
- Subsystem clocks: 122 μs at 32.768 kHz

Operating Voltage Range

- 1.8 V to 5.5 V at 1MHz/32.8kHz

Power Consumption(The LVD circuit needs 100uA or more current on all the below mode)

- Main: Operation - 0.5mA at 1MHz, 3V
- Sub: Operation - 12μA at LCD off, 3V
  Idle - 5μA at LCD off idle, 3V
  Stop - 1μA at 5.5V

Operating Temperature

- - 40 °C to 85 °C

Package Type

- 32-SOP-450A Package

BLOCK DIAGRAM

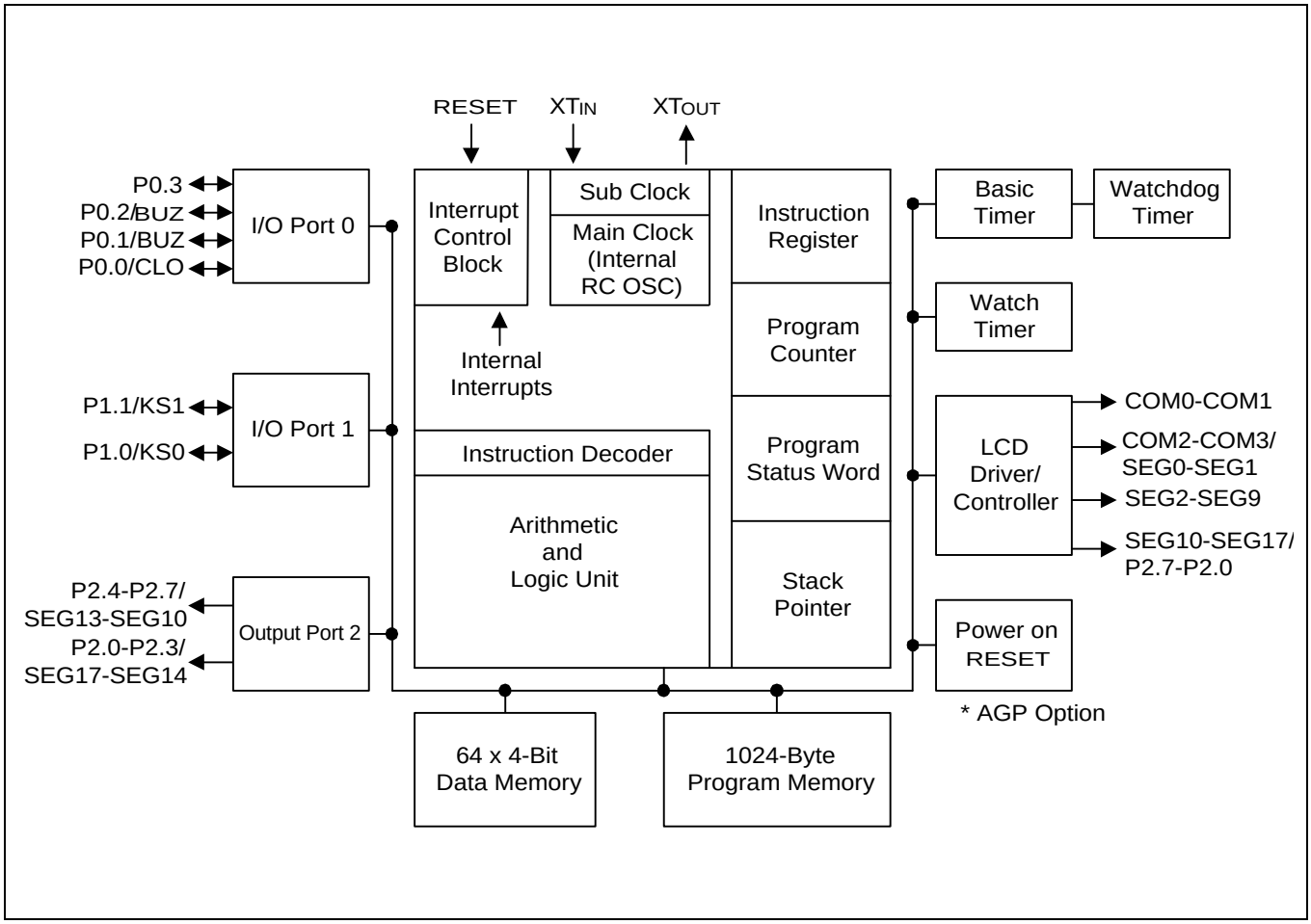
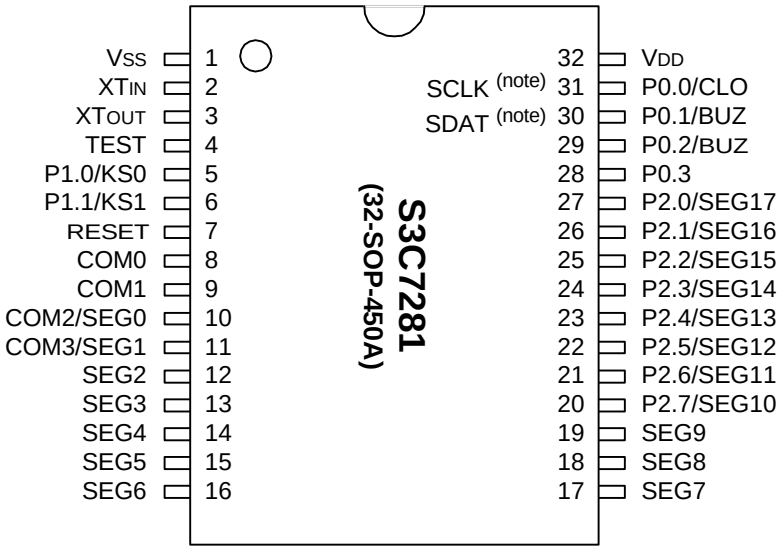


Figure 1-1. S3C7281 Simplified Block Diagram

PIN ASSIGNMENTS



NOTE: Reserved pins for the OTP version in the future

Figure 1-2. S3C7281 32-SOP Pin Assignment Diagram

PIN DESCRIPTIONS

Table 1-1. S3C7281 Pin Descriptions

Pin Name	Pin Type	Description	Number	Share Pin
P0.0 P0.1 P0.2 P0.3	I/O	4-bit I/O port. 1-bit or 4-bit read/write and test is possible. 1-bit unit pull-up resistors are assignable to input pins by software and are automatically disabled for output pins. Individual pins can be allocated as input or output(1-bit unit). The n-channel open-drain or push-pull output can be selected by software(1-bit unit).	31 30 29 28	CLO BUZ $\overline{BUZ}$
P1.0 P1.1	I/O	4-bit I/O port. 1-bit or 4-bit write and test is possible. 4-bit unit pull-up resistors are assignable to input pins by software and are automatically disabled for output pins. The pins can be allocated as input or output(4-bit unit). The n-channel open-drain or push-pull output can be selected by software(4-bit unit).	5 6	KS0 KS1
P2.0 - P2.7	O	8-bit output port. 1-bit, 4-bit, 8-bit read/write and test is possible. The n-channel open-drain or push-pull output can be selected by software(4-bit unit).	27 - 20	SEG17- SEG10
CLO	I/O	Clock output.	31	P0.0
BUZ	I/O	Buzzer signal output.	30	P0.1
$\overline{BUZ}$	I/O	Inverted buzzer signal output.	29	P0.2
KS0 KS1	I/O	External interrupt with falling edge detection.	5 6	P1.0 P1.1
SEG0 SEG1	O	LCD segment signal output.	10 11	COM0 COM1
SEG2-SEG9	O	LCD segment signal output.	12 - 19	–
SEG10-SEG17	O	LCD segment signal output.	20 - 27	P2.7 - P2.0
COM0 COM1	O	LCD common signal output.	8 9	–
COM2 COM3	O	LCD common signal output.	10 11	SEG0 SEG1
XT_{IN} XT_{OUT}	–	Crystal oscillator pins for subsystem clock.	2 3	–
V_{DD}	–	Main power supply.	32	–
V_{SS}	–	Ground.	1	–
RESET	I	Chip reset signal input.	7	–
TEST	I	Chip test signal input (must be connected to V_{SS}).	4	–

Table 1-1. S3C7281 Pin Descriptions (Continued)

Pin Name	Pin Type	Share Pin	Circuit Type	RESET Value
P0.0 - P0.2 P0.3	I/O	CLO, BUZ, BUZ	E-2	Input
P1.0 - P1.1	I/O	KS0, KS1	E-2	Input
P2.0 - P2.7	O	SEG17 - SEG10	H-28	Low output
COM0, COM1	O	–	H-4	Low output
COM2, COM3	O	SEG0, SEG1	H-6	Low output
SEG2 - SEG9	O	–	H-5	Low output
SEG10 - SEG17	O	P2.7 - P2.1	H-28	Low output
V_{DD}	–	–	–	–
V_{SS}	–	–	–	–
RESET	I	–	B	–
XT_{IN}, XT_{OUT}	–	–	–	–
TEST	I	–	–	–

PIN CIRCUIT DIAGRAMS

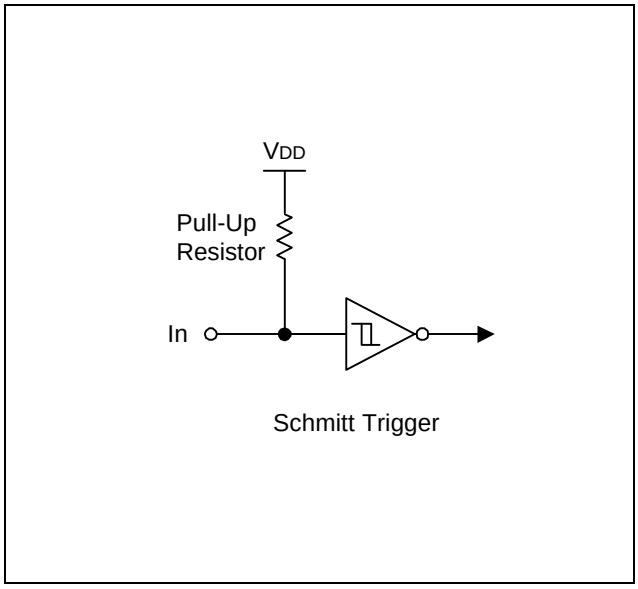


Figure 1-3. Pin Circuit Type B

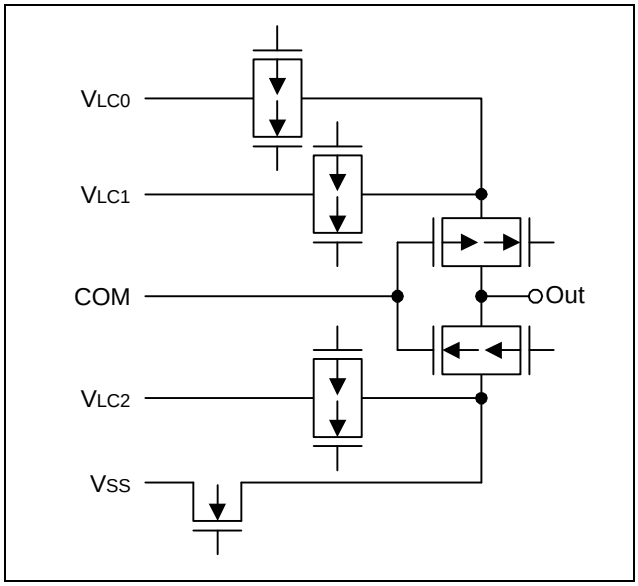


Figure 1-5. Pin Circuit Type H-4

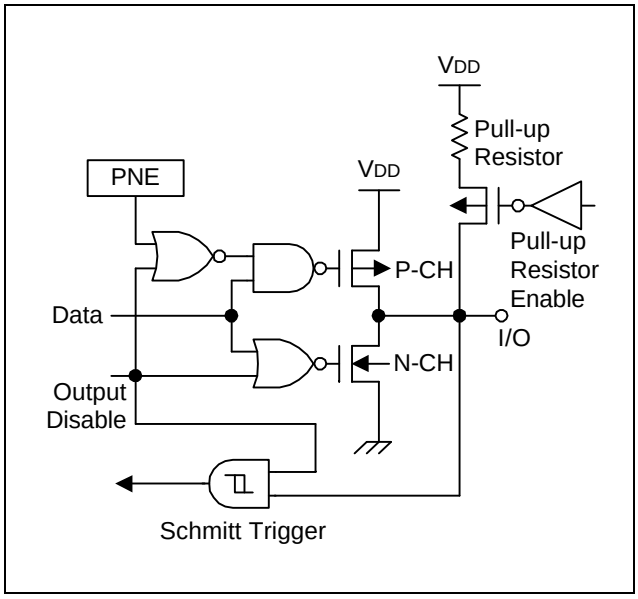


Figure 1-4. Pin Circuit Type E-2

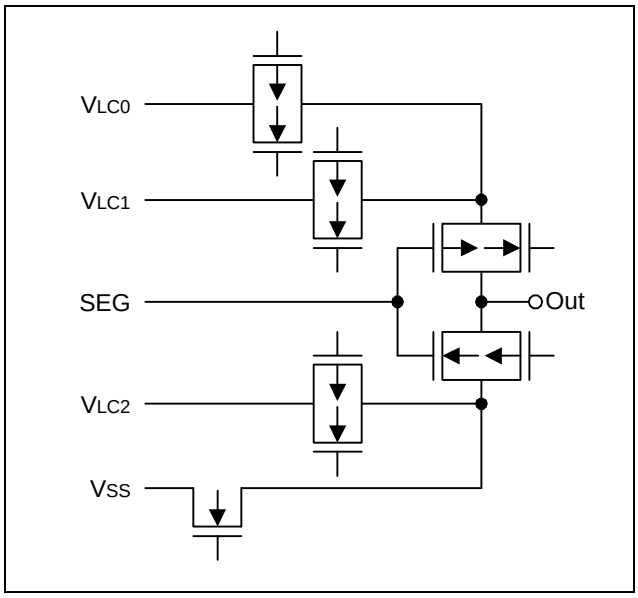


Figure 1-6. Pin Circuit Type H-5

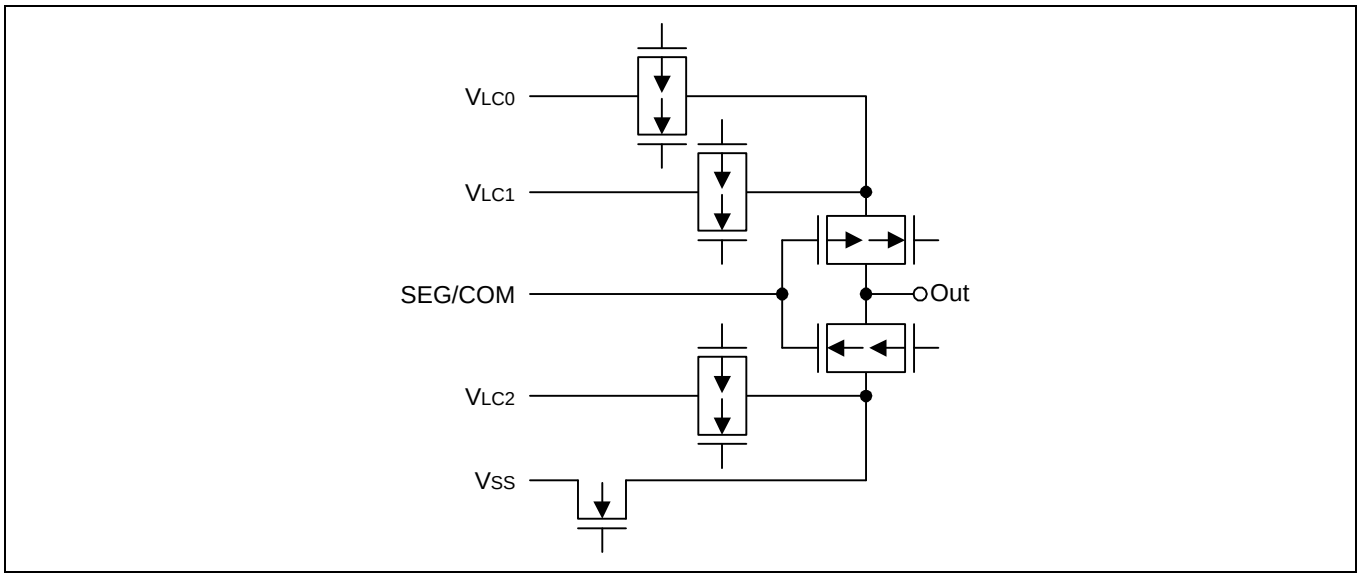


Figure 1-7. Pin Circuit Type H-6

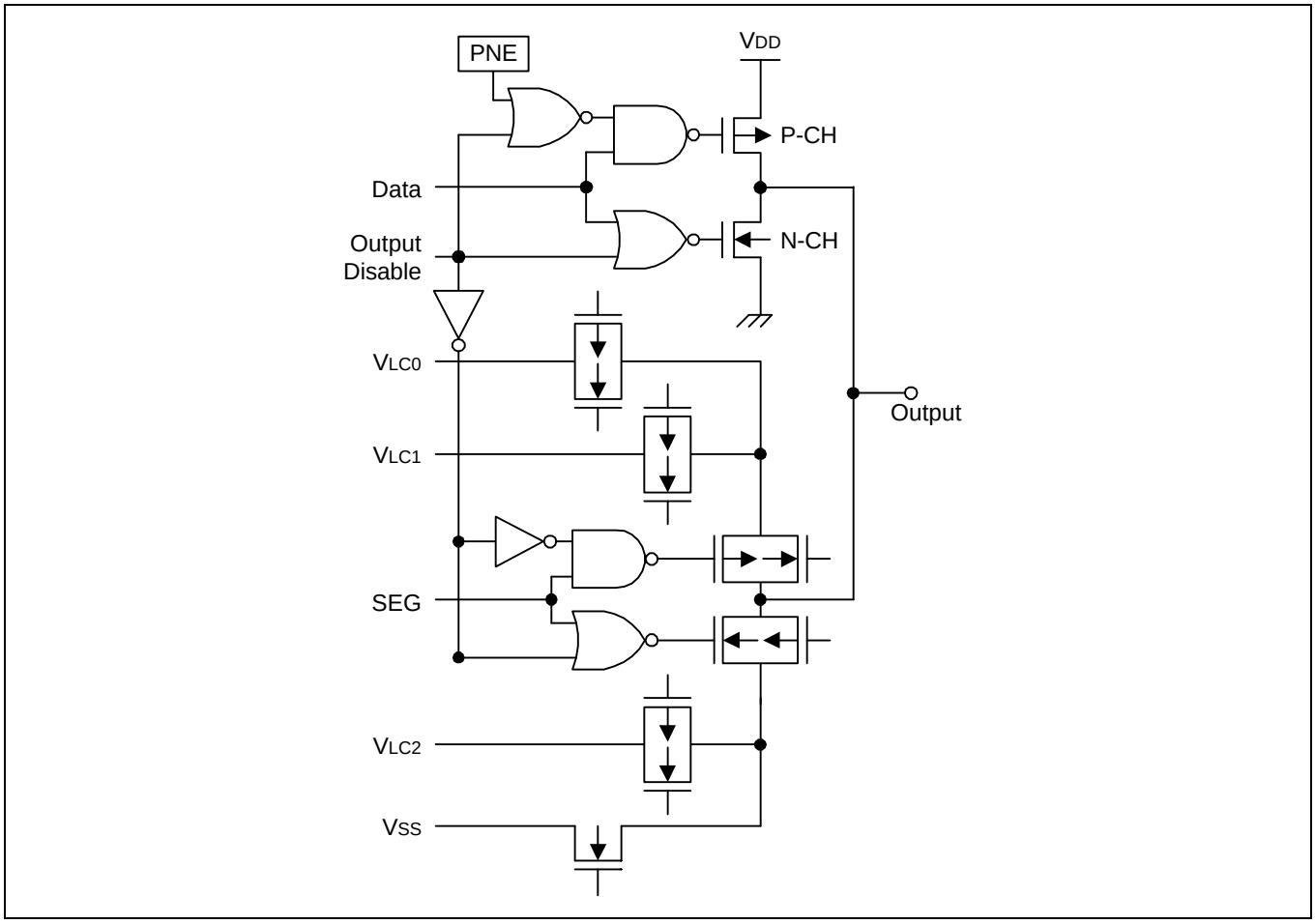


Figure 1-8. Pin Circuit Type H-28

13 ELECTRICAL DATA

OVERVIEW

In this section, information on S3C7281 electrical characteristics is presented as tables and graphics. The information is arranged in the following order:

Standard Electrical Characteristics

— Absolute maximum ratings
— D.C. electrical characteristics
— Power-On Reset Circuit characteristics
— Subsystem clock oscillator characteristics
— I/O capacitance
— A.C. electrical characteristics
— Operating voltage range

Miscellaneous Timing Waveforms

— A.C timing measurement point
— Power-On Reset timing
— Clock timing measurement at XT_{IN}
— TCL timing
— Input timing for RESET
— Input timing for external interrupts
— Serial data transfer timing

Stop Mode Characteristics and Timing Waveforms

— RAM data retention supply voltage in stop mode
— Stop mode release timing when initiated by RESET
— Stop mode release timing when initiated by an interrupt request

Table 13-1. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	V_{DD}	–	– 0.3 to + 6.5	V
Input Voltage	VI	Ports 0, 1	– 0.3 to V_{DD} + 0.3	V
Output Voltage	VO	–	– 0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O pin active	– 15	mA
		All I/O pins active	– 30	
Output Current Low	I_{OL}	One I/O pin active	+ 30 (Peak value)	mA
			+ 15(note)	
		Total for pins 0, 1, 2	+ 100 (Peak value)	
			+ 60(note)	
Operating Temperature	T_A	–	– 40 to + 85	°C
Storage Temperature	T_{STG}	–	– 65 to + 150	°C

NOTE: The values for Output Current Low (I_{OL}) are calculated as Peak Value $\times \sqrt{\text{Duty}}$.

Table 13-2. D.C. Electrical Characteristics

(T_A = - 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH1}	Ports 0, 1, and RESET	0.8V_{DD}	–	V_{DD}	V
	V_{IH2}	XT_{IN}	V_{DD} – 0.1		V_{DD}	
Input Low Voltage	V_{IL1}	Ports 0, 1, and RESET	–	–	0.2V_{DD}	V
	V_{IL2}	XT_{IN}			0.1	
Output High Voltage	V_{OH}	V_{DD} = 4.5 V to 5.5 V I_{OH} = - 1 mA Ports 0, 1, 2	V_{DD} – 1.0	–	–	V
Output Low Voltage	V_{OL}	V_{DD} = 4.5 V to 5.5 V I_{OL} = 15 mA Ports 0, 1, 2	–	–	2.0	V
		V_{DD} = 1.8 V to 5.5 V I_{OL} = 1.6 mA			0.4	

Table 13-2. D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Leakage Current	I_{LIH1}	$V_I = V_{DD}$ All input pins except those specified below for I_{LIH2}	–	–	3	µA
	I_{LIH2}	$V_I = V_{DD}$ XT_{IN}			20	
Input Low Leakage Current	I_{LIL1}	V_I = 0 V All input pins except RESET and XT_{IN}	–	–	– 3	
	I_{LIL2}	V_I = 0 V XT_{IN}			– 20	
Output High Leakage Current	I_{LOH}	$V_O = V_{DD}$ All output pins	–	–	3	
Output Low Leakage Current	I_{LOL}	V_O = 0 V All output pins	–	–	– 3	
Pull-Up Resistor	R_{L1}	V_I = 0 V; V_{DD} = 5V Ports 0, 1	25	50	75	kΩ
		V_{DD} = 3V	50	100	150	
	R_{L2}	V_I = 0 V; V_{DD} = 5V; RESET	100	200	300	
		V_{DD} = 3V	250	500	750	
LCD Voltage Dividing Resistor	R_{LCD}	T_A = + 25 °C	120	170	220	
$\lvert V_{LC0}$-COMi$\rvert$ Voltage Drop (i = 0-3)	V_{DC}	– 15 uA per common pin	–	–	120	mV
$\lvert V_{LC0}$-SEGx$\rvert$ Voltage Drop (x = 0–17)	V_{DS}	– 15 uA per common pin	–	–	120	
Middle Output Voltage (note)	V_{LC0}	V_{DD} = 1.8V to 5.5V, 1/3 bias	V_{DD}-0.2	V_{DD}	V_{DD}+0.2	V
	V_{LC1}	LCD clock = 0Hz	$2V_{DD}/3$-0.2	$2V_{DD}/3$	$2V_{DD}/3$+0.2	
	V_{LC2}		$V_{DD}/3$-0.2	$V_{DD}/3$	$V_{DD}/3$+0.2	

NOTE: It is middle output voltage when 1/4 duty and 1/3 bias.

Table 13-2. D.C. Electrical Characteristics (Continued)

(T_A = - 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply Current (1) Disable LVR (5)	I_{DD1} (2)	V_{DD} = 5 V ± 10% Internal RC oscillator	1.15 MHz	–	1.0	2.5	mA
		V_{DD} = 3 V ± 10%	1 MHz		0.5	1.2	
	I_{DD2} (2)	Idle mode V_{DD} = 5 V ± 10% Internal RC oscillator	1.15 MHz		0.5	1.0	
		V_{DD} = 3 V ± 10%	1 MHz		0.15	0.4	
	I_{DD3} (3)	V_{DD} = 3 V ± 10% 32 kHz crystal oscillator		–	12.0	24	µA
	I_{DD4} (3)	Idle mode; V_{DD} = 3 V ± 10% 32 kHz crystal oscillator			5.0	15	
	I_{DD5}	Stop mode; V_{DD} = 5 V ± 10%	SCMOD = 0000B		2.5	5	
		Stop mode; V_{DD} = 3 V ± 10%	XT_{IN} = 0V		0.5	3	
		V_{DD} = 5 V ± 10%	SCMOD =		0.2	3	
		V_{DD} = 3 V ± 10%	0000B		0.1	2	

NOTES:

1. Currents in the following circuits are not included; on-chip pull-up resistors, internal LCD voltage dividing resistors, output port drive currents.
2. Data includes power consumption for subsystem clock oscillation.
3. When the system clock control register, SCMOD, is set to 1001B, main system clock oscillation stops and the subsystem clock is used.
4. Every values in this table is measured when the power control register (PCON) is set to "0011B".
5. Current in the LVR circuit is not included.

Table 13-2. D.C. Electrical Characteristics (Concluded)

(T_A = - 40 °C to + 85 °C, V_{DD} = 2.2 V to 5.5 V)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Supply Current (1) Enable LVR (5)	I_{DD1} (2)	V_{DD} = 5 V ± 10% Internal RC oscillator	1.15 MHz	–	1.12	2.7	mA
		V_{DD} = 3 V ± 10%	1 MHz		0.6	1.35	
	I_{DD2} (2)	Idle mode V_{DD} = 5 V ± 10% Internal RC oscillator	1.15 MHz		0.62	1.2	
		V_{DD} = 3 V ± 10%	1 MHz		0.25	0.55	
	I_{DD3} (3)	V_{DD} = 3 V ± 10% 32 kHz crystal oscillator		–	112.0	174	µA
	I_{DD4} (3)	Idle mode; V_{DD} = 3 V ± 10% 32 kHz crystal oscillator			105.0	165	
	I_{DD5}	Stop mode; V_{DD} = 5 V ± 10%	SCMOD = 0000B XT_{IN} = 0V		122.5	205	
		Stop mode; V_{DD} = 3 V ± 10%			100.5	153	
		V_{DD} = 5 V ± 10%	SCMOD =		120.2	203	
		V_{DD} = 3 V ± 10%	0000B		100.1	152	

NOTES:

1. Currents in the following circuits are not included; on-chip pull-up resistors, internal LCD voltage dividing resistors, output port drive currents.
2. Data includes power consumption for subsystem clock oscillation.
3. When the system clock control register, SCMOD, is set to 1001B, main system clock oscillation stops and the subsystem clock is used.
4. Every values in this table is measured when the power control register (PCON) is set to "0011B".
5. When LVR is enabled, the LVR circuit needs 100µA or more current on the all below mode.

Table 13-3. Power-On Reset Circuit Characteristics

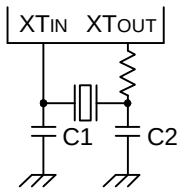
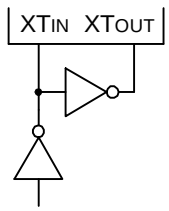
(T_A = - 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power-On Reset Voltage High	V_{DDH}	–	2.2	–	5.5	V
Power-On Reset Voltage Low	V_{DDL}	–	0	1.8	2.0	V
Power Supply Voltage Rise Time	t_R	–	10	–	(1)	µS
Power Supply Voltage Off Time	t_{OFF}	–	0.5	–	–	S
Power-On Reset Circuit Consumption Current (2)	I_{DDPR}	V_{DD} = 5 V ± 10%	–	120	200	µA
		V_{DD} = 3 V ± 10%	–	100	150	

NOTE:
1. 2**5/fx(= 8.19ms at fx = 1MHz)
2. Current consumed when power-on reset circuit is provided internally.

Table 13-4. Sub System Clock Oscillator Characteristics

(T_A = - 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Crystal Oscillator		Oscillation frequency(1)	–	32	32.768	35	kHz
		Stabilization time (2)	V_{DD} = 2.7 V to 5.5 V	–	1.0	2	s
			V_{DD} = 1.8 V to 5.5 V	–	–	10	
External Clock		XT_{IN} input frequency (1)	–	32	–	100	kHz
		XT_{IN} input high and low level width (t_{XTL}, t_{XTH})	–	5	–	15	µS

NOTES:
1. Oscillation frequency and XT_{IN} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs.

Table 13-5. Input/Output Capacitance

(T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Capacitance	C_{IN}	f = 1 MHz; Unmeasured pins are returned to V_{SS}	–	–	15	pF
Output Capacitance	C_{OUT}		–	–	15	pF
I/O Capacitance	C_{IO}		–	–	15	pF

Table 13-6. A.C. Electrical Characteristics

(T_A = - 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction Cycle Time (note)	t_{CY}	V_{DD} = 1.8 V to 5.5 V	4	–	80	µS
		With subsystem clock (fxt)	114	122	125	
Interrupt Input High, Low Width	f_{INTH}, f_{INTL}	KS0, KS1	10	–	–	
RESET Input Low Width	t_{RSL}	Input	10	–	–	

NOTE: Unless otherwise specified, Instruction Cycle Time condition values assume a main system clock (fx) source.

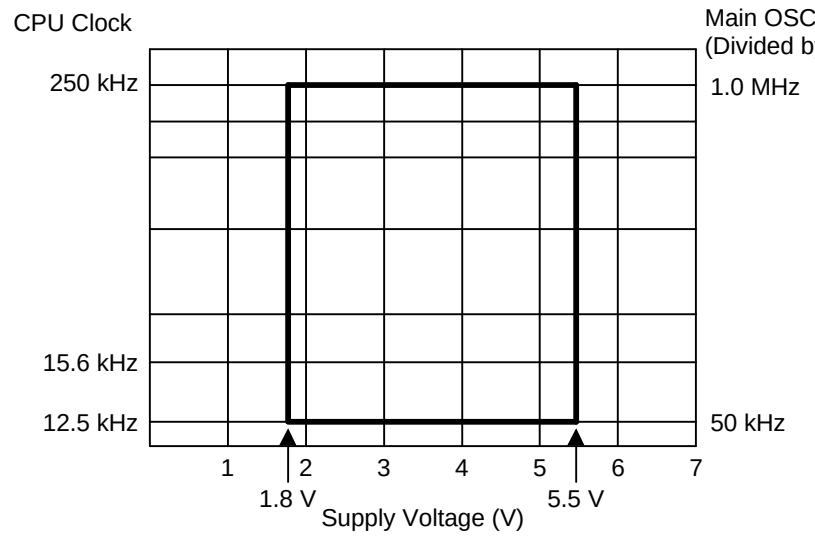


Figure 13-1. Standard Operating Voltage Range

Table 13-7. RAM Data Retention Supply Voltage in Stop Mode

(T_A = - 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	–	1.8	–	5.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8 V	–	0.1	10	µA
Release signal set time	t_{SREL}	–	0	–	–	µS
Oscillator stabilization wait time (1)	t_{WAIT}	Released by RESET	–	2^{17} / fx	–	ms
		Released by interrupt	–	(2)	–	

NOTES:

1. During oscillator stabilization wait time, all CPU operations must be stopped to avoid instability during oscillator start-up.
2. Use the basic timer mode register (BMOD) interval timer to delay execution of CPU instructions during the wait time.

TIMING WAVEFORMS

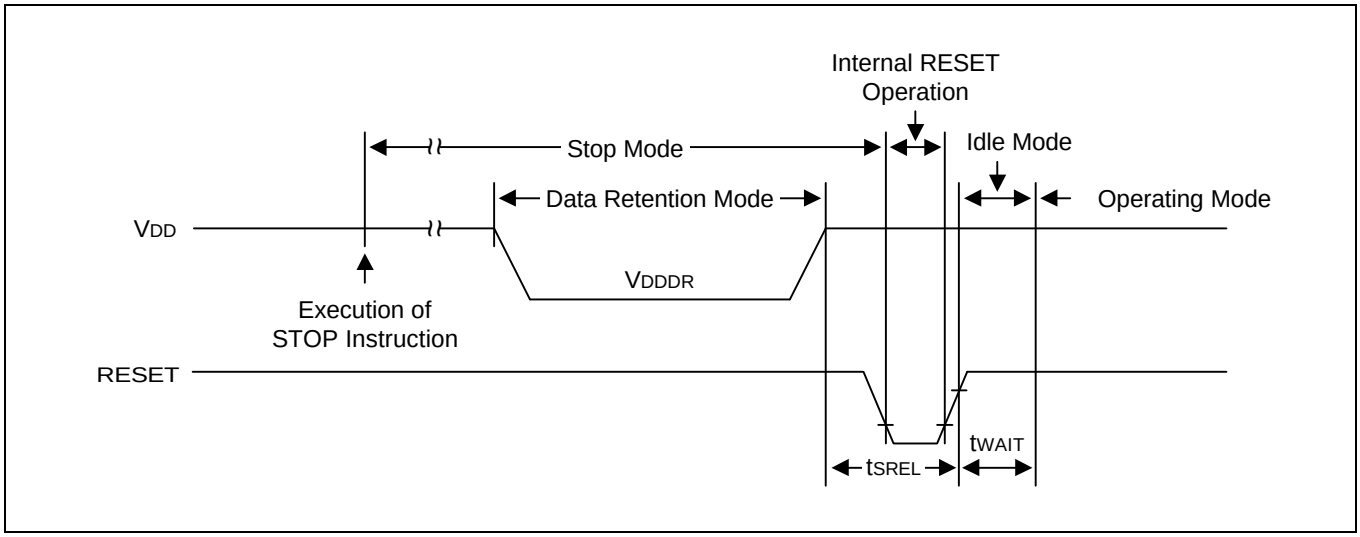


Figure 13-2. Stop Mode Release Timing When Initiated by RESET

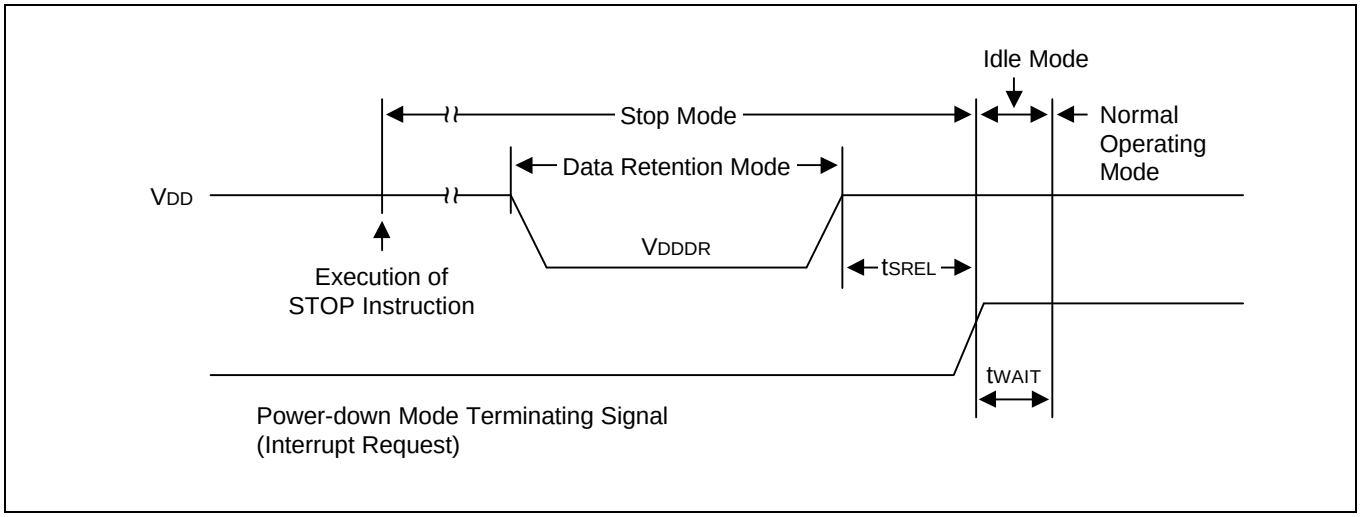


Figure 13-3. Stop Mode Release Timing When Initiated by Interrupt Request

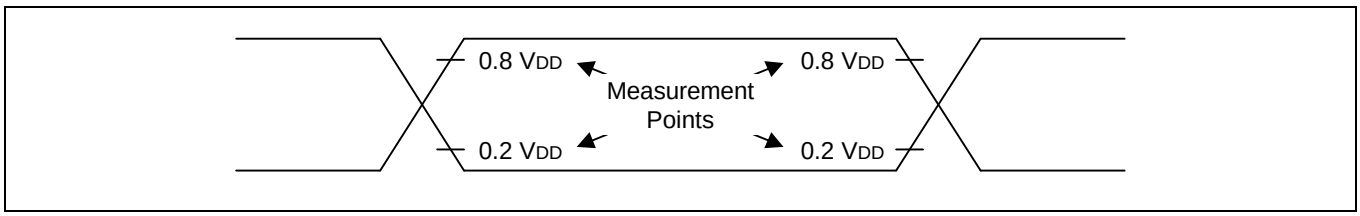


Figure 13-4. A.C. Timing Measurement Points (Except for XT_{IN})

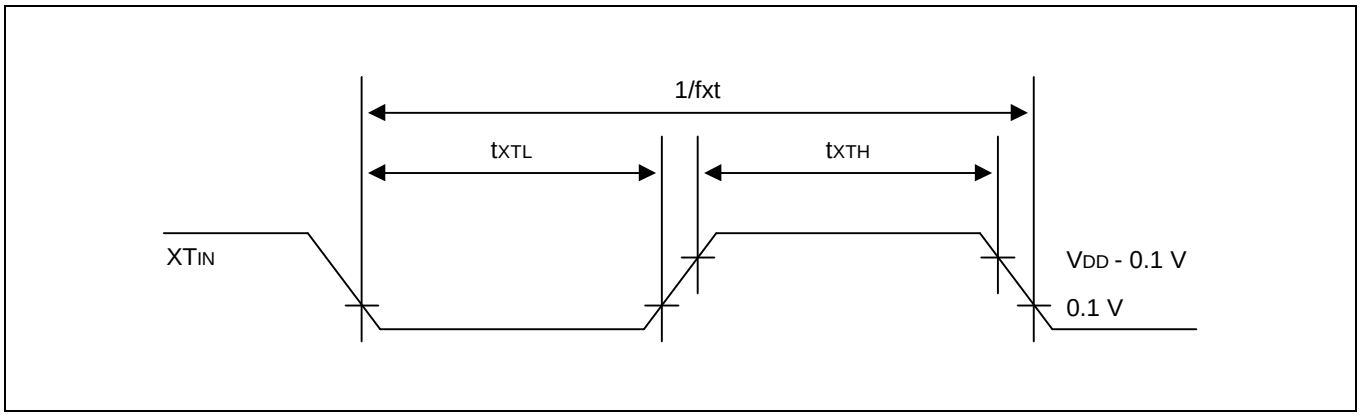


Figure 13-5. Clock Timing Measurement at XT_{IN}

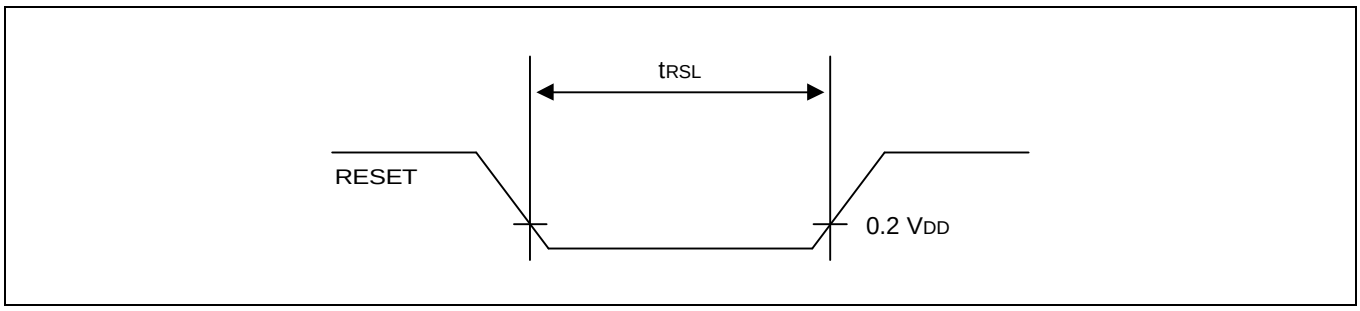


Figure 13-6. Input Timing for RESET Signal

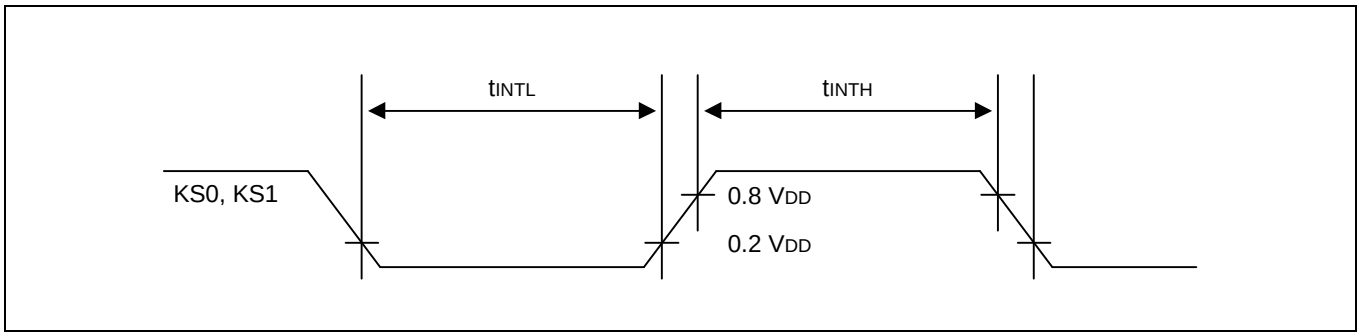


Figure 13-7. Input Timing for External Quais-Interrupts

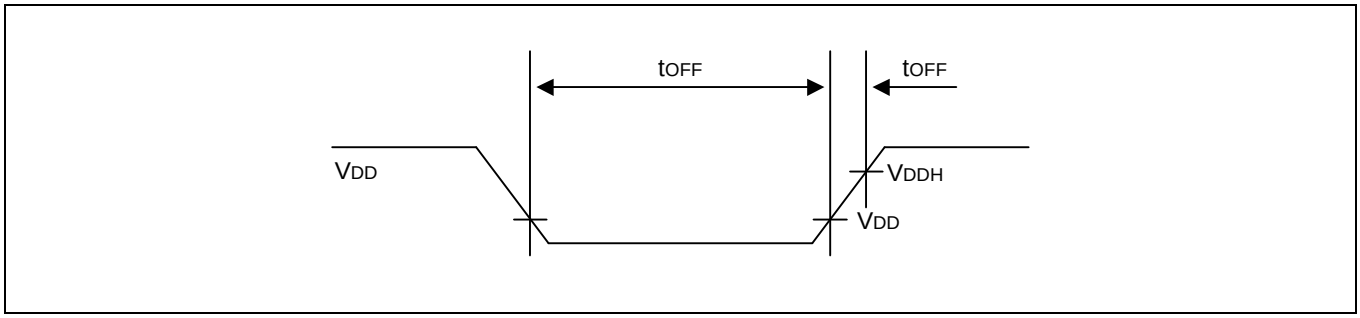


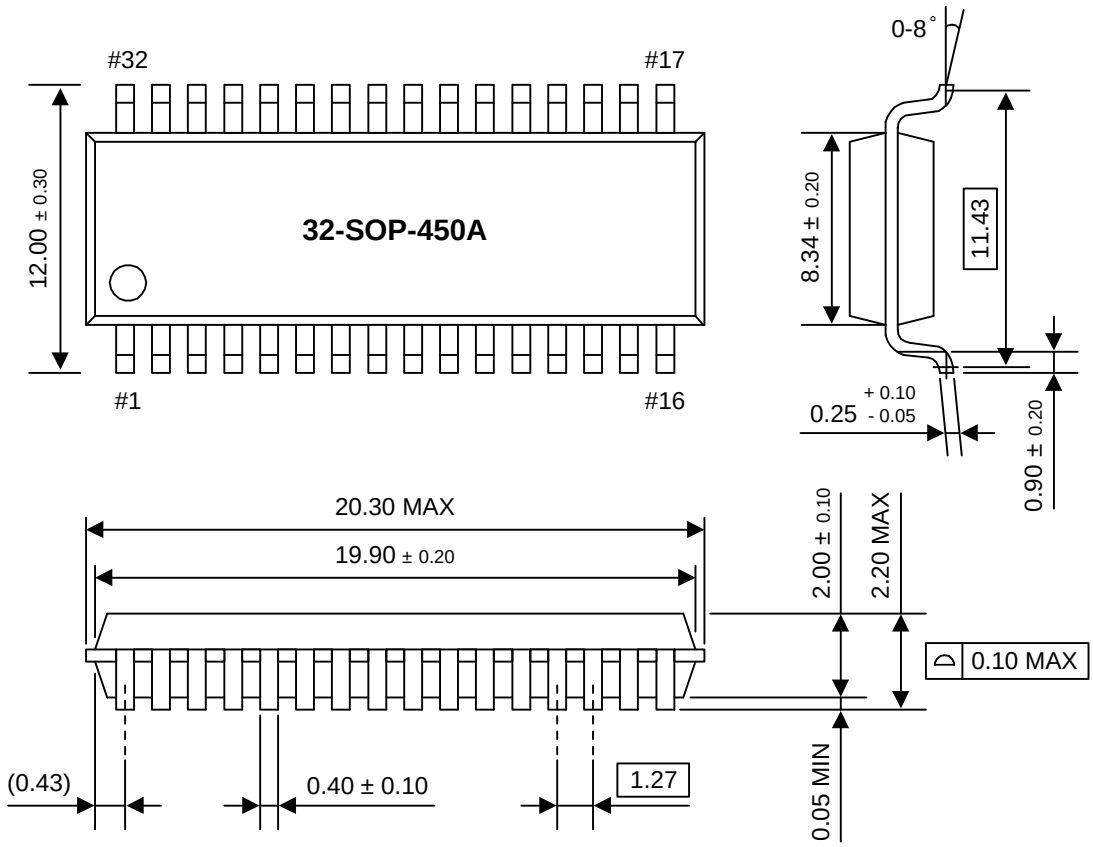
Figure 13-8. Power-On Reset timing

14 MECHANICAL DATA

OVERVIEW

This section contains the following information about the device package:

— Package dimensions in millimeters
— Pad diagram



NOTE: Dimensions are in millimeters.

Figure 14-1. 32-SOP Package Dimensions