National Semiconductor

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LM1276
150 MHz I²C Compatible RGB Preamplifier with Internal 512 Character OSD ROM, 512 Character RAM and 4 DACs

General Description

The LM1276 pre-amp is an integrated CMOS CRT preamp with an integrated Hi-Brite Window generator, 512 Character OSD generator, and an auto size measurement circuit. It has an I²C compatible interface, which allows control of all the parameters necessary to directly setup and adjust the gain and contrast in the CRT display. Brightness and bias can be controlled through the DAC outputs, which are well matched to the LM2479 and LM2480 integrated bias clamp ICs. The LM1276 preamp is also designed to be compatible with the LM247x high gain driver family.

Black level clamping of the video signal is carried out directly on the AC coupled input signal into the high impedance preamplifier input, thus eliminating the need for additional clamp capacitors. Horizontal and vertical blanking of the outputs is provided. Vertical blanking is optional and its duration is register programmable.

The IC is packaged in an industry standard 28-lead narrow DIP molded plastic package.

Features

- Integrated Hi-Brite Window Generator operation independent of the Microcontroller.
- Programmable Video Emphasis Control.
- 8 Programmable Hi-Brite Windows.
- Hi-Brite Enhancement on full screen, window only, or outside of windows.
- Fully addressable 512 Character OSD.
- Internal 512 character OSD ROM usable as either (a) 384 2-color plus 128 4-color characters, (b) 640 2-color characters, or (c) some combination in between.
- Internal 512 character RAM.
- Enhanced I²C compatible microcontroller interface to allow versatile Page RAM access.
- OSD Window Fade In/Fade Out.
- OSD Variable Tone Transparency.
- 3 Bit OSD Contrast.
- Video Data detection for Auto Centering & Sizing.
- 2 Bit Adjustable Burn-in screen Mode with no video input.
- 4 DAC outputs (8-bit resolution) for bus controlled CRT bias and brightness.
- Spot killer, which blanks the video outputs when V_{CC} falls below the specified threshold.
- Suitable for use with discrete or integrated clamp, with software configurable brightness mixer.
- Programmable ABL Onset for Multi-Limit Applications.
- 4-Bit Programmable start position for internal Horizontal Blanking.
- Horizontal blanking and OSD synchronization directly from deflection signals. The blanking can be disabled, if desired.
- Vertical blanking and OSD synchronization directly from sync signals. The blanking width is register programmable and can be disabled, if desired.
- Power Saving Mode with 65% power reduction.
- Matched to LM246x, LM247x drivers, and LM2479/80 bias IC's.

Applications

- Ideal preamplifier IC for total Hi-Brite Solution.
- 17" and 19" bus controlled monitors with OSD.
- Low cost systems with LM247x drivers.

Internal Block Diagram

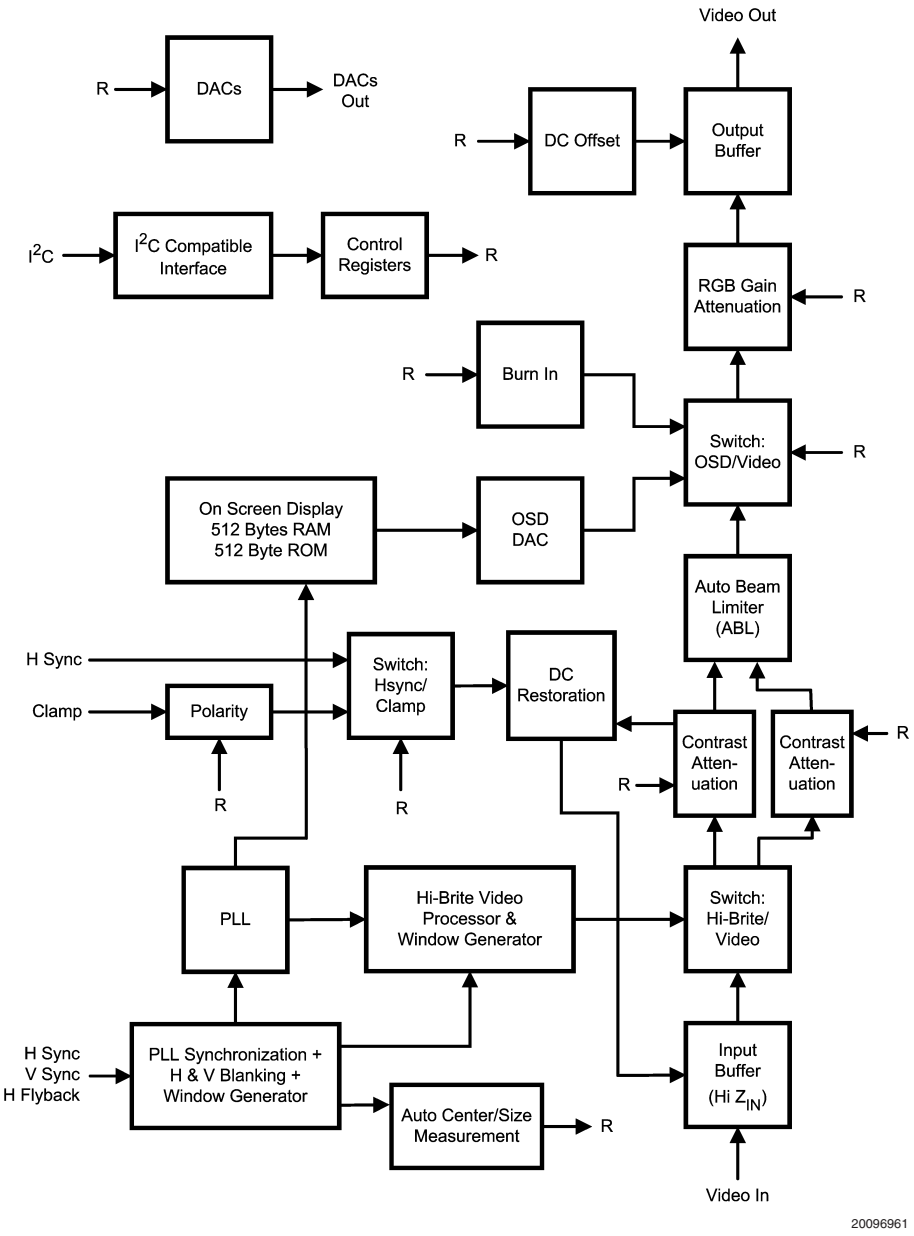


FIGURE 1. Block Diagram

Internal Block Diagram (Continued)

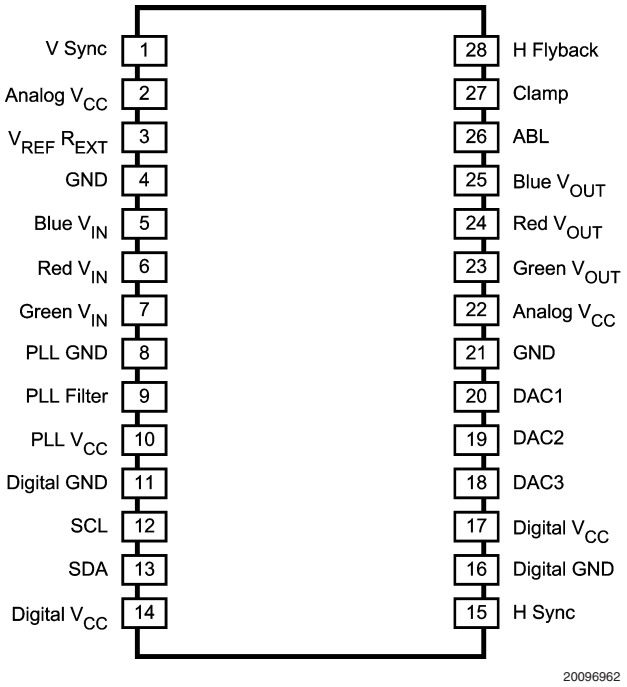


FIGURE 2. LM1276 Pinout
Order Number LM1276AAA/NA
See NS Package Number N28D

Absolute Maximum Ratings (Notes 1, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage V_{CC}, Pins 10, 14, 17, and 22	6.0V
Peak Video DC Output Source Current (Any One Amp) Pins 23, 24 or 25	1.5 mA
Voltage at Any Input Pin (V_{IN})	$-0.5V \le V_{IN} \le V_{CC}+0.5V$
Video Inputs (pk-pk)	$0.0V \le V_{IN} \le 1.2V$
Thermal Resistance to Ambient (θ_{JA})	51˚C/W
Power Dissipation (P_D) (Above 25˚C Derate Based on θ_{JA} and T_J)	2.4W
Thermal Resistance to Case (θ_{JC})	32˚C/W
Junction Temperature (T_J)	150˚C
ESD Susceptibility (Note 4)	3.0 kV
ESD Machine Model (Note 13)	350V
Storage Temperature	–65˚C to +150˚C
Lead Temperature (Soldering, 10 sec.)	265˚C

Operating Ratings (Note 2)

Temperature Range	0˚C to +70˚C
Supply Voltage V_{CC}	$4.75V \le V_{CC} \le 5.25V$
Video Inputs (pk-pk)	$0.0V \le V_{IN} \le 1.0V$

Video Signal Electrical Characteristics

Unless otherwise noted: T_A = 25˚C, V_{CC} = +5.0V, V_{IN} = 0.70 V_{P-P}, $V_{ABL} = V_{CC}$, C_L = 8 pF, Video Outputs = 2.0 V_{P-P}. Setting numbers refer to the definitions in *Table 1*. See (Note 7) for Min and Max parameters and (Note 6) for Typicals.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_S	Supply Current	Test Setting 1, both supplies, no output loading. See (Note 8).		220	300	mA
I_{S-PS}	Supply Current, Power Save Mode	Test Setting 1, both supplies, no output loading. See (Note 8).		55	85	mA
$V_{O\ BLK\ A-B}$	Typical Video Black Level Difference between Normal Video and Hi-Brite Video.	No AC Input Signal	-50	0	TBD	VDC
$V_{O\ BLK\ A-B,\ CH-CH}$	Typical Channel to Channel Video Black Level Difference between Normal Video and Hi-Brite Video.	No AC Input Signal	-50	0	50	VDC
$V_{O\ BLK}$	Active Video Black Level Output Voltage	Test Setting 4, no AC input signal, DC offset register (0x8438) set to 0xD5.		1.2		VDC
$V_{O\ BLK\ STEP}$	Active Video Black Level Step Size	Test Setting 4, no AC input signal.		100		mVDC
V_O Max	Maximum Video Output Voltage	Test Setting 3, Video in = 0.70 V_{P-P}	4.0	4.3		V
LE	Linearity Error	Test Setting 4, staircase input signal (see (Note 9)).		5		%
t_r	Video Rise Time	(Note 5), 10% to 90%, Test Setting 4, AC input signal.		3.1		ns
OS_R	Rising Edge Overshoot	(Note 5), Test Setting 4, AC input signal.		2		%
t_f	Video Fall Time	(Note 5), 90% to 10%, Test Setting 4, AC input signal.		2.9		ns
OS_F	Falling Edge Overshoot	(Note 5), Test Setting 4, AC input signal.		2		%
BW	Channel Bandwidth (–3 dB)	(Note 5), Test Setting 4, AC input signal.		150		MHz
V_{SEP} 10 kHz	Video Amplifier 10 kHz Isolation	(Note 14), Test Setting 8.		–60		dB
V_{SEP} 10 MHz	Video Amplifier 10 MHz Isolation	(Note 14), Test Setting 8.		–50		dB
A_V Max	Maximum Voltage Gain	Test Setting 8, AC input signal.	3.8	4.1		V/V
A_V C-50%	Contrast Attenuation @ 50%	Test Setting 5, AC input signal.		–5.2		dB
A_V Min/A_V Max	Maximum Contrast Attenuation (dB)	Test Setting 2, AC input signal.		–12		dB

Video Signal Electrical Characteristics (Continued)

Unless otherwise noted: T_A = 25˚C, V_{CC} = +5.0V, V_{IN} = 0.70 V_{P-P}, V_{ABL} = V_{CC}, C_L = 8 pF, Video Outputs = 2.0 V_{P-P}. Setting numbers refer to the definitions in *Table 1*. See (Note 7) for Min and Max parameters and (Note 6) for Typicals.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
A_V G-50%	Gain Attenuation @ 50%	Test Setting 6, AC input signal.		–4.0		dB
A_V G-Min	Maximum Gain Attenuation	Test Setting 7, AC input signal.		–11		dB
A_V Match	Maximum Gain Match between Channels	Test Setting 3, AC input signal.		±0.5		dB
A_V Track	Gain Change between Channels	Tracking when changing from Test Setting 8 to Test Setting 5. See (Note 11).		±0.5		dB
$Vid_{Threshold}$	Video Threshold	Normal Operation		80		mV
V_{ABL} TH	ABL Control Range Upper Limit	(Note 12), Test Setting 4, AC input signal.		4.8		V
V_{ABL} Range	ABL Gain Reduction Range	(Note 12), Test Setting 4, AC input signal.		2.8		V
$A_{V\ 3.5}/A_{V\ Max}$	ABL Gain Reduction at 3.5V	(Note 12), Test Setting 4, AC input signal. V_{ABL} = 3.5V		–2		dB
$A_{V\ 2.0}/A_{V\ Max}$	ABL Gain Reduction at 2.0V	(Note 12), Test Setting 4, AC input signal. V_{ABL} = 2.0V		–12		dB
I_{ABL} Max	ABL Input Current Sink Capability	(Note 12), Test Setting 4, AC input signal.			2.5	mA
V_{ABL} Max	Maximum ABL Input Voltage during Clamping	(Note 12), Test Setting 4, AC input signal. I_{ABL} = I_{ABL} MAX			V_{CC} + 0.1	V
A_V ABL Track	ABL Gain Tracking Error	(Note 9), Test Setting 4, 0.7 V_{P-P} input signal, ABL voltage set to 4.5V and 2.5V.			5.0	%
R_{IP}	Minimum Input Resistance (pins 5, 6, 7)	Test Setting 4.		20		MΩ

OSD Electrical Characteristics

Unless otherwise noted: T_A = 25˚C, V_{CC} = +5.0V. See (Note 7) for Min and Max parameters and (Note 6) for Typicals.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{OSDHIGH}$ max	Maximum OSD Level with OSD Contrast 111	Palette Set at 111, OSD Contrast = 111, Test Setting 3		3.02		V
$V_{OSDHIGH}$ 110	Maximum OSD Level with OSD Contrast 110	Palette Set at 111, OSD Contrast = 110, Test Setting 3		2.91		V
$V_{OSDHIGH}$ 101	Maximum OSD Level with OSD Contrast 101	Palette Set at 111, OSD Contrast = 01, Test Setting 3		2.79		V
$V_{OSDHIGH}$ 100	Maximum OSD Level with OSD Contrast 100	Palette Set at 111, OSD Contrast = 100, Test Setting 3		2.67		V
$V_{OSDHIGH}$ 011	Maximum OSD Level with OSD Contrast 011	Palette Set at 111, OSD Contrast = 011, Test Setting 3		2.55		V
$V_{OSDHIGH}$ 010	Maximum OSD Level with OSD Contrast 010	Palette Set at 111, OSD Contrast = 010, Test Setting 3		2.43		V
$V_{OSDHIGH}$ 001	Maximum OSD Level with OSD Contrast 001	Palette Set at 111, OSD Contrast = 001, Test Setting 3		2.32		V
$V_{OSDHIGH}$ 000	Maximum OSD Level with OSD Contrast 000	Palette Set at 111, OSD Contrast = 000, Test Setting 3		2.20		V
ΔV_{OSD} (Black)	Difference between OSD Black Level and Video Black Level (same channel)	Register 0x8438=0x18, Input Video = Black, Same Channel, Test Setting 8			±130	mV

OSD Electrical Characteristics (Continued)

Unless otherwise noted: T_A = 25˚C, V_{CC} = +5.0V. See (Note 7) for Min and Max parameters and (Note 6) for Typicals.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$\Delta V_{OSD\text{-}black}$ (Track)	Difference between OSD Black Level and Video Black Level between any 2 channels	Register 0x8438=0x18, Input Video = Black, Same Channel, Test Setting 8			±115	mV
ΔV_{OSD} (White)	Output Match between Channels	Palette Set at 111, OSD Contrast = 11, Maximum difference between R, G and B		3		%
$V_{OSD\text{-}out}$ (Track)	Output Variation between Channels	OSD contrast varied from max to min		3		%

DAC Output Electrical Characteristics

Unless otherwise noted: T_A = 25˚C, V_{CC} = +5.0V, V_{IN} = 0.7V, V_{ABL} = V_{CC}, C_L = 8 pF, Video Outputs = 2.0 $V_{P\text{-}P}$. See (Note 7) for Min and Max parameters and (Note 6) for Typicals. DAC parameters apply to all 4 DACs.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{Min\ DAC}$	Min Output Voltage of DAC	Register Value = 0x00		0.5	0.7	V
$V_{Max\ DAC}$ Mode 00	Max Output Voltage of DAC	Register Value = 0xFF, DCF[1:0] = 00b	3.7	4.2		V
$V_{Max\ DAC}$ Mode 01	Max Output Voltage of DAC in DCF Mode 01	Register Value = 0xFF, DCF[1:0] = 01b	1.85	2.35		V
$\Delta V_{Max\ DAC}$ (Temp)	DAC Output Voltage Variation with Temperature	0 < T < 70˚C ambient		±0.5		mV/˚C
$\Delta V_{Max\ DAC}$ (V_{CC})	DAC Output Voltage Variation with V_{CC}	V_{CC} varied from 4.75V to 5.25V, DAC register set to mid-range (0x7F)		50		mV
Linearity	Linearity of DAC over its Range			5		%
Monotonicity	Monotonicity of the DAC Excluding Dead Zones			±0.5		LSB
I_{MAX}	Max Load Current		–1.0		1.0	mA

System Interface Signal Characteristics

Unless otherwise noted: T_A = 25˚C, V_{CC} = +5.0V, V_{IN} = 0.7V, V_{ABL} = V_{CC}, C_L = 8 pF, Video Outputs = 2.0 $V_{P\text{-}P}$. See (Note 7) for Min and Max parameters and (Note 6) for Typicals. DAC parameters apply to all 4 DACs.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{VTH+}	VFLYBACK Positive Switching Guarantee	Vertical Blanking triggered	2.0			V
V_{SPOT}	Spot Killer Voltage	(Note 17), V_{CC} Adjusted to Activate	3.4	3.9	4.3	V
V_{Ref}	V_{Ref} Output Voltage (pin 2)		1.25	1.45	1.65	V
V_{IL} (SCL, SDA)	Logic Low Input Voltage		–0.5		1.5	V
V_{IH} (SCL, SDA)	Logic High Input Voltage		3.0		V_{CC} + 0.5	V
I_L (SCL, SDA)	Logic Low Input Current	SDA or SCL, Input Voltage = 0.4V		±10		µA
I_H (SCL, SDA)	Logic High Input Voltage	SDA or SCL, Input Voltage = 4.5V		±10		µA
V_{OL} (SCL, SDA)	Logic Low Output Voltage	I_O = 3 mA		0.5		V
f_H Min	Minimum Horizontal Frequency	PLL & OSD Functioning		25		kHz
f_H Max	Maximum Horizontal Frequency	PLL & OSD Functioning		110		kHz
$I_{HFB\ IN}$ Max	Horizontal Flyback Input	Current Absolute Maximum during Flyback			5	mA
I_{IN}	Peak Current during Flyback	Design Value		4		mA
$I_{HFB\ OUT}$ Max	Horizontal Flyback Input Current	Absolute Maximum during Scan	–700			µA
I_{OUT}	Peak Current during Scan	Not exact - Duty Cycle Dependent		–550		µA
$I_{IN\ THRESHOLD}$	I_{IN} H-Blank Detection Threshold			0		µA

System Interface Signal Characteristics (Continued)

Unless otherwise noted: T_A = 25˚C, V_{CC} = +5.0V, V_{IN} = 0.7V, V_{ABL} = V_{CC}, C_L = 8 pF, Video Outputs = 2.0 V_{P-P}. See (Note 7) for Min and Max parameters and (Note 6) for Typicals. DAC parameters apply to all 4 DACs.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{H\text{-}BLANK\ ON}$	H-Blank Time Delay - On	+ Zero crossing of I_{HFB} to 50% of output blanking start. I_{24} = +1.5mA		45		ns
$t_{H\text{-}BLANK\ OFF}$	H-Blank Time Delay - Off	– Zero crossing of I_{HFB} to 50% of output blanking end. I_{24} = –100µA		85		ns
V_{BLANK} Max	Maximum Video Blanking Level	Test Setting 4, AC input signal	0		0.25	V
$f_{FREERUN}$	Free Run H Frequency, Including H Blank			42		kHz
$t_{PW\ CLAMP}$	Minimum Clamp Pulse Width	See (Note 15)	200			ns
$V_{CLAMP\ MAX}$	Maximum Low Level Clamp Pulse Voltage	Video Clamp Functioning			2.0	V
$V_{CLAMP\ MIN}$	Minimum High Level Clamp Pulse Voltage	Video Clamp Functioning	3.0			V
I_{CLAMP} Low	Clamp Gate Low Input Current	V_{23} = 2V		–0.4		µA
I_{CLAMP} High	Clamp Gate High Input Current	V_{23} = 3V		0.4		µA
$t_{CLAMP\text{-}VIDEO}$	Time from End of Clamp Pulse to Start of Video	Referenced to Blue, Red and Green inputs	50			ns

Note 1: Limits of Absolute Maximum Ratings indicate below which damage to the device must not occur.

Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 3: All voltages are measured with respect to GND, unless otherwise specified.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Input from signal generator: t_r, t_f < 1 ns.

Note 6: Typical specifications are specified at +25˚C and represent the most likely parametric norm.

Note 7: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may change when the device is not operated under the listed test conditions.

Note 8: The supply current specified is the quiescent current for V_{CC} and 5V Dig with R_L = ∞. Load resistors are not required and are not used in the test circuit, therefore all the supply current is used by the pre-amp.

Note 9: Linearity Error is the maximum variation in step height of a 16 step staircase input signal waveform with a 0.7 V_{P-P} level at the input. All 16 steps equal, with each at least 100 ns in duration.

Note 10: $dt/dV_{CC} = 200*(t_{5.5V}–t_{4.5V})/ ((t_{5.5V} + t_{4.5V}))$ %/V, where: $t_{5.5V}$ is the rise or fall time at V_{CC} = 5.5V, and $t_{4.5V}$ is the rise or fall time at V_{CC} = 4.5V.

Note 11: ΔA_V track is a measure of the ability of any two amplifiers to track each other and quantifies the matching of the three gain stages. It is the difference in gain change between any two amplifiers with the contrast set to A_VC–50% and measured relative to the A_V max condition. For example, at A_V max the three amplifiers' gains might be 12.1 dB, 11.9 dB, and 11.8 dB and change to 2.2 dB, 1.9 dB and 1.7 dB respectively for contrast set to A_VC–50%. This yields a typical gain change of 10.0 dB with a tracking change of ±0.2 dB.

Note 12: The ABL input provides smooth decrease in gain over the operational range of 0 dB to –5 dB: $\Delta A_{ABL} = A(V_{ABL} = V_{ABL\ MAX\ GAIN}) – A\ (V_{ABL} = V_{ABL\ MIN\ GAIN})$. Beyond –5 dB the gain characteristics, linearity and pulse response may depart from normal values.

Note 13: Machine Model ESD test is covered by specification EIAJ IC-121-1981. A 200 pF cap is charged to the specific voltage, then discharged directly into the IC with no external series resistor (resistance of discharge path must be under 50Ω).

Note 14: Measure output levels of the other two undriven amplifiers relative to the driven amplifier to determine channel separation. Terminate the undriven amplifier inputs to simulate generator loading. Repeat test at f_{IN} = 10 MHz for V_{SEP} 10 MHz.

Note 15: A minimum pulse width of 200 ns is the guaranteed minimum for a horizontal line of 15 kHz. This limit is guaranteed by design. If a lower line rate is used then a longer clamp pulse may be required.

Note 16: Adjust input frequency from 10 MHz (A_V max reference level) to the –3 dB corner frequency ($f_{-3\ dB}$).

Note 17: Once the spot killer has been activated, the LM1276 remains in the off state until V_{CC} is cycled (reduced below 0.5V and then restored to 5V).

Hexadecimal and Binary Notation

Hexadecimal numbers appear frequently throughout this document, representing slave and register addresses, and register values. These appear in the format "0x...". For example, the slave address for writing the registers of the LM1276 is hexadecimal BA, written as 0xBA. On the other hand, binary values, where the individual bit values are shown, are indicated by a trailing "b". For example, 0xBA is equal to 10111010b. A subset of bits within a register is referred to by the bit numbers in brackets following the register value. For example, the OSD contrast bits are the fourth, fifth, and sixth bits of register 0x8538. Since the first bit is bit 0, the OSD contrast register is 0x8538[5:3].

Register Test Settings

Table 1 shows the definitions of the Test Settings 1–8 referred to in the specifications sections. Each test setting is a combination of five hexadecimal register values, Contrast, Gain (Blue, Red, Green) and DC offset.

Register Test Settings (Continued)

TABLE 1. Test Settings

Control	No. of Bits	Test Settings							
		1	2	3	4	5	6	7	8
Contrast	7	0x7F (Max)	0x00 Min	0x7F (Max)	0x7F (Max)	0x40 (50.4%)	0x7F (Max)	0x7F (Max)	0x7F (Max)
B, R, G Gain	7	0x7F (Max)	0x7F (Max)	0x7F (Max)	Set V_O to 2 V_{P-P}	0x7F (Max)	0x40 (50.4%)	0x00 (Min)	0x7F (Max)
DC Offset	3	0x00 (Min)	0x05	0x07 (Max)	0x05	0x05	0x05	0x05	0x05

OSD vs Video Intensity

The OSD amplitude has been increased over the LM1237 level. During monitor alignment the three gain registers are used to achieve the desired front of screen color balance. This also causes the OSD channels to be adjusted accordingly, since these are inserted into the video channels prior to the gain attenuators. This provides the means to fine-tune the intensity of the OSD relative to the video as follows. If a typical starting point for the alignment is to have the gains at maximum (0x7F) and the contrast at 0x55, the resultant OSD intensity will be higher than if the starting point is with the gains at 0x55 and the contrast at maximum (0x7F). This tradeoff allows the fine-tuning of the final OSD intensity relative to the video. In addition, the OSD contrast register, 0x85C8[5:3], provides 8 major increments of intensity. Together, these allow setting the OSD intensity to the most pleasing level.

ESD Protection

The LM1276 features a 3.0 kV ESD protection level (see (Notes 4, 13)). This is provided by special internal circuitry, which activates when the voltage at any pin goes beyond the supply rails by a preset amount. This protection is applied to all the pins, including SDA and SCL.

Typical Performance Characteristics V_{CC} = 5V, T_A = 25˚C unless otherwise specified

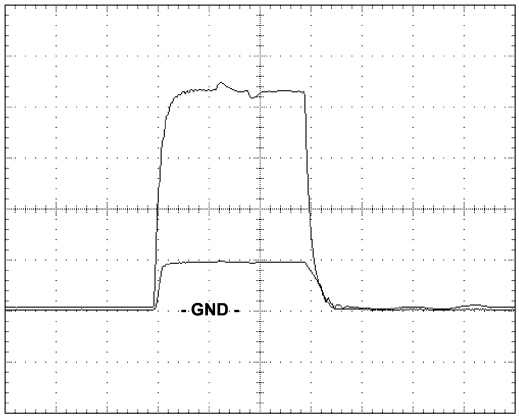


FIGURE 3. Logic Horizontal Blanking

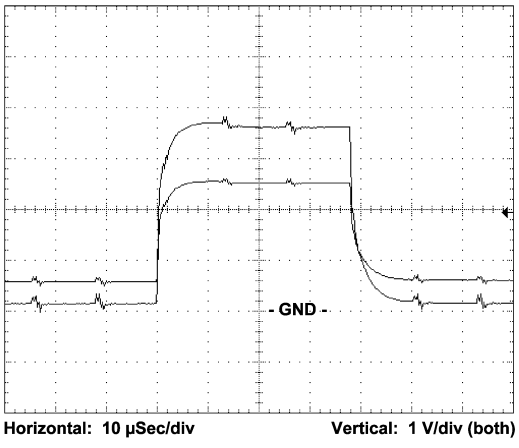


FIGURE 4. Logic Vertical Blanking

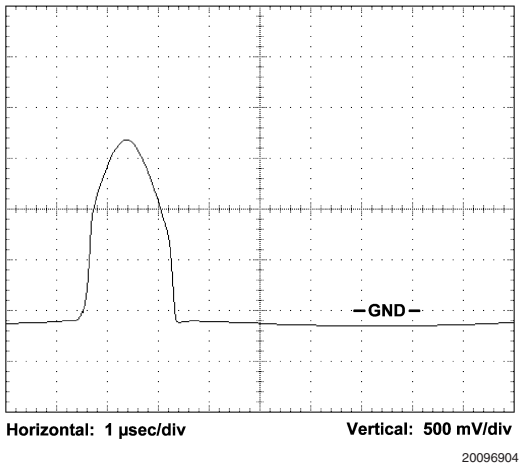


FIGURE 5. Deflection Horizonal Blanking

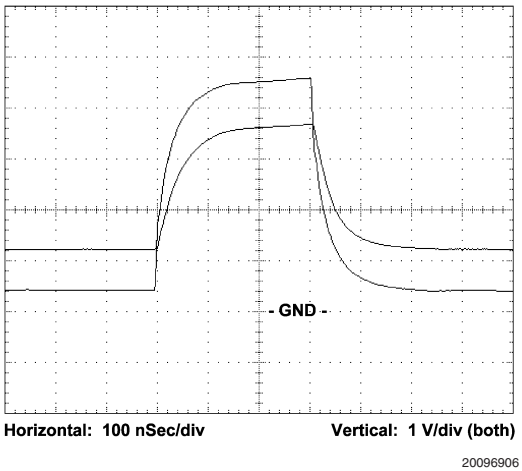


FIGURE 6. Logic Clamp Pulse

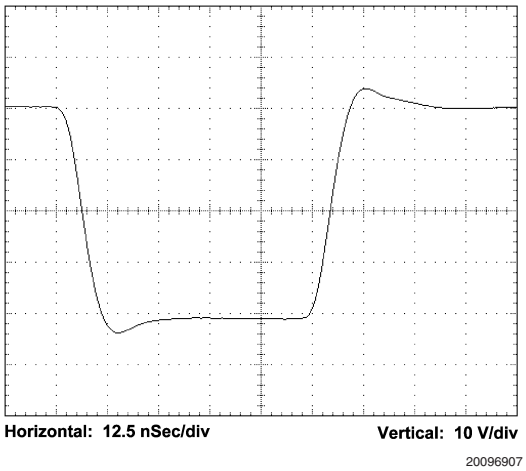


FIGURE 7. Red Cathode Response

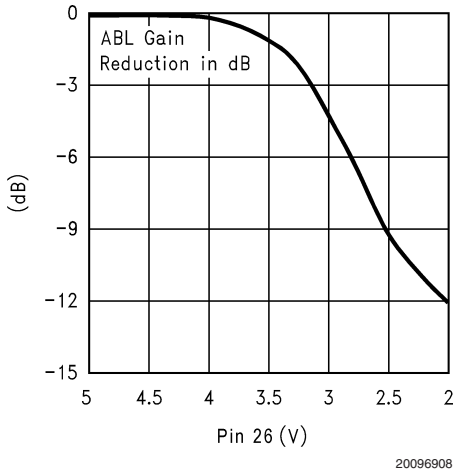


FIGURE 8. ABL Gain Reduction Curve

Typical Performance Characteristics V_{CC} = 5V, T_A = 25˚C unless otherwise specified (Continued)

SYSTEM INTERFACE SIGNALS

The Horizontal Sync, Flyback, Vertical Sync, and the Clamp input signals are important for proper functionality of the LM1276. Both blanking inputs must be present for OSD synchronization. In addition, the Horizontal blanking input also assists in setting the proper cathode black level, along with the Clamping pulse. The Vertical blanking input initiates a blanking level at the LM1276 outputs, which is programmable from 3 to 127 lines (at least 10 is recommended). This input is set up to only accept a vertical sync pulse, and the leading edge is used to start the programmable vertical blanking signal directly. The start position of the internal Horizontal blanking pulse is programmable from 0 to 64 pixels ahead of the start position of the Horizontal flyback input. Both horizontal and vertical blanking can be individually disabled, if desired.

Figure 3 and *Figure 4* show the Horizontal Flyback input when it is logic level and the Vertical input (which must always be logic level). *Figure 3* shows the smaller pin 28 voltage superimposed on the horizontal blanking pulse input to the neck board with R_H = 4.7k and C_1 = 0.1 µF. Note where the voltage at pin 28 is clamped to about 1V when the pin is sinking current. *Figure 4* shows the smaller pin 1 voltage superimposed on the vertical blanking input to the neck board with R_V = 4.7k. These component values correspond to the application circuit of *Figure 9*.

Please note that the Horizontal Flyback signal to pin 28 MUST be continuously provided to the IC, even during energy save or sleep modes. In the application, this signal should be always generated whether the VGA cable is disconnected, the monitor is in energy save mofe, or sleep mode.

Figure 5 show the case where the horizontal input is from deflection. *Figure 5* shows the pin 28 voltage which is derived from a horizontal flyback pulse of 35V peak to peak with R_H = 8.2K and C_1 jumpered.

Figure 6 shows the pin 27 clamp input voltage superimposed on the neck board clamp logic input pulse. R = 1k and should be chosen to limit the pin 27 voltage to about 2.5V peak to peak. This corresponds to the application circuit given in *Figure 9*. The clamp input pin can also be internally connected to the Horizontal Sync pin, thus eliminating the need for a Clamp signal supplied to the neckboard. This can be enabled with register 0x853E[4].

H SYNC & V SYNC

V Sync at pin 1 and H Sync at pin 15 must be supplied with logic level signals generated by the MCU. In an application where a logic level clamp pulse is used, the same signal can be used for the H Sync input. It is important that both V Sync and H Sync are always receiving signals, even during VGA cable disconnect, energy save mode, or sleep mode.

CATHODE RESPONSE

Figure 7 shows the response at the red cathode for the application circuit in *Figures 9, 10*. The input video rise time is 1.5 ns. The resulting leading edge has a 7.1 ns rise time and 7.6% overshoot, while the trailing edge has a 7.1 ns rise time and 6.9% overshoot using an LM2467 driver.

ABL GAIN REDUCTION

The ABL function reduces the contrast level of the LM1276 as the voltage on pin 26 is lowered from V_{CC} to around 2V. *Figure 8* shows the amount of gain reduction as the voltage is lowered from V_{CC} (5.0V) to 2V. The gain reduction is small until V_{26} reaches the knee around 3.7V, where the slope increases. Many system designs will require about 3 dB to 5 dB of gain reduction in full beam limiting. Additional attenuation is possible, and can be used in special circumstances. However, in this case, video performance such as video linearity and tracking between channels will tend to depart from normal specifications.

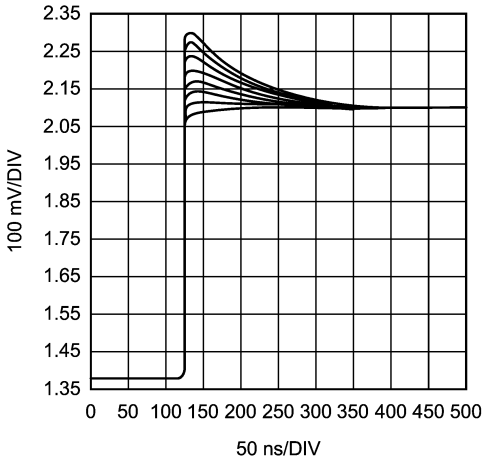
The onset of ABL in the LM1276 is adjustable so that the amount of beam limiting can be varied, especially for larger Hi-Brite window displays where the contrast level is not desired to be reduced as much as a normal video display. The beam current limiting is 4-bit adjustable in steps of 80 µA each all the way up to a delta of 1.2 mA. The value of the ABL pull up resistor (R2) to the external +80V supply must be selected carefully such that the ABL threshold current will be at the desired maximum (i.e. 2 mA) when register 0x85C4 is at the lowest setting, 0x00.

There are 4 different ABL current registers corresponding to 4 different ABL settings. Each setting or register (0x85C4 - 0x85C7) can be assigned a different ABL current threshold. ABL current register 0 can correspond to a minimal area of the screen being highlighted, and ABL current register 4 can correspond to the maximum area of the screen being highlighted. This area is calculated by the HiBrite software, and the particular ABL register that is is to be activated is selected by the software. The values of each register are written by the MCU.

Typical Performance Characteristics V_{CC} = 5V, T_A = 25˚C unless otherwise specified (Continued)

VIDEO PROCESSING

Emphasis, Center Frequency at Maximum



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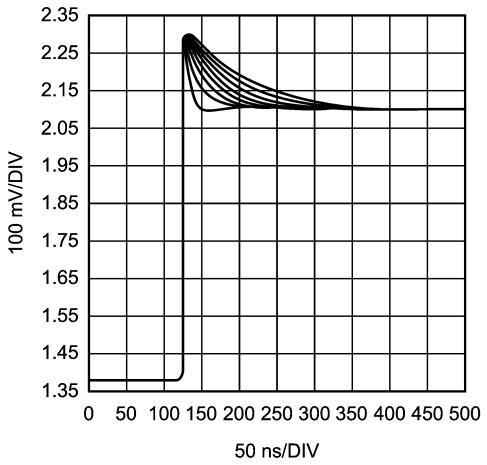
Center Frequency, Emphasis at Maximum



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These two plots show the processing done by the LM1276 on the video input signal. There are two variables for the video processing, emphasis and center frequency. **Emphasis is controlled by bits 0-2 in registers 0x85C8, 0x85CA, or 0x85CC.** This gives 8 different levels of emphasis. In the top plot the center frequency is set at its maximum level and the 8 different levels of emphasis are measured. The video with no emphasis is adjusted to a 0.7 V_{P-P} level. Using maximum emphasis the video is increased to a 0.9 V_{P-P} level at the rising edge of the video. If the falling edge was measured it would show a similar waveform, but going in the negative direction.

Center frequency is shown in the bottom plot. **Control of the center frequency is done with bits 4-7 in register 0x85C1**. This gives 16 adjustments for this feature. Every other adjustment is shown in the bottom plot, since showing all 16 adjustments would have made the plot too difficult to read. The curves closely approximate the peaking of an RC network. Therefore, the term center frequency means the RC time constant that is approximated by each curve in the above plot. A true RC peaking network would give very large overshoot. The LM1276 has special circuitry to clip the very large overshoot, yet has the complete benefit of the RC peaking. This special circuitry allows for much more overshoot than one could do with RC peaking and still not saturate the video channel.

Note that the video channel with the emphasis also has its own independent contrast control. This allows the user to adjust his monitor for a brighter picture within the Hi-Brite window and optimize the emphasis for the resolution he is using with the monitor. Now, the monitor user can give his pictures or video a special “sparkle” when using the capabilities of the LM1276.

OSD PHASE LOCKED LOOP

The PLL in the LM1276 serves both the OSD as well as the Hi-Brite Window generation. The pixels per line range for the LM1276 OSD is from 704 to 1152 pixels per line, in increments of 64. The maximum OSD pixel frequency available is 111 MHz. For example, if the horizontal scan rate is 106 kHz, 1024 pixels per line would be acceptable to use, since the OSD pixel frequency is:

Horizontal Scan Rate X PPL =
106kHz X 1024 = 108.5 MHz

If 1152 pixels per line is being used, the horizontal scan rate would have to be lower than 106 kHz in order to not exceed the maximum OSD pixel frequency of 111 MHz. The maximum number of video lines that may be used is 1536 lines as in a 2048x1536 display. At this line rate, using a PPL setting of 4 is recommended. The LM1276 has a **PLL Auto** feature, which will automatically select an internal PLL frequency range setting that will guarantee optimal OSD locking for any horizontal scan rate and for improved jitter performance over a wider temperature range. This eliminates the need for PLL register settings determined by the user, as well as improved PLL performance. To initialize the PLL Auto feature, set bit, 0x8439[4] to 1. This will effectively perform all necessary calibrations and activate the PLL Auto mode, which takes approximately 2–4 vertical scan period to complete, and must be done while the video is blanked. *Table 2* shows the recommended horizontal scan rate ranges (in kHz) for each pixels per line register setting, 0x8401[7:5]. These ranges are recommended for chip ambient temperatures of 0ºC to 70ºC, and the recommended PLL filter values are 6.2 kΩ, 0.01 uF, and 1000 pF. While the OSD PLL will lock for other register combinations and at scan rates outside these ranges, the performance of the loop will be improved if these recommendations are followed.

PLL AUTO MODE INITIALIZATION SEQUENCE

- Blank video.
- Set 0x8539[4] to 1.
- Wait for at least 2–4 vertical periods or vertical sync pulses to pass.
- Unblank Video.

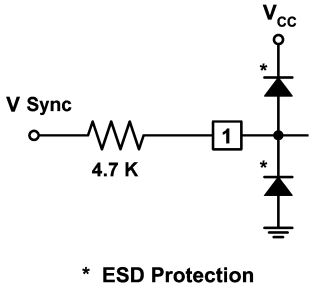
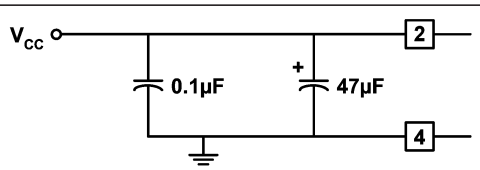
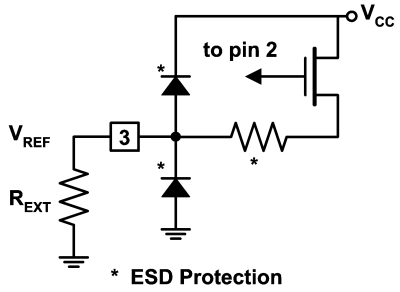
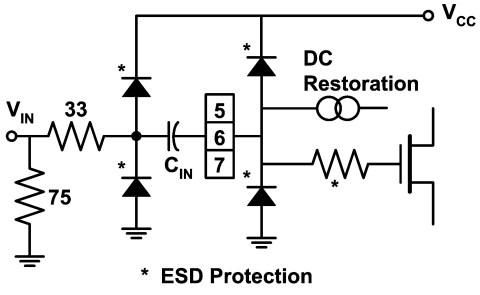
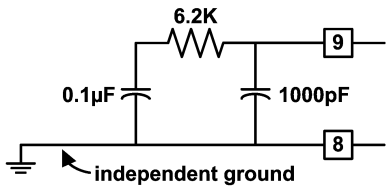
This sequence must be done by the microcontroller at system power up, as well as each time there is a horizontal line rate change from the video source, for the PLL Auto mode to function properly.

Typical Performance Characteristics V_{CC} = 5V, T_A = 25˚C unless otherwise specified (Continued)

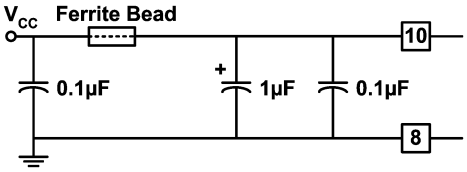
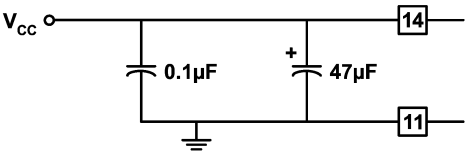
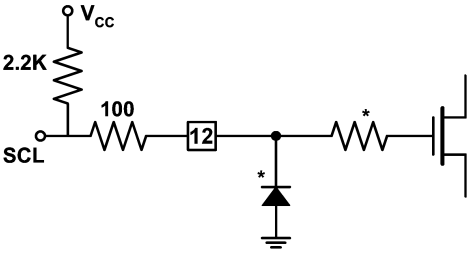
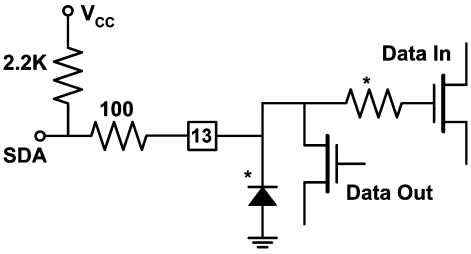
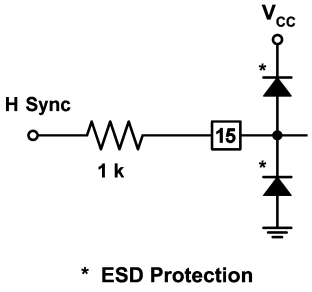
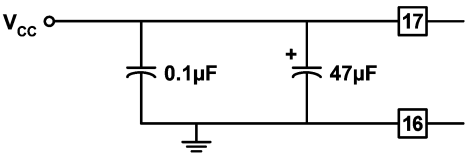
TABLE 2. OSD Register Recommendations

	PPL=0	PPL=1	PPL=2	PPL=3	PPL=4	PPL=5	PPL=6	PPL=7
PLL Auto	25 - 61	25 - 53	25 - 98	25 - 110	25 - 110	25 - 108	25 - 102	25 - 96

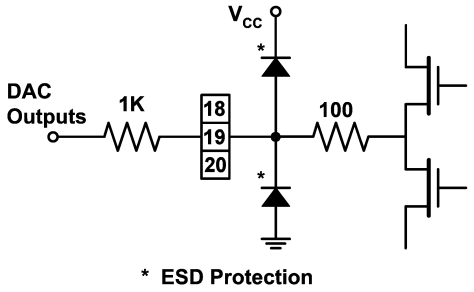
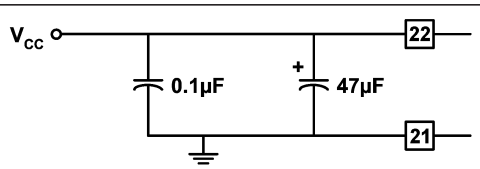
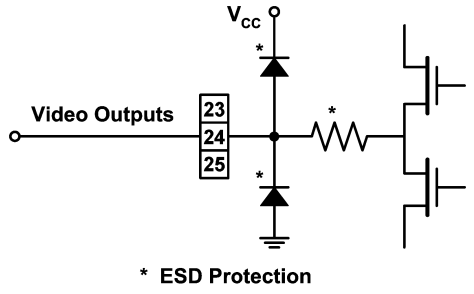
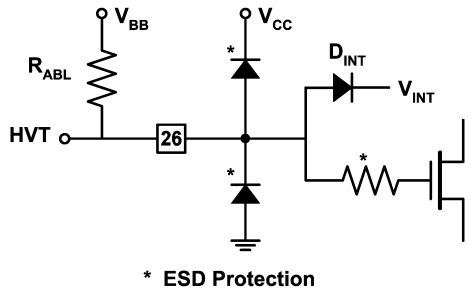
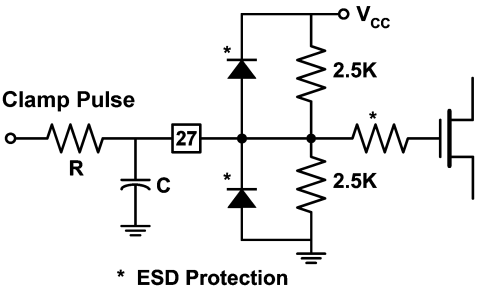
Pin Descriptions and Application Information

Pin No.	Pin Name	Schematic	Description
1	V Sync		Logic level vertical sync signal received from the video card in the PC or sync stripper circuit.
2 4	Analog V_{CC} Analog Ground		Ground pin and power supply pin for the input analog portion of the LM1276. Note the recommended charge storage and high frequency capacitors, which should be as close to pins 2 and 4 as possible.
3	$V_{REF}R_{EXT}$		External current set resistor, 10k 1%, sets the internal bias current level for optimum performance of the LM1276. This resistor should be placed as close to pin 3 and the pin 4 ground return as possible.
5 6 7	Blue Video In Red Video In Green Video In		These video inputs must be AC coupled with a .0047 µF cap. Internal DC restoration is done at these inputs. A series resistor of about 33Ω and external ESD protection diodes should also be used for protection from ESD damage.
8 9	PLL Ground PLL Filter		Recommended topology and values are shown to the left. It is recommended that both filter branches be bypassed to the independent ground as close to pin 8 as possible. Great care should be taken to prevent external signals from coupling into this filter from video, I^2C, etc.

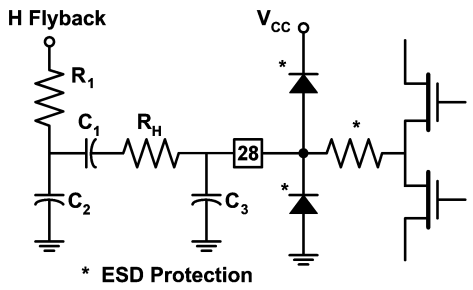
Pin Descriptions and Application Information (Continued)

Pin No.	Pin Name	Schematic	Description
10	PLL V_{CC}		The ground pin should be connected to the rest of the circuit ground by a short but independent PCB trace to prevent contamination by extraneous signals. The PLL V_{CC} pin should be isolated from the rest of the V_{CC} line by a ferrite bead and bypassed to pin 8 with an electrolytic capacitor and a high frequency ceramic.
11 14	Digital Ground Digital V_{CC}		Ground pin and power supply pin for the digital portion of the LM1276. Note the recommended charge storage and high frequency capacitors, which should be as close to pins 11 and 14 as possible.
12	SCL		The I^2C compatible clock line. A pull-up resistor of about 2.2 kΩ should be connected between this pin and V_{CC}. A resistor of at least 100Ω should be connected in series with the clock line for additional ESD protection.
13	SDA		The I^2C compatible data line. A pull-up resistor of about 2.2 kΩ should be connected between this pin and V_{CC}. A resistor of at least 100Ω should be connected in series with the data line for additional ESD protection.
15	H Sync		Logic level horizontal sync signal received from the MCU or sync stripper circuit. This input can also be derived from the clamp input as long as it is a logic level signal.
16 17	Digital Ground Digital V_{CC}		Ground pin and power supply pin for the digital portion of the LM1276. Note the recommended charge storage and high frequency capacitors, which should be as close to pins 16 and 17 as possible.

Pin Descriptions and Application Information (Continued)

Pin No.	Pin Name	Schematic	Description
18 19 20	DAC 3 Output DAC 2 Output DAC 1 Output		DAC outputs for cathode cut-off adjustments and brightness control. The DAC values are set through the I^2C compatible bus. A resistor of at least 1kΩ should be connected in series with these outputs for additional ESD protection.
21 22	Analog Ground Analog V_{CC}		Ground pin and power supply pin for the output analog portion of the LM1276. Note the recommended charge storage and high frequency capacitors which should be as close to pins 21 and 22 as possible.
23 24 25	Green Output Red Output Blue Output		These are the three video output pins. They are intended to drive the LM2476 and LM246X family of cathode drivers. Nominally, about 2V peak to peak will produce 40V peak to peak of cathode drive.
26	ABL		The Automatic Beam Limiter input is biased to the desired beam current limit by R_{ABL} and V_{BB} and normally keeps D_{INT} forward biased. When the current resupplying the CRT capacitance (averaged by C_{ABL}) exceeds this limit, then D_{INT} begins to turn off and the voltage at pin 26 begins to drop. The LM1276 then lowers the gain of the three video channels until the beam current reaches an equilibrium value.
27	CLAMP		This pin accepts either TTL or CMOS logic levels. This pin can also be internally connected to the Horizontal sync pin. The internal switching threshold is approximately one-half of V_{CC}. An external series resistor, R, of about 1k is recommended to avoid overdriving the input devices. In any event, R must be large enough to prevent the voltage at pin 27 from going higher than V_{CC} or below GND.

Pin Descriptions and Application Information (Continued)

Pin No.	Pin Name	Schematic	Description
28	H Flyback		Proper operation requires current reversal. R_H should be large enough to limit the peak current at pin 28 to about +4 mA during blanking, and −500 µA during scan. C_1 is usually needed for logic level inputs and should be large enough to make the time constant, R_HC_1 significantly larger than the horizontal period. R_1 and C_2 are typically 300Ω and 330 pF when the flyback waveform has ringing and needs filtering. C_3 may be needed to filter extraneous noise and can be up to 100 pF.

Schematic Diagram

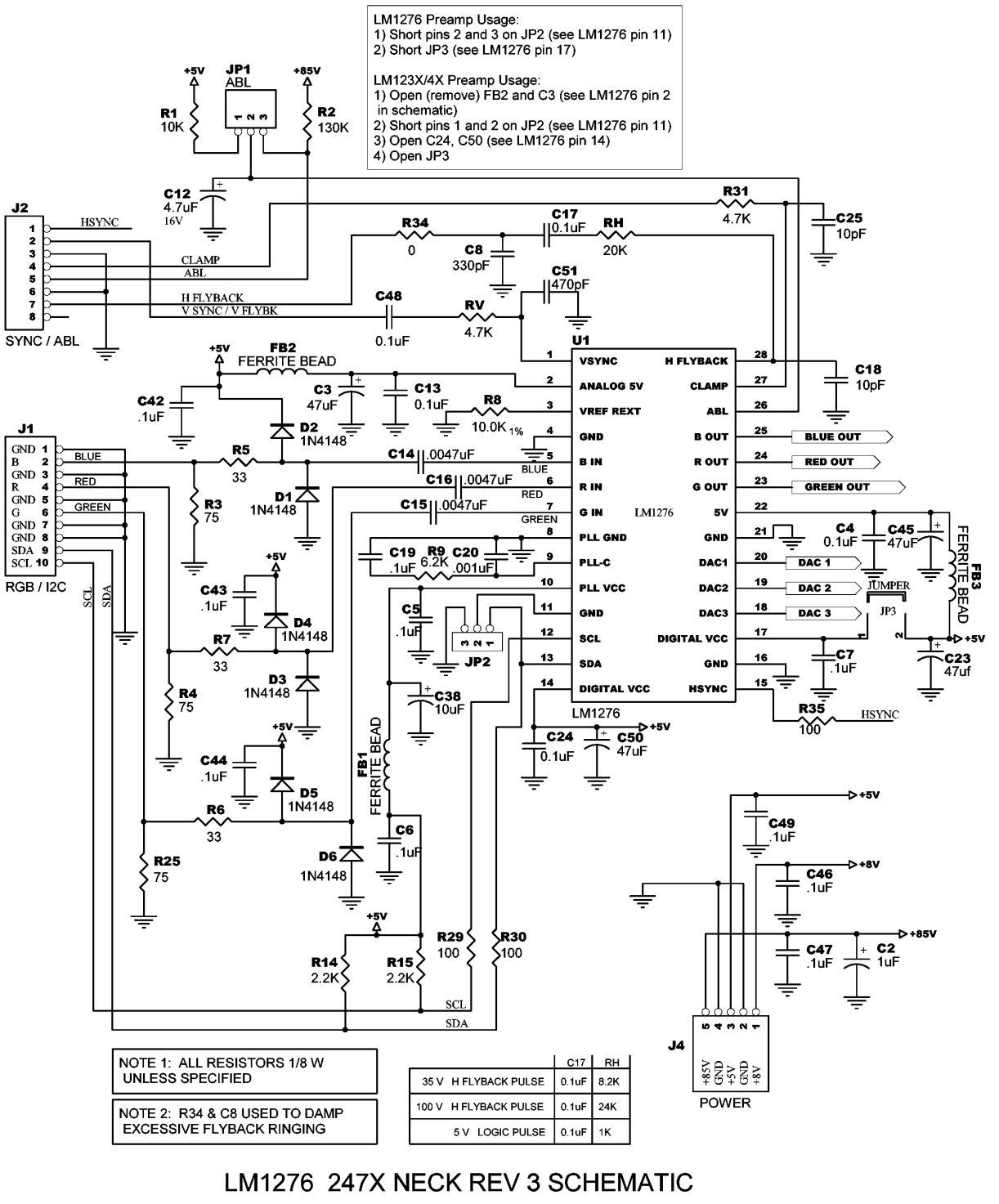


FIGURE 9. LM1276/LM2476 Demo Board Schematic

Schematic Diagram

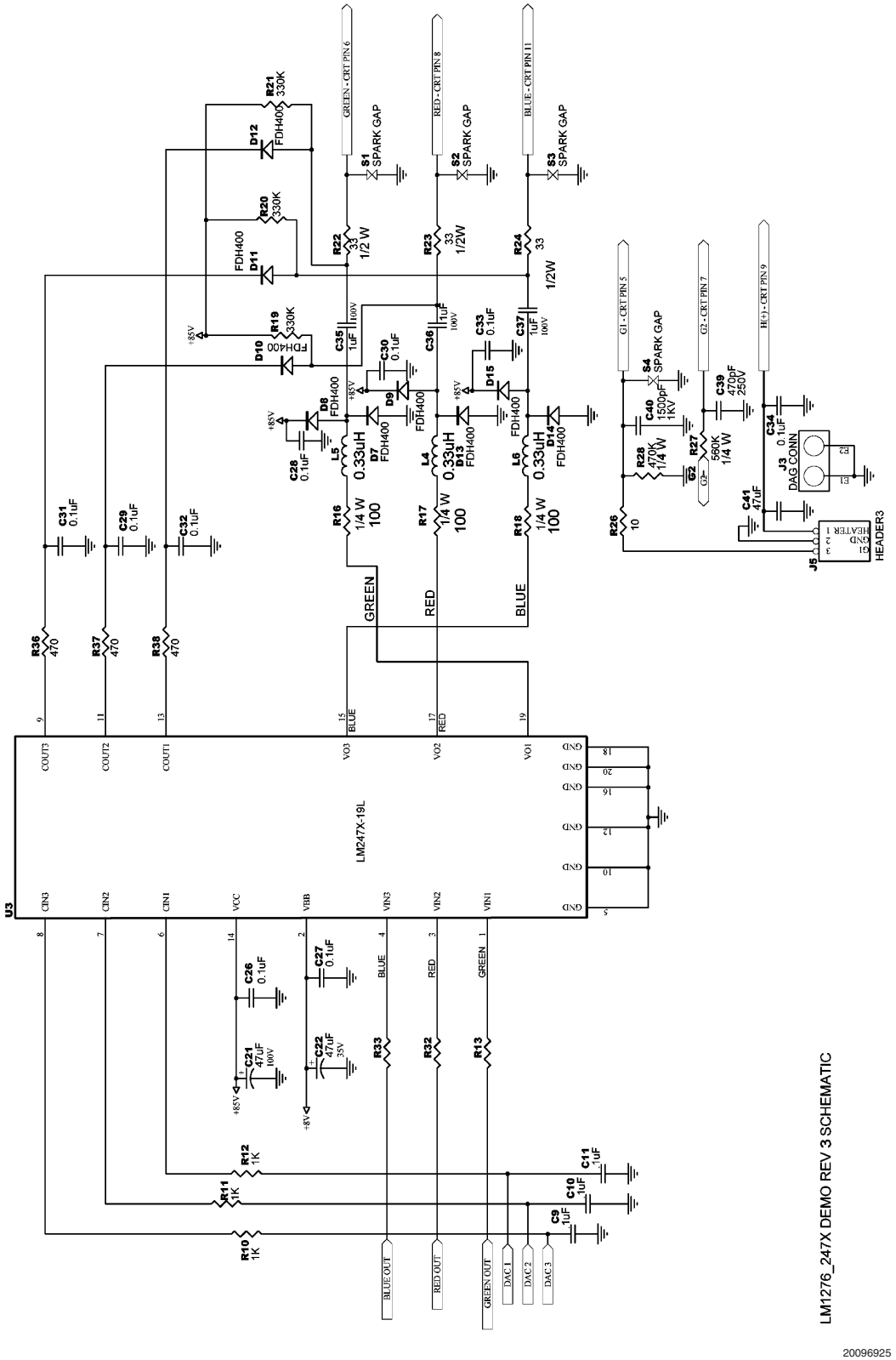


FIGURE 10. LM1276/LM2476 Demo Board Schematic (continued)

PCB Layout

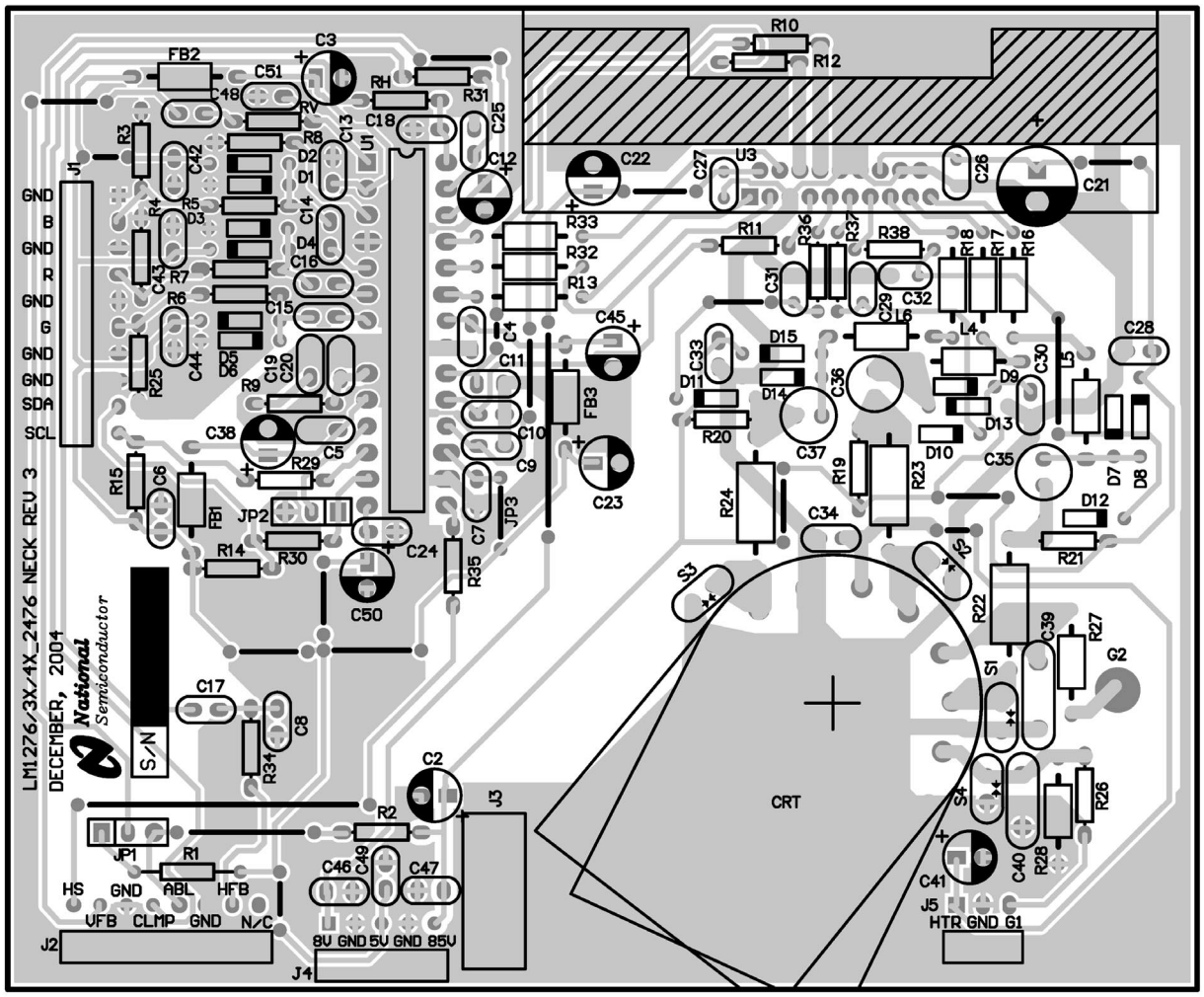


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FIGURE 11. LM1276/LM2476 Demo Board Layout

Burn In Screen

The LM1276 provides a Burn In Screen feature, where a full screen of white video will be displayed without the need for any video input. The Burn In Screen is enabled by setting bit 5 of register 0x8439 to 1. The contrast level of this Burn In display can be adjusted with a 2 Bit DAC over the range of 65% to 85% of normal white level video. This adjustment is made with register 0X8439[7:6].

Programmable Horizontal Blank

The leading edge position of the internal horizontal blank can be programmed with respect to the horizontal flyback zero crossing leading edge in steps of 1 OSD pixel up to a maximum of 31 steps as shown below in *Figure 12*. This start position of the horizontal blanking pulse is only programmable to occur before the horizontal flyback zero crossing edge, and cannot be programmed in the opposite direction. The trailing edge of the horizontal blanking pulse is independent of the programmable leading edge, and its relativity to the Horizontal flyback trailing edge remains unchanged. To use this feature, both Horizontal Blanking (**0x843A[0]**) and Programmable Horizontal Blanking (**0x843A[2]**) must be enabled. The number of steps is programmed with the bits in **0x843A[7:3]**. When this feature is disabled, please refer to the H-Blank Time Delay – On specification (+ Zero Crossing of I_{HFB} to 50% of output blanking end) listed under the System Interface Signal Characteristics section.

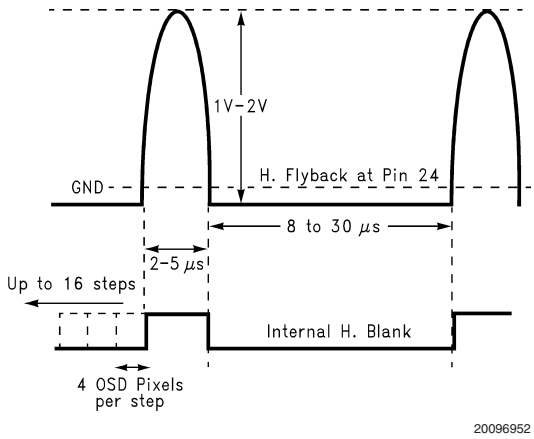


FIGURE 12. Programmable Internal H. Blank

Video Detection for Auto-Sizing & Auto-Centering

The LM1276 is capable of taking measurements necessary for the monitor's microcontroller to perform the auto-sizing and auto-centering operations. The horizontal and vertical flybacks/syncs are used as the reference for timing. Either the flyback or sync signals may be used. In this section, the flyback signals will be considered, although horizontal and vertical sync can be applied similarly. The resultant outputs are the flyback time, the position of the start of video relative to the flyback end, and the time from the end of the active video to the start of the flyback time. Since the total line time is known, the microcontroller can calculate the active video time. The microcontroller can center the video between the start and end of flyback for best image centering, and to calculate the duty cycle of the video with respect to the forward scan time, thus giving a measure of the relative size of the image.

VIDEO INPUT DETECTION

The LM1276 will detect even low-level video information to determine the video image size and position. The video detect logic must also find the extreme points of the displayed image during each frame with respect to the horizontal and vertical flyback pulses as measured using the internal PLL. For best performance in the auto-sizing mode, it is recommended that the application use the maximum pixels per line mode is used when measurements are made. The durations to be measured are shown generically in *Figure 13* and apply to both horizontal and vertical timings. **Since measurements are made in terms of OSD pixels, the ratio of OSD pixels per line to the video pixels per line must be applied to the data below to attain measurements in terms of video pixels.**

1. Flyback or sync period: The duration of either the sync input or the horizontal flyback, in either horizontal lines (vertical) or pixels (horizontal).
2. Back porch period: The duration between the trailing edge of the sync or flyback pulse and the leading edge of the first detected video, in either lines (vertical) or pixels (horizontal).
3. Front porch: The duration between the trailing edge of the last detected video and the leading edge of the sync or flyback pulse, in either lines (vertical) or pixels (horizontal).

The video period is the duration between the leading edge of the first detected video and the trailing edge of the last detected video, in either lines (vertical) or OSD pixels (horizontal). This period is calculated by the microcontroller with the measured periods above.

As the video may start and finish at different positions on the screen, depending upon the image, the measured horizontal porches and video time may vary from line to line. To overcome this, the periods should be measured over at least one entire field. The hardware records the shortest back porch and front porch periods used over the measured period. The possible error for the above measurements are within 1 to 2 OSD pixels.

The video period is the duration between the leading edge of the first detected video and the trailing edge of the last detected video, in either lines (vertical) or OSD pixels (horizontal). This period is calculated by the microcontroller with the measured periods above.

The analog front end video detection is also utilized by the Video Data Interface for decoding of color bar data. **It is critical to note again that the threshold for video detection is 80mV above the internal V_{REF} voltage, and also the minimum rise time requirement of the driving PC video card must be at least 10.0ns.** Excessively slow rise times in the PC video card will prevent the video detect circuit from working properly.

To perform an auto size calculation, the following instruction sequence must be done by the MCU:

Video Detection for Auto-Sizing & Auto-Centering (Continued)

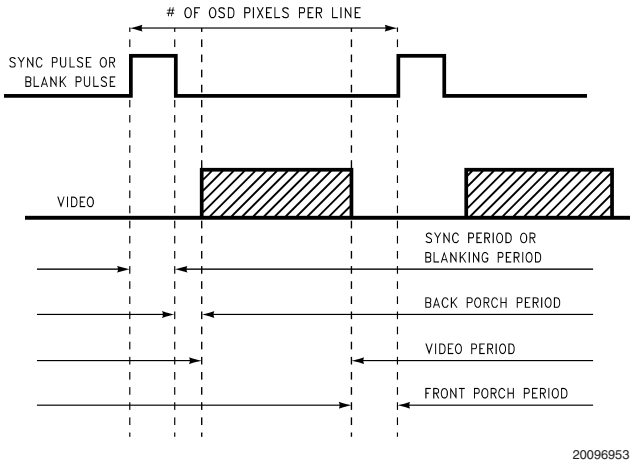


FIGURE 13. Timing Intervals

Auto Size Calculation Instruction Sequence

- Set register bits 0xFFF8[5] and 0xFFF8[4] to high
- Set register bits 0xFFFD[3] to low
- Set register bit 0x8400[6] to high
- Wait for 0x8400[7] to become high by itself
- When 0x8400[7] is high, then read auto size data registers 0x8580 to 0x858F
- Set register bits 0xFFFD[3] to high
- Set register bits 0xFFF8[5] and 0xFFF8[4] to low

PLL Lock Detect and Horizontal Input Select

During the monitor initialization routine by the MCU, register bit 0xFFFD[3] must be set high. This bit is only set low during OSD display operation and auto size calculations. Please see the instructions above for Auto Size calculations.

The following sequence which involves register 0xFFFD and 0xFFF8 must be done by the MCU when the OSD is enabled. Register bits, 0xFFF8[5:4], control the PLL lock detect override function.

Before writing to memory to setup the OSD, or enabling OSD:

- Set register bit 0x8400[0] to high
- Set register bits 0xFFF8[5] and 0xFFF8[4] to high
- Set register bits 0xFFFD[3] to low
- Initialize OSD and write to memory
- Set register bits 0x8400[1] and/or 0x8400[2] to high

Before disabling OSD:

- Set register bits 0x8400[1] and/or 0x8400[2] to low
- Set register bits 0xFFFD[3] to high
- Set register bits 0xFFF8[5] and 0xFFF8[4] to low
- Set register bit 0x8400[0] to low

Please see the OSD Programming section for more detailed information or displaying OSD pages and accessing the RAM

Hi-Brite Video Enhancement Functional Description

The LM1276 enables a desired area of the CRT monitor display to be enhanced for vivid TV quality images. The LM1276 along with the software that is provided by National Semiconductor is fully self-sufficient and independent of the microcontroller in generating and controlling Hi-Brite windows.

HI-BRITE VIDEO PROCESSING

The enhancement is achieved with programmable emphasis, programmable center frequency, and an additional Contrast adjustment control that is separate from the normal Video Contrast Control of the preamp. Having an independent contrast control allows the user to adjust the video gain normally, having the higher gain to have a “brighter” picture within the Hi-Brite window. The emphasis control is used to give more “sparkle” to the highlighted video. Video that is processed by the emphasis control has peaking added to the video. Both the amplitude and the duration of the peaking are adjustable through the NSC software, optimizing the emphasis for different video resolutions. Maximum peaking is 20%.

EMPHASIS

Emphasis is the amount of overshoot on the video signal. Referring to *Figure 14* the overshoot is the ratio of the overshoot voltage to the video level after the emphasis has settled out of the output signal. The typical overshoot is about 20%. The peak measurement is taken 9 ns from the rising edge. This delay gives a more accurate peak measurement by avoiding any ringing that may occur at the rising edge. Overshoot is defined in percent as:

$$\text{Overshoot} = \frac{B - A}{V_{PP}} \times 100$$

Hi-Brite Video Enhancement Functional Description (Continued)

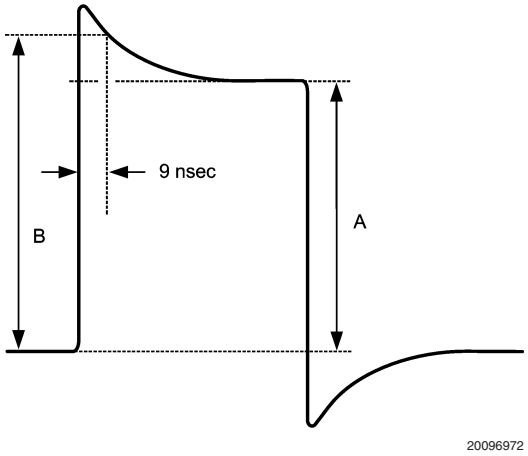


FIGURE 14. Overshoot Measurement

Bits 0 to 2 in registers 0x85C8, 0x85CA, or 0x85CC control the emphasis. When a "4" is programmed into these bits the overshoot is typically 11%. A "0" will give no overshoot in the Hi-Brite window.

CENTER FREQUENCY

Shown in *Figure 15* is how the center frequency is measured. The center frequency is expressed as the time it takes the overshoot to settle to within 5% of the DC level of the pulse.

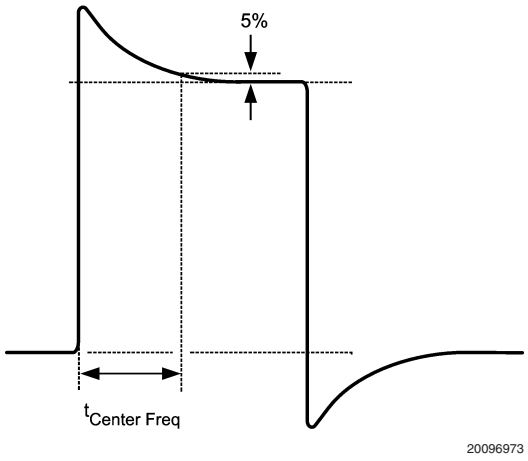


FIGURE 15. Center Frequency Measurement

Bits 4 to 7 in register 0x85C1 control the center frequency. When an "8" is programmed into 0x85C1[7:4] the $t_{Center\ Freq}$ is typically 80 ns. An "F" will give about 145 ns. A "0" will give no emphasis in the Hi-Brite window.

HI-BRITE USER MODES

There are 3 different modes whose settings are to be preset by the MCU. Text Mode, Movie Mode, and Picture Mode each have their own HiBrite Contrast and Overshoot registers (See the Preamp Interface Registers Table). When the user selects a particular mode, the preset register settings of that mode become in effect. There is also a 4th mode, which is the Custom Mode. The Custom Mode, however can be adjusted by the user through the HiBrite Software, and is not preset by the MCU. These modes can ONLY be selected or changed from one to another through the HiBrite Software. There is no I^2C register to select the effective mode. The default mode for the LM1276 is the Movie Mode. Thus, the Contrast and Overshoot settings that will be in effect when a window is initially drawn or when the Full Screen HiBrite function is called will be that of the settings preset for the Movie Mode.

FULL SCREEN HI-BRITE

The LM1276 is capable of applying HiBrite on the entire screen without the need for Software. In the absence of Software, this provides an alternative means of achieving emphasis and contrast boost on the picture through I^2C. The contrast setting and overshoot that will be applied when this function is enabled will be that of the previously selected User mode, during the last instance that the software was in operation. For example, if the user last selected the Picture Mode in the Software preference menu, before exiting the program, then the subsequent enabling of the Full Screen function through I^2C will result in the Picture Mode settings being in effect on the full screen. The I^2C bits that enable this function are 0x8590[5:4]. Setting 0x8590[5] high will disable the HiBrite Window Generation circuit that works together with the Software, and 0x8590[4] enables the Full Screen HiBrite. The Window Generation Circuit must be shut off by 0x8590[5] in order for 0x8590[4] to have an effect. Thus, to activate the Full Screen feature, simply set 0x8590[5:4] to high, and to deactivate, set 0x8590[5:4] to low.

HI-BRITE WINDOW GENERATION OPTIONS

Up to 8 separate windows can be drawn and enabled simultaneously, with programmable sizes and coordinates. The Hi-Brite video enhancement can also be applied to the entire desktop rather than to a specific window area or it can be applied to everything outside of the drawn window(s). All of this window programming can be achieved with National Semiconductor's software, and does not require any interfacing with a microcontroller.

OSD Generator Operation

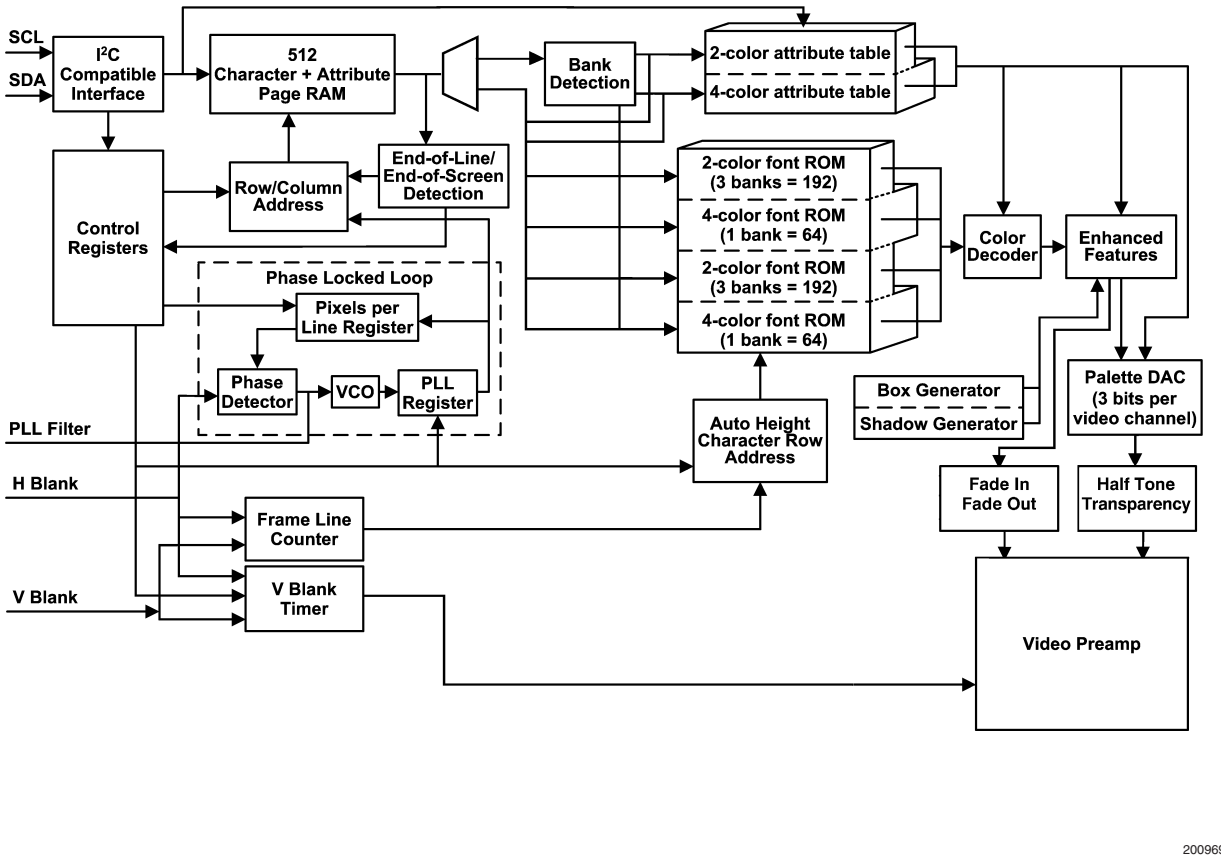


FIGURE 16. OSD Generator Block Diagram

PAGE OPERATION

Figure 16 shows the block diagram of the OSD generator. OSD screens are created using any of the 512 predefined characters stored in the mask programmed ROM. The LM1276 offers a full 9-bit character code operation, which allows the entire 512 ROM character set to be displayed at once. The 9-bit character code operation enables all 512 character addresses to be independently accessed on one page.

OSD ROM CONFIGURATION

The OSD ROM is equivalent to two 256 character ROMs of the type used in the LM1253A and LM1237. Each ROM can be considered as a group of 3 banks, (192) two-color characters followed by 1 bank (64) four-color characters. Physically, the combined ROM is then 192x2 + 64x4 + 192x2 + 64x4.

END-OF-LINE AND END-OF-SCREEN CODES

Please refer to the LM1247 datasheet for details.

BLANK CHARACTER REQUIREMENT

Five of the 512 Character ROM should be reserved as blank. ROM Addresses 0 and 1 are for the use of the End-Of-Screen and End-Of-Line characters as mentioned above. ROM addresses 32, 63, and 511 must be reserved for test engineering purposes. All other ROM addresses are usable, and any that are unused must be filled with at least a duplicate character. Any other addresses except for those listed above should not be left blank.

DISPLAYING AN OSD IMAGE

Consecutive lines of characters make up the displayed window. These characters are stored in the page RAM through the I^2C compatible bus. Each line can contain any number of characters up to the limit of the displayable line length (dependent on the pixels per line register), although some restrictions concerning the enhanced features apply on character lines longer than 32 characters. The number of characters across the width and height of the page can be varied under I^2C compatible control, but the total number of characters that can be stored and displayed on the screen is limited to 512 including any End-of-Line and End-of-Screen characters. The horizontal and vertical start position can also be programmed through the I^2C compatible bus.

WINDOWS

Please refer to the LM1247 datasheet for details.

OSD VIDEO DAC

The Gain of the OSD DAC is now programmable by a 3 Bit OSD contrast register, for 8 levels.

OSD Generator Operation (Continued)

OSD VIDEO TIMING

Please refer to the LM1247 datasheet for details.

CHARACTER CELL

Please refer to the LM1247 datasheet for details.

FOUR COLOR FONT AS TWO 2-COLOR

Please refer to the LM1247 datasheet for details.

ATTRIBUTE TABLES

Each character has an attribute value assigned to it in the page RAM. The attribute value is 4 bits wide, making each character entry in the page RAM 13 bits wide in total. The attribute value acts as an address, which points to one of 16 entries in either the two-color attribute table RAM or the four-color attribute table RAM. The attribute word in the table contains the coding information which defines which color is represented by color 0 and color 1 in the two color attribute table and color 0, color 1, color 2, color 3 in the four-color attribute table. Each color is defined by a 9-bit value, with 3 bits assigned to each channel of RGB. A dynamic look-up table defines each of the 16 different color 'palettes'. As the look-up table can be dynamically coded by the microcontroller over the I^2C compatible interface, each color can be assigned to any one of 2^9 (i.e. 512) choices. This allows a maximum of 64 different colors to be used within one page using the 4-color characters, with up to 4 different colors within any one character and 32 different colors using the 2-color characters, with 2 different colors within any one character.

TRANSPARENT DISABLE

In addition to the 9 lines of video data, a tenth data line is generated by the transparent disable bit. When this line is activated, the black color code will be translated as 'transparent' or invisible. This allows the video information from the PC system to be visible on the screen when this is present. Note that this feature is enabled on any black color in any of the first 8 attribute table entries.

VARIABLE TONE TRANSPARENCY

When the transparency is already in effect the tone of the transparency can be adjusted. The contrast of the PC video that is visible in the "transparent area" can be varied from 100% (fully transparent) to 0% (completely black). For example, 50% reduction in contrast would provide a semi-transparent effect. Just as in the conventional transparency mode, variable tone transparency is effective on backgrounds or foregrounds with black color codes from only the first 8 attribute table entries. This feature is controlled by 0x85C0[6:0], and is only available when the transparency mode is already enabled.

OSD WINDOW FADE IN/FADE OUT

The OSD window can be opened and closed with a fade in/fade out effect. The interval for fading in and fading out the OSD window in the horizontal and vertical direction is variable and can be set by the microcontroller. This allows the OSD window to be opened or closed in the vertical directions, horizontal direction, or from the upper left to lower right corner. Assuming the desired time to typically complete a full fade in or fade out is 0.5 seconds, and if the vertical scan frequency is for example, 60 Hz, the number of steps is:

$$\frac{\text{fade in/fade out time}}{\text{V. scan time}} = \frac{500\,\text{ms}}{16.67\,\text{ms}} = 30\ \text{steps}$$

With a typical OSD window that is 300 pixels wide and 180 video lines long, the horizontal and vertical intervals would be:

$$\text{Horizontal Interval} = \frac{300\ \text{pixels}}{30\ \text{steps}} = 10$$

$$\text{Vertical Interval} = \frac{180\ \text{lines}}{30\ \text{steps}} = 6$$

For a smooth fade in or fade out animation from the upper left corner to the lower right corner, the horizontal to vertical interval ratio must be matched to the aspect ratio of the OSD window. In the example above, the 300 pixel wide by 180 lines long OSD window has an aspect ratio of 5:3. Thus, the horizontal to vertical interval ratio should be set to 5/3 or 10/6. With an OSD window aspect ratio of 3:2, the H/V intervals can be set to 3/2, 6/4, 9/6, 12/8, or 15/10 for optimal operation. If the calculated aspect ratio of an OSD window is a non-integer ratio, the H/V interval ratio should meet or exceed the aspect ratio. For example, if the OSD aspect ratio is 3.7:2 (or 1.85:1), the H/V intervals should be set to 2/1, 4/2, 6/3, 8/4, 10/5, or 12/6. The fade in/out speed increases as H/V interval settings are increased. The OSD window can also be faded in or out in only one direction if desired, by setting the horizontal interval to 0 for fading in/out strictly in the vertical direction or setting the vertical interval to 0 for fading in/out in the horizontal direction. In interlaced video formats, it is not recommended to fade in and fade out the OSD in the vertical direction, and should be only faded in the horizontal direction. The fade in/out function can be enabled/disabled with bit 5 of the frame control register, 0x8400, and the horizontal & vertical intervals are controlled by setting register 0x8429. The OSD window fade in/out feature can only be used with OSD window 1.

ENHANCED FEATURES

Please refer to the LM1247 datasheet for details.

Microcontroller Interface

The microcontroller interfaces to the LM1276 preamp using the I^2C compatible interface. The protocol of the interface begins with a Start Pulse followed by a byte comprised of a 7-bit Slave Device Address and a Read/Write bit. Since the first byte is composed of both the address and the read/write bit, the address of the LM1276 for writing is 0xBA (10111010b) and the address for reading is 0xBB (10111011b). The development software provided by National Semiconductor will automatically take care of the difference between the read and write addresses if the target address under the communications tab is set to 0xBA. *Figures 17, 18* show a write and read sequence on the I^2C compatible interface.

WRITE SEQUENCE

The write sequence begins with a start condition, which consists of the master pulling SDA low while SCL is held high. The Slave Device Write Address, 0xBA, is sent next. Each byte that is sent is followed by an acknowledge bit. When SCL is high, the master will release the SDA line. The slave must pull SDA low to acknowledge. The register to be

Microcontroller Interface (Continued)

written to is next sent in two bytes, the least significant byte being sent first. The master can then send the data, which consists of one or more bytes. Each data byte is followed by an acknowledge bit. If more than one data byte is sent, the data will increment to the next address location. See *Figure 17*.

READ SEQUENCE

Read sequences are comprised of two I^2C compatible transfer sequences: The first is a write sequence that only transfers the two byte address to be accessed. The second is a read sequence that starts at the address transferred in the previous address only write access and increments to the next address upon every data byte read. This is shown in *Figure 18*. The write sequence consists of the Start Pulse, the Slave Device Write Address (0xBA), and the Acknowledge bit; the next byte is the least significant byte of the address to be accessed, followed by its Acknowledge bit. This is then followed by a byte containing the most significant address byte, followed by its Acknowledge bit. Then a Stop bit indicates the end of the address only write access. Next the read data access will be performed beginning with the Start Pulse, the Slave Device Read Address (0xBB), and the Acknowledge bit. The next 8 bits will be the read data driven out by the LM1276 preamp associated with the address indicated by the two address bytes. Subsequent read data bytes will correspond to the next increment address locations. Data should only be read from the LM1276 when both OSD windows and the Fade In/ Fade Out are disabled.

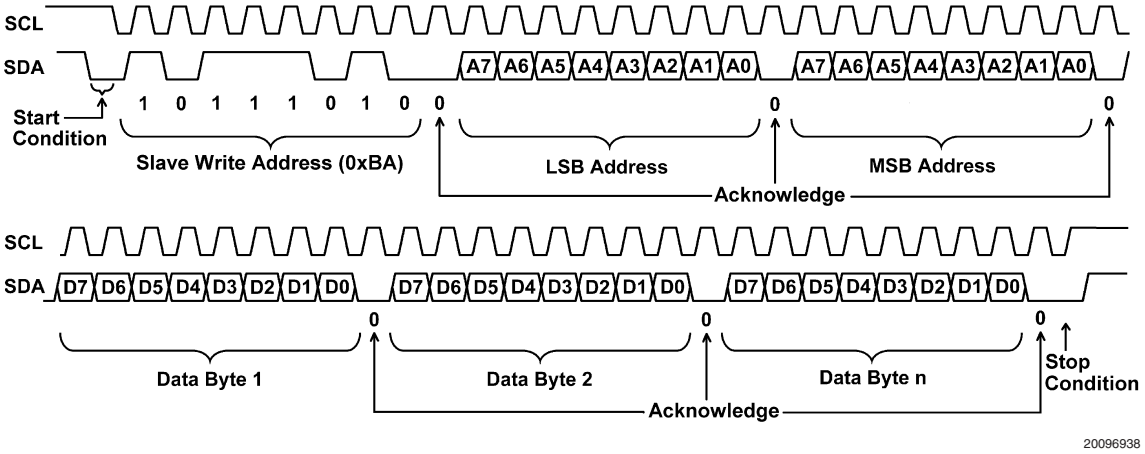


FIGURE 17. I^2C Compatible Write Sequence

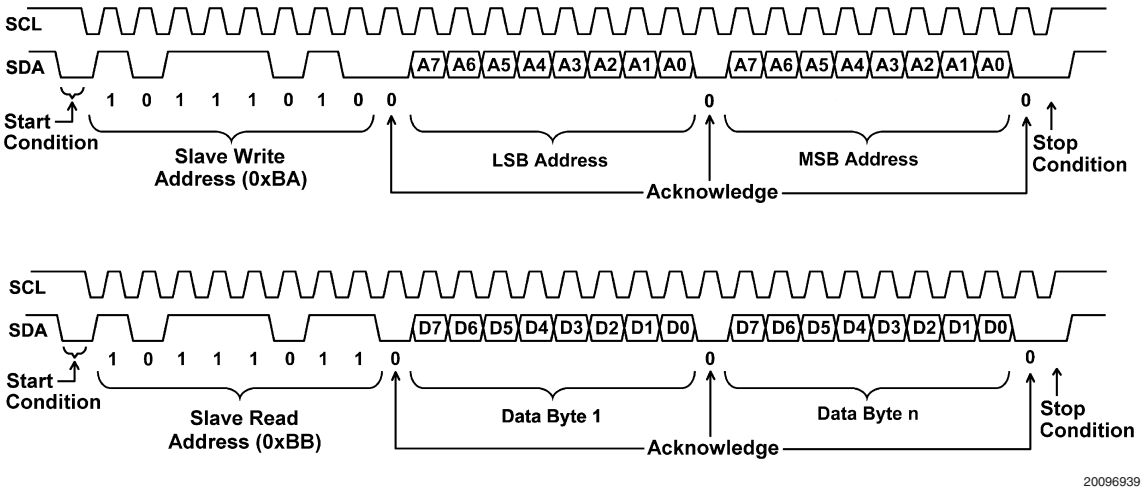


FIGURE 18. I^2C Compatible Read Sequence

LM1276 Address Map

LM1276 Address Map (Continued)

CHARACTER ROM

The 512 font characters from 0x0000 to 0x7FFF can be read from ROM by addressing the individual pixel rows of the desired character. Since the characters have 12 columns, it takes two bytes to read a given row of pixels within one character. Since the characters have 18 rows, a total of 36 bytes are needed to read the entire character. The 16-bit address for reading a row of pixels is formed as follows:

Address = (N * 0x1000) + (I * 0x40) + (R * 0x02) + H

where: N = bank number (0x0 ≤ N ≤ 0x7)

I = Character Index within its respective bank (0x00 ≤ I ≤ 0x3F)

R = row of pixels within the character (0x00 ≤ R ≤ 0x11)

H = 0 for low byte, 1 for high byte

Note that bit 0 of the Character Font Access Register, 0x8402, needs to be set to 0 to read the 2-color fonts. In order to read the four-color fonts, two complete reads are needed. Set bit 0 of the Character Font Access Register, 0x8402, to a 0 to read the least significant plane and to a 1 to read the most significant plane. See *Table 3*.

TABLE 3. Character ROM Addressing

Address Range	R/W	Description	0x8402[0]	N
0x0000–0x2FFF	R	These are the first 3 banks of two-color, read-only ROM character fonts. There are 192 total characters in this range.	0	0x0 0x1 0x2
0x3000–0x3FFF	R	This is bank 3 of four-color, read-only ROM character fonts. There are 64 total characters in this range.	0/1	0x3
0x4000–0x6FFF	R	These are banks 4, 5 and 6 of two-color, read-only ROM character fonts. There are 192 characters in this range.	0	0x4 0x5 0x6
0x7000–0x7FFF	R	This is bank 7 of four-color, read-only ROM character fonts. There are 64 total characters in this range.	0/1	0x7

When read back, the low byte will contain the first eight pixels of the row with data bit 0 corresponding to the left most bit in the pixel row. The high byte will contain the remaining four pixels in the least significant nibble. The remaining 4 bits, shown as "X", are "don't care" bits, and should be discarded. Bit 3 of the high byte corresponds to the right most pixel in the pixel row. This is shown in *Table 4*.

TABLE 4. Character ROM Read Data

Register	Address	D7	D6	D5	D4	D3	D2	D1	D0
Fonts - 2 Color	0x0000–0x2FFE	PIXEL[7:0]							
	+1	X	X	X	X	PIXEL[11:8]			
Fonts - 4 Color	0x3000–0x3FFE	PIXEL[7:0]							
	+1	X	X	X	X	PIXEL[11:8]			
Fonts - 2 Color	0x4000–0x6FFE	PIXEL[7:0]							
	+1	X	X	X	X	PIXEL[11:8]			
Fonts - 4 Color	0x7000–0x7FFE	PIXEL[7:0]							
	+1	X	X	X	X	PIXEL[11:8]			
Display Page	0x8000–0x83FF	X	CHAR_CODE[7:4] or reserved			CHAR_CODE[3:0] or ATTR_CODE			

DISPLAY PAGE RAM

Full 512 Displayable Character Access

This address range (0x8000–0x81FF) contains the 512 characters, which comprise the displayable OSD screens. There must be at least one End-Of-Screen code (0x00) in this range to prevent unpredictable behavior. **NOTE:** To avoid any unpredictable behavior, this range should be cleared by writing a 0 to bit 3 of the FRMCTRL1 Register, 0x8400, immediately after power up. There may also be one or more pairs of End-Of-Line and Skip Line codes. The character code is 9 bits long. The codes and characters are written as 8-bit bytes, but are stored with their attributes in groups of 13 bits. When writing, one byte describes a displayed character (CC), Attribute Code (AC), End-Of-Screen (EOS), End-Of-Line (EOL) or Skip Line (SL) code.

When reading characters from RAM, bit 1 of the Character Font Access Register (0x8402) determines whether the lower 8 bits or upper 5 bits of the Page RAM are returned. *Table 5* gives the lower byte read, which is the first 8 character code bits when bit 1 of the Character Font Access Register is a 0. *Table 6* gives the upper byte read, which is the 9th character code bit and 4 attribute code bits when this bit is set to a 1.

LM1276 Address Map (Continued)

TABLE 5. Page RAM Lower Byte Read Data

Address Range	D7	D6	D5	D4	D3	D2	D1	D0
0x8000–0x81FF	CHAR_CODE[7:0]							

TABLE 6. Page RAM Upper Byte Read Data

Address	D7	D6	D5	D4	D3	D2	D1	D0
0x8000–0x81FF	X	X	X	CC[8]	ATTR_CODE[3:0]			

RAM Data Format

Each of the 512 locations in the page RAM is comprised of a 13-bit code consisting of an 9-bit character or control code, and a 4-bit attribute code. Each of the characters is stored in sequence in the page RAM in bits 8:0. Special codes are used between lines to show where one line ends and the next begins, and also to allow blank (or 'skipped') single scan lines to be added between character lines. *Table 7* shows the format of a character stored in RAM. Note that even though this is a 13-bit format, reading and writing characters and codes is done in 8-bit bytes.

TABLE 7. Page RAM Format (9-bit mode)

ATTRIBUTE CODE	CHARACTER CODE
ATT[3:0]	CC[8:0]

Bits 8-0 determined which of the 512 characters is to be called from the character ROM. Bits 12–9 address one of the 16 attributes in the table containing the colors and enhanced features to be used for this particular character. Two separate attribute tables are used, one for 2-color characters, and the other for 4-color characters. Note there are 16 available attributes for 2-color characters and a different set of 16 available attributes for 4-color characters.

End-Of-Line Code

To signify the end of a line of characters, a special End-Of-Line (EOL) code is used in place of a character code. This code, shown in *Table 8* tells the OSD generator that the character and attribute codes which follow must be placed on a new line in the displayed window. Bits 8–1 are zeros, bit 0 is a one. The attribute that is stored in Page RAM along with this code is not used.

TABLE 8. End-Of-Line Code

ATTRIBUTE CODE	END-OF-LINE CODE								
ATT[3:0]	0	0	0	0	0	0	0	0	1

Skip-Line Code

In order to allow finer control of the vertical spacing of character lines, each displayed line of characters may have up to 15 skipped (i.e., blank) lines between it and the line beneath it. Each skipped line is treated as a single character pixel line, so multiple scan lines may actually be displayed in order to maintain accurate size relative to the character cell. An internal algorithm maintains vertical height proportionality (see the section on Constant Character Height Mechanism). To specify the number of skipped lines, the first character in each new line of characters is interpreted differently than the others in the line. Its data are interpreted as shown in *Table 9*, with the attribute bits setting the color of the skipped lines.

TABLE 9. Skipped-Line Code

ATTRIBUTE CODE	NUMBER OF SKIPPED LINES					
ATT[3:0]	X	X	X	X	X	SL[3:0]

Bits 8–4 are reserved and should be set to zero. Bits 3–0 determine how many blank pixel lines will be inserted between the present line of display characters and the next. A range of 0–15 may be selected. Bits 12–9 determine which attribute the pixels in the skipped lines will have, which is always called from the two-color attribute table. The pixels will have the background color (Color 0) of the selected attribute table entry.

Note that the pixels in the first line immediately below the character may be overwritten by the pixel override system that creates the button box. (Refer to the Button Box Formation Section for more information).

After the first line, each new line always starts with an SL code, even if the number of skipped lines to follow is zero. This means an SL code must always follow an EOL code. An EOL code may follow an SL code if several 'transparent' lines are required between sections of the window. See Example 3 in the LM1247 data sheet for a case where skipped lines of zero characters are displayed, resulting in one window being displayed in two segments.

End-Of-Screen Code

To signify the end of the window, a special End-Of-Screen (EOS) code is used in place of a End-Of-Line (EOL) code. There must be at least one EOS code in the Page RAM to avoid unpredictable behavior. This can be accomplished by clearing the RAM by writing a 0 to bit 3 of the FRMCTRL1 Register, 0x8400, immediately after power up.

LM1276 Address Map (Continued)

TABLE 10. End-Of-Screen Code

ATTRIBUTE CODE	END-OF-SCREEN CODE								
ATT[3:0]	0	0	0	0	0	0	0	0	0

Bits 8–0 are all zeros. Bits 12–9 will have the previously entered AC but this is not used and so these bits are “don’t cares”.

OSD CONTROL REGISTERS

These registers, shown in *Table 11*, control the size, position, enhanced features and ROM bank selection of up to two independent OSD windows. **These registers are compatible to the LM1246 OSD control Registers.** Any bits marked as “X” are reserved and should be written to with zeros and should be ignored when the register is read. Additional register detail is provided in the *Control Register Definitions Section,* later in this document.

TABLE 11. OSD Control Register Detail

Register	Address	Default	D7	D6	D5	D4	D3	D2	D1	D0
FRMCTRL1	0x8400	0x98	ASZDN	ASZEN	FEN	TD	CDPR	D2E	D1E	OSE
FRMCTRL2	0x8401	0x80	PIXELS_PER_LINE[2:0]			BLINK_PERIOD[4:0]				
CHARFONTACC	0x8402	0x00	SRST	RSV	RSV	LIMIT	VSYPOL	HSYPOL	ATTR	FONT4
VBLANKDUR	0x8403	0x10	X	VBLANK_DURATION[6:0]						
CHARHTCTRL	0x8404	0x51	CHAR_HEIGHT[7:0]							
BBHLCTRLB0	0x8405	0xFF	G[1:0]		R[2:0]			B[2:0]		
BBHLCTRLB1	0x8406	0x01	X	X	X	X	X	X	X	G[2]
BBLLCTRLB0	0x8407	0x00	G[1:0]		R[2:0]			B[2:0]		
BBLLCTRLB1	0x8408	0x00	X	X	X	X	X	X	X	G[2]
CHSDWCTRLB0	0x8409	0x00	G[1:0]		R[2:0]			B[2:0]		
CHSDWCTRLB1	0x840A	0x00	X	X	X	X	X	X	X	G[2]
ROMSIGCTRL	0x840D	0x00	X	X	X	X	X	X	X	CRS
ROMSIGDATAB0	0x840E	0x00	CRC[7:0]							
ROMSIGDATAB1	0x840F	0x00	CRC[15:8]							
HSTRT1	0x8410	0x62	HPOS1[7:0]							
VSTRT1	0x8411	0x32	VPOS1[7:0]							
W1STRTADRL	0x8412	0x00	ADDR1[7:0]							
W1STRTADRH	0x8413	0x00	X	X	X	X	X	X	X	ADDR1[8]
COLWIDTH1B0	0x8414	0x00	COL1[7:0]							
COLWIDTH1B1	0x8415	0x00	COL1[15:8]							
COLWIDTH1B2	0x8416	0x00	COL1[23:16]							
COLWIDTH1B3	0x8417	0x00	COL1[31:24]							
HSTRT2	0x8418	0x56	HPOS2[7:0]							
VSTRT2	0x8419	0x5B	VPOS2[7:0]							
W2STRTADRL	0x841A	0x00	ADDR2[7:0]							
W2STRTADRH	0x841B	0x01	X	X	X	X	X	X	X	ADDR2[8]
COLWIDTH2B0	0x841C	0x00	COL2[7:0]							
COLWIDTH2B1	0x841D	0x00	COL2[15:8]							
COLWIDTH2B2	0x841E	0x00	COL2[23:16]							
COLWIDTH2B3	0x841F	0x00	COL2[31:24]							
Any registers in the range of 0x8420–0x8426 are for National Semiconductor internal use only and should not be written to under application conditions.										
FADE_INTVL	0x8429	0x35	V_INTVL[3:0]				H_INVTVL[3:0]			

PREAMPLIFIER CONTROL

These registers, shown in *Table 12*, control the gains, DAC outputs, PLL, horizontal and vertical blanking, OSD contrast and DC offset of the video outputs. **Registers 0x8430–0x8437 are compatible to the LM1246 Registers.** Any bits marked as “X” are reserved and should be written to with zeros and should be ignored when the register is read. Additional register detail is provided in the *Control Register Definitions Section*, later in this document.

LM1276 Address Map (Continued)

TABLE 12. LM1276 Preamplifier Interface Registers

Register	Address	Default	D7	D6	D5	D4	D3	D2	D1	D0
BGAINCTRL	0x8430	0x60	X	BGAIN[6:0]						
GGAINCTRL	0x8431	0x60	X	GGAIN[6:0]						
RGAINCTRL	0x8432	0x60	X	RGAIN[6:0]						
CONTRCTRL	0x8433	0x60	X	CONTRAST[6:0]						
DAC1CTRL	0x8434	0x80	DAC1[7:0]							
DAC2CTRL	0x8435	0x80	DAC2[7:0]							
DAC3CTRL	0x8436	0x80	DAC3[7:0]							
DAC4CTRL	0x8437	0x80	DAC4[7:0]							
DACOSDDCOFF	0x8438	0x24	DCF[1:0]		OSD CONT[2:0]			DC OFFSET[2:0]		
GLOBALCTRL	0x8439	0x00	BI[7:6]		BI_EN	PLLCAL	RSV	RSV	PS	BV
AUXCTRL1	0x843A	0x03	HB_POS[4:0]					HBPOS _EN	RSV	HBD
AUXCTRL2	0x843E	0x06	RSV	RSV	CLMP	CLMP SW	OOR	VB2	RSV	RSV
OSD_TRANSP TONE	0x85C0	0x7F	RSV	OSD TONE[6:0]						
EMPHASIS CENTF	0x85C1	0x80	CENTF[3:0]				RSV			
ABLCTRL0	0x85C4	0x0F	RSV				ABL0[3:0]			
ABLCTRL1	0x85C5	0x0F	RSV				ABL1[3:0]			
ABLCTRL2	0x85C6	0x0F	RSV				ABL2[3:0]			
ABLCTRL3	0x85C7	0x0F	RSV				ABL3[3:0]			
PEAKCNTLTXT	0x85C8	0x30	RSV					TM_OVRSHT[2:0]		
HLCONTRTXT	0x85C9	0x60	RSV	HILIGHT_CONTRAST[6:0]						
PEAKCNTLPIC	0x85CA	0x03	RSV					PM_OVRSHT[2:0]		
HLCONTRPIC	0x85CB	0x60	RSV	HILIGHT_CONTRAST[6:0]						
PEAKCNTLMOV	0x85CC	0x03	RSV					MM_OVRSHT[2:0]		
HLCONTRTMOV	0x85CD	0x60	RSV	HILIGHT_CONTRAST[6:0]						

TWO-COLOR ATTRIBUTE RAM

This RAM is identical to that of the LM1247. Please refer to the LM1247 datasheet for details.

FOUR-COLOR ATTRIBUTE RAM

This RAM is identical to that of the LM1247. Please refer to the LM1247 datasheet for details.

AUTO SIZE AND HI-BRITE REGISTERS

These registers, shown in *Table 13* provide measured values for the Auto size function and control the Hi-Brite function. **Registers 0x8580 — 0x858A are compatible to the LM1246 Auto Size Registers.** Reserved bits are for internal use and should not be written to, and any value read should be ignored.

TABLE 13. LM1276 Auto Size Registers

Register	Address	Default	D7	D6	D5	D4	D3	D2	D1	D0
H_FP0	0x8580	0xFF	HFP[7:0]							
H_FP1	0x8581	0x07	RSV					HFP[10:8]		
HF_S0	0x8582	0xFF	HFL_HS[7:0]							
HF_S1	0x8583	0x03	RSV						HFL HS[9:8]	
H_BP0	0x8584	0xFF	HBP[7:0]							
H_BP1	0x8585	0x07	RSV					HBP[10:8]		
V_FP0	0x8586	0xFF	VFP[7:0]							
V_FP1	0x8587	0x07	RSV					VFP[10:8]		
V_SYN_D	0x8588	0xFF	VSYNC[7:0]							

LM1276 Address Map (Continued)

TABLE 13. LM1276 Auto Size Registers (Continued)

Register	Address	Default	D7	D6	D5	D4	D3	D2	D1	D0
V_BP0	0x8589	0xFF	VBP[7:0]							
V_BP1	0x858A	0x07	RSV					VBP[10:8]		
V_FP0_PRV	0x858B	0xFF	VFP PREV [7:0]							
V_FP1_PRV	0x858C	0x07						VFP PREV[10:8]		
V_SYN_PRV	0x858D	0xFF	VSYNC PREV [7:0]							
V_BP0_PRV	0x858E	0xFF	VBP PREV [7:0]							
V_BP1_PRV	0x858F	0x07						VBP PREV[10:8]		
HB CONTROL	0x8590	0x40	INTR_EN	LIMIT	WHLDIS	FSHEN	RSV	RSV	RSV	RSV
STATUS	0x8591	0x00	INTR	RSV	RSV	RSV	RSV	RSV	RSV	RSV
MCU COMMAND	0x8592	0xFF	MCU COMMAND[7:0]							
SUB COMMAND	0x8593	0xFF	SUB COMMAND[7:0]							
SEQ NUM	0x859A	0xFF	SEQ NUM[7:0]							
PLL LOCK	0xFFF8	0x00	RSV	RSV	LOCK SET	LOCK ORR	RSV	RSV	RSV	RSV
H INPUT SEL	0xFFFD	0x01	RSV	RSV	RSV	RSV	HSEL	RSV	RSV	RSV

Building Display Pages

THE OSD WINDOW

The Display Page RAM contains all of the 9-bit display character codes and their associated 4-bit attribute codes, and the special 13-bit page control codes—the End-of-Line, skip-line parameters and End-of-Screen characters. The LM1276 has a distinct advantage over many OSD Generators in that it allows variable size and format windows. The window size is not dictated by a fixed geometric area of RAM. Instead, 512 locations of 13-bit words are allocated in RAM for the definition of the windows, with special control codes to define the window size and shape.

Window width can be any length supported by the number of pixels per line that is selected divided by the number of pixels in a character line. It must be remembered that OSD characters displayed during the monitor blanking time will not be displayed on the screen, so the practical limit to the number of horizontal characters on a line is reduced by the number of characters within the horizontal blanking period.

The EOS code tells the OSD generator that the character codes following belong to another displayed window at the next window location. An EOS code may follow normal characters or an SL code, but never an EOL control code, because EOL is always followed by an AC plus an SL code.

WRITING TO THE PAGE RAM

The Display Page RAM can contain up to 512 of the above listed characters and control codes. Each character, or control code will consume one of the possible 512 locations. For convenience, writing a 1 to bit 3 of the Frame Control Register (0x8400) resets all page RAM values to zero. This should be done at power up to avoid unpredictable behavior.

Display Window 1 will also start at the first location (corresponding to the I^2C address 0x8000). This location must always contain the Skip-Line (SL) code associated with the first line of Display Window 1. The attribute for this SL code must be written before the SL code itself, and will be stored in the lower four bits of this memory location. Subsequent locations should contain the characters to be displayed on line 1 of Display Window 1, until the EOL code or EOS code is written into the Display Page-RAM.

The skip-line parameters associated with the next line must always be written to the location immediately after the preceding line's End-of-Line character. The only exception to this rule is when an End-of-Screen character (value 0x0000) is encountered. It is important to note that an End-of-Line character should not precede an End-of-Screen character (otherwise the End-of-Screen character will be interpreted as the next line's skip-line code). Instead, the End-of-Screen code will end the line and also end the window, making it unnecessary to precede it with an EOL. The I^2C Format for writing a sequence of display characters is minimized by allowing sequential characters with the same attribute code to send in a string as follows:

Byte #1: I^2C Slave Address

Byte #2: LSB Register Address

Byte #3: MSB Register Address

Byte #4: Attribute Table Entry to use for the following s skip-line code or characters

Byte #5: First display character, SL parameter, EOL or EOS control code

Byte #6: Second display character, SL parameter, EOL or EOS control code

Byte #7: Third display character, SL parameter, EOL or EOS control code

Byte #n: Last display character in this color sequence, SL parameter, EOL or EOS control code to use the associated Attribute Table Entry.

Building Display Pages (Continued)

This communication protocol is known as the Auto Attribute Mode, which is also used by the LM1237 and LM1247. Please see examples of usage for this mode in the LM1247 datasheet.

TABLE 14. Sequence of Transmitted Bytes

ENHANCED PAGE RAM ADDRESS MODES

Since the LM1276 is able to support 9-bit character codes, usually two bytes of Page RAM information has to be sent to every location. To avoid this, the LM1276 addressing control system has 3 additional addressing modes offering increased flexibility that may be helpful in sending data to the Page RAM. Some of the left over bits in the Attribute byte are employed as data control bits to select the desired addressing mode as shown in *Table 6*. This is identified as the first byte sent in a write operation or the Page RAM's upper byte read in Table 7.

TABLE 15. Attribute Byte

ATTRIBUTE Byte				
X	DC[1]	DC[0]	CC[8]	ATT[3:0]

AUTO ATTRIBUTE MODE

The Auto Attribute mode is the standard LM1247 mode that is described above in the WRITING TO THE PAGE RAM section. The attribute byte is shown in *Table 16*.

TABLE 16. Auto Attribute Mode

ATTRIBUTE Byte				
X	0	0	0	ATT[3:0]

When bits 6–5 are 0, the 9th character code and the 4-bit attribute code will be automatically applied to all the character codes transmitted after this attribute byte, as in the LM1237 and LM1247. This mode is useful for sending character codes that use the same attribute, and which are in the same 4 out of 8 banks of the Page ROM. A new transmission must be started to access another character that is not in the same 4 banks of the Page ROM, and no further attribute codes can follow without stopping and restarting a new transmission. The Page RAM address is automatically incremented starting with the initial LSB and MSB address in the beginning of the sequence.

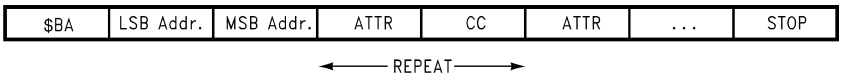
TWO BYTE COMMUNICATION MODE

The Two Byte Communication mode allows different attribute and character codes to be sent within one transmission without stopping. The entire 512-character Page ROM is also fully accessible in this mode, without the need to stop and restart transmission. The attribute byte is shown in *Table 17*, and the sequence of transmitted bytes is shown in *Table 18*. Either another attribute & character code pair or a STOP must follow after each character code. The Page RAM address is automatically incremented just as in the Auto Attribute mode above.

TABLE 17. Two Byte Communication Mode

ATTRIBUTE Byte				
X	0	1	CC[8]	ATT[3:0]

TABLE 18. Sequence of Transmitted Bytes



HALF RANDOM ADDRESS MODE

The Half Random Address mode allows different attribute and character codes to be sent within one transmission in the same way as the Two Byte Communication mode. The entire 512-character Page ROM is fully accessible in this mode, without the need to stop and restart transmission. The advantage of Half Random Addressing over the Two Byte mode is that the Page RAM addresses do not have to be written to in a sequential order. However, the Page RAM addresses cannot be entirely random, as they must be within one half of the Page RAM. A new transmission must be restarted to switch to another half of the Page RAM.

Building Display Pages (Continued)

The Page RAM address is not automatically incremented in this mode. This mode is very useful for modifying character codes and attributes in the first 256 locations of the Page RAM. The attribute byte is shown in *Table 19*, and the sequence of transmitted bytes is shown in *Table 20*. Either another LSB address & attribute & character code or a STOP must follow after each character code.

TABLE 19. Half Random Address Mode

ATTRIBUTE Byte				
X	1	0	CC[8]	ATT[3:0]

TABLE 20. Sequence of Transmitted Bytes

$BA	LSB Addr.	MSB Addr.	ATTR	CC	LSB Addr.	ATTR	CC	...	STOP
					← REPEAT →				

FULL RANDOM ADDRESS MODE

The Full Random Address mode is very similar to the Half Random Address mode. However, the advantage is that the Page RAM addresses can now be entirely random. There is no longer a restriction to only one half of the Page RAM. The Page RAM address is not automatically incremented in this mode. This is very useful for modifying character codes and attributes anywhere in the Page RAM without starting a new transmission sequence. The Full Random Address mode is the most flexible mode of transmission. The attribute byte is shown in *Table 21*, and the sequence of transmitted bytes is shown in *Table 22*. Either another LSB address & MSB address & attribute & character code or a STOP must follow after each character code.

TABLE 21. Full Random Address Mode

ATTRIBUTE Byte				
X	1	1	CC[8]	ATT[3:0]

TABLE 22. Sequence of Transmitted Bytes

$BA	LSB Addr.	MSB Addr.	ATTR	CC	LSB Addr.	MSB Addr.	ATTR	CC	...	STOP
					← REPEAT →					

Control Register Definitions

OSD INTERFACE REGISTERS

Frame Control Register 1:

FRMCTRL1 (0x8400)							
Autosize done	**Autosize**	**Fade I/O**	**Trans**	**Clear**	**Win2**	**Win1**	**OSD**
ASZDN	ASZEN	FEN	TD	CDPR	D2E	D1E	OSE

Bit 0	On-Screen Display Enable. The On-Screen Display will be disabled when this bit is a zero. When this bit is a one the On-Screen Display will be enabled. This controls both Window 1 and Window 2.
Bit 1	Display Window 1 Enable. When this bit and Bit 0 of this register are both ones, Display Window 1 is enabled. If either bit is a zero, then Display Window 1 will be disabled.
Bit 2	Display Window 2 Enable. When this bit and Bit 0 of this register are both ones, Display Window 2 is enabled. If either bit is a zero, then Display Window 2 will be disabled.
Bit 3	Clear Display Page RAM. Writing a one to this bit will result in setting all of the Display Page RAM values to zero. This bit is automatically cleared after the operation is complete. This bit is initially asserted by default at power up, and will clear itself back to zero shortly after. Thus, the default value is one only momentarily, and then will remain zero until manually asserted again or until the power is cycled.
Bit 4	Transparent Disable. When this bit is a zero, a palette color of black (i.e., color palette look-up table value of 0x00) in the first 8 palette look-up table address locations (i.e., ATT0–ATT7) will be interpreted as transparent. When this bit is a one, the color will be interpreted as black.

Control Register Definitions (Continued)

Bit 5	Fade In/Out Enable. When this bit is a 1, the OSD Fade In/Fade Out function is enabled. When this bit is a 0, the function is disabled.
Bit 6	Auto Size Enable. When this bit is a 1, the Auto Size function is enabled. Once video detection and measurement is completed, the bit will automatically clear itself back to 0.
Bit 7	Auto Size Done. When the device has completed Auto Size calculations, this bit will automatically be set high by the chip to indicate to the MCU that the Auto Size data registers are valid and available. This bit is automatically cleared when the MCU sets the ASZEN bit (0x8400[6]), or when the device programs a calibration sequence for the Windows HiBrite software.

Frame Control Register 2:

FRMCTRL2 (0x8401)	
Pixels per Line	**Blink Period**
PL[2:0]	BP[4:0]

Bits 4–0	Blink Period. These five bits set the blink period of the blinking feature, which is determined by mulitiplying the value of these bits by 8, and then multiplying the result by the vertical field rate.
Bits 7–5	Pixels per Line. These three bits determine the number of pixels per line of **OSD characters**. See *Table 23*, which gives the maximum horizontal scan rate. Also see *Table 2*.

TABLE 23. OSD Pixels per Line

Bits 7–5	Description	Max Horizontal Frequency (kHz)
0x0	704 pixels per line	110
0x1	768 pixels per line	110
0x2	832 pixels per line	110
0x3	896 pixels per line	110
0x4	960 pixels per line	110
0x5	1024 pixels per line	108
0x6	1088 pixels per line	102
0x7	1152 pixels per line	96

Character Font Access Register:

CHARFONTACC (0x8402)							
RESET	**Reserved**	**Reserved**	**VDI**	**V Sync**	**H Sync**	**Select**	**Plane**
SRST	RSV	RSV	LIMIT	VSYPOL	HSYPOL	ATTR	FONT4

Bit 0	This is the Color Bit Plane Selector. This bit must be set to 0 to read or write a two-color attribute from the range 0x0000 to 0x2FFF. When reading or writing four-color attributes from the range 0x3000 to 0x3FFF, this bit is set to 0 for the least significant plane and to 1 for the most significant plane. It is also required to set this bit to read the individual bit planes of the four color character fonts in 0x3000 to 0x3FFF and 0x7000 to 0x7FFF.
Bit 1	This is the Character/Attribute Selector. This applies to reads from the Display Page RAM (address range 0x8000–0x81FF). When a 0, the character code is returned and when a 1, the attribute code is returned.
Bit 2	This selects the V input polarity. If bit = 0, a positive H Sync input signal is required. (Default) If bit = 1, a negative H Sync input signal is required.
Bit 3	This selects the V sync input polarity. If bit = 0, a positive V Sync input signal is required. (Default) If bit = 1, a negative V Sync input signal is required.
Bit 4	This bit limits the period during which video data may be detected. If the bit is set to 1 then the valid data active period is limited to the vertical blanking time, as set by the vertical blanking register. If a string of 80 clock pulses is received during this time it is accepted as valid. If a string of 80 pulses is not received until during the active video time, then this data is ignored. If the bit is set to '0' (default), then the first 80 pulse clock string that is detected is considered to be valid, even if this is during the active video time.

Control Register Definitions (Continued)

Bit 5	Reserved. This bit should be set to zero.
Bit 6	Reserved. This bit should be set to zero.
Bit 7	Setting this bit will cause a software reset. All registers (except this one) are loaded with their default values. All operations currently in progress are aborted (except for I^2C transactions). This bit automatically clears itself when the reset has been completed.

Vertical Blank Duration Register:

VBLANKDUR (0x8403)	
Reserved	**Vertical Blanking Duration**
RSV	VB[6:0]

Bits 6–0	This register determines the duration of the vertical blanking signal in scan lines. When vertical blanking is enabled, it is recommended that this register be set to a number greater than 0x0A.
Bit 7	Reserved. This bit should be set to zero.

OSD Character Height Register:

CHARHTCTRL (0x8404)
CH[7:0]

Bits 7–0	This register determines the OSD character height as described in the section Constant Character Height Mechanism. The values of this register is equal to the approximate number of OSD height compensated lines required on the screen, divided by 4. This value is not exact due to the approximation used in scaling the character. Example: If approximately 384 OSD lines are required on the screen (regardless of the number of scan lines) then the Character Height Control Register is programmed with 81 (0x51).

Enhanced Feature Register 1: **Button Box Highlight Color**

BBHLCTRLB1 (0x8406)							BBHLCTRLB0 (0x8405)		
Reserved							Highlight - Green	Highlight - Red	Highlight - Blue
X	X	X	X	X	X	X	G[2:0]	R[2:0]	B[2:0]

Bits 8–0	These determine the button box highlight color.
Bits 15–9	Reserved. These bits should be set to zero.

Enhanced Feature Register 2: **Button Box Lowlight Color**

BBLLCTRLB1 (0x8408)							BBLLCTRLB0 (0x8407)		
Reserved							Lowlight - Green	Lowlight - Red	Lowlight - Blue
X	X	X	X	X	X	X	G[2:0]	R[2:0]	B[2:0]

Bits 8–0	These determine the button box lowlight color.
Bits 15–9	Reserved. These bits should be set to zero.

Enhanced Feature Register 3: **Heavy Button Box Lowlight/Shading/Shadow**

CHSDWCTRLB1 (0x840A)							CHSDWCTRLB0 (0x8409)		
Reserved							Shadow - Green	Shadow - Red	Shadow - Blue
X	X	X	X	X	X	X	G[2:0]	R[2:0]	B[2:0]

Bits 8–0	These registers determine the heavy button box lowlight, shading or shadow color.
Bits 15–9	Reserved. These bits should be set to zero.

Control Register Definitions (Continued)

ROM Signature Control Register:

ROMSIGCTRL (0x840D)							
Reserved							Check
X	X	X	X	X	X	X	CRS

Bit 0	This controls the calculation of the ROM signature. Setting this bit causes the ROM to be read sequentially and a 16-bit checksum calculated over the 256 characters. The sum, modulo 65535, is stored in the ROM Signature Data Register, and this bit is then automatically cleared.
Bits 7–1	Reserved. These should be set to zero.

ROM Signature Data:

ROMSIGDATAB1 (0x840F)	ROMSIGDATAB0 (0x840E)
16-Bit Checksum	
CRC[15:0]	

Bits 15–0	This is the checksum of the 256 ROM characters truncated to 16 bits (modulo 65535). All devices with the same masked ROM will have the same checksum.

Display Window 1 Horizontal Start Address:

HSTRT1 (0x8410)
Window 1 Horizontal Start Location
HPOS1[7:0]

Bits 7–0	There are two possible OSD windows which can be displayed simultaneously or individually. This register determines the horizontal start position of Window 1 in OSD pixels (not video signal pixels). The actual position, to the right of the horizontal flyback pulse, is determined by multiplying this register value by 4 and adding 30. Due to pipeline delays, the first usable start location is approximately 42 OSD pixels following the horizontal flyback time. For this reason, we recommend this register be programmed with a number larger than 2, otherwise improper operation may result.

Display Window 1 Vertical Start Address:

VSTRT1 (0x8411)
Window 1 Vertical Start Address
VPOS1[7:0]

Bits 7–0	This register determines the Vertical start position of the Window 1 in constant-height character lines (not video scan lines). The actual position is determined by multiplying this register value by 2. (Note: each character line is treated as a single auto-height character pixel line, so multiple scan lines may actually be displayed in order to maintain accurate position relative to the OSD character cell size. (See the *Constant Character Height Mechanism* section.) This register should be set so the entire OSD window is within the active video.

Display Window 1 Start Address:

W1STRTADRH (0x8413)							W1STRTADRL (0x8412)
Reserved							Window 1 Start Address
X	X	X	X	X	X	X	ADDR1[8:0]

Bits 8–0	This register determines the starting address of Display Window 1 in the Display Page RAM. The power-on default of 0x00 starts Window 1 at the beginning of the Page RAM (0x8000). This first address location always contains the SL code for the first line of Display Window 1. This register is new for the LM1276 and allows Window 1 to start anywhere in the Page RAM rather than just at 0x8000. Note that the address this points to in Page RAM must always contain the SL code for the first line of the window.
Bits 15–9	These bits are reserved and should be set to zero.

Control Register Definitions (Continued)

Display Window 1 Column Width:

COLWIDTH1B3 (0x8417)	COLWIDTH1B2 (0x8416)
Window 1 Column Width - High Bytes	
COL1[31:16]	

COLWIDTH1B1 (0x8415)	COLWIDTH1B0 (0x8414)
Window 1 Column Width - Low Bytes	
COL1[15:0]	

Bits 31–0	These are the Display Window 1 Column Width 2x Enable Bits. These 32 bits correspond to columns 31–0 of Display Window 1, respectively. A value of zero indicates the column will have normal width (12 pixels). A "1" indicates the column will be twice as wide as normal (24 pixels). For the double wide case, each Character Font pixel location will be displayed twice, in two consecutive horizontal pixel locations. The user should note that if more than 32 display characters are programmed to reside on a line, then all display characters after the first thirty-two will have normal width (12 pixels).

Display Window 2 Horizontal Start Address:

HSTRT2 (0x8418)
Window 2 Horizontal Start Address
HPOS2[7:0]

Bits 7–0	This register determines the horizontal start position of Window 2 in OSD pixels (not video signal pixels). The actual position, to the right of the horizontal flyback pulse, is determined by multiplying this register value by 4 and adding 30. Due to pipeline delays, the first usable start location is approximately 42 OSD pixels following the horizontal flyback time. For this reason, we recommend this register be programmed with a number larger than 2, otherwise improper operation may result.

Display Window 2 Vertical Start Address:

VSTRT2 (0x8419)
Window 2 Vertical Start Address
VPOS2[7:0]

Bits 7–0	This register determines the Vertical start position of Window 2 in constant-height character lines (not video scan lines). The actual position is determined by multiplying this register value by 2. (Note: each character line is treated as a single auto-height character pixel line, so multiple scan lines may actually be displayed in order to maintain accurate position relative to the OSD character cell size. (See the *Constant Character Height Mechanism* section.) This register should be set so the entire OSD window is within the active video.

Display Window 2 Start Address:

W2STRTADRH (0x841B)							W2STRTADRL (0x841A)
Reserved							**Window 2 Start Address**
X	X	X	X	X	X	X	ADDR2[8:0]

Bits 8–0	This register determines the starting address of Display Window 2 in the Display Page RAM. The power-on default of 0x10 starts Window 2 at the midpoint of the Page RAM (0x8100). This location always contains the SL code for the first line of Display Window 2.
Bits 15–9	These bits are reserved and should be set to zero.

Display Window 2 Column Width:

COLWIDTH2B3 (0x841F)	COLWIDTH2B2 (0x841E)
Window 2 Column Width - High Bytes	
COL2[31:16]	

Control Register Definitions (Continued)

COLWIDTH2B1 (0x841D)	COLWIDTH2B0 (0x841C)
Window 2 Column Width - Low Bytes	
COL2[15:0]	

Bits 31–0	These are the Display Window 2 Column Width 2x Enable Bits. These thirty-two bits correspond to columns 31–0 of Display Window 2, respectively. A value of zero indicates the column will have normal width (12 OSD pixels). A value of one indicates the column will be twice as wide as normal (24 OSD pixels). For the double wide case, each Character Font pixel location will be displayed twice, in two consecutive horizontal pixel locations. The user should note that if more than 32 display characters are programmed to reside on a line, then all display characters after the first thirty-two will have normal width (12 pixels).

Fade In/Fade Out Interval Register:

FADE_INTVL (0x8429)	
Vertical Interval	**Horizontal Interval**
V_INTVL[3:0]	H_INTVL[3:0]

Bits 7–4	These three bits determine the interval for fading in or fading out the OSD window in the vertical direction.
Bits 3–0	These three bits determine the interval for fading in or fading out the OSD window in the horizontal direction.

Pre-Amplifier Interface Registers

Blue Channel Gain:

BGAINCTRL (0x8430)	
Res'd	**Blue Gain**
RSV	BGAIN[6:0]

Bits 6–0	This register determines the gain of the blue video channel. This affects only the blue channel whereas the contrast register (0x8433) affects all channels.
Bit 7	Reserved and should be set to zero.

Green Channel Gain:

GGAINCTRL (0x8431)	
Res'd	**Green Gain**
RSV	GGAIN[6:0]

Bits 6–0	This register determines the gain of the green video channel. This affects only the green channel whereas the contrast register (0x8433) affects all channels.
Bit 7	Reserved and should be set to zero.

Red Channel Gain:

RGAINCTRL (0x8432)	
Res'd	**Red Gain**
RSV	RGAIN[6:0]

Bits 6–0	This register determines the gain of the red video channel. This affects only the red channel whereas the contrast register (0x8433) affects all channels.
Bit 7	Reserved and should be set to zero.

Contrast Control:

CONTRCTRL (0x8433)	
Res'd	**Contrast**
RSV	CONTRAST[6:0]

Pre-Amplifier Interface Registers (Continued)

Bits 6–0	This register determines the contrast gain and affects all three channels, blue, red and green.
Bit 7	Reserved and should be set to zero.

DAC 1 Output Level:

DAC1CTRL (0x8434)
DAC 1 Output Level
DAC1[7:0]

Bits 7–0	This register determines the output of DAC 1. The full-scale output is determined by bit 6 of the DAC Config, OSD Contrast & DC Offset Register (0x8438).

DAC 2 Output Level:

DAC2CTRL (0x8435)
DAC 2 Output Level
DAC2[7:0]

Bits 7–0	This register determines the output of DAC 2. The full-scale output is determined by bit 6 of the DAC Config, OSD Contrast & DC Offset Register (0x8438).

DAC 3 Output Level:

DAC3CTRL (0x8436)
DAC 3 Output Level
DAC3[7:0]

Bits 7–0	This register determines the output of DAC 3. The full-scale output is determined by bit 6 of the DAC Config, OSD Contrast & DC Offset Register (0x8438).

DAC 4 Output Level:

DAC4CTRL (0x8437)
DAC 4 Output Level
DAC4[7:0]

Bits 7–0	This register determines the output of DAC 4. The output of this DAC can be scaled and mixed with the outputs of DACs 1–3 as determined by bit 7 of the DAC Config, OSD Contrast & DC Offset Register (0x8438).

DAC Config, OSD Contrast & DC Offset:

DACOSDDCOFF (0x8438)		
DAC Options	**OSD Contrast**	**DC Offset**
DCF[1:0]	OSD[2:0]	DC[2:0]

Bits 2–0	These determine the DC offset of the three video outputs, blue, red and green.
Bits 5–3	These determine the contrast of the internally generated OSD.
Bit 6	When this bit is a 0, the full-scale outputs of DACs 1–3 are 0.5V to 4.5V. When it is a 1, the full-scale range is 0.5V to 2.5V.
Bit 7	When this bit is a 0, the DAC 4 output is independent. When it is a 1, the DAC 4 output is scaled by 50% and added to the outputs of DACs 1–3.

Global Video Control:

GLOBALCTRL (0x8439)						
Burn In Contrast	**Burn In**	**PLL**	**Res'd**	**Res'd**	**Power**	**Blank**
BI[1:0]	BI_EN	PLLCAL	RSV	RSV	PS	BV

Pre-Amplifier Interface Registers (Continued)

Bit 0	When this bit is a 1, the video outputs are blanked (set to black level). When it is a 0, video is not blanked.
Bit 1	When this bit is a 1, the analog sections of the preamplifier are shut down for low power consumption. When it is a 0, the analog sections are enabled.
Bits 3–2	Reserved.
Bit 4	When this bit is set high, the calibration sequence for the PLL Auto Mode is initiated, the PLL Auto mode is activated, and will unset itself upon completion.
Bit 5	This bit will enable the Burn In Screen.
Bits 7–6	These bits determine the contrast level of the Burn In Screen.

Auxiliary Control 1:

AUXCTRL1 (0x843A)			
Horizontal Blank Position	**H. Blank**	**Reserved**	**H Blnk**
HBPOS[4:0]	HBPOS_EN	RSV	HBD

Bit 0	When this bit is a 0, the horizontal blanking input at pin 28 is gated to the video outputs to provide horizontal blanking. When it is a 1, the horizontal blanking at the outputs is disabled.
Bit 1	Reserved.
Bit 2	When this bit is a 1, the position of the Horizontal Blanking pulse can be programmably varied relative to the horizontal flyback in number of pixels. When this bit is a 0, which is by default, the horizontal blanking pulse position will not be programmable.
Bits 7–3	These 5 bits determine the position of the Horizontal Blanking Pulse with respect to the horizontal flyback in number of pixels.

Auxiliary Control 2:

AUXCTRL2 (0x843E)							
Res'd	**Res'd**	**Clamp**	**Clamp Switch**	**OSD**	**VBlank**	**Res'd**	**Res'd**
RSV	RSV	CLMP	CLMP SW	OOR	VBL	RSV	RSV

Bits 1–0	Reserved and should be set to zero.
Bit 2	This is the Vertical Blanking register. When this bit is a 1, vertical blanking is gated to the video outputs. When set to a 0, the video outputs do not have vertical blanking.
Bit 3	This is the OSD override bit. This should be set to 0 for normal operation. When set to a 1, the video outputs are disconnected and OSD only is displayed. This is useful for the OSD display of special conditions such as "No Signal" and "Input Signal Out of Range", to avoid seeing unsynchronized video.
Bit 4	Setting this bit will internally tie the clamp pin to the horizontal sync pin, and the clamp pin will not require an external input signal.
Bit 5	This is the Clamp Polarity bit. When set to a 0, the LM1276 expects a positive going clamp pulse. When set to a 1, the expected pulse is negative going.
Bits 7–6	Reserved and should be set to zero.

OSD Tone Transparency:

OSD TRANSP TONE (0x85C0)	
Res'd	**OSD TONE**
RSV	OSDTONE[6:0]

Bits 6–0	These bits determine the transparency level of the OSD background.
Bit 7	Reserved and should be set to zero.

Pre-Amplifier Interface Registers (Continued)

Center Frequency:

EMPHASIS_CENTF(0x85C1)				
Center Frequency	**Res'd**	**Res'd**	**Res'd**	**Res'd**
CENTF[3:0]	RSV	RSV	RSV	RSV

Bits 3–0	Reserved and should be set to zero.
Bits 7–4	These 4 bits control the Center Frequency adjustment of the Hi-Brite window video signal for enhancement.

ABL Control 0

ABLCTRL0 (0x85C4)	
Reserved	**ABL Current**
RSV	ABL0[3:0]

Bits 3–0	These bits determine the ABL current limiting threshold for ABL setting 0.
Bits 7–4	Reserved and should be set to zero.

ABL Control 1

ABLCTRL1 (0x85C5)	
Reserved	**ABL Current**
RSV	ABL1[3:0]

Bits 3–0	These bits determine the ABL current limiting threshold for ABL setting 1.
Bits 7–4	Reserved and should be set to zero.

ABL Control 2

ABLCTRL2 (0x85C6)	
Reserved	**ABL Current**
RSV	ABL2[3:0]

Bits 3–0	These bits determine the ABL current limiting threshold for ABL setting 2.
Bits 7–4	Reserved and should be set to zero.

ABL Control 3

ABLCTRL3 (0x85C7)	
Reserved	**ABL Current**
RSV	ABL3[3:0]

Bits 3–0	These bits determine the ABL current limiting threshold for ABL setting 3.
Bits 7–4	Reserved and should be set to zero.

Peak Control TEXT

PEAKCNTLTXT (0x85C8)		
Reserved	**RSV**	**TEXT MODE OVERSHOOT**
RSV	RSV	TM_OVRSHT[2:0]

Bits 2–0	These bits determine the amount of overshoot for the TEXT mode
Bits 7–3	Reserved and should be set to zero.

Pre-Amplifier Interface Registers (Continued)

Highlight Contrast TEXT:

HLCONTRTXT (0x85C9)	
Res'd	**HILIGHT_CONTRAST**
RSV	HILIGHT_CONTRAST[6:0]

Bits 6–0	These bits determine the amount of Highlight Contrast for the TEXT mode.
Bit 7	Reserved and should be set to zero.

Peak Control PIC

PEAKCNTLPIC (0x85CA)	
Reserved	**PIC MODE OVERSHOOT**
RSV	PM_OVRSHT[2:0]

Bits 2–0	These bits determine the amount of overshoot for the PIC mode
Bits 7–3	Reserved and should be set to zero.

Highlight Contrast PIC:

HLCONTRPIC (0x85CB)	
Res'd	**HILIGHT_CONTRAST**
RSV	HILIGHT_CONTRAST[6:0]

Bits 6–0	These bits determine the amount of Highlight Contrast for the PIC mode.
Bit 7	Reserved and should be set to zero.

Peak Control MOVIE

PEAKCNTLMOV (0x85CC)	
Reserved	**TEXT MODE OVERSHOOT**
RSV	MM_OVRSHT[2:0]

Bits 2–0	These bits determine the amount of overshoot for the MOVIE mode
Bits 7–3	Reserved and should be set to zero.

Highlight Contrast MOVIE:

HLCONTRTXT (0x85CD)	
Res'd	**HILIGHT_CONTRAST**
RSV	HILIGHT_CONTRAST[6:0]

Bits 6–0	These bits determine the amount of Highlight Contrast for the MOVIE mode.
Bit 7	Reserved and should be set to zero.

Auto Size Registers

Horizontal Front Porch Duration:

H_FP1 (0x8581)					H_FP0 (0x8580)
Reserved					**Horizontal Front Porch Duration**
RSV	RSV	RSV	RSV	RSV	HFP[10:0]

Bits 10–0	This is an 11-bit wide register that records the lowest measured value of the horizontal front porch during video detect. When no video is detected, this register should return a value of zero. Once measurement is completed and the auto size enable bit has cleared itself back to 0, the measured data is ready to be read by the microcontroller. Reading this register before that may give erroneous results. This register resets to default values, ready to record new measured values when the auto size enable bit is set again.

Auto Size Registers (Continued)

Horizontal Flyback or Sync Duration:

HF_S1 (0x8583)						HF_S0 (0x8582)
Reserved						Horizontal Flyback or Sync Duration
RSV	RSV	RSV	RSV	RSV	RSV	HFL_HS[9:0]

Bits 9–0	This is a 10-bit wide register that records the measured value of the horizontal flyback or sync during video detect. When no video is detected, this register should return a value of zero. Once measurement is completed and the auto size enable bit has cleared itself back to 0, the measured data is ready to be read by the microcontroller. Reading this register before that may give erroneous results. This register resets to default values, ready to record new measured values when the auto size enable bit is set again.

Horizontal Back Porch Duration:

H_BP1 (0x8585)					H_BP0 (0x8584)
Reserved					Horizontal Back Porch Duration
RSV	RSV	RSV	RSV	RSV	HBP[10:0]

Bits 10–0	This is an 11-bit wide register that records the lowest measured value of the horizontal back porch during video detect. When no video is detected, the sum of this register and the horizontal flyback or sync should be within 1 pixel of the total number of pixels per line. Once measurement is completed and the auto size enable bit has cleared itself back to 0, the measured data is ready to be read by the microcontroller. Reading this register before that may give erroneous results. This register resets to default values, ready to record new measured values when the auto size enable bit is set again.

Vertical Front Porch Duration:

V_FP1 (0x8587)					V_FP0 (0x8586)
Reserved					Vertical Front Porch Duration
RSV	RSV	RSV	RSV	RSV	VFP[10:0]

Bits 10–0	This is an 11-bit wide register that records the lowest measured value of the vertical front porch in terms of horizontal line periods during video detect. When no video is detected, this register should return a value of zero. Once measurement is completed and the auto size enable bit has cleared itself back to 0, the measured data is ready to be read by the microcontroller. Reading this register before that may give erroneous results. This register resets to default values, ready to record new measured values when the auto size enable bit is set again.

Vertical Sync Duration:

V_SYN_D (0x8588)
Vertical Flyback or Sync Duration
VSYNC[7:0]

Bits 7–0	This is an 8-bit wide register that records the measured value of the vertical flyback or sync in terms of horizontal line periods during video detect. Once measurement is completed and the auto size enable bit has cleared itself back to 0, the measured data is ready to be read by the microcontroller. Reading this register before that may give erroneous results. This register resets to default values, ready to record new measured values when the auto size enable bit is set again.

Vertical Back Porch Duration:

V_BP1 (0x858A)					V_BP0 (0x8589)
Reserved					Vertical Back Porch Duration
RSV	RSV	RSV	RSV	RSV	VBP[10:0]

Auto Size Registers (Continued)

Bits 10–0	This is an 11-bit wide register that records the lowest measured value of the vertical back porch in terms of horizontal line periods during video detect. When no video is detected, the sum of this register and the vertical flyback or sync should be within 1 line of the total number of lines per field. Once measurement is completed and the auto size enable bit has cleared itself back to 0, the measured data is ready to be read by the microcontroller. Reading this register before that may give erroneous results. This register resets to default values, ready to record new measured values when the auto size enable bit is set again.

Previous Field Vertical Front Porch Duration:

PREV_V_BP1 (0x858C)					PREV_V_BP0 (0x858B)
Reserved					Previous Vertical Front Porch Duration
RSV	RSV	RSV	RSV	RSV	VFP PREV[10:0]

Bits 10–0	This is an 11-bit wide register that retains the previous lowest measured value of the vertical front porch during video detect in horizontal line periods from the previous field. It is used when interlace mode is present, in order to accurately determine the correct parameter value for the frame. When no video is detected, this register should return a value of zero. Reading this register within less than one complete field period after the Video Detect Reset may give erroneous results. This register resets to zero after the Video Detect Reset has been written.

Previous Field Vertical Sync Duration:

V_SYN_PREV (0x858D)
Previous Vertical Sync Duration
VSYNC PREV[7:0]

Bits 7–0	This is an 8-bit wide register that records the previous measured value of the vertical sync during video detect in horizontal line periods from the previous field. It is used when interlace mode is present, in order to accurately determine the correct parameter value for the frame. Reading this register within less than one complete field period after the Video Detect Reset may give erroneous results. This register resets to zero after the Video Detect Reset has been written.

Previous Vertical Back Porch Duration:

PREV_V_BP1 (0x858F)					PREV_V_BP0 (0x858E)
Reserved					Previous Vertical Back Porch Duration
RSV	RSV	RSV	RSV	RSV	VBP PREV[10:0]

Bits 10–0	This is an 11-bit wide register that records the previous lowest measured value of the vertical back porch during video detect in horizontal line periods from the previous field. It is used when interlace mode is present, in order to accurately determine the correct parameter value for the frame. When no video is detected, this sum of this register and the VSYNC should be with 1 line of the total number of lines per field. Reading this register within less than one complete field period after the Video Detect Reset may give erroneous results. This register resets to zero after the Video Detect Reset has been written.

HiBrite Control Register:

HB CONTROL (0x8590)							
INTR_EN	LIMIT	WHDIS	FSHEN	RSV	RSV	RSV	RSV

Bits 3–0	Reserved and should be set to zero.
Bit 4	This bit must be low for the device to display HiBrite Software driven windows. This bit must be set high for Full Screen HiBrite by the MCU. **Bits 4 and 5 must be both high for Full Screen HiBrite.**
Bit 5	This bit when set high will enable the Full Screen Hi-Brite feature. This bit can be used by the MCU to highlight the entire screen without the use of the HiBrite software.
Bit 6	This bit must be set to 1 at all times for proper color bar communication.

Auto Size Registers (Continued)

Bits 7	Interrupt Enable. This bit must be set to 1 to activate the use of the interrupt bit in 0x8591

HiBrite Status Register:

STATUS (0x8591)							
INTR	RSV	RSV	RSV	RSV	RSV	RSV	RSV

Bits 6–0	Reserved and should be set to zero.
Bits 7	This bit is the interrupt bit and must be frequently polled (at least 480ms interval) by the MCU for a value of 1, and must be also reset by the MCU thereafter. The interrupt bit will automatically be set high when the software has attempted to send a command to the MCU, with the chip as the messenger. It must be set back to 0 by the MCU afterwards so that it can be set high the next time the MCU software makes another attempt to send a command.

MCU Command Register:

MCU COMMAND (0x8592)
MCU COMMAND[7:0]

Bits 7–0	Command. These bits are the MCU command bits. **The MCU must read a value of 0x80 from this register.**

Sub Command Register:

SUB COMMAND (0x8593)
SUB COMMAND[7:0]

Bits 7–0	Sub Command. These bits are the sub command bits. If a value of this register is 0x01: This value corresponds to a HiBrite Software "UP" command. 0x02: This value corresponds to a HiBrite Software "DOWN" command. 0x01: This value corresponds to a prompt for the MCU to perform a "V Blank Duration Adjustment."

Sequence Number:

SEQ NUM (0x859A)
SEQ NUM[7:0]

Bits 7–0	Sequence. These bits are the Sequence number command bits. The MCU should read this register and take note of the sequence number to compare with the current sequence number. Since an MCU sub command is continuously transmitted by the software for a duration of time, the interrupt bit will be set back to high again redundantly, which will falsely notify the MCU of another sub command. To prevent this, the sequence number which is only updated on truly new commands, will prevent redundant commands and have the the MCU set the interrupt but low accordingly.

Please see the "MCU Programmer's Guide" Applications note on more detailed information regarding the use of registers 0x8590 - 0x859A.

Internal PLL Lock Detect Control Register:

STATUS (0xFFF8)							
RSV	RSV	LOCK SET	LOCK ORR	RSV	RSV	RSV	RSV

Bits 3–0	Reserved and should be set to zero.
Bits 5-4	When enabling the OSD display, these 2 bits must be enabled first, and then disabled when the OSD display is disabled. This should also be done before performing an auto size calculation.
Bits 7-6	Reserved and should be set to zero.

H INPUT SEL (0xFFFD)							
RSV	RSV	RSV	RSV	HSEL	RSV	RSV	RSV

Auto Size Registers (Continued)

Bits 2–0	Reserved and should be set to zero.
Bit 3	When enabling this bit, the H Flyback input is internally received from the H Sync input.
Bits 7-4	Reserved and should be set to zero.

Attribute Table and Enhanced Features

Each display character and SL in the Display Page RAM will have a 4-bit Attribute Table entry associated with it. The user should note that two-color display characters and four-color display characters use two different Attribute Tables, effectively providing 16 attributes for two-color display characters and 16 attributes for four-color display characters.

For two-color characters, the attribute contains the code for the 9-bit foreground color (Color 1), the code for the 9-bit background color (Color 0), and the character's enhanced features (Button Box, Blinking, Heavy Box, Shadowing, Bordering, etc.).

For four-color characters, the attribute contains the code for the 9-bit Color 0, the code for the 9-bit Color 1, the code for the 9-bit Color 2, the code for the 9-bit Color 3, and the character's enhanced features (Button Box, Blinking, Heavy Box, Shadowing, Bordering, etc.).

TWO COLOR ATTRIBUTE FORMAT

The address range for an attribute number, 0 ≤ n ≤ 15, is provided in *Table 25*.

ATT2C3n (0x8443+n*4)								ATT2C2n (0x8442+n*4)			
Reserved										Enhanced Feature	Color 1 -
X	X	X	X	X	X	X	X	X	X	EFB[3:0]	C1B[2:1]

ATT2C1n (0x8441+n*4)			ATT2C0n (0x8440+n*4)		
Blue	Color 1 - Green	Color 1 - Red	Color 0 - Blue	Color 0 - Green	Color 0 - Red
C2B0	C1G[2:0]	C1R[2:0]	C0B[2:0]	C0G[2:0]	C0R[2:0]

Bits 8–0	These nine bits determine the background color (color1), which is displayed when the corresponding OSD pixel is a 0.
Bits 17–9	These nine bits determine the foreground color (color2), which is displayed when the corresponding OSD pixel is a 1.
Bits 21–18	These are the enhanced feature (EF) bits, which determine which feature is applied to the displayed character. The features and their corresponding codes are shown in *Table 24*.
Bits 31–22	Reserved and should be set to zero.

TABLE 24. Enhanced Feature Descriptions

Bits 21–18	Feature Description
0000b	Normal Display
0001b	Blinking
0010b	Shadowing
0011b	Bordering
0100b	RESERVED
0101b	RESERVED
0110b	RESERVED
0111b	RESERVED
1000b	Raised Box
1001b	Blinking and Raised Box
1010b	Depressed Box
1011b	Blinking and Depressed Box
1100b	Heavy Raised Box
1101b	Blinking and Heavy Raised Box
1110b	Heavy Depressed Box
1111b	Blinking and Heavy Depressed Box

FOUR COLOR ATTRIBUTE FORMAT

The address range for an attribute number, 0 ≤ n ≤ 15, is provided in *Table 25*.

Attribute Table and Enhanced Features (Continued)

ATT4C7n (0x8507+n*4)								ATT4C6n (0x8506+n*4)						
Reserved														Color 3 -
X	X	X	X	X	X	X	X	X	X	X	X	X	X	C3B[2:1]

ATT4C5n (0x8505+n*4)				ATT4C4n (0x8504+n*4)	
Blue	Color 3 - Green	Color 3 - Red	Color 2 - Blue	Color 2 - Green	Color 2 - Red
C3B0	C3G[2:0]	C3R[2:0]	C2B[2:0]	C2G[2:0]	C2R[2:0]

ATT4C3n (0x8503+n*4)								ATT4C2n (0x8502+n*4)			
Reserved										Enhanced Features	Color 1 -
X	X	X	X	X	X	X	X	X	X	EFB[3:0]	C1B[2:1]

ATT4C1n (0x8501+n*4)			ATT4C0n (0x8500+n*4)		
Blue	Color 1 - Green	Color 1 - Red	Color 0 - Blue	Color 0 - Green	Color 0 - Red
C1B0	C1G[2:0]	C1R[2:0]	C0B[2:0]	C0G[2:0]	C0R[2:0]

Bits 8–0	These nine bits determine color 0 which is displayed when the corresponding OSD pixel code is 00b.
Bits 17–9	These nine bits determine color 1 which is displayed when the corresponding OSD pixel code is 01b.
Bits 21–18	These are the enhanced feature (EF) bits, which determine which feature is applied to the displayed character. The features and their corresponding codes are shown in *Table 24*.
Bits 31–22	Reserved and should be set to zero.
Bits 40–32	These nine bits determine color2, which is displayed when the corresponding OSD pixel code is 10b.
Bits 49–41	These nine bits determine color3, which is displayed when the corresponding OSD pixel code is 11b.
Bits 63–50	Reserved and should be set to zero.

TABLE 25. Attribute Tables and Corresponding Addresses

Attribute Number, n	Two-Color Attribute Table Address	Four-Color Attribute Table Address
0000b	0x8440–0x8443	0x8500–0x8507
0001b	0x8444–0x8447	0x8508–0x850F
0010b	0x8448–0x844B	0x8510–0x8517
0011b	0x844C–0x844F	0x8518–0x851F
0100b	0x8450–0x8453	0x8520–0x8527
0101b	0x8454–0x8457	0x8528–0x852F
0110b	0x8458–0x845B	0x8530–0x8537
0111b	0x845C–0x845F	0x8538–0x853F
1000b	0x8460–0x8463	0x8540–0x8547
1001b	0x8464–0x8467	0x8548–0x854F
1010b	0x8468–0x846B	0x8550–0x8557
1011b	0x846C–0x846F	0x8558–0x855F
1100b	0x8470–0x8473	0x8560–0x8567
1101b	0x8474–0x8477	0x8568–0x856F
1110b	0x8478–0x847B	0x8570–0x8577
1111B	0x847C–0x847F	0x8578–0x857F

BUTTON BOX FORMATION

Please refer to the LM1247 datasheet for details.

Operation of the Shadow Feature

Please refer to the LM1247 datasheet for details.

Operation of the Bordering Feature

Please refer to the LM1247 datasheet for details.

Constant Character Height Mechanism

Please refer to the LM1247 datasheet for details.

Attribute Table and Enhanced Features (Continued)

Display Window 1 to Display Window 2 Spacing

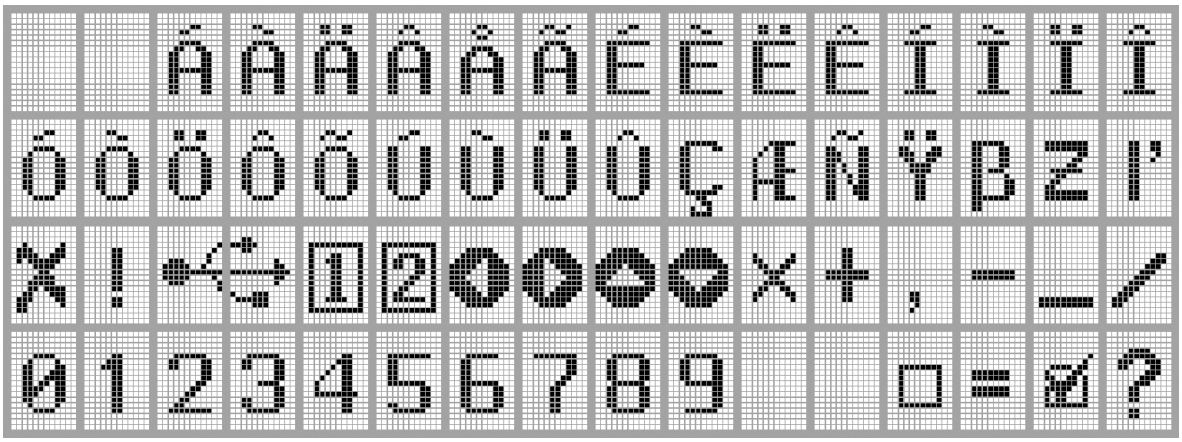
Please refer to the LM1247 datasheet for details.

Evaluation Character Fonts

The character font for evaluation of the LM1276 is shown in *Figure 19* through *Figure 26*, where each represents one of the 8 available ROM banks. Each bank is shown with increasing character address going from upper left to lower right. The actual font will depend on customer customization requirements.

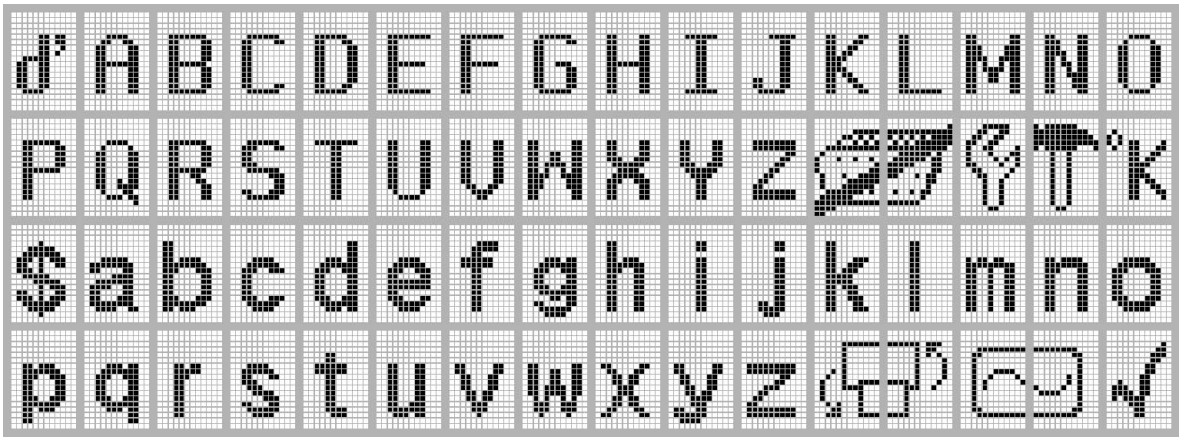
Note that the first two character codes of the two-color font in ROM bank 4 (0x00 and 0x01) are carried over from the LM1237 ROM where they were reserved for the End-Of-Screen (EOS) and End-Of-Line (EOL) codes respectively.

In the case of the LM1276, these two locations can be used for displayable characters as long as they are not needed when this bank is addressed from Bank Select Register 0. If it is addressed from Bank Select Registers 1, 2 or 3, then these two lower characters will be usable. Please see the section “END-OF-LINE and END-OF-SCREEN CODES”. Similarly, the first two characters in any bank, which is addressed from Bank Select Register 0 will not be usable since those addresses will be interpreted as the EOL and EOS codes.



20096944

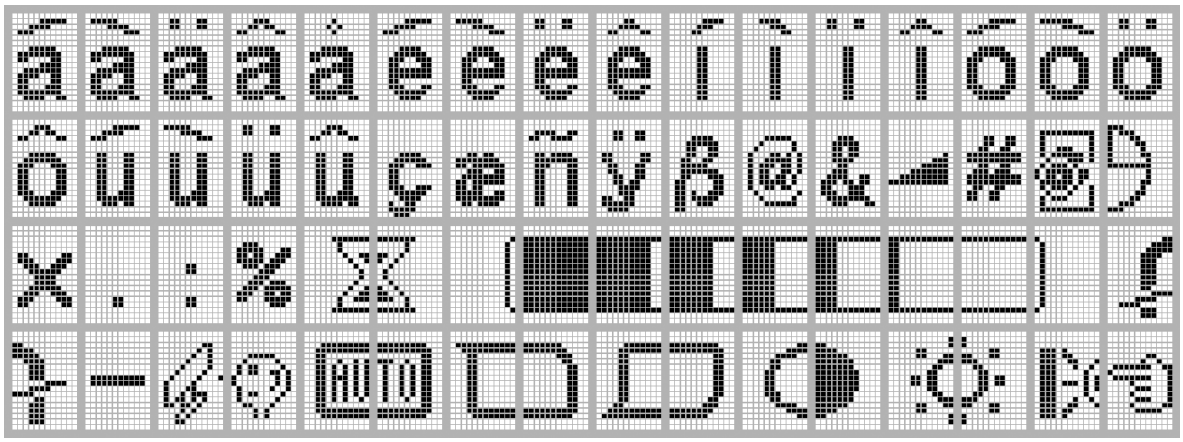
FIGURE 19. ROM Bank 0 Two Color Character Font



20096945

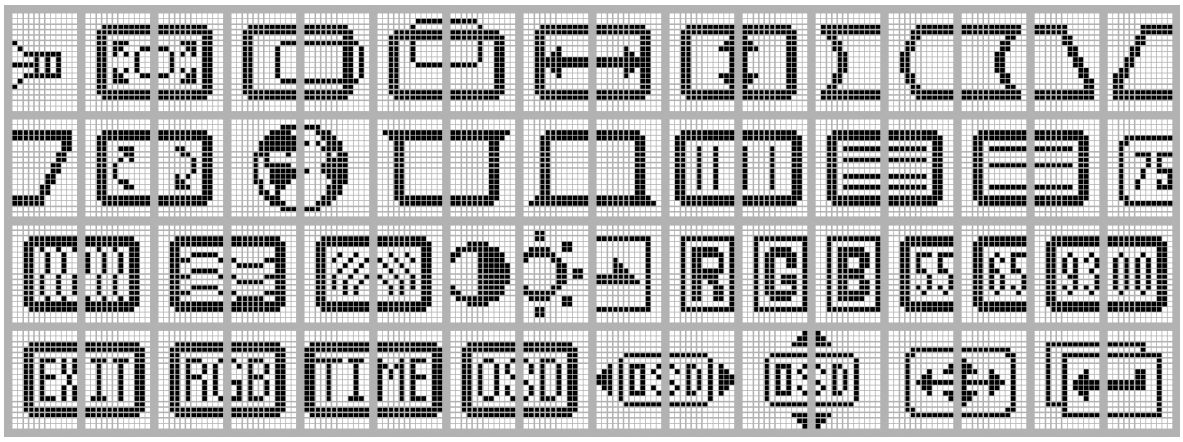
FIGURE 20. ROM Bank 1 Two Color Character Font

Attribute Table and Enhanced Features (Continued)



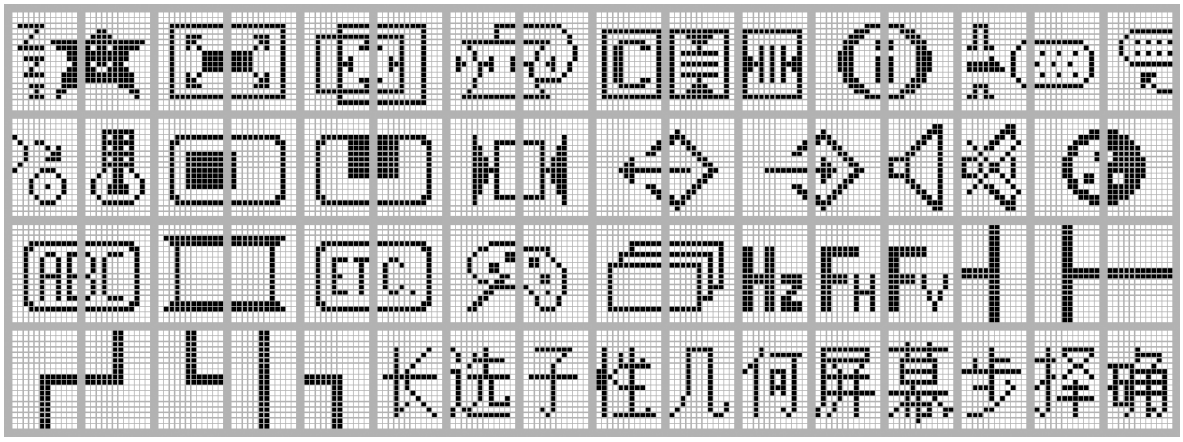
20096946

FIGURE 21. ROM Bank 2 Two Color Character Font



20096947

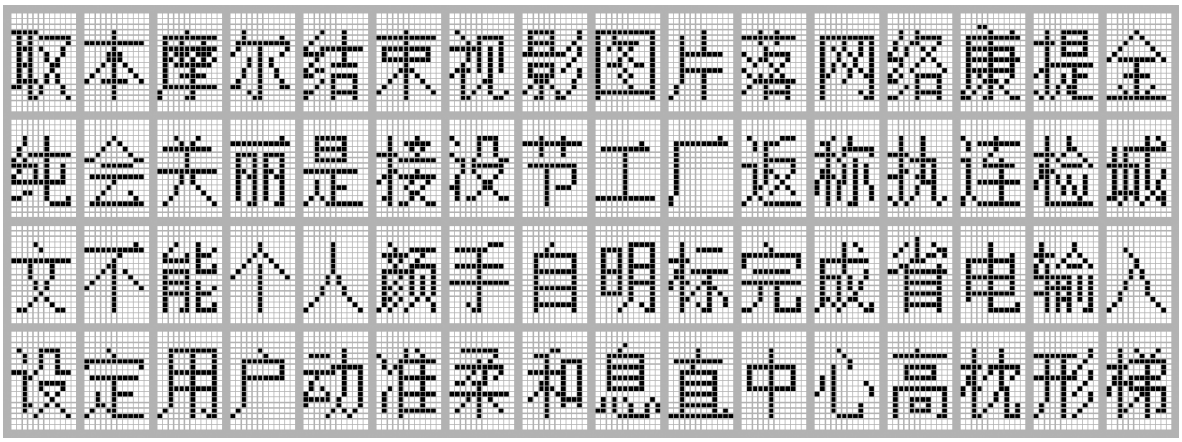
FIGURE 22. ROM Bank 3 Four Color Character Font



20096948

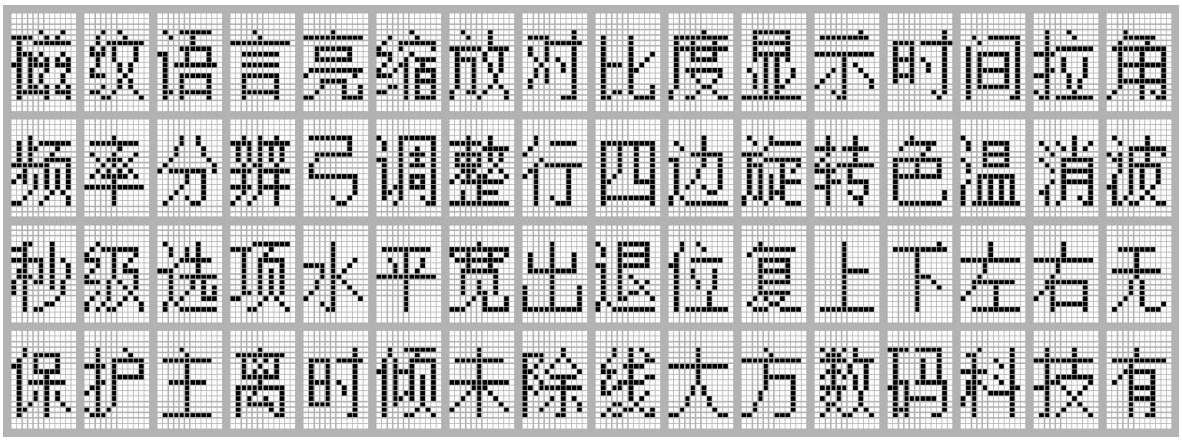
FIGURE 23. ROM Bank 4 Two Color Character Font

Attribute Table and Enhanced Features (Continued)



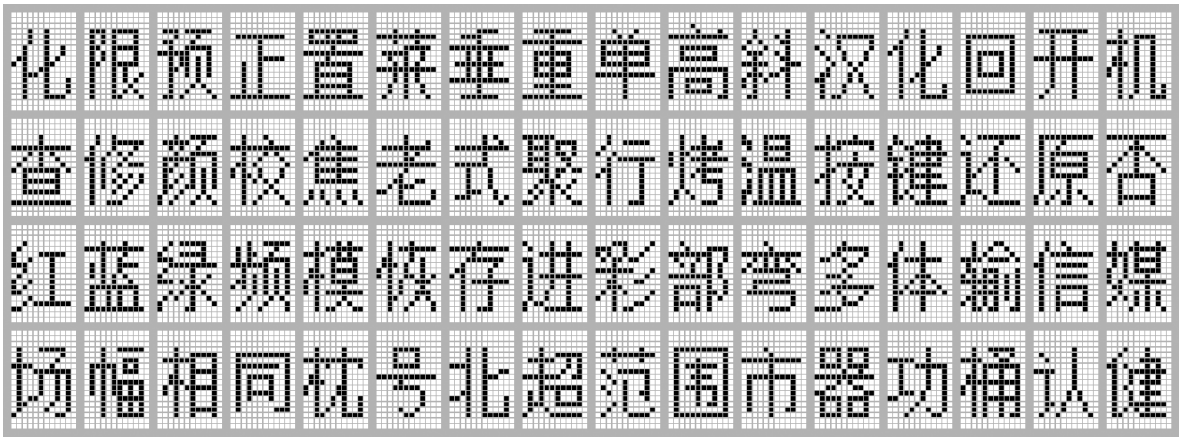
20096949

FIGURE 24. ROM Bank 5 Two Color Character Font



20096950

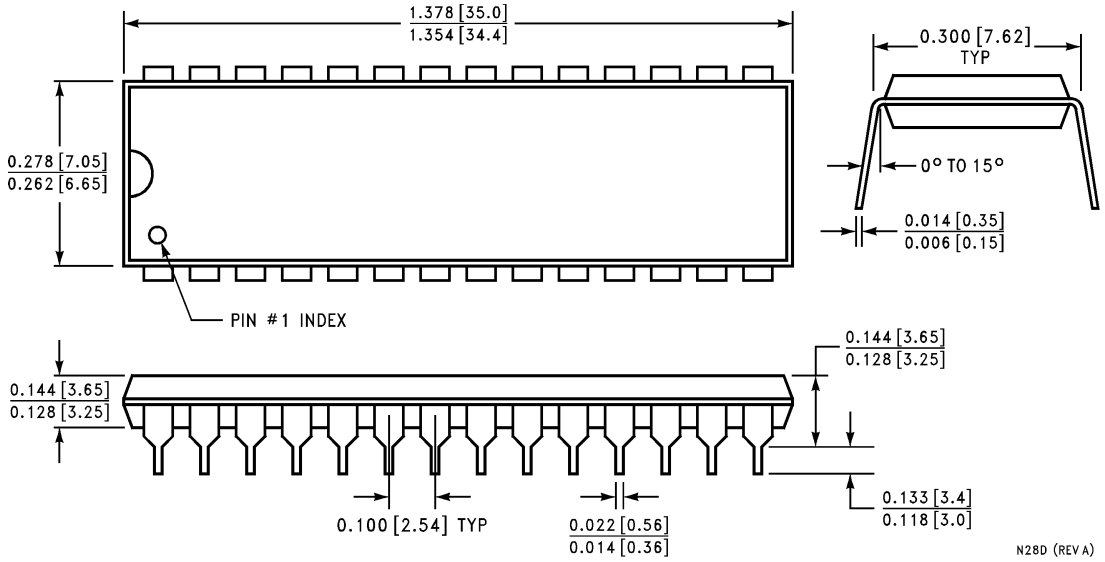
FIGURE 25. ROM Bank 6 Two Color Character Font



20096951

FIGURE 26. ROM Bank 7 Four Color Character Font

Physical Dimensions inches (millimeters) unless otherwise noted



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