July 17, 2008

DS16EV5110
Video Equalizer (3D+C) for DVI, HDMI Sink-Side Applications

General Description

The DS16EV5110 is a multi-channel equalizer optimized for video cable extension sink-side applications. It operates between 250Mbps and 2.25Gbps with common applications at 1.65Gbps and 2.25Gbps (per data channel). It contains three Transition-Minimized Differential Signaling (TMDS) data channels and one clock channel as commonly found in DVI and HDMI cables. It provides compensation for skin-effect and dielectric losses, a common phenomenon when transmitting video on commercially available high definition video cables.

The inputs conform to DVI and HDMI requirements and features programmable levels of input equalization. The programmable levels of equalization provide optimal signal boost and reduces inter-symbol interference. Eight levels of boost are selectable via a pin interface or by the optional System Management Bus.

The clock channel is optimized for clock rates of up to 225 MHz and features a signal detect circuit. To maximize noise immunity, the DS16EV5110 features a signal detector with programmable thresholds. The threshold is adjustable through a System Management Bus (SMBus) interface.

The DS16EV5110 also provides support for system power management via output enable controls. Additional controls are provided via the SMBus enabling customization and optimization for specific applications requirements. These controls include programmable features such as output amplitude and boost controls as well as system level diagnostics.
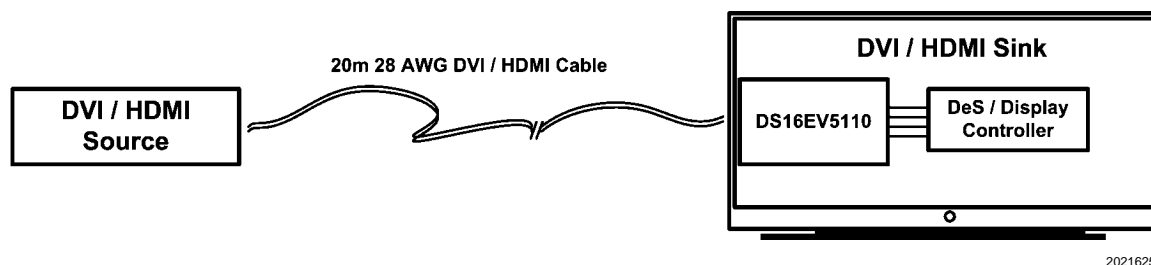
Features

- 8 levels of equalization settable by 3 pins or through the SMBus interface
- DC-Coupled inputs and outputs
- Optimized for operation from 250 Mbps to 2.25 Gbps in support of UXGA, 480 I/P, 720 I/P, 1080 I, and 1080 P with 8, 10, and 12–bit Color Depth Resolutions
- Two DS16EV5110 devices support DVI/HDMI Dual Link
- DVI 1.0, and HDMI 1.3a Compatible TMDS Interface
- Clock channel signal detect (LOS)
- Enable for power savings standby mode
- System Management Bus (SMBus) provides control of boost, output amplitude, enable, and clock channel signal detect threshold
- Low power consumption: 475mW (Typical)
- 0.13 UI total jitter at 1.65 Gbps including cable
- Single 3.3V power supply
- Small 7mm x 7mm, 48-pin leadless LLP package
- -40°C to +85°C operating temperature range
- Extends TMDS cable reach over:
  1. > 40 meters 24 AWG DVI Cable (1.65Gbps)
  2. > 20 meters 28 AWG DVI Cable (1.65Gbps)
  3. > 20 meters Cat5/Cat5e/Cat6 cables (1.65Gbps)
  4. > 20 meters 28 AWG HDMI cables (2.25Gbps)

Applications

- Sink–side Video Applications:
- Projectors
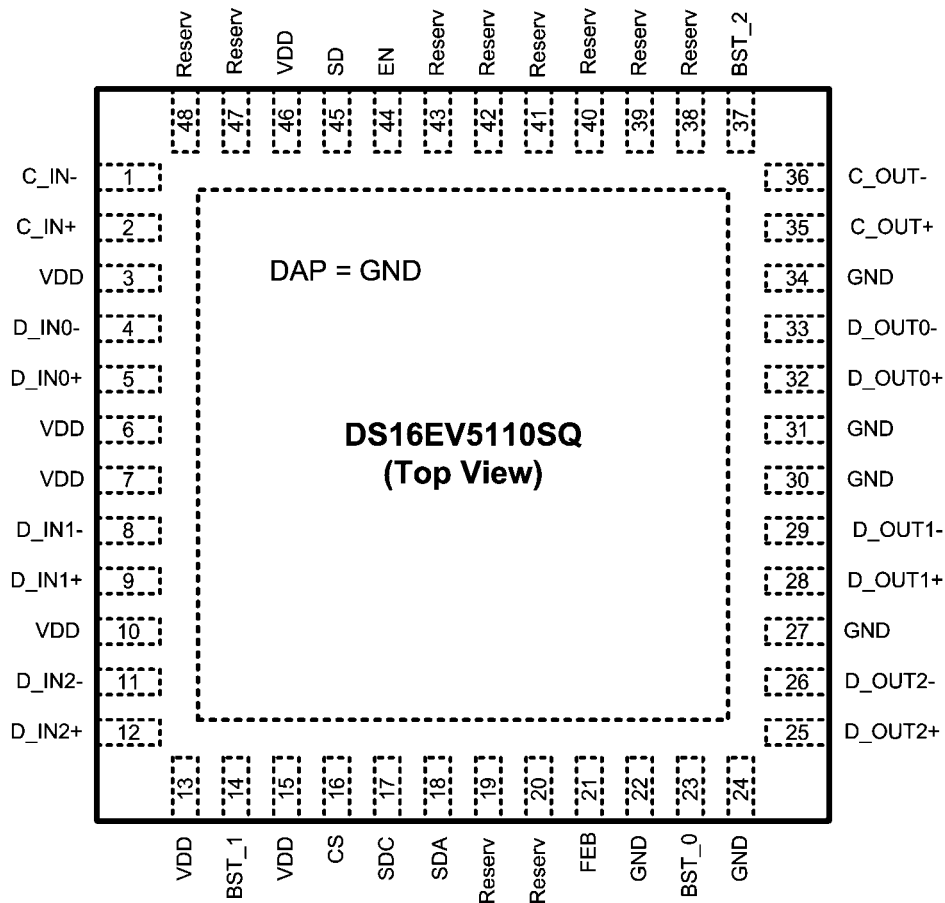- High Definition Displays

Typical Application

20216251

Pin Descriptions

Pin Name	Pin Number	I/O, Type	Description
HIGH SPEED DIFFERENTIAL I/O			
C_IN– C_IN+	1 2	I, CML	Inverting and non-inverting TMDS Clock inputs to the equalizer. An on-chip 50Ω terminating resistor connects C_IN+ to VDD and C_IN- to VDD.
D_IN0– D_IN0+	4 5	I, CML	Inverting and non-inverting TMDS Data inputs to the equalizer. An on-chip 50Ω terminating resistor connects D_IN0+ to VDD and D_IN0- to VDD.
D_IN1– D_IN1+	8 9	I, CML	Inverting and non-inverting TMDS Data inputs to the equalizer. An on-chip 50Ω terminating resistor connects D_IN1+ to VDD and D_IN1- to VDD.
D_IN2– D_IN2+	11 12	I, CML	Inverting and non-inverting TMDS Data inputs to the equalizer. An on-chip 50Ω terminating resistor connects D_IN2+ to VDD and D_IN2- to VDD.
C_OUT- C_OUT+	36 35	O, CML	Inverting and non-inverting TMDS outputs from the equalizer. Open collector.
D_OUT0– D_OUT0+	33 32	O, CML	Inverting and non-inverting TMDS outputs from the equalizer. Open collector.
D_OUT1– D_OUT1+	29 28	O, CML	Inverting and non-inverting TMDS outputs from the equalizer. Open collector.
D_OUT2– D_OUT2+	26 25	O, CML	Inverting and non-inverting TMDS outputs from the equalizer. Open collector.
Equalization Control			
BST_0 BST_1 BST_2	23 14 37	I, LVCMOS	BST_0, BST_1, and BST_2 select the equalizer boost level for EQ channels. BST_0, BST_1, and BST_2 are internally pulled Low. See *Table 2*.
Device Control			
EN	44	I, LVCMOS	Enable Equalizer input. When held High, normal operation is selected. When held Low, standby mode is selected. EN is internally pulled High. Signal is global to all Data and Clock channels.
FEB	21	I, LVCMOS	Force External Boost. When held High, the equalizer boost setting is controlled by the BST_[0:2] pins. When held Low, the equalizer boost level is controlled through the SMBus (see *Table 1*) control pins. FEB is internally pulled High.
SD	45	O, LVCMOS	Equalizer Clock Channel Signal Detect Output. Produces a High when signal is detected.
POWER			
V_{DD}	3, 6, 7, 10, 13, 15, 46	Power	V$_{DD}$ pins should be tied to the V$_{DD}$ plane through a low inductance path. A 0.1µF bypass capacitor should be connected between each V$_{DD}$ pin to the GND planes.
GND	22, 24, 27, 30, 31, 34	GND	Ground reference. GND should be tied to a solid ground plane through a low impedance path.
Exposed Pad	DAP	GND	The exposed pad at the center of the package must be connected to the ground plane.
System Management Bus (SMBus) Interface Control Pins			
SDA	18	IO, LVCMOS	SMBus Data Input / Output. Internally pulled High to 3.3V with High-Z pull up.
SDC	17	I, LVCMOS	SMBus Clock Input. Internally pulled High to 3.3V with High-Z pull up.
CS	16	I, LVCMOS	SMBus Chip select. When held High, the equalizer SMBus register is enabled. When held Low, the equalizer SMBus register is disabled. CS is internally pulled Low. CS is internally gated with SDC.
Other			
Reserv	19, 20, 38, 39, 40,41, 42, 43, 47, 48		Reserved. Do not connect.

Note: I = Input, O = Output, IO =Input/Output,

Connection Diagram

Pins (left side, top to bottom): 1 C_IN-, 2 C_IN+, 3 VDD, 4 D_IN0-, 5 D_IN0+, 6 VDD, 7 VDD, 8 D_IN1-, 9 D_IN1+, 10 VDD, 11 D_IN2-, 12 D_IN2+

Pins (top, left to right): 48 Reserv, 47 Reserv, 46 VDD, 45 SD, 44 EN, 43 Reserv, 42 Reserv, 41 Reserv, 40 Reserv, 39 Reserv, 38 Reserv, 37 BST_2

Pins (right side, top to bottom): 36 C_OUT-, 35 C_OUT+, 34 GND, 33 D_OUT0-, 32 D_OUT0+, 31 GND, 30 GND, 29 D_OUT1-, 28 D_OUT1+, 27 GND, 26 D_OUT2-, 25 D_OUT2+

Pins (bottom, left to right): 13 VDD, 14 BST_1, 15 VDD, 16 CS, 17 SDC, 18 SDA, 19 Reserv, 20 Reserv, 21 FEB, 22 GND, 23 BST_0, 24 GND

DAP = GND

DS16EV5110SQ (Top View)

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TOP VIEW — Not to Scale

Ordering Information

NSID	Tape & Reel Quantity	Package
DS16EV5110SQ	250	SQA48D
DS16EV5110SQX	2,500	SQA48D

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	-0.5V to +4.0V
LVCMOS Input Voltage	-0.5V + 4.0V
LVCMOS Output Voltage	-0.5V to 4.0V
CML Input/Output Voltage	-0.5V to 4.0V
Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temp. (Soldering, 5 sec.)	+260°C

ESD Rating

HBM, 1.5 kΩ, 100 pF	>8 kV
CML Inputs	>10 kV
Thermal Resistance	
θ_{JA}, No Airflow	30°C/W

Recommended Operating Conditions (Notes 2, 3)

	Min	Typ	Max	Units
Supply Voltage (V_{DD} to GND)	3.0	3.3	3.6	V
Ambient Temperature	-40	25	+85	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless other specified. (Notes 2, 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVCMOS DC SPECIFICATIONS						
I_{IH-PU}	High Level Input Leakage Current	LVCMOS pins with internal pull-up resistors	-10		+10	μA
I_{IH-PD}	High Level Input Leakage Current	LVCMOS pins with internal pull-down resistors	80		105	μA
I_{IL-PU}	Low Level Input Leakage Current	LVCMOS pins with internal pull-up resistors	-20		-10	μA
I_{IL-PD}	Low Level Input Leakage Current	LVCMOS pins with internal pull-down resistors	-10		+10	μA
V_{IH}	High Level Input Voltage		2.0		VDD	V
V_{IL}	Low Level Input Voltage		0		0.8	V
V_{OH}	High Level Output Voltage	SD Pin, I_{OH} = -3mA	2.4			V
V_{OL}	Low Level Output Voltage	SD Pin, I_{OL} = 3mA			0.4	V
POWER						
PD	Power Dissipation	EN = High, Device Enabled		475	700	mW
		EN = Low, Power Down Mode			70	mW
N	Supply Noise Tolerance (Note 4)	DC to 50MHz		100		mV_{P-P}
CML INPUTS						
V_{TX}	Input Voltage Swing (Launch Amplitude)	Measured differentially at TPA (*Figure 2*)	800		1200	mV_{P-P}
V_{ICMDC}	Input Common-Mode Voltage	DC-Coupled Requirement Measured at TPA (*Figure 2*)	V_{DD}-0.3		V_{DD}-0.2	V
V_{IN}	Input Voltage Swing	Measured differentially at TPB (*Figure 2*)		120		mV_{P-P}
R_{LI}	Differential Input Return Loss	100 MHz– 825 MHz, with fixture's effect de-embedded		10		dB
R_{IN}	Input Resistance	IN+ to VDD and IN– to VDD	45	50	55	Ω
CML OUTPUTS						
V_O	Output Voltage Swing	Measured differentially with OUT+ and OUT– terminated by 50Ω to VDD	800		1200	mV_{P-P}
V_{OCM}	Output common-mode Voltage	Measured Single-ended	V_{DD}-0.3		V_{DD}-0.2	V
t_R, t_F	Transition Time	20% to 80% of differential output voltage, measured within 1" from output pins.	75		240	ps
t_{CCSK}	Inter Pair Channel-to-Channel Skew (all 4 Channels)	Difference in 50% crossing between shortest and longest channels		25		ps

Symbol	Parameter	Conditions	Min	Typ	Max

Electrical Characteristics — System Management Bus Interface (Notes 2, 3)

Over recommended operating supply and temperature ranges unless other specified.

| Symbol	Parameter	Conditions	Min	Typ	Max	Units
System Bus Interface — DC Specifications						
V_{IL}	Data, Clock Input Low Voltage				0.8	V
V_{IH}	Data, Clock Input High Voltage		2.8		V_{DD}	V
I_{PULLUP}	Current through pull-up resistor or current source	VOL = 0.4V		10		mA
V_{DD}	Nominal Bus Voltage		3.0		3.6	V
$I_{LEAK-Bus}$	Input Leakage per bus segment	(Note 9)	—200		+200	µA
$I_{LEAK-Pin}$	Input Leakage per device pin			—15		µA
C_I	Capacitance for SDA and SDC	(Notes 9, 10)			10	pF
R_{TERM}	Termination Resistance	$V_{DD3.3}$, (Notes 9, 10, 11)		1000		Ω
System Bus Interface Timing Specification						
FSMB	Bus Operating Frequency	(Note 12)	10		100	kHz
TBUF	Bus Free Time Between Stop and Start Condition		4.7			µs
THD:STA	Hold Time After (Repeated) Start Condition. First CLK generated after this period.	At I_{PULLUP}, Max	4.0			µs
TSU:STA	Repeated Start Condition Setup Time		4.7			µs
TSU:STO	Stop Condition Setup Time		4.0			µs
THD:DAT	Data Hold Time		300			ns
TSU:DAT	Data Setup Time		250			ns
$T_{TIMEOUT}$	Detect Clock Low Timeout	(Note 12)	25		35	ms
T_{LOW}	Clock Low Period		4.7			µs
T_{HIGH}	Clock High Period	(Note 12)	4.0		50	µs
T_{LOW}:SEXT	Cumulative Clock Low Extend Time (Slave Device)	(Note 12)			2	ms
t_F	Clock/Data Fall Time	(Note 12)			300	ns
t_R	Clock/Data Rise Time	(Note 12)			1000	ns
t_{POR}	Time in which a device must be operational after power-on reset	(Note 12)			500	ms

Note 9: Recommended value. Parameter not tested in production.

Note 10: Recommended maximum capacitance load per bus segment is 400pF.

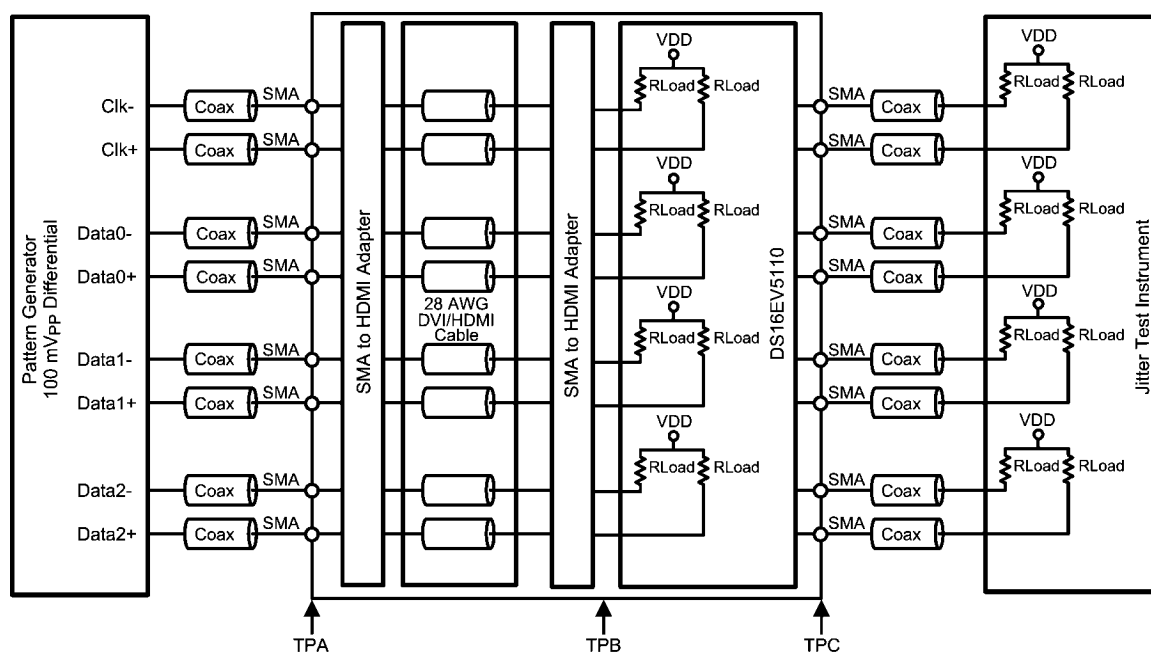**Note 11:** Maximum termination voltage should be identical to the device supply voltage.

Note 12: Compliant to SMBus 2.0 physical layer specification. See System Management Bus (SMBus) Specification Version 2.0, section 3.1.1 SMBus common AC specifications for details.

Timing Diagrams
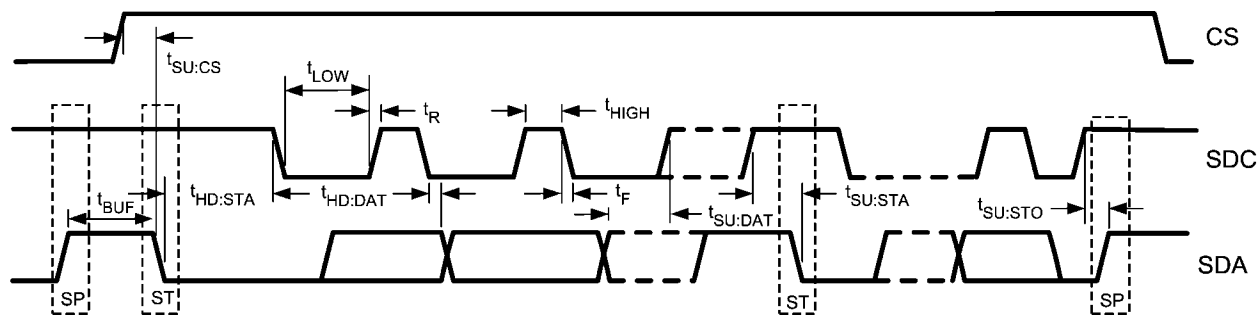
FIGURE 1. SMBus Timing Diagram

FIGURE 2. Test Setup Diagram for Jitter Measurement

System Management Bus (SMBus) and Configuration Registers

The System Management Bus interface is compatible to SM-Bus 2.0 physical layer specification. The use of the Chip Select signal is **required**. Holding the CS pin High enables the SMBus port allowing access to the configuration registers. Holding the CS pin Low disables the device's SMBus allowing communication from the host to other slave devices on the bus. In the STANDBY state, the System Management Bus remains active. When communication to other devices on the SMBus is active, the CS signal for the DS16EV5110s must be driven Low.

The address byte for all DS16EV5110s is AC'h. Based on the SMBus 2.0 specification, the DS16EV5110 has a 7-bit slave address of 1010110'b. The LSB is set to 0'b (for a WRITE), thus the 8-bit value is 1010 1100 'b or AC'h.

The SDC and SDA pins are 3.3V LVCMOS signaling and include high-Z internal pull up resistors. External low impedance pull up resistors maybe required depending upon SMBus loading and speed. Note, these pins are not 5V tolerant.

Transfer of Data via the SMBus

During normal operation the data on SDA must be stable during the time when SDC is High.

There are three unique states for the SMBus:

START: A High-to-Low transition on SDA while SDC is High indicates a message START condition.

STOP: A Low-to-High transition on SDA while SDC is High indicates a message STOP condition.

IDLE: If SDC and SDA are both High for a time exceeding t_{BUF} from the last detected STOP condition or if they are High for a total exceeding the maximum specification for t_{HIGH} then the bus will transfer to the IDLE state.

SMBus Transactions

The device supports WRITE and READ transactions. See Register Description table for register address, type (Read/Write, Read Only), default value and function information.

Writing a Register

To write a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host (Master) selects the device by driving its SMBus Chip Select (CS) signal High.
2. The Host drives a START condition, the 7-bit SMBus address, and a "0" indicating a WRITE.
3. The Device (Slave) drives the ACK bit ("0").
4. The Host drives the 8-bit Register Address.
5. The Device drives an ACK bit ("0").
6. The Host drive the 8-bit data byte.
7. The Device drives an ACK bit ("0").
8. The Host drives a STOP condition.
9. The Host de-selects the device by driving its SMBus CS signal Low.

The WRITE transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

Reading a Register

To read a register, the following protocol is used (see SMBus 2.0 specification).

1. The Host (Master) selects the device by driving its SMBus Chip Select (CS) signal High.
2. The Host drives a START condition, the 7-bit SMBus address, and a "0" indicating a WRITE.
3. The Device (Slave) drives the ACK bit ("0").
4. The Host drives the 8-bit Register Address.
5. The Device drives an ACK bit ("0").
6. The Host drives a START condition.
7. The Host drives the 7-bit SMBus Address, and a "1" indicating a READ.
8. The Device drives an ACK bit "0".
9. The Device drives the 8-bit data value (register contents).
10. The Host drives a NACK bit "1"indicating end of the READ transfer.
11. The Host drives a STOP condition.
12. The Host de-selects the device by driving its SMBus CS signal Low.

The READ transaction is completed, the bus goes IDLE and communication with other SMBus devices may now occur.

Please see *Table 1* for more information.

TABLE 1. SMBus Register Descriptions

Name	Address	Default	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Status	0x00	0x00	RO	ID Revision				Reserved	Reserved	Reserved	SD
Status	0x01	0x00	RO	Reserved	Boost 1			EN	Reserved		
Status	0x02	0x00	RO	Reserved	Boost 3			Reserved	Boost 2		
Internal Enable/ Individual Channel Boost Control for C_IN±, D_IN0±	0x03	0x77	RW	EN (Int.) 0:Enable 1:Disable (D_IN0±)	Boost Control (BC for CH0) 000 (Min Boost) 001 010 011 100 101 110 111 (Max Boost)			EN (Int.) 0:Enable 1:Disable (C_IN±)	Reserved		
Individual Channel Boost Control for D_IN1±, D_IN2±	0x04	0x77	RW	EN (Int.) 0:Enable 1:Disable (D_IN2±)	Boost Control (BC for CH2) 000 (Min Boost) 001 010 011 100 101 110 111 (Max Boost)			EN (Int.) 0:Enable 1:Disable (D_IN1±)	Boost Control (BC for CH1) 000 (Min Boost) 001 010 011 100 101 110 111 (Max Boost)		
Signal Detect ON (SD_ON)	0x05	0x00	RW	Reserved						Threshold (mV) 00: 70 (Default) 01: 55 10: 90 11: 75	
Signal Detect OFF (SD_OFF)	0x06	0x00	RW	Reserved						Threshold (mV) 00: 40 (Default) 01: 30 10: 55 11: 45	
SMBus or CMOS Control for EN	0x07	0x00	RW	Reserved							SMBus Enable 0: Disable 1: Enable
Output Level	0x08	0x78	RW	Reserved				Output Level: 00: 540 mVp-p 01: 770 mVp-p 10: 1000 mVp-p 11: 1200 mVp-p		Reserved	

Note: RO = Read Only, RW = Read/Write

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DS16EV5110 Device Description

The DS16EV5110 video equalizer comprises three data channels, a clock channel, and a control interface including a Systeml Management Bus (SMBus) port.

DATA CHANNELS

The DS16EV5110 provides three data channels. Each data channel consists of an equalizer stage, a limiting amplifier, a DC offset correction block, and a TMDS driver as shown in *Figure 3*.

EQUALIZER BOOST CONTROL

The data channel equalizers support eight programmable levels of equalization boost. The state of the FEB pin determines how the boost settings are controlled. If the FEB pin is held High, then the equalizer boost setting is controlled by the Boost Set pins (BST_[0:2]) in accordance with *Table 2*. If this programming method is chosen, then the boost setting selected on the Boost Set pins is applied to all three data channels. When the FEB pin is held Low, the equalizer boost level is controlled through the SMBus. This programming method is accessed via the appropriate SMBus registers (see *Table 1*). Using this approach, equalizer boost settings can be programmed for each channel individually. FEB is internally pulled High (default setting); therefore if left unconnected, the boost settings are controlled by the Boost Set pins (BST_[0:2]). The range of boost settings provided enables the DS16EV5110 to address a wide range of transmission line path loss scenarios, enabling support for a variety of data rates and formats.

TABLE 2. EQ Boost Control Table

Control Via SMBus BC_2, BC_1, BC_0 (FEB = 0)	Control Via Pins BST_2, BST_1, BST_0 (FEB = 1)	EQ Boost Setting at 825 MHz (dB) (TYP)
000	000	9
001	001	14
010	010	18
011	011	21
100	100	24
101	101	26
110	110	28
111	111	30

DEVICE STATE AND ENABLE CONTROL

The DS16EV5110 has an Enable feature which provides the ability to control device power consumption. This feature can be controlled either via the Enable Pin (EN Pin) or via the Enable Control Bit which is accessed through the SMBus port (see *Table 1* and *Table 3*). If Enable is activated, the data channels and clock channel are placed in the ACTIVE state and all device blocks function as described. The DS16EV5110 can also be placed in STANDBY mode to save power. In this mode only the control interface including the SMBus port as well as the clock channel signal detection circuit remain active.

TABLE 3. Enable and Device State Control

| Register 07[0] (SMBus)	EN Pin (CMOS)	Register 03[3] (EN Control) (SMBus)	Device State
0 : Disable	1	X	ACTIVE
0 : Disable	0	X	STANDBY
1 : Enable	X	0	ACTIVE
1 : Enable	X	1	STANDBY

CLOCK CHANNEL

The clock channel incorporates a limiting amplifier, a DC offset correction, and a TMDS driver as shown in *Figure 4*.

CLOCK CHANNEL SIGNAL DETECT

The DS16EV5110 features a signal detect circuit on the clock channel. The status of the clock signal can be determined by either reading the Signal Detect bit (SD) in the SMBus registers (see *Table 1*) or by the state of the SD pin. A logic High indicates the presence of a signal that has exceeded a specified threshold value (called SD_ON). A logic Low means that the clock signal has fallen below a threshold value (called SD_OFF). These values are programmed via the SMBus (*Table 1*). If not programmed via the SMBus, the thresholds take on the default values for the SD_OFF and SD_ON values as indicated in *Table 4*. The Signal Detect threshold values can be changed through the SMBus. All threshold values specified are DC peak-to-peak differential signals (positive signal minus negative signal) at the input of the device.
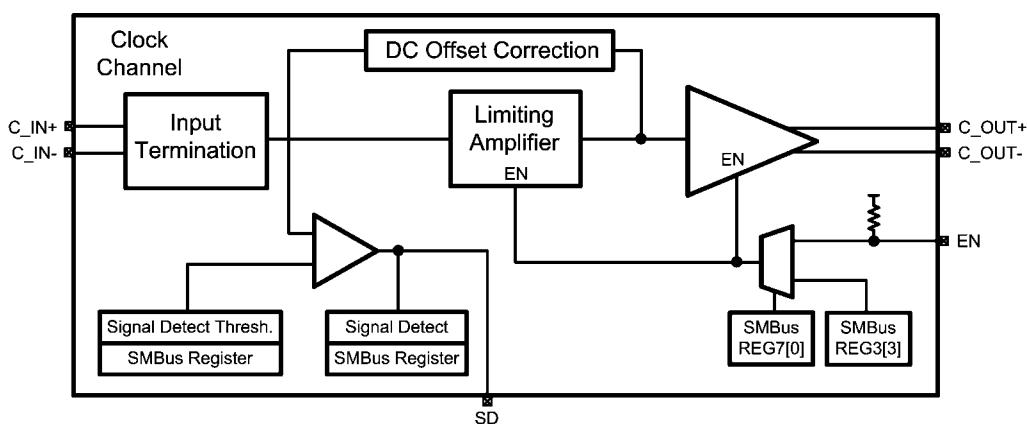
TABLE 4. Clock Channel Signal Detect Threshold Values

Bit 1	Bit 0	SD_OFF Threshold Register 06 (mV)	SD_ON Threshold Register 05 (mV)
0	0	40 (Default)	70 (Default)
0	1	30	55
1	0	55	90
1	1	45	75
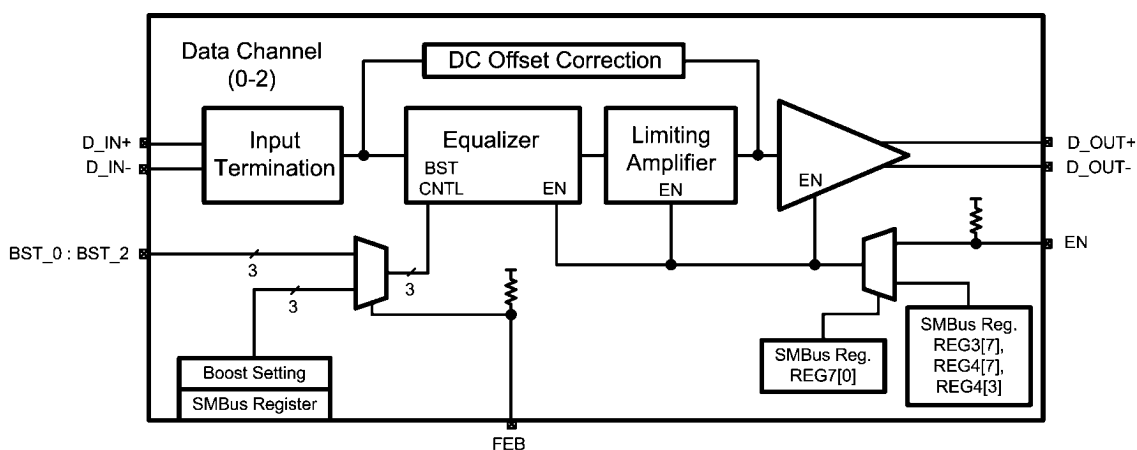
FIGURE 3. DS16EV5110 Data Channel

FIGURE 4. DS16EV5110 Clock Channel

OUTPUT LEVEL CONTROL

The output amplitude of the TMDS drivers for both the data channels and the clock channel can be controlled via the SM-Bus (see *Table 1*). The default output level is 1000mV p-p. The following Table presents the output level values supported:

TABLE 5. Output Level Control Settings – REG 0x08[3:2]

Bit 3	Bit 2	Output Level (mV)
0	0	540
0	1	770
1	0	1000 (default)
1	1	1200

AUTOMATIC ENABLE FEATURE

It may be desired for the DS16EV5110 to be configured to automatically enter STANDBY mode if no clock signal is

present. STANDBY mode can be implemented by connecting the Signal Detect (SD) pin to the external (LVCMOS) Enable (EN) pin. In order for this option to function properly, REG07[0] should be set to a "0" (default value). If the clock signal applied to the clock channel input swings above the SD_ON threshold specified in the threshold register via the SMBus, then the SD pin is asserted High. If the SD pin is connected to the EN pin, this will enable the equalizer, limiting amplifier, and output buffer on the data channels and the limiting amplifier and output buffer on the clock channel; thus the DS16EV5110 will automatically enter the ACTIVE state. If the clock signal present falls below SD_OFF threshold specified in the threshold register, then the SD pin will be asserted Low, causing the aforementioned blocks to be placed in the STANDBY state.

Application Information

The DS16EV5110 is used to recondition DVI/HDMI video signals or differential signals with similar characteristics after signal loss and degradation due to transmission through a length of shielded or unshielded cable. It is intended to be used on the Sink-side of the video link. The DS16EV5110A maybe used on the Source or Sink side of the application. The DS16EV5110 ESD protection circuitry will not support the V_{OFF} specification when the downstream device (e.g. DES) is powered ON and the DS16EV5110 is powered OFF. *Figure 10* shows the CML output circuitry and the ESD protection diode (current path). It is also not recommneded to enable the DS16EV5110 CML outputs without a load attached.
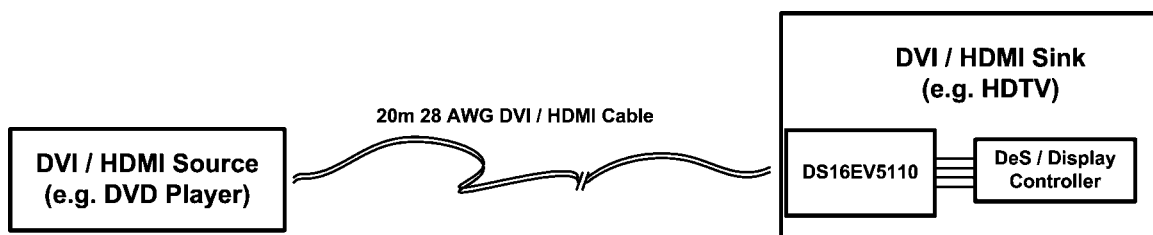
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FIGURE 5. DS16EV5110 Sink-side application

The DS16EV5110 may also be used in certain Source-side application with certain restrictions. The DS16EV5110 CML outputs will not meet the VOFF parameter required by the HDMI Compliance Test Specification (v1.3b) when the DS16EV5110 is powered off and the sink device is powered on. A current path will be enabled through the ESD protection diode (see *Figure 10*). If full compliance is not required, the DS16EV5110 may be used in repeater type application as shown in *Figure 6* .
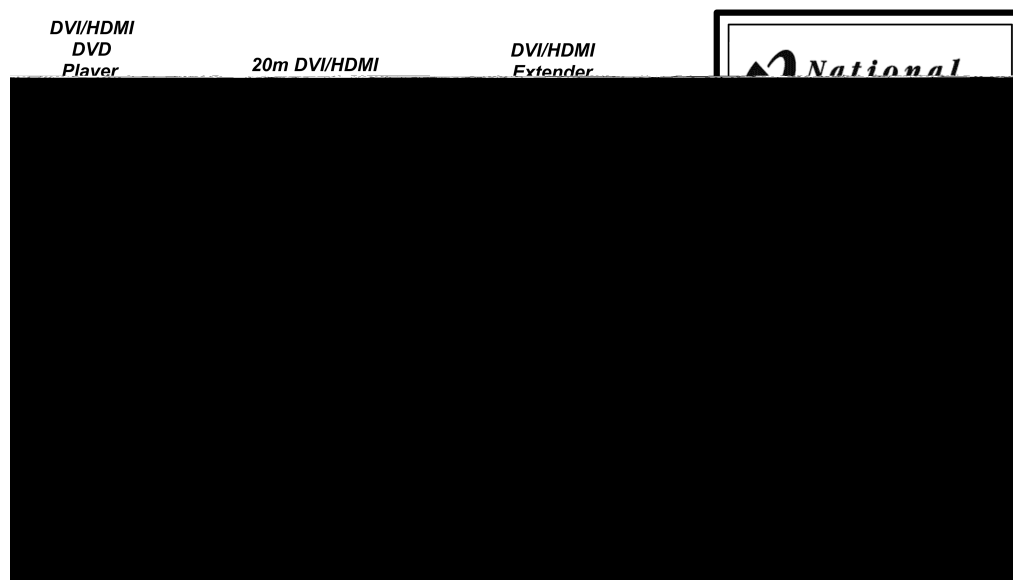
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FIGURE 6. DS16EV5110 Repeater Application with CAT 5 cable

DVI 1.0 AND HDMI V1.2a APPLICATIONS

A single DS16EV5110 can be used to implement cable extension solutions with various resolutions and screen refresh rates. The range of digital serial rates supported is between 250 Mbps and 1.65 Gbps. For applications requiring ultra-high resolution for DVI applications (e.g., QXGA and WQX-GA), a "dual link" TMDS interface is required. This is easily configured by using two DS16EV5110 devices as shown in *Figure 7*.

Note the recommended connections between LVCMOS control pins. This provides the Automatic Enable feature for both devices based on the one active clock channel. In many applications the SMBus is not required (device is pin controlled), for this application simply leave the three SMBus pins open. SDC and SDA are internally pulled High, and CS is internally pulled Low, thus the SMBus is in the disabled state.
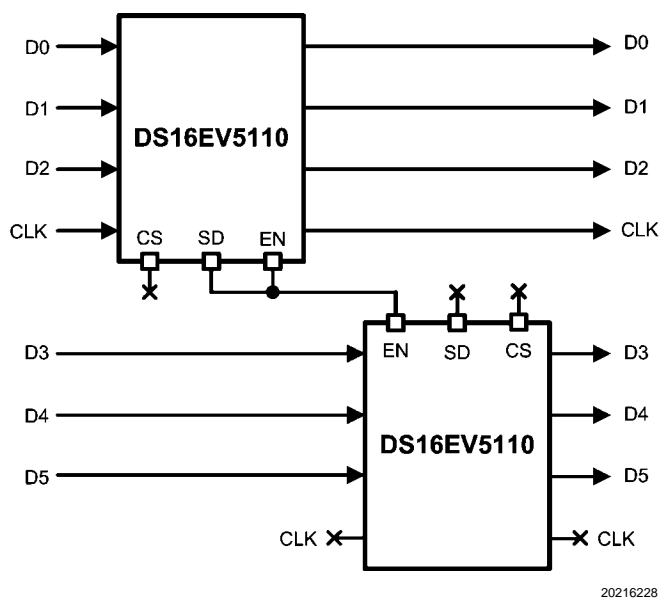
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FIGURE 7. Connection in Dual Link Application

HDMI V1.3 APPLICATION

The DS16EV5110 can reliably extend operation to distances greater than 20 meters of 28 AWG HDMI cable at 2.25 Gbps, thereby supporting HDMI v1.3 for 1080p HDTV resolution with 12-bit color depth. Please note that the Electrical Characteristics specified in this document have not been tested for and are not guaranteed for 2.25 Gbps operation.

DC COUPLED DATA PATHS AND DVI/HDMI COMPLIANCE

The DS16EV5110 is designed to support TMDS differential pairs with DC coupled transmission lines. It contains integrated termination resistors (50Ω), pulled up to VDD at the input stage, and open collector outputs for DVI / HDMI for signal swing.

CABLE SELECTION

At higher frequencies, longer cable lengths produce greater losses due to the skin effect. The quality of the cable with respect to conductor wire gauge and shielding heavily influences performance. Thicker conductors have lower signal degradation per unit length. In nearly all applications, the DS16EV5110 equalization can be set to 0x04, and equalize up to 22 dB skin effect loss for all input cable configurations at all data rates, without degrading signal integrity.

28 AWG STP DVI / HDMI CABLES RECOMMENDED BOOST SETTINGS

The following table presents the recommended boost control settings for various data rates and cable lengths for 28 AWG DVI/HDMI compliant configurations. Boost setting maybe done via the three BST[2:0] pins or via the respective register values.

TABLE 6. Boost Control Setting for STP Cables

Setting	Data Rate	28 AWG DVI / HDMI
0x04	750 Mbps	0–25m
0x04	1.65 Gbps	0–20m
0x06	750 Mbps	25m to greater than 30m
0x06	1.65 Gbps	20m to greater than 25m
0x03	2.25 Gbps	0–15m
0x06	2.25 Gbps	15m to greater than 20m

Figure 8 shows the cable extension and jitter reduction obtained with the use of the equalizer. *Table 6* lists the various gain settings used versus cable length recommendations.
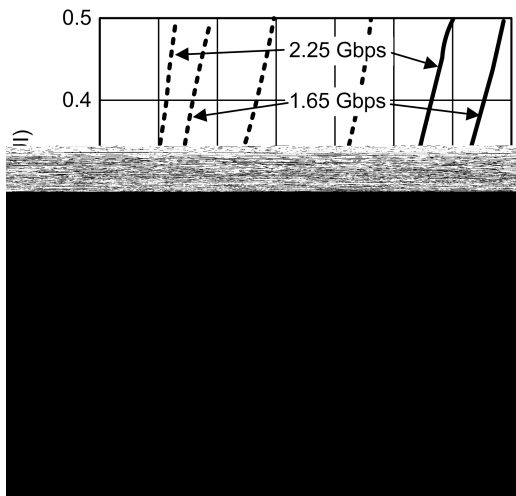
20216242

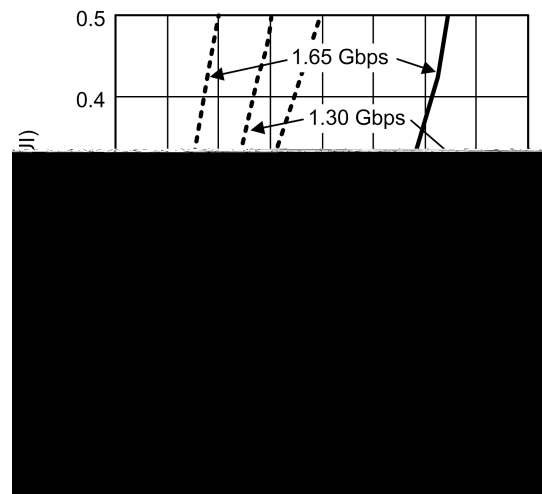**FIGURE 8. Equalized vs. Unequalized Jitter Performance Over 28 AWG DVI/HDMI Cable**

UTP (UNSHIELDED TWIST PAIRS) CABLES

The DS16EV5110 can be used to extend the length of UTP cables, such as Cat5, Cat5e and Cat6 to distances greater than 20 meters at 1.65 Gbps with < 0.13 UI of jitter. Please note that for non-standard DVI/HDMI cables, the user must ensure the clock-to-data channel skew requirements are met. Table 7 presents the recommended boost control settings for various data rates and cable lengths for UTP configurations:

TABLE 7. Boost Control Setting for UTP Cables

Setting	Data Rate	Cat5 Cable
0x03	750 Mbps	0–25m
0x06	750 Mbps	25–45m
0x03	1.65 Gbps	Greater than 20m

Figure 9 shows the cable extension and jitter reduction obtained with the use of the equalizer. *Table 7* lists the various gain settings used versus cable length recommendations.

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FIGURE 9. Equalized vs. Unequalized Jitter Performance Over Cat5 Cable

General Recommendations

The DS16EV5110 is a high performance circuit capable of delivering excellent performance. Careful attention must be paid to the details associated with high-speed design as well as providing a clean power supply. Refer to the LVDS Owner's Manual for more detailed information on high-speed design tips as well as many other available resources available addressing signal integrity design issues.

PCB LAYOUT CONSIDERATIONS FOR DIFFERENTIAL PAIRS

The TMDS differential inputs and outputs must have a controlled differential impedance of 100Ω. It is preferable to route TMDS lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Route the TMDS signals away from other signals and noise sources on the printed circuit board. All traces of TMDS differential inputs and outputs must be equal in length to minimize intra-pair skew.

LLP FOOTPRINT RECOMMENDATIONS

See National application note: AN-1187 for additional information on LLP packages footprint and soldering information.

POWER SUPPLY BYPASSING

Two approaches are recommended to ensure that the DS16EV5110 is provided with an adequate power supply. First, the supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The layer thickness of the dielectric should be minimized so that the VDD and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.1µF bypass capacitor should be connected to each VDD pin such that the capacitor is placed as close as possible to the DS16EV5110. Smaller body size capacitors can help facilitate proper component placement. Additionally, three capacitors with capacitance in the range of 2.2µF to 10µF should be incorporated in the power supply bypassing design as well. These capacitors can be either tantalum or an ultra-low ESR ceramic and should be placed as close as possible to the DS16EV5110.
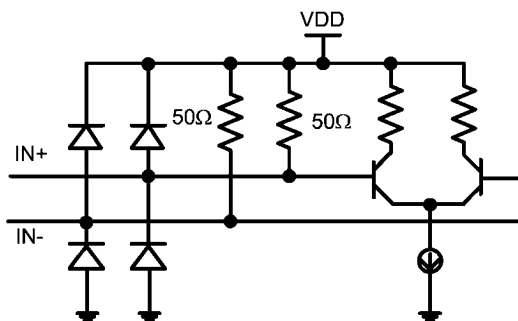
EQUIVALENT I/O STRUCTURES

Figure 10 shows the DS16EV5110 CML output structure and ESD protection circuitry.

Figure 11 shows the DS16EV5110 CML input structure and ESD protection circuitry.
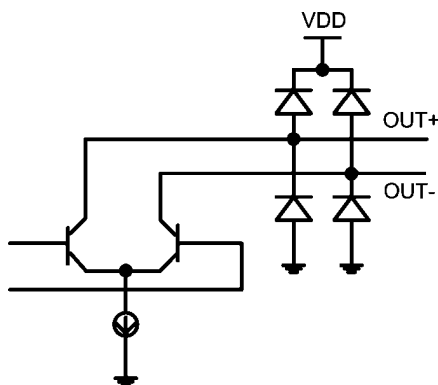
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FIGURE 10. Equivalent Output Structure

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FIGURE 11. Equivalent Input Structure
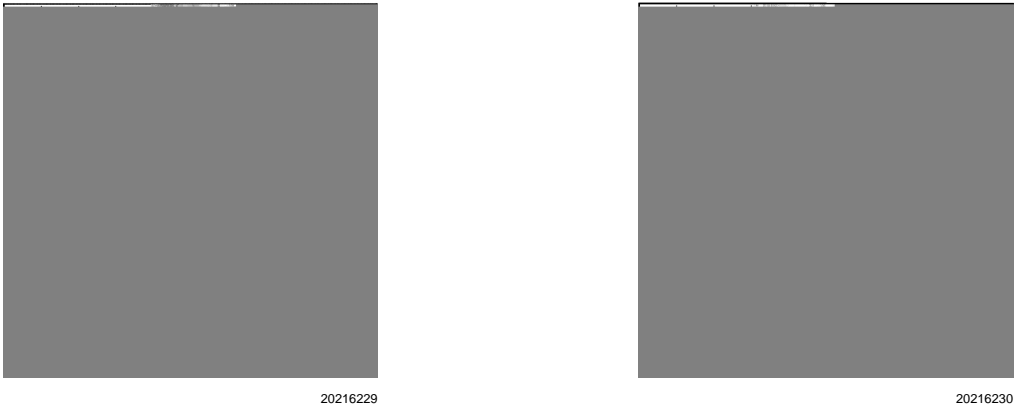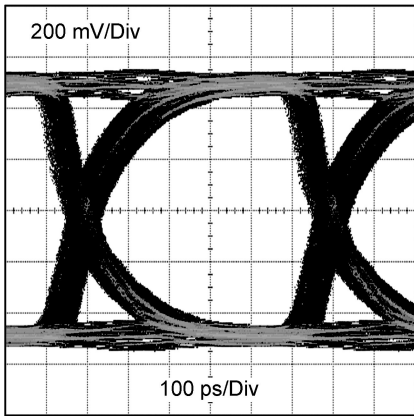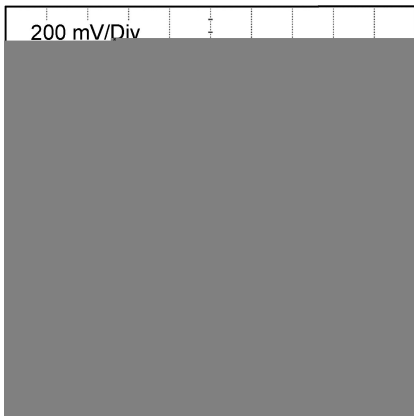
Typical Performance Characteristics

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FIGURE 12. Un-equalized vs. Equalized Signal after 25m of 28 AWG DVI Cable at 1.65 Gbps (0x06 Setting)

200 mV/Div
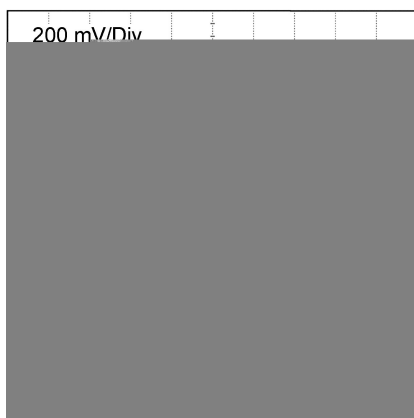
100 ps/Div

20216231

FIGURE 13. Output Signal after 20m of Cat5 Cable at 1.65 Gbps (0x06 Setting)
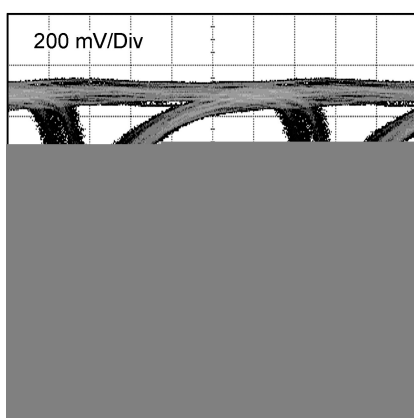

200 mV/Div

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FIGURE 14. Output Signal after 30m of 28 AWG DVI Cable at 750 Mbps (0x06 Setting)
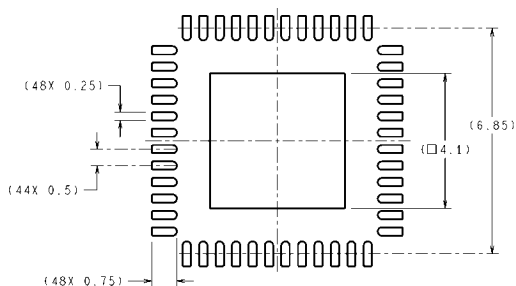
200 mV/Div

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FIGURE 15. Output Signal after 0.3m of 28 AWG DVI Cable at 1.65 Gbps (0x04 Setting)
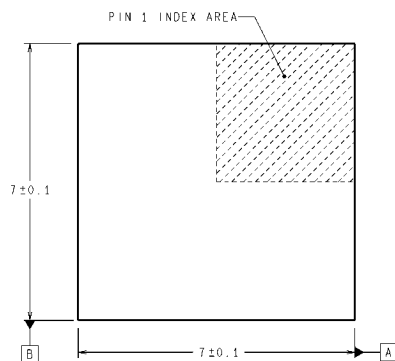

200 mV/Div

20216234

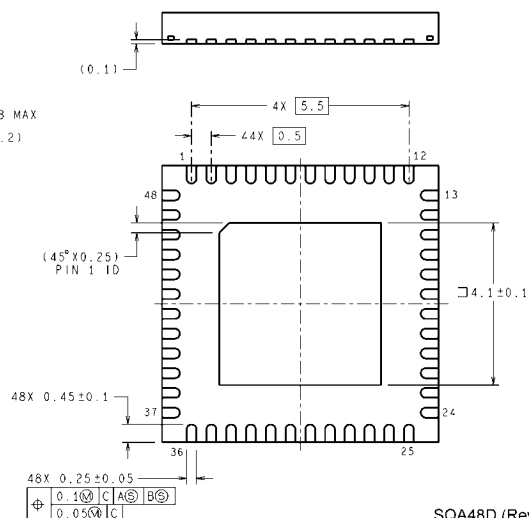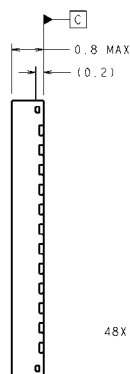**FIGURE 16. Output Signal after 20m of 28 AWG HDMI Cable at 2.25 Gbps (0x06 Setting)**

Physical Dimensions inches (millimeters) unless otherwise noted

(48X 0.25)

(44X 0.5)

(6.85)

(□4.1)

(48X 0.75)

RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

PIN 1 INDEX AREA

7±0.1

7±0.1

B   A

0.8 MAX
(0.2)

(0.1)

4X 5.5
44X 0.5

1   12

48   13

(45°X0.25)
PIN 1 ID

□4.1±0.1

48X 0.45±0.1

37   24

36   25

48X 0.25±0.05

⊕	0.1Ⓜ	C	AⓈ	BⓈ
	0.05Ⓜ	C		

SQA48D (Rev A)

7mm x 7mm 48-pin LLP Package
Order Number DS16EV5110SQ
Package Number SQA48D
To order lead-free products, call your National Semiconductor distributors. They can order products for you with an "NOPB" specification. For more information on our Lead-free program, please check out our Lead-Free Status page.

Notes

Notes

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Data Converters	www.national.com/adc	Distributors	www.national.com/contacts
Displays	www.national.com/displays	Green Compliance	www.national.com/quality/green
Ethernet	www.national.com/ethernet	Packaging	www.national.com/packaging
Interface	www.national.com/interface	Quality and Reliability	www.national.com/quality
LVDS	www.national.com/lvds	Reference Designs	www.national.com/refdesigns
Power Management	www.national.com/power	Feedback	www.national.com/feedback
Switching Regulators	www.national.com/switchers		
LDOs	www.national.com/ldo		
LED Lighting	www.national.com/led		
PowerWise	www.national.com/powerwise		
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