MX506

Advance

November 1989

MX·COM, INC.

DATA BULLETIN

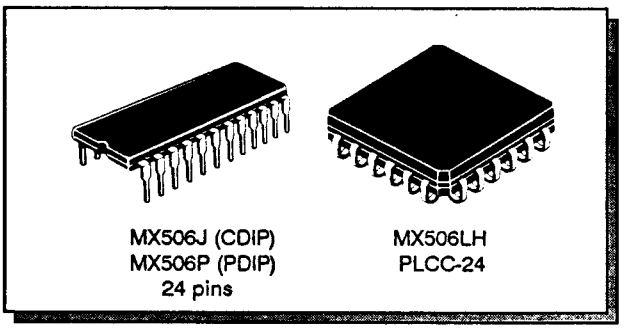
Single Chip LMR Audio Processor

Features

- AGC Amplifier
- Digital Gain Controls
- RX/TX Switching & Filtering
- Squelch Filter
- TX VOGAD
- Serial Bus for all Chip Functions

Benefits

- Serves both Hand-held and Mobiles
- Improves Range
- Saves Space, Power, Cost



MX506J (CDIP)
MX506P (PDIP)
24 pins

MX506LH
PLCC-24

Description

The MX506 is a microprocessor-controlled, single-chip device containing ALL the circuit elements necessary to perform the audio functions of a mobile (or portable) radio system.

Each function in the signal path can be addressed or bypassed -- providing "real time" dynamic control -- through an externally produced serial control word.

This half-duplex device is comprised of two signal stages. The Pre-process path sets the incoming audio (RX or TX) to levels and frequencies that can be used together with auxiliary systems such as Scrambling, Sub-Audible tones, or In-band data signaling.

This path can be output to external processes or internally routed to the Post-process path.

The Post-process path can adjust and prepare the input audio (either internal or external) for output to the chosen transmitter driver or loudspeaker amplifier.

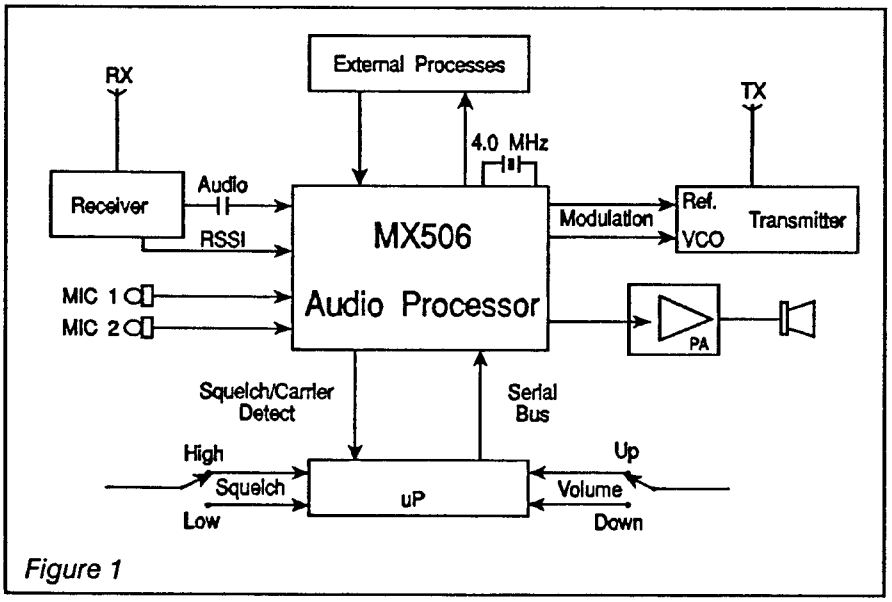


Figure 1

The MX506 can operate on Voice, Direct Digital or Tone data, and is compatible with FM, AM and SSB type transceivers. Digital gain elements are on-chip for dynamic control and balance of signal levels during manufacturing test and operation.

System squelch is derived from either the input audio signal or the Received Signal Strength Indicator (RSSI) in the radio.

This low-power 5 volt CMOS device is available in 24-pin Cerdip, PDIP and PLCC.

The PC5060, an evaluation printed circuit board, will be available to assist in MX506 application design.

Block Diagram for a Typical Land Mobile Radio

The MX506 performs all the functions contained in the gray box in the diagram below.

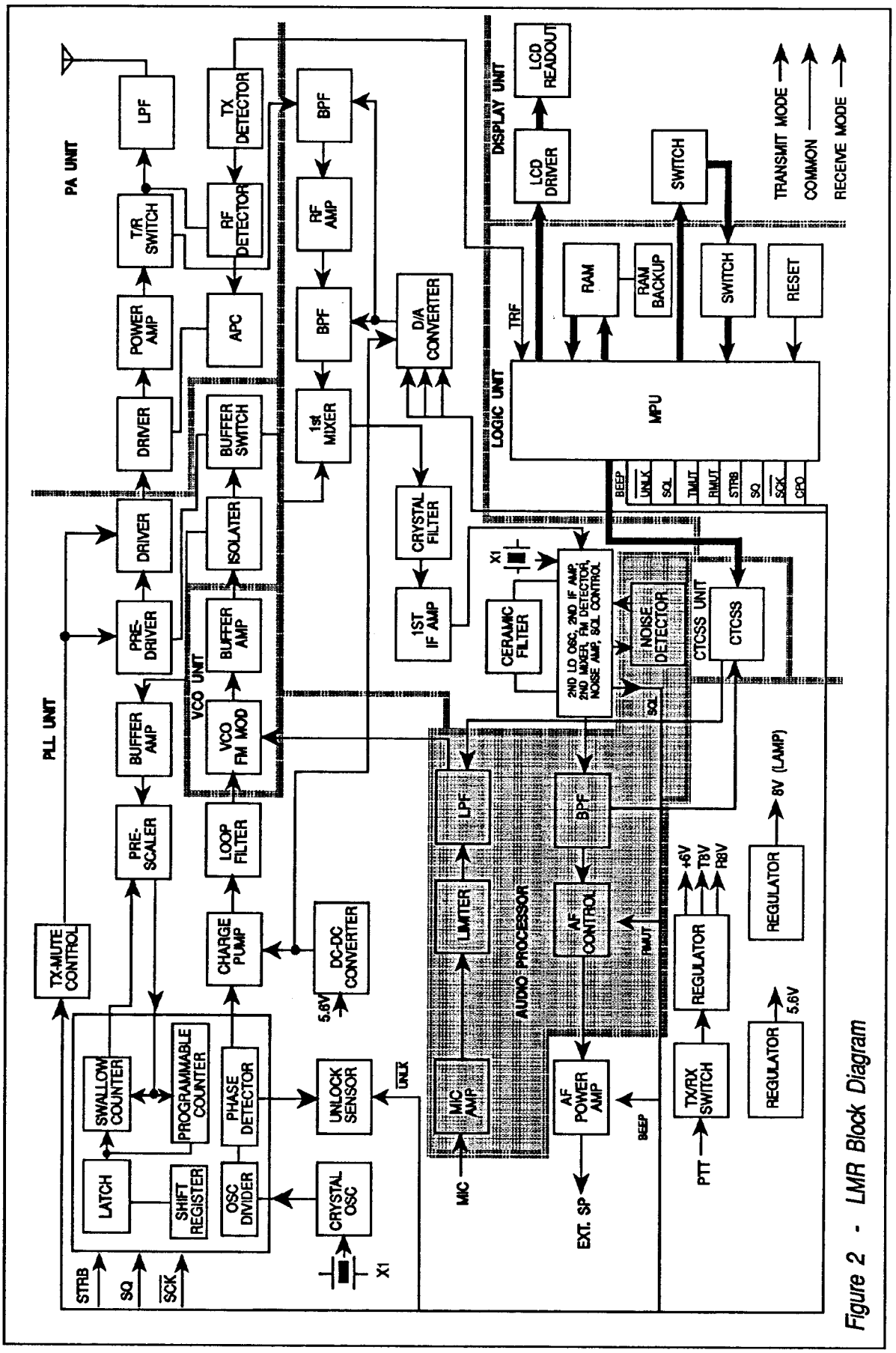


Figure 2 - LMR Block Diagram

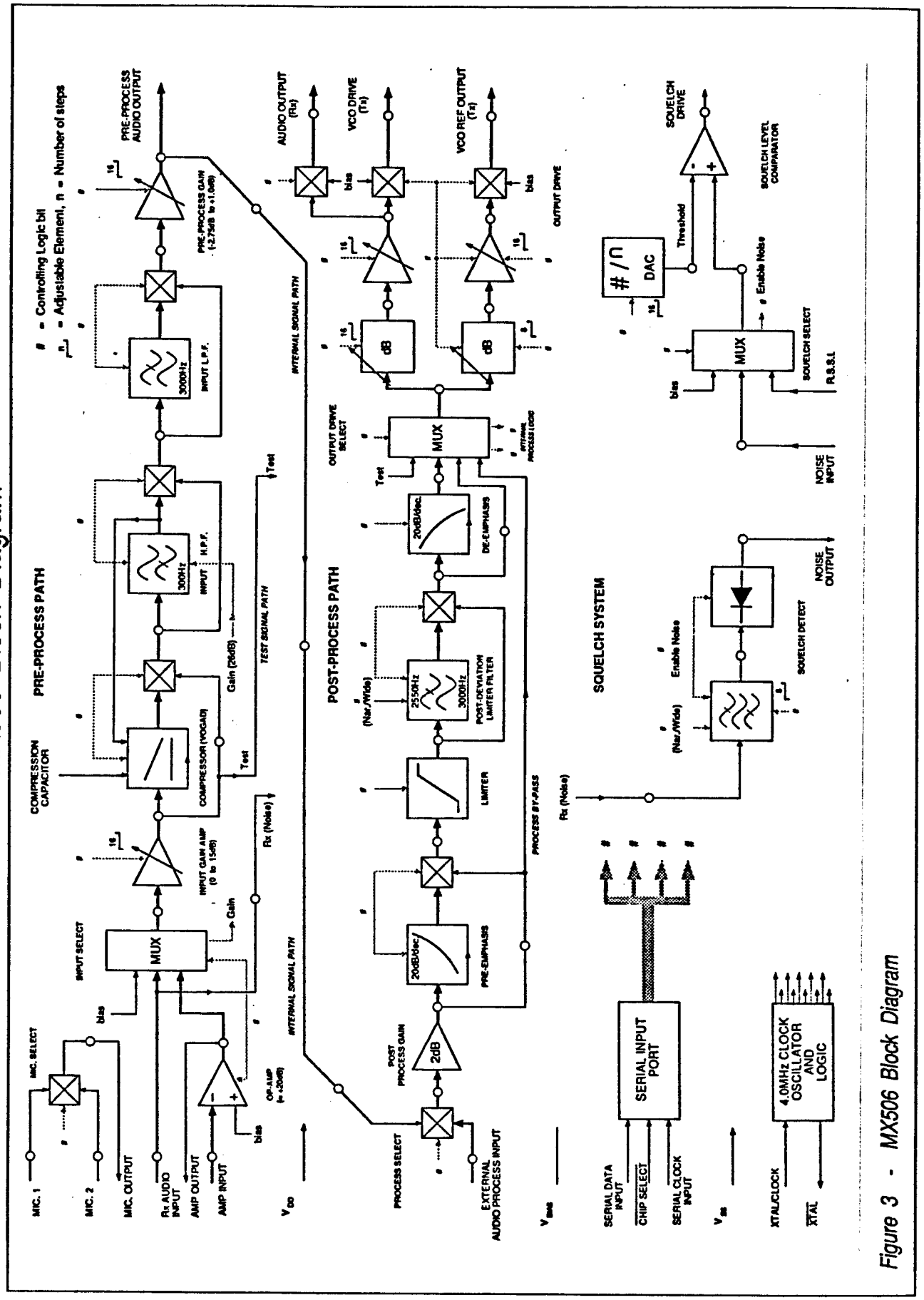
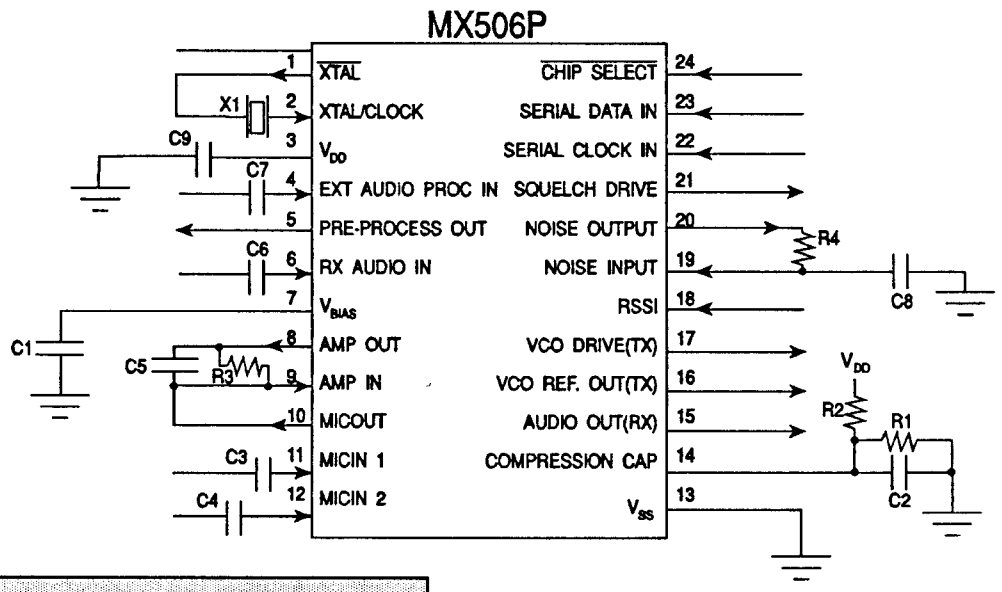


Figure 3 - MX506 Block Diagram

Pin Function Chart

Pin	Function
1	$\overline{\text{Xtal}}$: The output of the 4.0MHz on-chip clock oscillator.
2	Xtal: This is the input to the on-chip 4.0MHz clock oscillator inverter. All oscillator components are included on-chip. An external 4 MHz Xtal or externally derived clock should be connected here. See Figure 4.
3	V_{DD}: Positive supply rail. A single, stable +5 volt supply is required.
4	External Audio Process Input: This is the analog input to the Post-Process Path from external audio operations. It is selected by input serial data. When not selected, it is connected internally to the Pre-Process Audio Output via the Internal Signal Path. Inputs to this pin should be a.c. coupled via capacitor C7. See Figures 3 and 4.
5	Pre-Process Audio Output: The analog output to external audio operations. The signal at this output can be directed through the Internal Signal Path to the Post-Process Path. See Figure 3.
6	RX Audio Input: The input from the radio receiver demodulator. This input, which requires a.c. coupling via capacitor C6, is selected by serial data. Audio at this input will be available for use as a signal-squelch noise source. See Figures 3 and 4.
7	V_{BIAS}: The output of the on-chip analog bias circuitry, internally set to $V_{DD}/2$. This pin should be decoupled to V_{SS} with capacitor C1. See Figure 4.
8	Amp Output: With external components, this amplifier can be used as a microphone pre-amplifier and pre-emphasis circuit. For a "gain only" configuration a serial resistor may be employed at the Amp Input (-). See Figure 4.
9	Amp Input:
10	Microphone Output: This is the output of the microphone multiplexer, selected by serial input data. It should be connected to the Op-Amp Input (-). See Figures 3 and 4.
11	Mic. 1 Input: These separate microphone audio inputs are individually selected by the serial input data. See Figure 3.
12	Mic. 2 Input:
13	V_{SS}: Negative supply rail (GND).
14	Compression Capacitor: External components connected to this pin provide the required compression time constant. See Figure 4.
15	RX Audio Output: This is the received audio output from the Post-Process Path. This output is data selected. When in powersave it is held at V_{BIAS}.
16	VCO Ref. Drive Output: This output is used to drive the modulation reference oscillator. This output is data selected. When in powersave it is held at V_{BIAS}.
17	VCO Drive (TX) Output: This is the output drived to the Modulation VCO. It is data selected. When powersaved it is held at V_{BIAS}.
18	RSSI: This is the input to the Squelch Selection Circuitry from the radio's Received Signal Strength Indicator. It is a data-selected input.
19	Noise Input: The noise level can be applied to this pin. The noise level is the Noise Output integrated by external components, as shown in Figure 4. An externally produced noise level can also be used.
20	Noise Output: This is the output of the on-chip "squelch noise rectifier." It is a half-wave rectified d.c. level that can be applied to the Noise Input with external integrating components. This output could also be used by an external signal detector circuit. This output level is at V_{BIAS} for no input. See Figures 3 and 4.
21	Squelch Drive: A TTL-compatible output. The inputs to the comparator are the logically selected threshold level from the Digital-to-Analog converter and the selected noise input. This output will be a logic "1" when the selected noise is greater than the set threshold, and a logic "0" when less

Pin	Function
	than the set threshold.
22	**Serial Clock**: This is the externally produced serial data loading clock input (See Figure 5). This input has an internal 1MΩ pullup resistor.
23	**Serial Data**: This is the controlling 47-bit serial data input. When $\overline{\text{Chip Select}}$ is kept at logical "0," serial data is entered at this pin, bit 46 first and bit 0 last. Details concerning the allocation and function of serial data bits is on pages 6-9. Data load timing should be carried out as shown in Figure 4. This input has an internal 1 MΩ pullup resistor.
24	$\overline{\text{Chip Select}}$: This controls data loading. During serial data loading this input should be operated as shown in Figure 5. New data is latched on the rising edge of this waveform. This input has an internal 1 MΩ pullup resistor.



Component	Value	Tolerance
R1	390kΩ	±10%
R2	100kΩ	±10%
R3	100kΩ	±10%
R4	10kΩ	±10%
C1	1.0μF	±20%
C2	1.0μF	±20%
C3	3.3nF	±10%
C4	3.3nF	±10%
C5	39pF	±20%
C6	0.1μF	±20%
C7	0.1μF	±20%
C8	0.1μF	±20%
C9	1.0μF	±20%
X1	4.0MHz	

Input Components: C3 or C4, C5, R3

Mic. Input (1 or 2) coupling and Op-Amp gain/ pre-emphasis. Component values recommended are to provide gain of 6.0dB at 1kHz. C3/C4 or R3 may be varied to provide alternative gain settings.

For a "gain only" configuration a resistor can be used at the Amp Input (-).

Compression Time Constant: R1, R2, C2

Noise "Signal" Integration: R4, C8

Figure 4 - Recommended External Components

Layout Recommendations

Audio Microcircuit performance will be affected by external noise.

All external components should be kept as close to the device as possible.

Tracks to the device should be kept short, particularly to the Audio and VBIAS inputs.

A "ground plane" connected to VSS will help to eliminate external pick-up.

Make sure that all inputs are free from noise.

Xtal/clock and digital tracks should be kept well away from analog circuitry. Analog inputs and outputs should be screened wherever possible with high-level outputs isolated from very low-level inputs.

Control bits	Element	Notes
46 45	**Squelch Source Selector**	
0 0	- Internal Bias Path	Enable Detector Filter and Rectifier
0 1	- Integrated external Noise input	Enable Detector Filter and Rectifier
1 0	- RSSI Input	Enable Detector Filter and Rectifier
1 1		Do not use this setting. Itfs is for future use.
44 43 42 41	**Squelch Threshold Voltage**	The fine squelch adjustment from the Digital-to Analog converter. These threshold levels are used as a comparison with the selected input noise voltage (bits 46 and 45). Variation in V_{DD} will produce variation in threshold levels.
0 0 0 0	3.500 Vd.c. 70.0% V_{DD}	
0 0 0 1	3.366 67.3%	
0 0 1 0	3.233 64.6%	
0 0 1 1	3.100 62.0%	
0 1 0 0	2.966 59.3%	
0 1 0 1	2.833 56.6%	
0 1 1 0	2.700 54.0%	
0 1 1 1	2.566 51.3%	
1 0 0 0	2.433 48.6%	
1 0 0 1	2.300 46.0%	
1 0 1 0	2.166 43.3%	
1 0 1 1	2.033 40.6%	
1 1 0 0	1.900 38.0%	
1 1 0 1	1.766 35.3%	
1 1 1 0	1.633 32.6%	
1 1 1 1	1.500 30.0%	
40	**Squelch Filter (Narrow/Wide)**	For use in narrow or wide channel systems. The squelch function is set by bits 46 and 45.
0	- Narrow (*fc* = 18kHz ± 6.5kHz)	
1	- Wide (*fc* = 25kHz ± 8.5kHz)	
39 38 37	**Squelch Filter (Gain)**	The squelch function is set by bits 46 & 45. The center frequency gain of this element is 35dB; data-selected gain variations (-3.0dB to 4dB) are around this value.
0 0 0	- Gain Set -3.0dB	
0 0 1	-2.0dB	
0 1 0	-1.0dB	
0 1 1	0dB	
1 0 0	1.0dB	
1 0 1	2.0dB	
1 1 0	3.0dB	
1 1 1	4.0dB	
36	**Audio Output (RX)**	This function is designated for use in the RX mode, but can be used as a parallel output to the VCO Drive (TX).
0	- Output at bias, disabled	
1	- RX Audio Output Enabled	
35 34 33 32	**VCO Drive Amplifier**	The in-line control amplifier/attenuator for the VCO TX channel drive output.
0 0 0 0	- Gain Set -2.75dB	
0 0 0 1	-2.50dB	This channel is also selected as Audio Output (RX) under the control of bit 36. This amplifier can be used in a volume control application.
0 0 1 0	-2.25dB	
0 0 1 1	-2.00dB	
0 1 0 0	-1.75dB	
0 1 0 1	-1.50dB	
0 1 1 0	-1.25dB	
0 1 1 1	-1.00dB	
1 0 0 0	-0.75dB	
1 0 0 1	-0.50dB	
1 0 1 0	-0.25dB	
1 0 1 1	0dB	
1 1 0 0	0.25dB	
1 1 0 1	0.50dB	
1 1 1 0	0.75dB	
1 1 1 1	1.00dB	

Note: Bit 46 is transmitted first, bit 0 last.

Control bits	Element	Notes
31 30 29 28	**VCO Drive Attenuator**	The in-line control attenuator for the VCO TX channel drive output.
0 0 0 0	- Gain Set -48.0dB	
0 0 0 1	-44.8dB	
0 0 1 0	-41.6dB	This channel is also selected as the Audio Output (RX) under the control of bit 36. This attenuator can be used in a volume control application.
0 0 1 1	-38.4dB	
0 1 0 0	-35.3dB	
0 1 0 1	-32.0dB	
0 1 1 0	-28.8dB	
0 1 1 1	-25.6dB	
1 0 0 0	-22.4dB	
1 0 0 1	-19.2dB	
1 0 1 0	-16.0dB	
1 0 1 1	-12.8dB	
1 1 0 0	-9.6dB	
1 1 0 1	-6.4dB	
1 1 1 0	-3.2dB	
1 1 1 1	0dB	
27	**Output Control**	
0	- Powersave VCO Ref. Amplifier and Attenuator, disable Ref. and Drive Outputs. V_{BIAS} at both outputs.	
1	- Enable Ref. TX and VCO TX Outputs.	
26 25 24 23	**VCO Reference Drive Amplifier**	The in-line control amplifier/attenuator for the VCO reference channel drive output.
0 0 0 0	- Gain Set -2.75dB	
0 0 0 1	-2.50dB	
0 0 1 0	-2.25dB	
0 0 1 1	-2.00dB	
0 1 0 0	-1.75dB	
0 1 0 1	-1.50dB	
0 1 1 0	-1.25dB	
0 1 1 1	-1.00dB	
1 0 0 0	-0.75dB	
1 0 0 1	-0.50dB	
1 0 1 0	-0.25dB	
1 0 1 1	0dB	
1 1 0 0	0.25dB	
1 1 0 1	0.50dB	
1 1 1 0	0.75dB	
1 1 1 1	1.00dB	
22 21 20	**VCO Reference Drive Attenuator**	The in-line control attenuator for the VCO reference channel drive output.
0 0 0	- Gain Set -28dB	
0 0 1	-24dB	
0 1 0	-20dB	
0 1 1	-16dB	
1 0 0	-12dB	
1 0 1	-8.0dB	
1 1 0	-4.0dB	
1 1 1	0.0dB	
19 18	**Output Drive Selector**	To select the path to the output drive stages.
0 0	- Test signal path 1	
0 1	- Process path 2	Via de-emphasis element.
1 0	- Process path 3	Via de-emphasis bypass.
1 1	- Process Bypass path 4	
	De-emphasis	A selectable stage set around 1.0kHz with a characteristic of 6dB per octave.

Control bits	Element	Notes
17 0 1	Post-Deviation Limiter Filter - Powersave and bypass filter - Enable filter path	
16 0 1	Post-Deviation Limiter Filter - Narrow filter bandwidth, cut-off = 2550Hz. - Wide filter bandwidth, cut-off = 3000Hz.	This selectable lowpass filter is adjustable to Narrow (2550Hz) and Wide (3000Hz) bandwidths, allowing for different channel spacing requirements. See Figure 7.
	Deviation Limiter	A selectable, pre-set amplitude limiting stage for deviation control. Powersaved when Process Bypass is selected (bits 19 and 18).
15 0 1	Pre-emphasis - Powersave and bypass pre-emphasis. - Enable pre-emphasis path.	A selectable pre-emphasis stage set around 1.0kHz with a characteristic of 6dB per octave. It is powersaved when Process Bypass is selected (bits 19, 18).
	Post-process Gain	A fixed 2.0dB gain stage.
14 0 1	Process Select - Pre-process Internal Path - External Audio Process	To select either the Internal Signal path or the External Audio Process Input. This external input could be from a "Voice Scrambler" or the composite audio from a Sub-Audio or data signaling system.
13 12 11 10 0 0 0 0 0 0 0 1 0 0 1 0 0 0 1 1 0 1 0 0 0 1 0 1 0 1 1 0 0 1 1 1 1 0 0 0 1 0 0 1 1 0 1 0 1 0 1 1 1 1 0 0 1 1 0 1 1 1 1 0 1 1 1 1	Pre-process Gain - Gain Set -2.75dB -2.50dB -2.25dB -2.00dB -1.75dB -1.50dB -1.25dB -1.00dB -0.75dB -0.50dB -0.25dB 0dB 0.25dB 0.50dB 0.75dB 1.00dB	An in-line output drive stage that provides adjustable gain or attenuation to compensate for level tolerances in the external audio processes and peripherals. The output of this amplifier stage can be routed through an external path, or output to further voice processing (e.g. Frequency Inversion Voice Scrambling), or the introduction of Sub-Audible tones or In-Band data to the system.
9 0 1	Input Lowpass Filter - Bypass and powersave filter. - Enable Input Lowpass Filter.	A 3000Hz speech-path shaping low-pass filter. See Figure 5.
8 0 1	Input Highpass Filter - Bypass and powersave filter. - Enable Input Highpass Filter.	A 300Hz speech-path shaping highpass filter. See Figure 5. The filter gain is increased to +26dB when Mic. is selected (bits 2 and 1).
7 0 1	Compressor (VOGAD) - Bypass and powersave compressor. - Enable signal through compressor.	Pre-set, selectable voice amplitude compression circuitry that provides optimum drive levels to the transmission medium from differing signal level inputs. The Input Highpass Filter must be used with this element.

Control bits				Element	Notes
6	5	4	3	Input Gain Amplifier	This is a gain element intended to adjust the drive level to the compressor, catering to differing signal sources and microphone sensitivities.
0	0	0	0	- Gain Set 0.0dB	
0	0	0	1	1.0dB	
0	0	1	0	2.0dB	
0	0	1	1	3.0dB	
0	1	0	0	4.0dB	
0	1	0	1	5.0dB	
0	1	1	0	6.0dB	
0	1	1	1	7.0dB	
1	0	0	0	8.0dB	
1	0	0	1	9.0dB	
1	0	1	0	10.0dB	
1	0	1	1	11.0dB	
1	1	0	0	12.0dB	
1	1	0	1	13.0dB	
1	1	1	0	14.0dB	
1	1	1	1	15.0dB	
				Input Op-Amp	With external components, this amplifier can be used as a pre-amplifier and pre-emphasis circuit in the TX speech path. This gain element is available to adjust the drive level from differing signal sources and microphone sensitivities. Enabled by bits 2 and 1.
2	1			Input Select	Transmit or receive audio sources are selected, inserting the appropriate path gain for the chosen input. The input path can be set to bias while allowing receiver monitoring. Input Op-Amp is enabled for transmit selection.
0	0			- Internal bias path, no input selected.	
0	1			- Selected Microphone Input. Highpass Filter gain set to 26dB.	
1	0			- RX Audio Input. Powersave Op-Amp.	
1	1			- Internal bias path, no input selected. Powersave Input Op-Amp.	
0				Mic. Select	A Multiplexed "microphone" input allowing the use of differing type and level voice inputs.
0				- Microphone Input 1	
1				- Microphone Input 2	

Note: Bit 46 is transmitted first, bit 0 last.

RX Noise Path
Any audio present at the RX Audio Input will also be available through the squelch filter (when enabled) for use as a squelch detection level. Therefore the MX506 can be set to "idle" with the majority of elements powersaved until a "significant noise" level is used to produce a "squelch drive output."

Test Signal Path
This path, when selected, can be used as a direct path, via the Output Drive Selector (bits 19 and 18), to dynamically set and balance the VCO drive and reference output levels.

Powersave
The following elements can be powersaved via serial control:
Pre-process Path: Op-Amp, Compressor Circuit, Input Highpass Filter, Input Lowpass Filter.
Post-process Path: Pre-emphasis, Limiter, Post Deviation Limiter Filter, De-emphasis, VCO Ref. Attenuator and Amplifier.
Squelch System: Bandpass Filter, Squelch Rectifier.

The following elements are active at all times:
Input Gain Amp, Pre-process Gain Amp, Post-process Amp (+2.0dB), VCO Drive Attenuator and Amplifier, Digital-to-Analog Converter, Squelch Level Comparator

Control bits - Loading and Timing

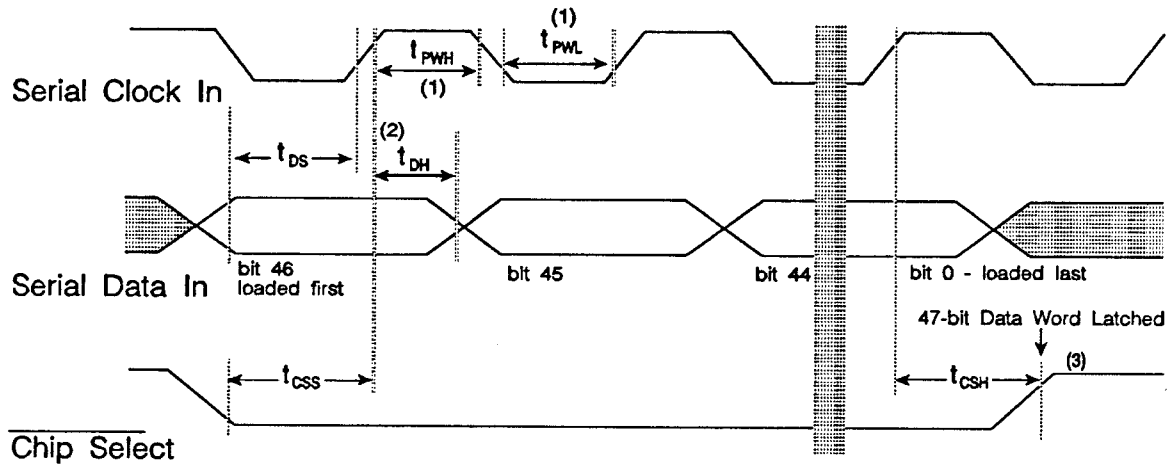


Figure 5 - Data Load Timing

Data Loading

Serial Data Bits, whose functions are described on Pages 6, 7, 8 and 9, are loaded to the MX506 using the timing format illustrated on this page. All 47 bits must be loaded. Data is loaded bit 46 first, bit 0 last.

Function		Min.	Typ.	Max.	Unit
Serial Clock (1)					
"High Pulse Width	t_{PWH}	600	-	-	ns
"Low" Pulse Width	t_{PWL}	600	-	-	ns
Serial Data (2)					
Data Set-up Time	t_{DS}	360	-	-	ns
Data Hold Time	t_{DH}	120	-	-	ns
Chip Select (3)					
Select Set-up Time	t_{CSS}	600	-	-	ns
Select Hold Time	t_{CSH}	600	-	-	ns

(1) The Serial Clock pulses do not have to be symmetrical, as shown above, but pulse lengths must conform to the "minimum" time specification.

(2) Individual data bits (logic"1" or "0") are loaded to the device on the rising edge of the Input Serial Data clock pulse. The data hold period (t_{DH}) is to ensure that the data level is steady when it is sampled.

(3) The full 47-bit data word is latched into the device on the rising edge of the Chip Select waveform. At this time the loaded data is acted upon and the circuit configuration will change.

System Frequency Characteristics

Figure 6 shows a typical response curve of the Pre-process path (in receive mode) set against the device specification. The characteristic shape is produced by the Input Highpass and Lowpass Filters without the pre-emphasis element.

Figure 7 shows a typical response curve of the Post-process path set against the device specification. The characteristic shape is produced by the Post-deviation Limiter Filter without the de-emphasis element.

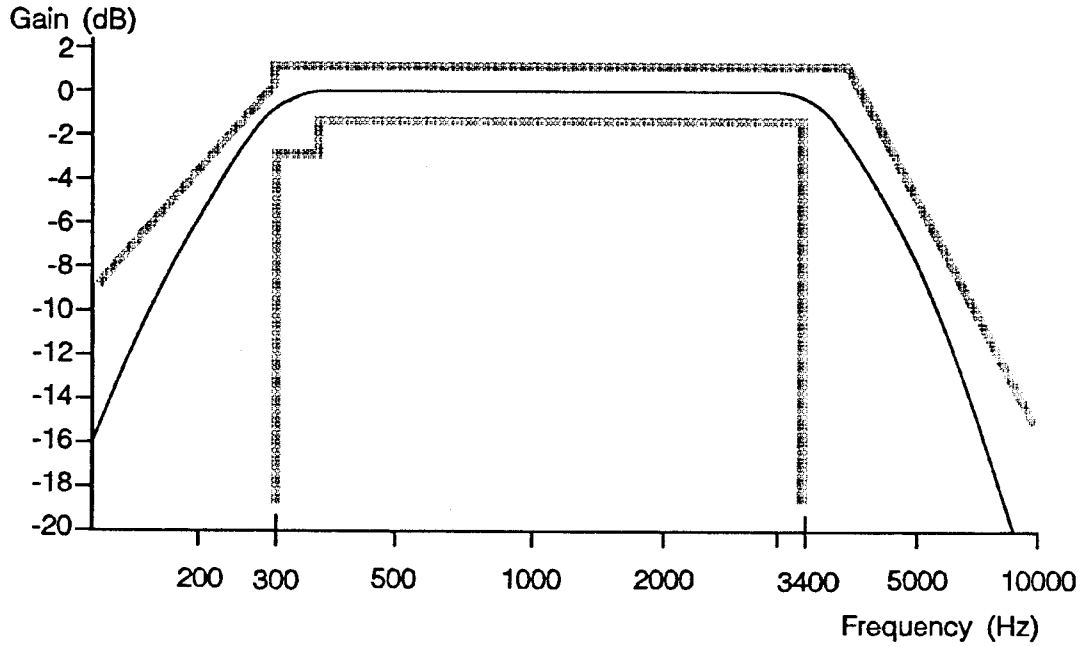


Figure 6 - Typical Pre-process Path Frequency Response

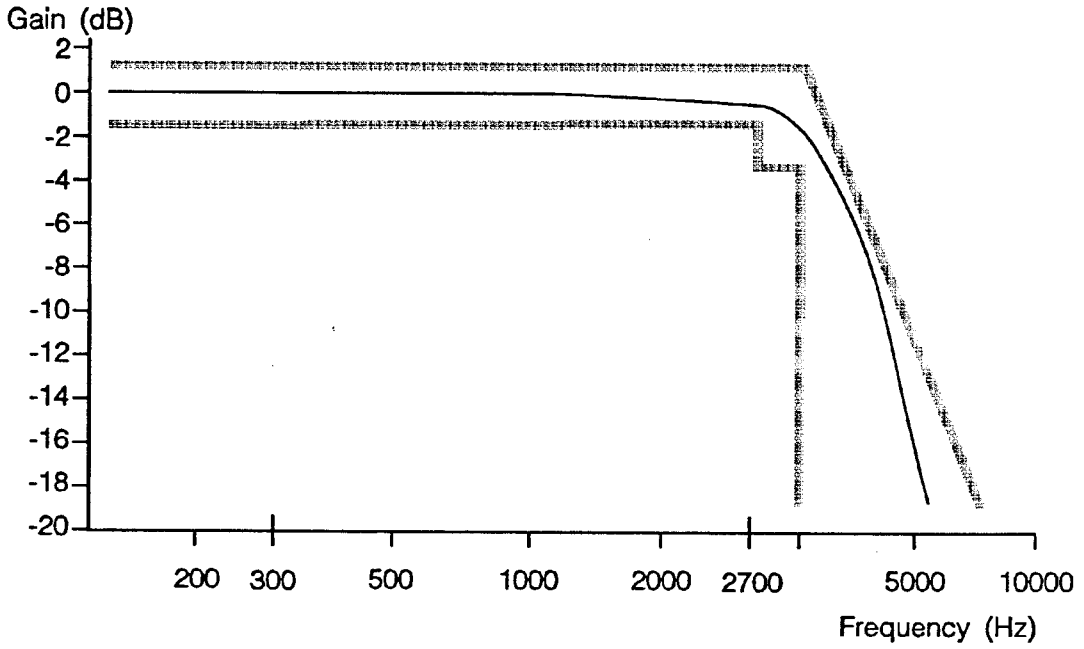


Figure 7 - Typical Post-process Path Frequency Response

Specifications

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)	-0.3 to (V_{DD} + 0.3V)
Sink/source current	±20mA
Total device dissipation @ 25°C	800mW Max.
Derating	10mW/°C
Operating temperature	-40°C to +85°C
Storage temperature	-55°C to 125°C

Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

V_{DD} = 5.0V

T_{AMB} = 25°C

Xtal/Clock f_0 = 4.0 MHz

Audio level 0dB ref. = 600 mVrms *(60% deviation, FM)*

Characteristics	See Note	Min.	Typ.	Max.	Unit
Supply Voltage (V_{DD})		4.5	5.0	5.5	V
Supply Current					
All Elements Enabled		-	8.0	-	mA
Maximum Powersave		-	3.0	-	mA
Dynamic Values					
Input Logic "1"	1	3.5	-	-	V
Input Logic "0"	1	-	-	1.5	V
Input Impedance					
Digital Input		0.1	1.0	-	MΩ
Mic 1 or 2		-	1.0	-	kΩ
RX Audio		50.0	-	-	kΩ
External Audio Process		1.0	-	-	MΩ
Amp Input		1.0	-	-	MΩ
Noise, RSSI		1.0	-	-	MΩ
Output Impedances					
Pre-Process Audio		-	-	3.0	kΩ
Audio Out (RX)		-	-	3.0	kΩ
VCO Drive and Ref. Out		-	-	3.0	kΩ
Squelch Drive Logic"1"		-	1.25	-	kΩ
Logic"0"		-	150	-	Ω
Noise Output Diode conducting		-	10.0	-	kΩ
Diode not conducting		-	400	-	kΩ
Signal Path Switch Isolation (Disabled)					
Switches		40.0	-	-	dB
Test Path		-	80.0	-	dB

Characteristics		See Note	Min.	Typ.	Max.	Unit
Signal Input Levels		11				
MIC 1 or 2			1.0	-	100	mVrms
RX Audio			-	123	200	mVrms
External Audio Process			-	-	795.0	mVrms
Noise, RSSI		2	-	-	5	V
Signal Output Levels		11				
Pre-Process Audio			-	600	1000	mVrms
VCO (Drive, Ref.)			-	-	1000	mVrms
Audio (RX)			-	-	1000	mVrms
Variable Element Step Tolerance						
Input Gain amp			-	-	±30.0	%
Pre-Process Gain			-	-	±40.0	%
VCO Ref. Attenuator			-	-	±12.5	%
VCO Drive Attenuator			-	-	±15.625	%
VCO Amplifiers (Drive and Ref.)			-	-	±40.0	%
Output Distortion						
Output S/N		3	-	45.0	48.0	dB
THD		3	-	-	-40.0	dB
Compressor						
Dynamic Range			-	30.0	-	dB
Attack time			-	0.55	-	ms
Decay time			-	8.5	-	ms
Deviation Limiter						
Input thresholds		4	-	2.828	-	V p-p
Frequency Response						
Pre-Process Path (See Figure 5)		6				
Passband Frequencies (-3dB)			300	-	3400	Hz
Passband Ripple	(300-400Hz)	5	-3.0	-	1.0	dB
	(400-3400 Hz)	5	-1.5	-	1.0	dB
Stopband Attenuation	(f = 5 kHz)		3.0	4.2	-	dB
High Frequency Roll-off	(f >5kHz, <20kHz)		12.0	-	-	dB/oct
Stopband Attenuation	(f = 250 Hz)		-	2.3	-	dB
Low Frequency Roll-off	(f <250Hz)		6.0	-	-	dB/oct
Post-Process Path (See Figure 6)		7				
Wideband: Lowpass Frequency (-3dB)			-	-	3000	Hz
Passband Ripple	(<2700 Hz)	8	-1.5	-	1.0	dB
	(2700 -3000 Hz)	8	-3.0	-	1.0	dB

Characteristics		See Note	Min.	Typ.	Max.	Unit
Stopband Attenuation	(f = 5 kHz)		12.2	17.0	-	dB
High Frequency Roll-off	(f >3 kHz, <20 kHz)		18	-	-	dB/oct
Narrowband: Lowpass Frequency (-3dB)			-	-	2550	Hz
Passband Ripple	(<2300 Hz)		-1.5	-	1.0	dB
	(2300-2550 Hz)		-3.0	-	1.0	dB
Stopband Attenuation	(f = 4.25 kHz)		12.2	17.0	-	dB
High Frequency Roll-off	(f >2300 Hz, <5100 Hz)		18	-	-	dB/oct.
Pre-emphasis: Passband Frequencies			300	-	3000	Hz
	Gain at 1kHz		-	0	-	dB
	Slope Characteristic	9	-	6.0	-	dB/oct.
De-emphasis: Passband Frequencies			300	-	3000	Hz
	Gain at 1kHz		-	0	-	dB
	Slope Characteristic	9	-	6.0	-	dB/oct.
Squelch Bandpass Filter						
Center Frequency Gain	(Wide and Narrow)		-	35.0	-	dB
Selectable Gain	(8 x 1.0 dB steps)	10	-3.0	-	4.0	dB
Narrow Band:						
Center Frequency	(fc)		-	18.75	-	kHz
Bandwidth	(fc±)		-	6.5	-	kHz
Wideband:						
Center Frequency	(fc)		-	25.5	-	kHz
Bandwidth	(fc±)		-	8.5	-	kHz

Notes:

1. A percentage of the applied V_{DD} (70% or 30%).
2. These inputs are compared internally with the Digital-to-Analog converter.
3. With a signal output level of 600 mVrms, measured in a 30.0 kHz bandwidth.
4. Levels at the input of the Limiter element, centered around V_{BIAS} (note 2).
5. This parameter remains within specification when pre-emphasis is employed.
6. With both input H.P.F. and L.P.F. in circuit, but without pre-emphasis.
7. With Limiter B.P.F., but without de-emphasis characteristics.
8. This parameter remains within specification when de-emphasis is employed.
9. Accuracy = ±0.5dB from nominal slope characteristic.
10. The gain variation around the center frequency (fc).
11. See Suggested Evaluation Tests for information on gain element settings.

Package Outline

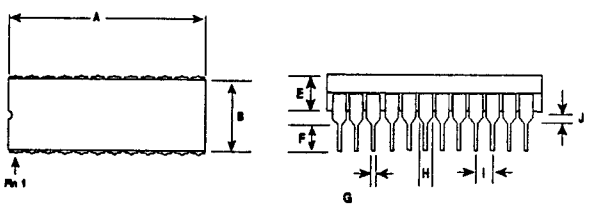
The MX506J Cerdip package is shown in Figure 5. The PDIP version is shown in Figure 6, and the LH in Figure 7.

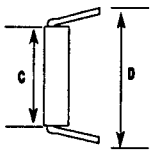
For identification purposes the LH package has an ident spot adjacent to pin 1 and a chamfered corner between pins 3 and 4. Pins number counter-clockwise when viewed from the top (indent side).

Handling Precautions

The MX506LH is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which may cause damage.

Fig. 6 - MX506P 24-pin Plastic DIP

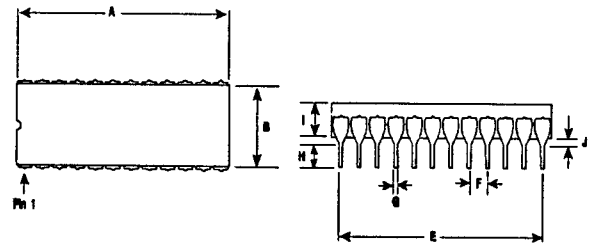


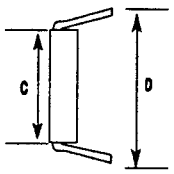


Package Tolerances

Dimension [in. (mm)]	Min.	Max.
A	1.23 (31.24)	1.26 (32.004)
B	0.53 (13.46)	0.55 (13.97)
C	0.59 (14.98)	0.610 (15.49)
D	0.63 (16.002)	0.67 (17.018)
E	0.170 (4.318)	.220 (5.588)
F	0.125 (3.175)	.160 (4.064)
G	0.015 (.381)	.020 (.508)
H	0.40 (1.016)	0.65 (1.651)
I	.090 (2.286)	.110 (2.794)
J	.015 (0.381)	.065 (1.651)

Figure 5 - MX506J 24-pin Cerdip

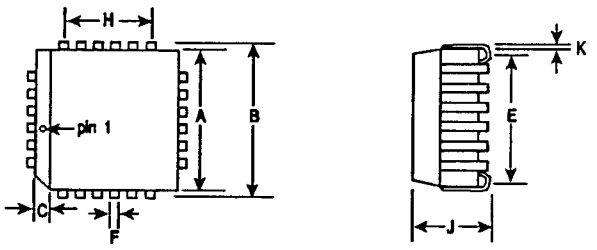


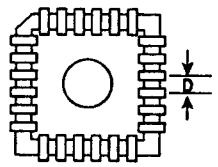


Package Tolerances

Dimension [in. (mm)]	Min.	Max.
A	1.24 (31.50)	1.26 (32.03)
B	.514 (13.06)	.583 (14.81)
C	.60 (15.14)	.615 (15.61)
D	.63 (16.002)	.67 (17.018)
E	1.10(27.84)	1.11(28.04)
F	.100 (2.54)	typical
G	.018 (0.46)	typical
H	.171 (4.35)	typical
I	.171 (4.35)	.196 (4.99)
J	.020 (0.50)	------

Figure 7 - MX506LH PLCC-24 Package





Package Tolerances

Dimension [in, (mm)]	Min.	Max.
A	.398 (10.10)	.410 (10.40)
B	.423 (10.75)	.435 (11.05)
C	.044 (1.15)x45°	typical
D	.050 (1.27)	typical
E	.366 (9.30)	typical
F	.018 (0.45)	.022 (0.55)
H	.244 (6.20)	.254 (6.45)
J	.134 (3.40)	.146 (3.70)
K	.007 (0.17)	.011 (0.27)

Ordering Information

MX506J 24-pin Cerdip

MX506P 24-pin PDIP

MX506LH 24-lead Plastic Leaded Chip Carrier

MX-COM, INC. ICs are available throughout the free world:

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CAUTION
MOS Device. May be damaged by static discharge. Observe handling precautions

Specifications subject to change.

Document No. 20480014.002

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MX·COM, INC.
COMMUNICATION MICROSYSTEMS

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CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CML Product Data

In the process of creating a more global image, the three standard product semiconductor companies of CML Microsystems Plc *(Consumer Microcircuits Limited (UK), MX-COM, Inc (USA) and CML Microcircuits (Singapore) Pte Ltd)* have undergone name changes and, whilst maintaining their separate new names *(CML Microcircuits (UK) Ltd, CML Microcircuits (USA) Inc and CML Microcircuits (Singapore) Pte Ltd*), now operate under the single title **CML Microcircuits**.
These companies are all 100% owned operating companies of the CML Microsystems Plc Group and these changes are purely changes of name and do not change any underlying legal entities and hence will have no effect on any agreements or contacts currently in force.

CML Microcircuits Product Prefix Codes

Until the latter part of 1996, the differentiator between products manufactured and sold from MXCOM, Inc. and Consumer Microcircuits Limited were denoted by the prefixes MX and FX respectively. These products use the same silicon etc. and today still carry the same prefixes. In the latter part of 1996, both companies adopted the common prefix: CMX.

This notification is relevant product information to which it is attached.

CML Microcircuits (USA) [formerly MX-COM, Inc.] Product Textual Marking

On CML Microcircuits (USA) products, the **'MX-COM'** textual logo is being replaced by a **'CML'** textual logo.

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