



# I<sup>2</sup>C Port Expander with 8 Open-Drain I/Os

MAX7321

## General Description

The MAX7321 2-wire serial-interfaced peripheral features eight open-drain I/O ports with selectable internal pullups and transition detection. Any port may be used as a logic input or an open-drain output. Ports are overvoltage protected to +6V independent of supply voltage.

All I/O ports configured as inputs are continuously monitored for state changes (transition detection). State changes are indicated by the open-drain, +6V tolerant  $\overline{\text{INT}}$  output. The interrupt is latched, allowing detection of transient changes. When the MAX7321 is subsequently accessed through the serial interface, any pending interrupt is cleared.

The open-drain outputs are rated to sink 20mA and are capable of driving LEDs.

The +6V tolerant  $\overline{\text{RST}}$  input clears the serial interface, terminating any I<sup>2</sup>C\* communication to or from the MAX7321.

The MAX7321 uses two address inputs with four-level logic to allow 16 I<sup>2</sup>C slave addresses. The slave address also determines the power-up logic level for the I/O ports, and enables or disables internal 40k $\Omega$  pullups in groups of four ports.

The MAX7321 supports hot insertion. All eight I/O ports, the serial interface SDA, SCL, AD0, AD2,  $\overline{\text{INT}}$ , and  $\overline{\text{RST}}$  remain high impedance in power-down ( $V_+ = 0$ ) with up to +6V asserted on them.

The MAX7321 is one device in a family of pin-compatible port expanders with a choice of input ports, open-drain I/O ports, and push-pull output ports (see Table 1).

The MAX7321 is available in 16-pin QSOP and 16-pin TQFN packages, and is specified over the automotive temperature range (-40°C to +125°C).

## Applications

Cell Phones  
SAN/NAS  
Servers

Notebooks  
Satellite Radio  
Automotive

**Pin Configurations, Typical Application Circuit, and Functional Diagram appear at end of data sheet.**

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## Features

- ◆ 400kHz, +6V Tolerant I<sup>2</sup>C Serial Interface
- ◆ +1.71V to +5.5V Operating Voltage
- ◆ 8 Open-Drain I/O Ports Rated to 20mA Sink Current
- ◆ I/O Ports Are Overvoltage Protected to +6V
- ◆ Any Port Can Be a Logic Input or an Open-Drain Output
- ◆ Selectable I/O Port Power-Up Default Logic Levels
- ◆ Transient Changes Are Latched, Allowing Detection Between Read Operations
- ◆  $\overline{\text{INT}}$  Output Alerts Change on Inputs
- ◆ AD0 and AD2 Inputs Select from 16 Slave Addresses
- ◆ Low 0.6 $\mu$ A (typ), 1.5 $\mu$ A (max) Standby Current
- ◆ -40°C to +125°C Operating Temperature

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK	PKG CODE
MAX7321AEE	-40°C to +125°C	16 QSOP	—	E16-4
MAX7321ATE	-40°C to +125°C	16 TQFN 3mm x 3mm x 0.8mm	ADC	T1633-4
MAX7321ASE*	-40°C to +125°C	16 SO	—	—
MAX7321AUP*	-40°C to +125°C	20 TSSOP	—	—
MAX7321AAP*	-40°C to +125°C	20 SSOP	—	—

\*Future product—contact factory for availability.

## Selector Guide

PART	INPUTS	INTERRUPT MASK	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS
MAX7319	8	Yes	—	—
MAX7320	—	—	—	8
MAX7321	Up to 8	—	Up to 8	—
MAX7322	4	Yes	—	4
MAX7323	Up to 4	—	Up to 4	4
MAX7328	Up to 8	—	Up to 8	—
MAX7329	Up to 8	—	Up to 8	—



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**For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at [www.maxim-ic.com](http://www.maxim-ic.com).**

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## ABSOLUTE MAXIMUM RATINGS

All Voltages Referenced to GND

Supply Voltage V <sub>+</sub> .....	-0.3V to +6V
SCL, SDA, AD0, AD2, $\overline{\text{RST}}$ , $\overline{\text{INT}}$ , P0–P7 .....	-0.3V to +6V
P0–P7 Sink Current .....	25mA
SDA Sink Current .....	10mA
INT Sink Current .....	10mA
Total V <sub>+</sub> Current .....	50mA
Total GND Current .....	100mA

Continuous Power Dissipation (T<sub>A</sub> = +70°C)

16-Pin QSOP (derate 8.3mW/°C above +70°C) .....	667mW
16-Pin TQFN (derate 15.6mW/°C above +70°C) .....	1250mW
Operating Temperature Range .....	-40°C to +125°C
Junction Temperature .....	+150°C
Storage Temperature Range .....	-65°C to +150°C
Lead Temperature (soldering, 10s) .....	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>+</sub> = +1.71V to +5.5V, T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at V<sub>+</sub> = +3.3V, T<sub>A</sub> = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V <sub>+</sub>		1.71		5.5	V
Power-On Reset Voltage	V <sub>POR</sub>				1.6	V
Standby Current (Interface Idle)	I <sub>STB</sub>	SCL and SDA and other digital inputs at V <sub>+</sub>		0.6	1.5	μA
Supply Current (Interface Running)	I <sub>+</sub>	f <sub>SCL</sub> = 400kHz; other digital inputs at V <sub>+</sub>		23	51	μA
Input High Voltage SDA, SCL, AD0, AD2, $\overline{\text{RST}}$ , P0–P7	V <sub>IH</sub>	V <sub>+</sub> ≤ 1.8V	0.8 × V <sub>+</sub>			V
		V <sub>+</sub> ≥ 1.8	0.7 × V <sub>+</sub>			
Input Low Voltage SDA, SCL, AD0, AD2, $\overline{\text{RST}}$ , P0–P7	V <sub>IL</sub>	V <sub>+</sub> ≤ 1.8V			0.2 × V <sub>+</sub>	V
		1.71V ≤ V <sub>+</sub> ≤ 1.8V			0.3 × V <sub>+</sub>	
Input Leakage Current SDA, SCL, AD0, AD2, $\overline{\text{RST}}$ , P0–P7	I <sub>IH</sub> , I <sub>IL</sub>	SDA, SCL, AD0, AD2, $\overline{\text{RST}}$ , P0–P7 at V <sub>+</sub> or GND	-0.2		+0.2	μA
Input Capacitance SDA, SCL, AD0, AD2, $\overline{\text{RST}}$ , P0–P7				10		pF
Output Low Voltage P0–P7	V <sub>OL</sub>	V <sub>+</sub> = +1.71V, I <sub>SINK</sub> = 5mA		90	180	mV
		V <sub>+</sub> = +2.5V, I <sub>SINK</sub> = 10mA		110	210	
		V <sub>+</sub> = +3.3V, I <sub>SINK</sub> = 15mA		130	230	
		V <sub>+</sub> = +5V, I <sub>SINK</sub> = 20mA		140	250	
Output Low Voltage SDA	V <sub>OLSDA</sub>	I <sub>SINK</sub> = 6mA			250	mV
Output Low Voltage INT	V <sub>OLINT</sub>	I <sub>SINK</sub> = 5mA		130	250	mV
Port Input Pullup Resistor	R <sub>PU</sub>		25	40	55	kΩ

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## PORT AND INTERRUPT $\overline{\text{INT}}$ TIMING CHARACTERISTICS

(V<sub>+</sub> = +1.71V to +5.5V, T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at V<sub>+</sub> = +3.3V, T<sub>A</sub> = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Port Output Data Valid	t <sub>PPV</sub>	C <sub>L</sub> ≤ 100pF			4	μs
Port Input Setup Time	t <sub>PSU</sub>	C <sub>L</sub> ≤ 100pF	0			μs
Port Input Hold Time	t <sub>PH</sub>	C <sub>L</sub> ≤ 100pF	4			μs
$\overline{\text{INT}}$ Input Data Valid Time	t <sub>IV</sub>	C <sub>L</sub> ≤ 100pF			4	μs
$\overline{\text{INT}}$ Reset Delay Time from STOP	t <sub>IP</sub>	C <sub>L</sub> ≤ 100pF			4	μs
$\overline{\text{INT}}$ Reset Delay Time from Acknowledge	t <sub>IR</sub>	C <sub>L</sub> ≤ 100pF			4	μs

## TIMING CHARACTERISTICS

(V<sub>+</sub> = +1.71V to +5.5V, T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at V<sub>+</sub> = +3.3V, T<sub>A</sub> = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	f <sub>SCL</sub>				400	kHz
Bus Free Time Between a STOP and a START Condition	t <sub>BUF</sub>		1.3			μs
Hold Time (Repeated) START Condition	t <sub>HD, STA</sub>		0.6			μs
Repeated START Condition Setup Time	t <sub>SU, STA</sub>		0.6			μs
STOP Condition Setup Time	t <sub>SU, STO</sub>		0.6			μs
Data Hold Time	t <sub>HD, DAT</sub>	(Note 2)			0.9	μs
Data Setup Time	t <sub>SU, DAT</sub>		100			ns
SCL Clock Low Period	t <sub>LOW</sub>		1.3			μs
SCL Clock High Period	t <sub>HIGH</sub>		0.7			μs
Rise Time of Both SDA and SCL Signals, Receiving	t <sub>R</sub>	(Notes 3, 4)		20 + 0.1C <sub>b</sub>	300	ns
Fall Time of Both SDA and SCL Signals, Receiving	t <sub>F</sub>	(Notes 3, 4)		20 + 0.1C <sub>b</sub>	300	ns
Fall Time of SDA, Transmitting	t <sub>F, TX</sub>	(Notes 3, 4)		20 + 0.1C <sub>b</sub>	250	ns
Pulse Width of Spike Suppressed	t <sub>SP</sub>	(Note 5)		50		ns
Capacitive Load for Each Bus Line	C <sub>b</sub>	(Note 3)			400	pF
$\overline{\text{RST}}$ Pulse Width	t <sub>W</sub>		500			ns
$\overline{\text{RST}}$ Rising to START Condition Setup Time	t <sub>RST</sub>		1			μs

**Note 1:** All parameters tested at T<sub>A</sub> = +25°C. Specifications over temperature are guaranteed by design.

**Note 2:** A master device must provide a hold time of at least 300ns for the SDA signal (referred to V<sub>IL</sub> of the SCL signal) in order to bridge the undefined region of SCL's falling edge.

**Note 3:** Guaranteed by design.

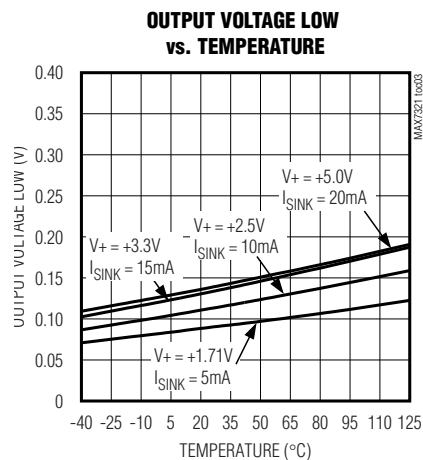
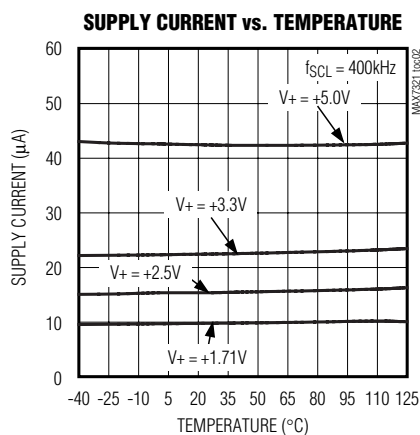
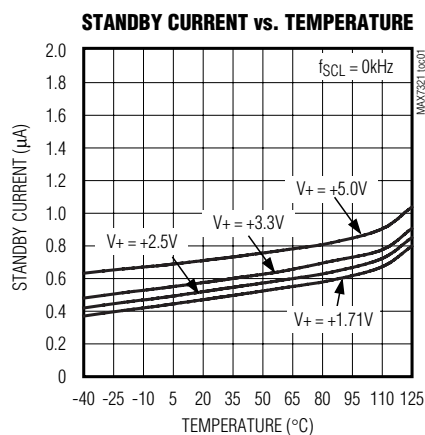
**Note 4:** C<sub>b</sub> = total capacitance of one bus line in pF. t<sub>R</sub> and t<sub>F</sub> measured between 0.3 × V<sub>+</sub> and 0.7 × V<sub>+</sub>. I<sub>SINK</sub> ≤ 6mA.

**Note 5:** Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

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## Typical Operating Characteristics

(T<sub>A</sub> = +25°C, unless otherwise noted.)



## Pin Description

PIN			NAME	FUNCTION
QSOP	TQFN	TSSOP/SSOP		
1, 3	15, 1	6, 9	AD0, AD2	Address Inputs. Select device slave address with AD0 and AD2. Connect AD0 and AD2 to either GND, V <sub>+</sub> , SCL, or SDA to give four logic combinations (see Table 3).
2	16	7	$\overline{\text{RST}}$	Reset Input, Active Low. Drive $\overline{\text{RST}}$ low to clear the 2-wire interface.
4–7, 9–12	2–5, 7–10	10, 11, 12, 14, 16, 17, 19, 20	P0–P7	Input/Output Ports. P0 to P7 are open-drain I/Os rated at +6V, 20mA.
8	6	15	GND	Ground
13	11	1	$\overline{\text{INT}}$	Interrupt Output. $\overline{\text{INT}}$ is an open-drain output rated at +6V.
14	12	2	SCL	I <sup>2</sup> C-Compatible Serial Clock Input
15	13	4	SDA	I <sup>2</sup> C-Compatible Serial Data I/O
16	14	5	V <sub>+</sub>	Positive Supply Voltage. Bypass V <sub>+</sub> to GND with a ceramic capacitor of at
—	—	3, 18	N.C.	No Connection. Internally not connected.
—	EP	—	EP	Exposed Pad. Connect exposed pad to GND.

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## Detailed Description

### MAX7319–MAX7329 Family Comparison

The MAX7319–MAX7323 family consists of five pin-compatible, eight-port expanders. Each version is optimized for different applications. The MAX7328 and MAX7329 are second sources to the PCF8574 and PCF8574A.

The MAX7324–MAX7327 family consists of four pin-compatible, 16-port expanders that integrate the functions of the MAX7320 and one of either the MAX7319, MAX7321, MAX7322, or MAX7323.

## Functional Overview

The MAX7321 is a general-purpose port expander operating from a +1.71V to +5.5V supply that provides eight open-drain I/O ports. Each open-drain output is rated to sink 20mA, and the entire device is rated to sink 100mA into all ports combined. The outputs drive loads connected to supplies up to +6V, independent of the MAX7321's supply voltage.

The MAX7321 is set to one of 16 I<sup>2</sup>C slave addresses (0x60 to 0x6F) using the address select inputs AD0 and AD2, and is accessed over an I<sup>2</sup>C serial interface up to 400kHz. The RST input clears the serial interface in

**Table 1. MAX7321–MAX7329 Family Comparison**

PART	I <sup>2</sup> C SLAVE ADDRESS	INPUTS	INPUT INTERRUPT MASK	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS	APPLICATION
<b>8-PORT EXPANDERS</b>						
MAX7319	110xxxx	8	Yes	—	—	Input-only versions: 8 input ports with programmable latching transition detection interrupt and selectable pullups.  Offers maximum versatility for automatic input monitoring. An interrupt mask selects which inputs cause an interrupt on transitions, and transition flags identify which inputs have changed (even momentarily) since the ports were last read.
MAX7320	101xxxx	—	—	—	8	Output-only versions: 8 push-pull outputs with selectable power-up default levels.  Push-pull outputs offer faster rise time than open-drain outputs, and require no pullup resistors.
MAX7321	110xxxx	Up to 8	—	Up to 8	—	I/O versions: 8 open-drain I/O ports with latching transition detection interrupt and selectable pullups.  Open-drain outputs can level shift the logic-high state to a higher or lower voltage than V <sub>+</sub> using external pullup resistors. Any port can be used as an input by setting the open-drain output to logic high. Transition flags identify which inputs have changed (even momentarily) since the ports were last read.
MAX7322	110xxxx	4	Yes	—	4	4 input-only, 4 output-only versions: 4 input ports with programmable latching transition detection interrupt and selectable pullups; 4 push-pull outputs with selectable power-up default levels.

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Table 1. MAX7321–MAX7329 Family Comparison (continued)

PART	I <sup>2</sup> C SLAVE ADDRESS	INPUTS	INPUT INTERRUPT MASK	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS	APPLICATION
MAX7323	110xxxx	Up to 4	—	Up to 4	4	4 I/O, 4 output-only versions: 4 open-drain I/O ports with latching transition detection interrupt and selectable pullups. 4 push-pull outputs with selectable power-up default levels.
MAX7328 MAX7329	0100xxx 0111xxx	Up to 8	—	Up to 8	—	PCF8574-, PCF8574A-compatible versions: 8 open-drain I/O ports with nonlatching transition detection interrupt and pullups on all ports.  All ports power up as inputs (or logic-high outputs).  Any port can be used as an input by setting the open-drain output to logic high.
<b>16 PORTS IN 24-PIN PACKAGES</b>						
MAX7324	101xxxx and 110xxxx	8	Yes	—	8	Software equivalent to a MAX7320 plus a MAX7321.
MAX7325		Up to 8	—	Up to 8	8	Software equivalent to a MAX7320 plus a MAX7319.
MAX7326		4	Yes	—	12	Software equivalent to a MAX7320 plus a MAX7322.
MAX7327		Up to 4	—	Up to 4	12	Software equivalent to a MAX7320 plus a MAX7323.

case of a hung bus, terminating any serial transaction to or from the MAX7321.

Any port can be configured as a logic input by setting the port output logic high (logic high for an open-drain output is high impedance). When the MAX7321 is read through the serial interface, the actual logic levels at the ports are read back.

The open-drain ports offer latching transition detection when used as inputs. All input ports are continuously monitored for changes. An input change sets 1 of 8 flag bits that identify changed input(s). All flags are cleared upon a subsequent read or write transaction to the MAX7321.

A latching interrupt output,  $\overline{\text{INT}}$ , is programmed to flag logic changes on ports used as inputs. Data changes on any input port forces  $\overline{\text{INT}}$  to a logic low. Changing the I/O port level through the serial interface does not cause an interrupt. The interrupt output  $\overline{\text{INT}}$  is cleared when the MAX7321 is next accessed through the serial interface.

Internal pullup resistors to V+ are selected by the address select inputs, AD0 and AD2. Pullups are enabled on the input ports in groups of four (see Table 3).

Use the slave address selection to ensure that I/O ports used as inputs are high on power-up. To simplify I/O

port and slave address configuration, I/O ports with internal pullups enabled also default with their open-drain outputs logic high (high impedance). I/O ports with internal pullups disabled default with open-drain outputs logic low. Output port power-up logic levels are selected by the address select inputs AD0 and AD2. Ports default to logic high or logic low on power-up in groups of four (see Table 3).

## Initial Power-Up

On power-up, the transition detection logic is reset, and  $\overline{\text{INT}}$  is released to a high-impedance state. The transition flags are cleared to indicate no data changes. The power-up default states of the eight I/O ports are set according to the I<sup>2</sup>C slave address selection inputs, AD0 and AD2 (Table 3). **For I/O ports used as inputs, ensure that the default states are logic high so that the I/O ports power up in the high-impedance state. All I/O ports configured with pullups enabled also have a logic-high power-up state.**

## $\overline{\text{RST}}$ Input

The  $\overline{\text{RST}}$  input voids any I<sup>2</sup>C transaction involving the MAX7321, forcing the MAX7321 into the I<sup>2</sup>C STOP condition. A reset does not affect the interrupt output ( $\overline{\text{INT}}$ ) or change the contents of the interrupt mask register.  $\overline{\text{RST}}$  is overvoltage tolerant to +6V.

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**Table 2. Read and Write Access to Eight-Port Expander Family**

PART	I <sup>2</sup> C SLAVE ADDRESS	INPUTS	INTERRUPT MASK	OPEN-DRAIN OUTPUTS	PUSH-PULL OUTPUTS	I <sup>2</sup> C DATA WRITE	I <sup>2</sup> C DATA READ
MAX7319	110xxxx	8	Yes	—	—	<I7–I0 interrupt mask>	<I7–I0 port inputs> <I7–I0 transition flags>
MAX7320	101xxxx	—	—	—	8	<O7–O0 port outputs>	<O7–O0 port inputs>
MAX7321	110xxxx	Up to 8	—	Up to 8	—	<P7–P0 port outputs>	<P7–P0 port inputs> <P7–P0 transition flags>
MAX7322	110xxxx	4	Yes	—	4	<O7, O6 outputs, I5–I2 interrupt mask, O1, O0 outputs>	<O7, O6, I5–I2, O1, O0 port inputs> <O, 0, I5–I2 transition flags, 0, 0>
MAX7323	110xxxx	Up to 4	—	Up to 4	4	<port outputs>	<O7, O6, P5–P2, O1, O0 port inputs> <O, 0, P5–P2 transition flags, 0, 0>
MAX7328	0100xxx	Up to 8	—	Up to 8	—	<P7–P0 port outputs>	<P7–P0 port inputs>
MAX7329	0111xxx	Up to 8	—	Up to 8	—	<P7–P0 port outputs>	<P7–P0 port inputs>

## Standby Mode

When the serial interface is idle, the MAX7321 automatically enters standby mode, drawing minimal supply current.

## Slave Address, Power-Up Default Logic Levels, and Input Pullup Selection

Address inputs AD0 and AD2 determine the MAX7321 slave address, set the power-up I/O state for the ports, and select which inputs have pullup resistors. Internal pullups and power-up default states are set in groups of four (Table 3). The MAX7319, MAX7321, MAX7322, and MAX7323 use a different range of slave addresses (110xxxx) than the MAX7320 (101xxxx) (Table 2).

The MAX7321 slave address is determined on each I<sup>2</sup>C transmission, regardless of whether the transmission is actually addressing the MAX7321. The MAX7321 distinguishes whether address inputs AD2 and AD0 are connected to SDA or SCL instead of fixed logic levels V+ or GND during this transmission. This means that the MAX7321 slave address can be configured dynamically in the application without cycling the device supply.

On initial power-up, the MAX7321 cannot decode address inputs AD0 and AD2 fully until the first I<sup>2</sup>C

transmission, and AD0 and AD2 initially appear to be connected to V+ or GND. This is important because the address selection is used to determine the power-up logic level (output low or input/output high), and whether pullups are applied. However, at power-up, the I<sup>2</sup>C SDA and SCL bus interface lines are high impedance at the pins of every device (master or slave) connected to the bus, including the MAX7321. This is guaranteed as part of the I<sup>2</sup>C specification. Therefore, address inputs AD2 and AD0 that are connected to SDA or SCL normally appear at power-up to be connected to V+. The power-up logic uses AD0 to select the power-up state and whether pullups are enabled for ports P3–P0, and AD2 for ports P7–P4. The rule is that a logic high, SDA, or SCL connection selects the pullups (and sets the default port condition to input or logic-high output), while a logic low deselects the pullups (and sets the default port condition to logic-low output) (Table 3). The port configuration is correct on power-up for a standard I<sup>2</sup>C configuration, where SDA or SCL are pulled up to V+ by the external I<sup>2</sup>C pullup resistors.

There are circumstances where the assumption that SDA = SCL = V+ on power-up is not true—for example, in true hot-swap applications in which there is legiti-

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Table 3. MAX7321 Address Map

PIN CONNECTION		DEVICE ADDRESS							OUTPUTS POWER-UP DEFAULT								40kΩ INPUT PULLUPS ENABLED							
AD2	AD0	A6	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	P7	P6	P5	P4	P3	P2	P1	P0
SCL	GND	1	1	0	0	0	0	0	1	1	1	1	0	0	0	0	Y	Y	Y	Y	—	—	—	—
SCL	V+	1	1	0	0	0	0	1	1	1	1	1	1	1	1	1	Y	Y	Y	Y	Y	Y	Y	Y
SCL	SCL	1	1	0	0	0	1	0	1	1	1	1	1	1	1	1	Y	Y	Y	Y	Y	Y	Y	Y
SCL	SDA	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1	Y	Y	Y	Y	Y	Y	Y	Y
SDA	GND	1	1	0	0	1	0	0	1	1	1	1	0	0	0	0	Y	Y	Y	Y	—	—	—	—
SDA	V+	1	1	0	0	1	0	1	1	1	1	1	1	1	1	1	Y	Y	Y	Y	Y	Y	Y	Y
SDA	SCL	1	1	0	0	1	1	0	1	1	1	1	1	1	1	1	Y	Y	Y	Y	Y	Y	Y	Y
SDA	SDA	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	Y	Y	Y	Y	Y	Y	Y	Y
<b>GND</b>	<b>GND</b>	1	1	<b>0</b>	1	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	—	—	—	—	—	—	—	—
<b>GND</b>	<b>V+</b>	1	1	<b>0</b>	1	<b>0</b>	<b>0</b>	1	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	1	1	1	1	—	—	—	—	<b>Y</b>	<b>Y</b>	<b>Y</b>	<b>Y</b>
GND	SCL	1	1	0	1	0	1	0	0	0	0	0	1	1	1	1	—	—	—	—	Y	Y	Y	Y
GND	SDA	1	1	0	1	0	1	1	0	0	0	0	1	1	1	1	—	—	—	—	Y	Y	Y	Y
<b>V+</b>	<b>GND</b>	1	1	<b>0</b>	1	1	<b>0</b>	<b>0</b>	1	1	1	1	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>Y</b>	<b>Y</b>	<b>Y</b>	<b>Y</b>	—	—	—	—
<b>V+</b>	<b>V+</b>	1	1	<b>0</b>	1	1	<b>0</b>	1	1	1	1	1	1	1	1	1	<b>Y</b>	<b>Y</b>	<b>Y</b>	<b>Y</b>	<b>Y</b>	<b>Y</b>	<b>Y</b>	<b>Y</b>
V+	SCL	1	1	0	1	1	1	0	1	1	1	1	1	1	1	1	Y	Y	Y	Y	Y	Y	Y	Y
V+	SDA	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	Y	Y	Y	Y	Y	Y	Y	Y

mate bus activity during power-up. Also, if SDA and SCL are terminated with pullup resistors to a different supply voltage than the MAX7321's supply voltage, and if that pullup supply rises later than the MAX7321's supply, then SDA or SCL may appear at power-up to be connected to GND. In such applications, use the four address combinations that are selected by connecting address inputs AD2 and AD0 to V+ or GND (shown in **bold** in Table 3). These selections are guaranteed to be correct at power-up, independent of SDA and SCL behavior. If one of the other 12 address combinations is used, be aware that an unexpected combination of pullups might be asserted until the first I<sup>2</sup>C transmission (to any device, not necessarily the MAX7321) is put on the bus, and an unexpected combination of ports may initialize as logic-low outputs instead of inputs or logic-high outputs.

## Port Inputs

I/O port inputs switch at the CMOS-logic levels as determined by the expander's supply voltage, and are overvoltage tolerant to +6V, independent of the expander's supply voltage.

## I/O Port Input Transition Detection

All I/O ports configured as inputs are monitored for changes since the expander was last accessed through the serial interface. The state of the input ports is stored in an internal "snapshot" register for transition monitoring. The snapshot is continuously compared with the actual input conditions, and if a change is detected for any port,  $\overline{\text{INT}}$  signals a state change by going logic low. An internal transition flag is set for that port. The input is sampled (internally latched into the snapshot register) and the old transition flags cleared during the I<sup>2</sup>C acknowledge of every MAX7321 read and write access. The previous port transition flags are read through the serial interface as the second byte of a 2-byte read sequence.

# I<sup>2</sup>C Port Expander with 8 Open-Drain I/Os

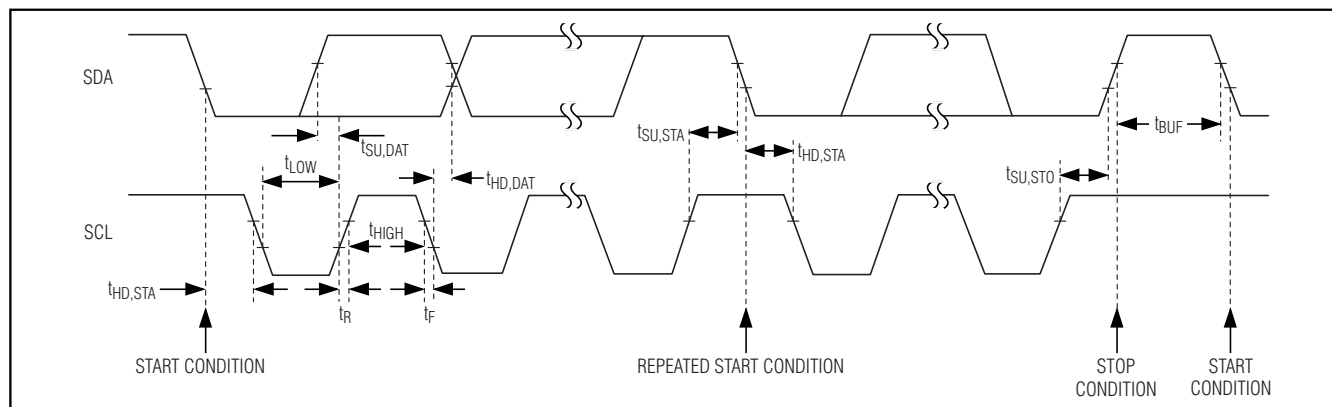


Figure 1. 2-Wire Serial Interface Timing Details

## Serial Interface

### Serial Addressing

The MAX7321 operates as a slave that sends and receives data through an I<sup>2</sup>C interface. The interface uses a serial data line (SDA) and a serial clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). The master initiates all data transfers to and from the MAX7321 and generates the SCL clock that synchronizes the data transfer (Figure 1).

SDA operates as both an input and an open-drain output. A pullup resistor, typically 4.7k $\Omega$ , is required on SDA. SCL operates only as an input. A pullup resistor, typically 4.7k $\Omega$ , is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START condition sent by a master, followed by the MAX7321's 7-bit slave address plus R/W bit, and then optionally 1 or more data bytes, and finally a STOP condition (Figure 2).

### START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, the master issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 2).

### Bit Transfer

One data bit is transferred during each clock pulse. The data on SDA must remain stable while SCL is high (Figure 3).

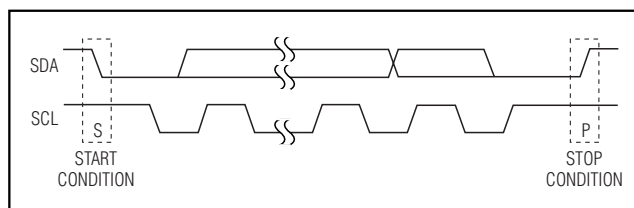


Figure 2. START and STOP Conditions

### Acknowledge

The acknowledge bit is a clocked 9th bit the recipient uses to handshake receipt of each byte of data (Figure 4). Each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, such that the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX7321, the MAX7321 generates the acknowledge bit because the device is the recipient. When the MAX7321 is transmitting to the master, the master generates the acknowledge bit because the master is the recipient.

### Slave Address

The MAX7321 has a 7-bit-long slave address (Figure 5). The eighth bit following the 7-bit slave address is the R/W bit. It is low for a write command, and high for a read command.

The first (A6), second (A5), and third (A4) bits of the MAX7321 slave address are always 1, 1, and 0. Connect AD2 and AD0 to GND, V+, SDA, or SCL to select slave address bits A3, A2, A1, and A0. The MAX7321 has 16 possible slave addresses (Table 3), allowing up to 16 MAX7321 devices on an I<sup>2</sup>C bus.

# I<sup>2</sup>C Port Expander with 8 Open-Drain I/Os

## Accessing the MAX7321

I<sup>2</sup>C interface access to the MAX7321 is summarized as follows (Table 2).

A **single-byte read** from the MAX7321 returns the status of the eight I/O ports, and clears both the internal transition flags and the  $\overline{\text{INT}}$  output when the master acknowledges the slave address byte.

A **2-byte read** returns first the status of the eight I/O ports (as for a single-byte read), followed by the transition flags. Again, the internal transition flags and the  $\overline{\text{INT}}$  output are cleared automatically when the master acknowledges the slave address byte (but the previous transition flag data is sent as the second byte).

A **multibyte** (more than 2 bytes before the I<sup>2</sup>C STOP bit) **read** repeatedly returns the port data, followed by the transition flags. As the port data is resampled for each transmission, and the transition flags are reset each time, a multibyte read continuously returns the current data and identifies any changing input ports.

If a port input data change occurs during the read sequence, then  $\overline{\text{INT}}$  is reasserted during the I<sup>2</sup>C STOP bit. The MAX7321 does not generate another interrupt during a single-byte or multibyte read.

Input port data is sampled during the preceding I<sup>2</sup>C acknowledge bit (the acknowledge bit for the I<sup>2</sup>C slave address in the case of a single-byte or 2-byte read).

A **single-byte write** to the MAX7321 sets the logic state of all eight I/O ports.

A **multibyte write** to the MAX7321 repeatedly sets the logic state of all eight I/O ports.

## Reading the MAX7321

A read from the MAX7321 starts with the master transmitting the MAX7321's slave address with the R/W bit set high. The MAX7321 acknowledges the slave address, and samples the input ports (takes a snapshot) during the acknowledge bit.  $\overline{\text{INT}}$  goes high (high impedance if an external pullup resistor is not fitted) during the slave address acknowledge. The master can then issue a STOP condition after the acknowledge (Figure 6). The snapshot is not taken, and  $\overline{\text{INT}}$  status remains unchanged if the master terminates the serial transaction with a no acknowledge.

Typically, the master reads 1 or 2 bytes from the MAX7321, each byte being acknowledged by the master upon reception.

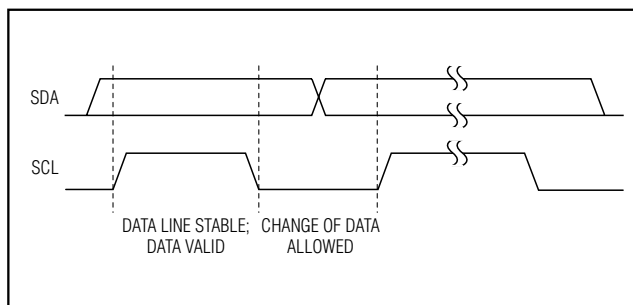


Figure 3. Bit Transfer

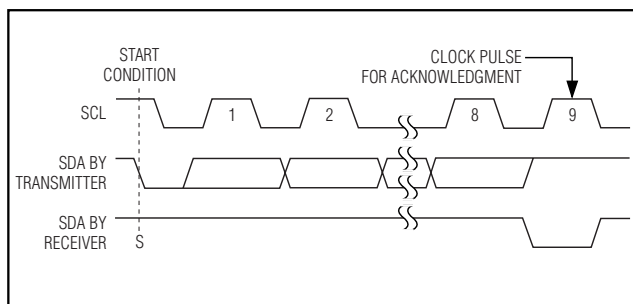


Figure 4. Acknowledge

The master can read 1 byte from the MAX7321 and then issue a STOP condition (Figure 7). In this case, the MAX7321 transmits the current port data, clears the change flags, and resets the transition detection.  $\overline{\text{INT}}$  goes high (high impedance if an external pullup resistor is not fitted) during the slave address acknowledge. The new snapshot data is the current port data transmitted to the master; therefore, port changes occurring during the transmission are detected.  $\overline{\text{INT}}$  remains high until the STOP condition.

The master can read 2 bytes from the MAX7321 and then issue a STOP condition (Figure 8). In this case, the MAX7321 transmits the current port data, followed by the change flags. The change flags are then cleared, and transition detection resets.  $\overline{\text{INT}}$  goes high (high impedance if an external pullup resistor is not fitted) during the slave address acknowledge. The new snapshot data is the current port data transmitted to the master; therefore, port changes occurring during the transmission are detected.  $\overline{\text{INT}}$  remains high until the STOP condition.

# I<sup>2</sup>C Port Expander with 8 Open-Drain I/Os

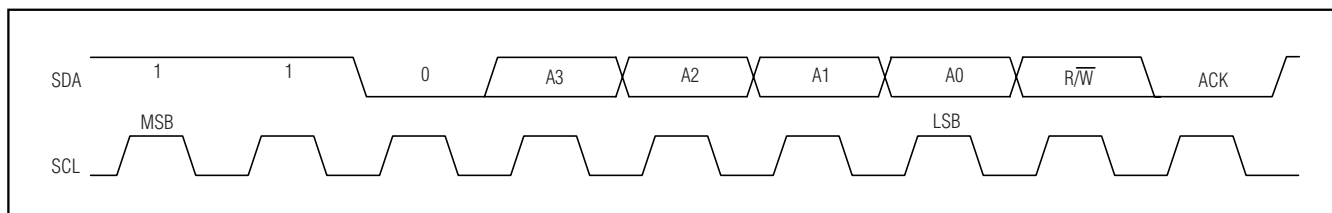


Figure 5. Slave Address

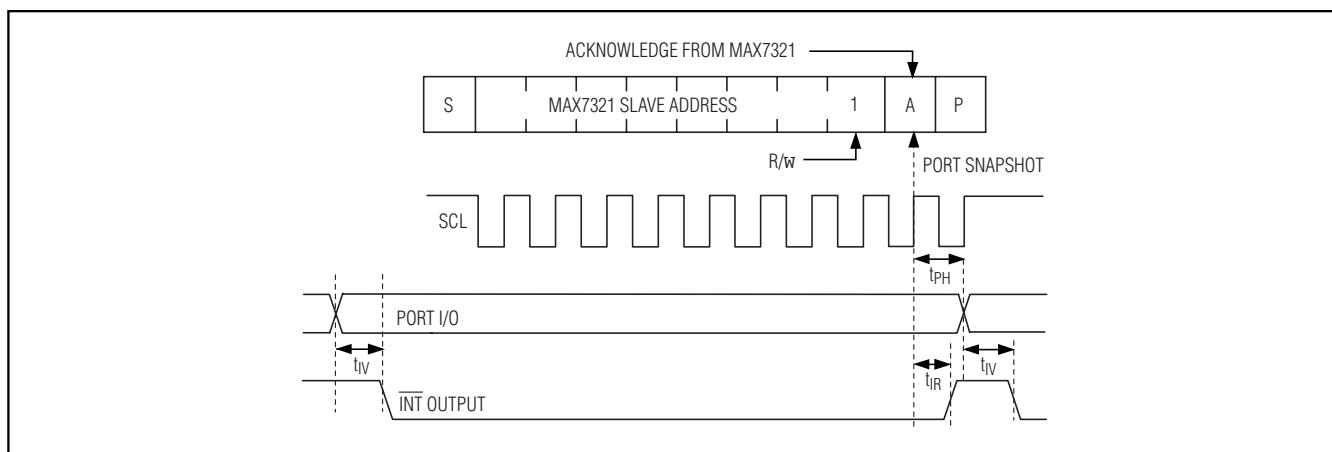


Figure 6. Reading the MAX7321 (No Data)

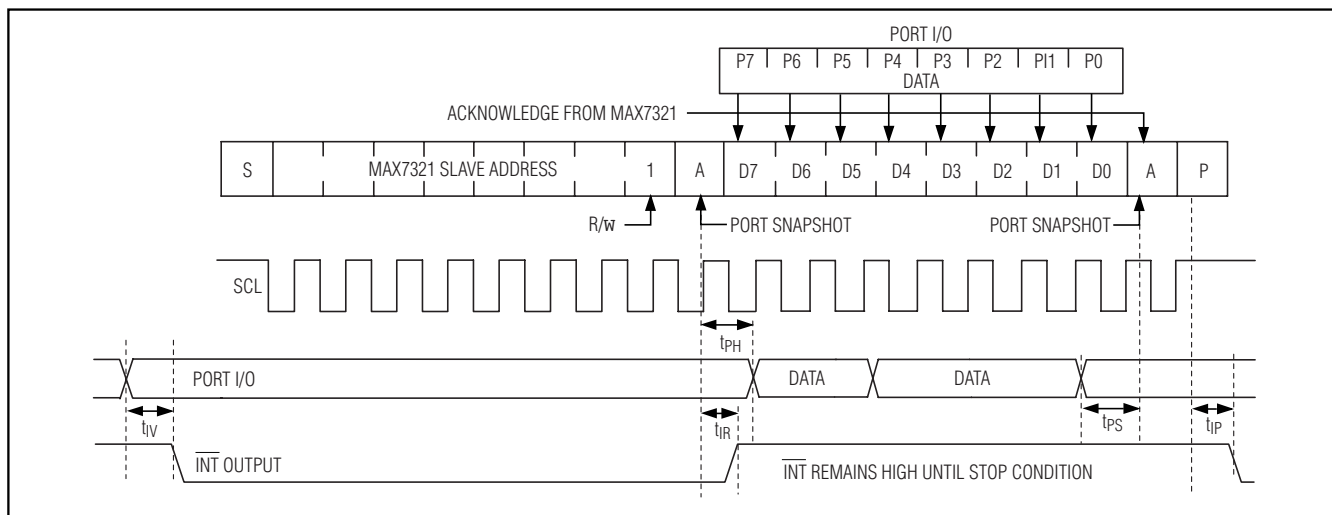


Figure 7. Reading the MAX7321 (1 Data Byte)

# I<sup>2</sup>C Port Expander with 8 Open-Drain I/Os

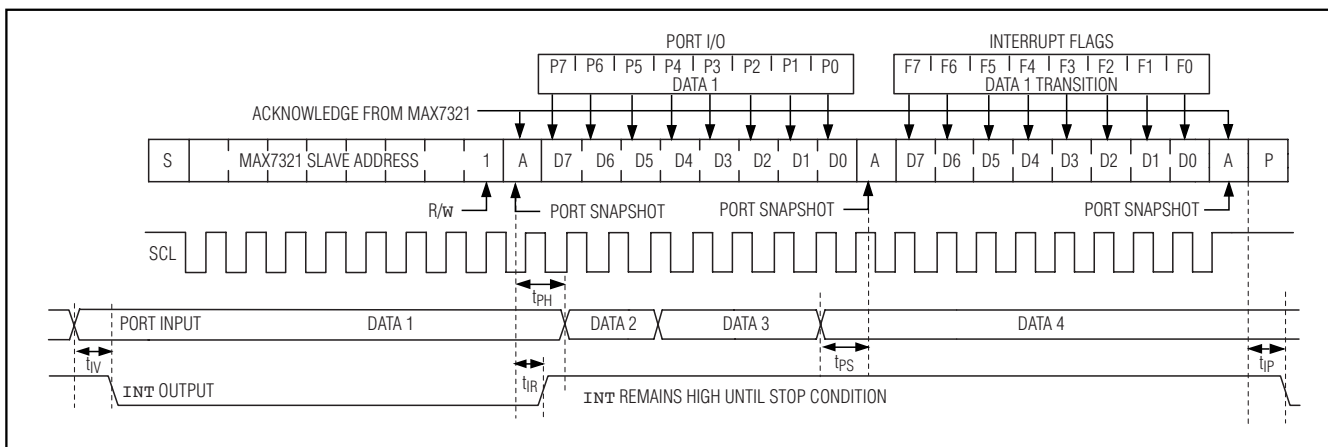


Figure 8. Reading the MAX7321 (2 Data Bytes)

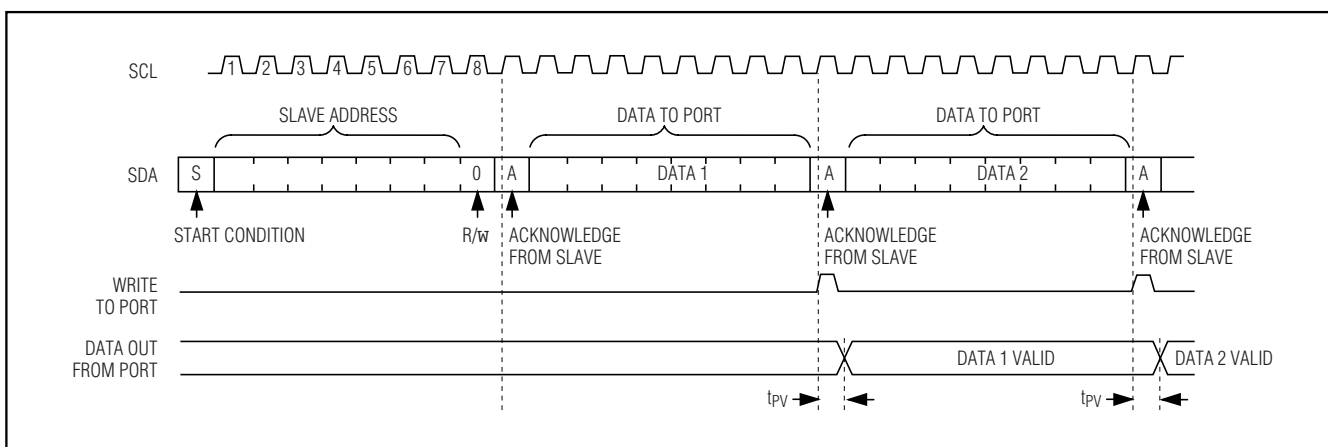


Figure 9. Writing the MAX7321

## Writing the MAX7321

A write to the MAX7321 starts with the master transmitting the MAX7321's slave address with the  $R/\overline{W}$  bit set low. The MAX7321 acknowledges the slave address, and samples the ports (takes a snapshot) during acknowledge.  $\overline{INT}$  goes high (high impedance if an external pullup resistor is not fitted) during the slave address acknowledge. The master can then issue a STOP condition after the acknowledge (Figure 6), but typically the master proceeds to transmit 1 or more bytes of data. The MAX7321 acknowledges these subsequent bytes of data and updates the I/O ports with each new byte until the master issues a STOP condition (Figure 9).

## Applications Information

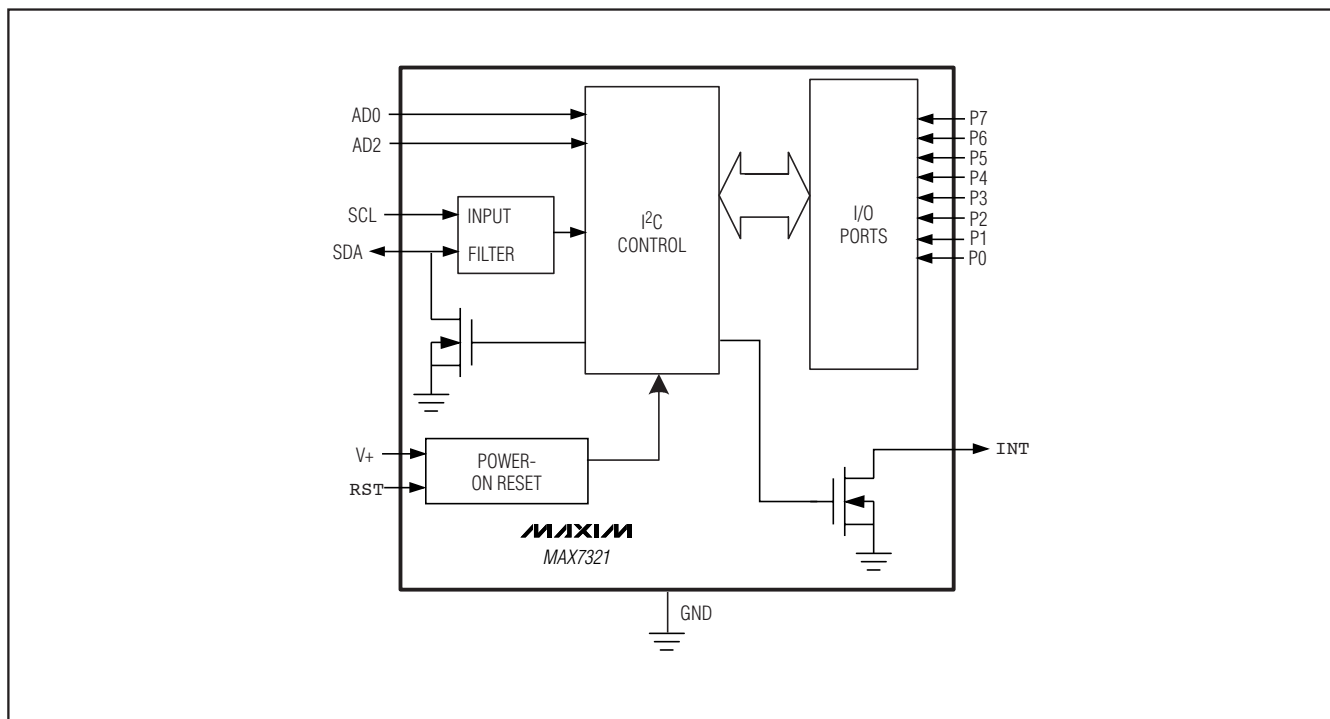
### Port Input and I<sup>2</sup>C Interface Level Translation from Higher or Lower Logic Voltages

The MAX7321's I<sup>2</sup>C interface (SDA, SCL, AD0, AD2), reset input  $\overline{RST}$ , interrupt output  $\overline{INT}$ , and the eight I/O ports P0–P7 are overvoltage protected to +6V independent of  $V_{+}$ . This allows the MAX7321 to operate from a lower supply voltage, such as +3.3V, while the I<sup>2</sup>C interface and/or any of the eight I/O ports are driven as inputs driven from a higher logic level, such as +5V.

The MAX7321 can operate from a higher supply voltage, such as +3V, while the I<sup>2</sup>C interface and/or some of the I/O ports P0–P7 are driven from a lower logic level, such as +2.5V. Apply a minimum voltage of 0.7 x

# I<sup>2</sup>C Port Expander with 8 Open-Drain I/Os

## Functional Diagram



V+ to assert a logic high on any I/O port. For example, a MAX7321 operating from a +5V supply may not recognize a +3.3V nominal logic high. One solution for input-level translation is to drive MAX7321 I/Os from open-drain outputs. Use a pullup resistor to V+ or a higher supply to ensure a high logic voltage of greater than  $0.7 \times V+$ .

### Port-Output Port-Level Translation

The open-drain output architecture allows for level translation to higher or lower voltages than the MAX7321's supply. Use an external pullup resistor on any output to convert the high-impedance logic-high condition to a positive voltage level. The resistor can be connected to any voltage up to +6V, and the resistor value chosen to ensure no more than 20mA is sunk in the logic-low condition. For interfacing CMOS inputs, a pullup resistor value of 220k $\Omega$  is a good starting point. Use a lower resistance to improve noise immunity, in applications where power consumption is less critical, or where a faster rise time is needed for a given capacitive load.

### Hot Insertion

RST, SCL, SDA, AD0, and AD2 and the P0–P7 I/Os remain high impedance with up to +6V asserted on

them when the MAX7321 is powered down ( $V+ = 0$ ). The MAX7321 can therefore be used in hot-swap applications.

Each of the I/O P0–P7 has a protection diode to GND (Figure 10). When a port is driven to a voltage lower than GND, the protection diode clamps the voltage to a diode drop below GND.

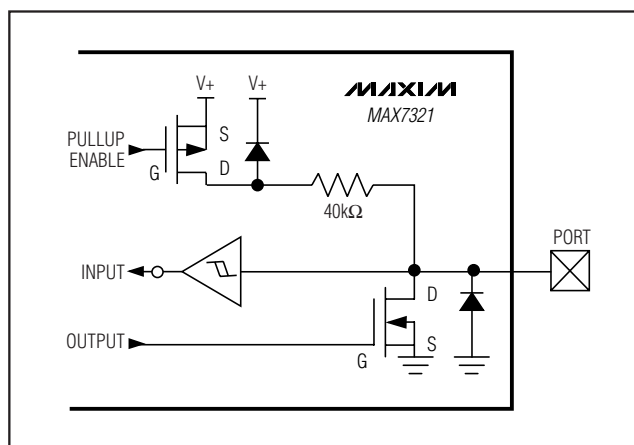


Figure 10. MAX7321 Input Port Structure

# I<sup>2</sup>C Port Expander with 8 Open-Drain I/Os

**Table 4. MAX7321, MAX6965, MAX7315, and MAX7316 Pin Compatibility**

PIN-PACKAGE		PIN FUNCTION		
16 QSOP	16 TQFN	MAX7321	MAX7315	MAX6965 AND MAX7316
1	15	AD0	AD0	BLINK
2	16	RST	AD1	RST
3	1	AD2	AD2	AD0

Each of the I/O ports P0–P7 also has a 40k $\Omega$  (typ) pullup resistor that can be enabled or disabled. When a port driven to a voltage higher than V+, the body diode of the pullup enable switch conducts and the 40k $\Omega$  pullup resistor is enabled. When the MAX7321 is powered down (V+ = 0), each I/O port appears as a 40k $\Omega$  resistor in series with a diode connected to zero. I/O ports are protected to +6V under any of these circumstances (Figure 10).

## Driving LED Loads

When driving LEDs, a resistor must be fitted in series with the LED to limit the LED current to no more than 20mA. Connect the LED cathode to the MAX7321 port, and the LED anode to V+ through the series current-limiting resistor, R<sub>LED</sub>. Set the port output low to illuminate the LED. Choose the resistor value according to the following formula:

$$R_{LED} = (V_{SUPPLY} - V_{LED} - V_{OL}) / I_{LED}$$

where:

R<sub>LED</sub> is the resistance of the resistor in series with the LED ( $\Omega$ ).

V<sub>SUPPLY</sub> is the supply voltage used to drive the LED (V).

V<sub>LED</sub> is the forward voltage of the LED (V).

V<sub>OL</sub> is the output-low voltage of the MAX7321 when sinking I<sub>LED</sub> (V).

I<sub>LED</sub> is the desired operating current of the LED (A).

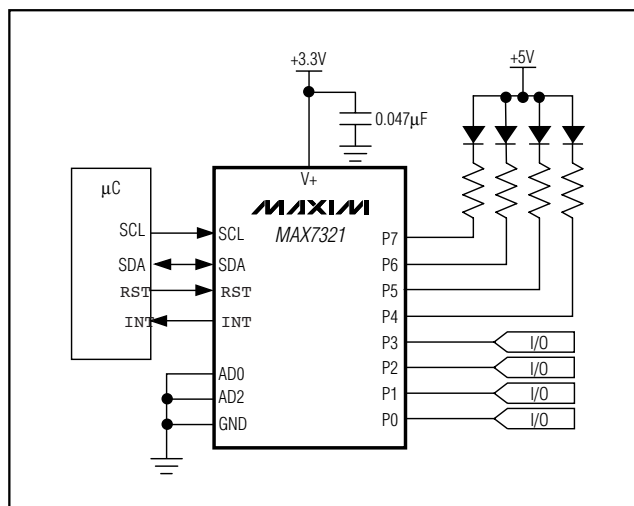
For example, to operate a 2.2V red LED at 10mA from a +5V supply:

$$R_{LED} = (5 - 2.2 - 0.07) / 0.010 = 270\Omega$$

## Driving Load Currents Higher than 20mA

The MAX7321 can be used to drive loads, such as relays, that draw more than 20mA by paralleling outputs. Use at least one output per 20mA of load current; for example, a 5V, 330mW relay draws 66mA and therefore requires four paralleled outputs. Any combination of outputs can be used as part of a load-sharing design because any com-

## Typical Application Circuit



ination of ports can be set or cleared at the same time by writing the MAX7321. Do not exceed a total sink current of 100mA for the device.

The MAX7321 must be protected from the negative voltage transient generated when switching off inductive loads (such as relays), by connecting a reverse-biased diode across the inductive load. Choose the peak current for the diode to be greater than the inductive load's operating current.

## Power-Supply Considerations

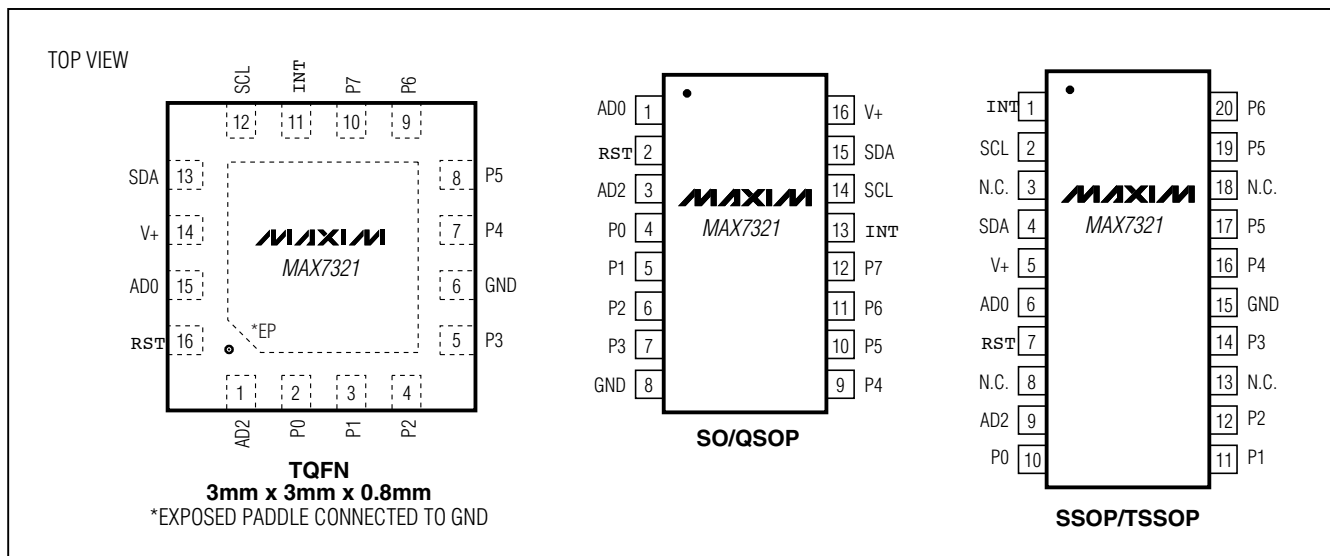
The MAX7321 operates with a supply voltage of +1.71V to +5.5V over the -40°C to +125°C temperature range. Bypass the supply to GND with a ceramic capacitor of at least 0.047 $\mu$ F as close to the device as possible. For the TQFN version, additionally connect the exposed pad to GND.

## Compatibility with MAX6965, MAX7315, and MAX7316

The MAX7321 is subset pin compatible with the MAX6965, MAX7315, and MAX7316. The pin differences are shown in Table 4. The MAX7321 is not software compatible with the MAX6965, MAX7315, or MAX7316. In many cases, it is possible to design a PC board to work with all these port expanders, providing design flexibility.

# I<sup>2</sup>C Port Expander with 8 Open-Drain I/Os

## Pin Configurations



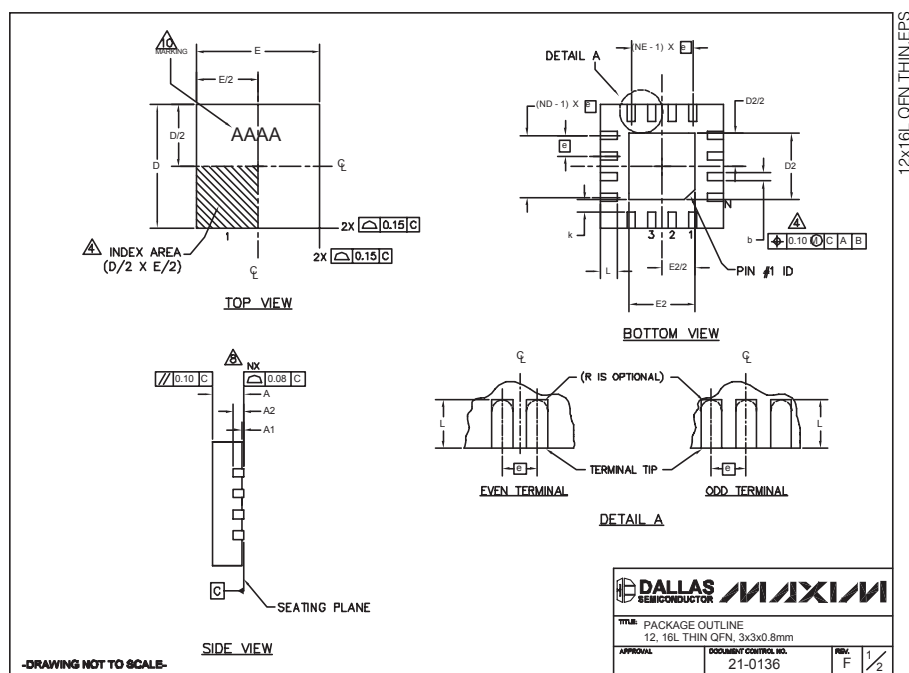
## Chip Information

PROCESS: BICMOS

## I<sup>2</sup>C Port Expander with 8 Open-Drain I/Os

## ***Package Information***





(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



12L 3x3				16L 3x3			
PKG	REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	
B	0.20	0.25	0.30	0.20	0.25	0.30	
D	2.90	3.00	3.10	2.90	3.00	3.10	
E	2.90	3.00	3.10	2.90	3.00	3.10	
e	0.50 BSC			0.50 BSC			
L	0.45	0.55	0.65	0.30	0.40	0.50	
N	12			16			
ND	3			4			
NE	3			4			
A1	0	0.02	0.05	0	0.02	0.05	
A2	0.20 REF			0.20 REF			
K	0.25	-	-	0.25	-	-	

EXPPOSED PAD VARIATIONS									
PKG CODES	D2			E2			PIN ID	JEDEC	GOWN ALLOWED
	MIN	NOM	MAX	MIN	NOM	MAX			
T12331	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 4.5"	WEED-1	NO
T12333	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 4.5"	WEED-1	YES
T12334	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 4.5"	WEED-1	YES
T16331	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 4.5"	WEED-2	NO
T16332	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 4.5"	WEED-2	YES
T1633F3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 4.5"	WEED-2	N/A
T1633FH3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 4.5"	WEED-2	N/A
T16334	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 4.5"	WEED-2	NO

NOTES:

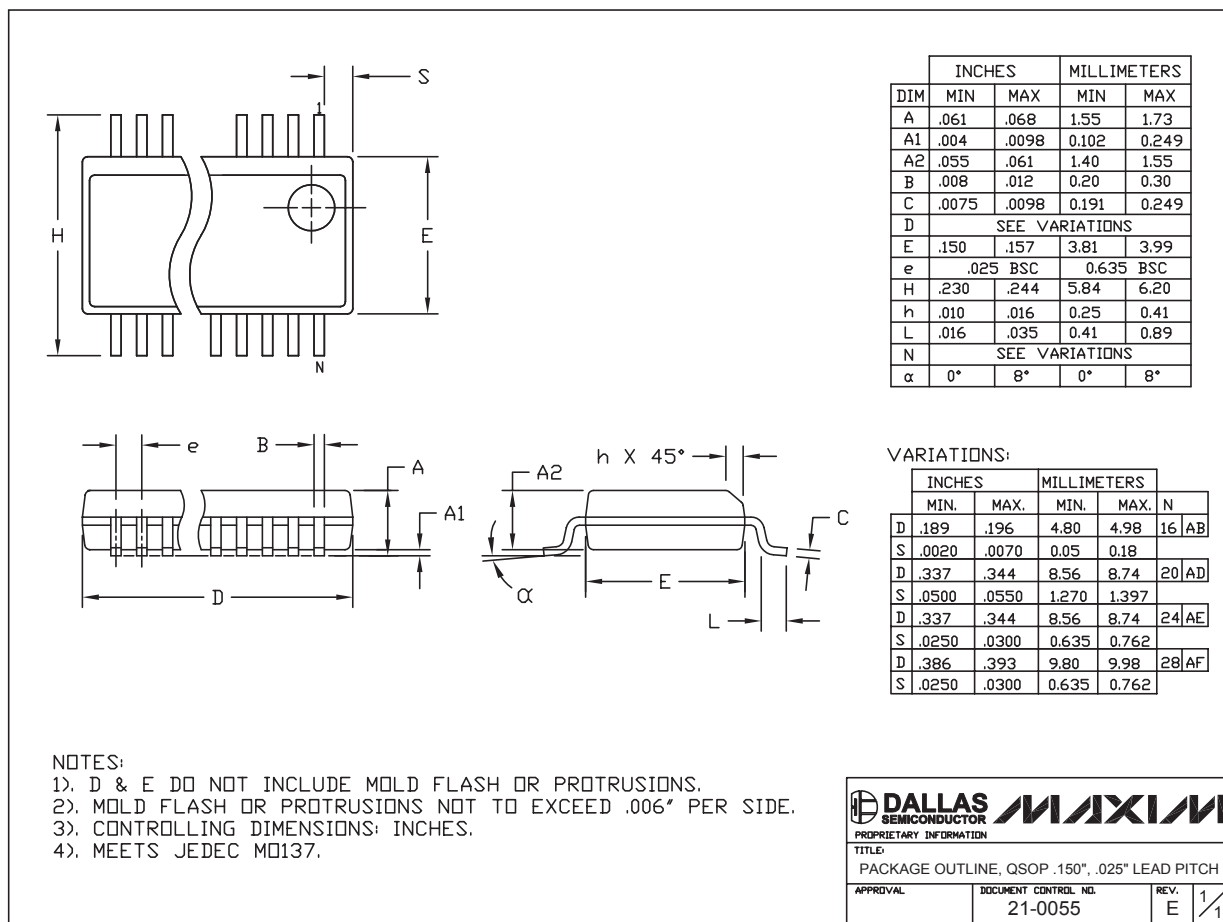
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4.  THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5.  DIMENSION D APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOSITION IS POSSIBLE IN A SYMMETRICAL FASHION.
8.  COPLANARITY APPLIES TO THE EXPOSED HETEROGENEOUS SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO2020 REVISION C.
10.  MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
11. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY



# I<sup>2</sup>C Port Expander with 8 Open-Drain I/Os

## Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



QSOPEPS

MAX7321

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