19-2964; Rev 0; 8/03

EVALUATION KIT AVAILABLE

MAXIM

# Parallelable, Clamped Two-Switch Power-Supply Controller IC



## General Description

The MAX5051 is a clamped, two-switch power-supply controller IC. This device can be used both in forward or flyback configurations with input voltage ranges from 11V to 76V. It provides comprehensive protection mechanisms against possible faults, resulting in very high reliability power supplies. When used in conjunction with secondary-side synchronous rectification, power-supply efficiencies can easily reach 92% for a +3.3V output power supply operated from a 48V bus. The integrated high- and low-side gate drivers provide more than 2A of peak gate-drive current to two external N-channel MOSFETs. Low startup current reduces the power loss across the bootstrap resistor. A feed-forward voltage-mode topology provides excellent line rejection while avoiding the pitfalls of traditional current-mode control.

The MAX5051 power-supply controller is primary as well as secondary-side parallelable, allowing the design of scaleable power systems when necessary. When paralleling the primary side, dedicated pins allow for simultaneous wakeup or shutdown of all paralleled units, thus preventing current-hogging during startup or fault conditions.

The MAX5051 generates a lookahead signal for driving secondary-side synchronous MOSFETs. Special primary-side synchronization inputs/outputs allow two primaries to be operated 180° out of phase for increased output power and lower input ripple currents.

The MAX5051 is available in a 28-pin TSSOP-EP package and operates over a wide -40°C to +125°C temperature range.

**Warning: The MAX5051 is designed to work with high voltages. Exercise caution.**

## Applications

High-Efficiency, Isolated Telecom/Datacom Power Supplies

48V and 12V Server Power Supplies

48V Power-Supply Modules

42V Automotive Power Systems

Industrial Power Supplies

## Features

- ♦ **Wide Input Voltage Range, 11V to 76V**
- ♦ **Voltage Mode with Input Voltage Feed-Forward**
- ♦ **Ripple-Phased Parallel Topology for High Current/Power Output**
- ♦ **2A Integrated High- and Low-Side MOSFET Drivers**
- ♦ **SYNCIN And SYNCOUT Pins Enable 180° Out-Of-Phase Operation**
- ♦ **Programmable Brownout and Bootstrap UVLOs**
- ♦ **High-Side Driver Bootstrap Capacitor Precharge Driver**
- ♦ **Low Current-Limit Threshold for High Efficiency**
- ♦ **Programmable Switching Frequency**
- ♦ **Reference Voltage Soft-Start for Startup Without Overshoots**
- ♦ **Startup Synchronization with Multiple Paralleled Primaries**
- ♦ **Programmable Integrating Current-Limit Fault Protection**
- ♦ **Look-Ahead PWM Signal for Secondary-Side Synchronous Rectifier Drivers**
- ♦ **Look-Ahead Drivers for Either A High-Speed Optocoupler or Pulse Transformer**
- ♦ **Wide -40°C to +125°C Operating Range**
- ♦ **Thermally Enhanced 28-Pin TSSOP Package**

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX5051AUI | -40°C to +125°C | 28-TSSOP-EP* |

**EP = Exposed pad.*

***Pin Configuration appears at end of data sheet.***

# Parallelable, Clamped Two-Switch Power-Supply Controller IC

## ABSOLUTE MAXIMUM RATINGS

AVIN, PVIN, XFRMRH to GND .....-0.3V to +80V
BST to GND .....-0.3V to +95V
BST, DRVH to XFRMRH.....-0.3V to +12V
REG9, DRVDD, DRVL to GND.....-0.3V to +12V
DRVB, LXVDD, LXL, LXH to GND .....-0.3V to +12V
UVLO, STT, COMP, CON to GND .....-0.3V to +12V
FLTINT, RCFF to GND .....-0.3V to +12V
REG5, CS, CSS, FB to GND .....-0.3V to +6V
STARTUP, SYNCIN to GND.....-0.3V to +6V
SYNCOUT, RCOSC to GND .....-0.3V to +6V
PGND to GND .....-0.3V to +0.3V
LXL, LXH Current Continuous.....±50mA
DRVL, DRVH Current Continuous.....±100mA
DRVL, DRVH Peak Current (<500ns) .....±5A
PVIN, REG9 Continuous Current .....+120mA
REG5 Continuous Current .....+80mA
DRVB, RCFF, RCOSC, CSS Continuous Current .....±20mA
COMP, SYNCOUT Continuous Current.....±20mA
REG9, REG5, and COMP Short to GND .....Continuous
Continuous Power Dissipation ($T_A$ = +70°C)
28-Pin TSSOP (derate 23.8mW/°C above +70°C) .....1905mW
28-Pin TSSOP ($\theta_{JA}$).....42°C/W
Operating Temperature Range .....-40°C to +125°C
Maximum Junction Temperature ($T_J$) .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

(AVIN = 12V, PVIN = 12V, $V_{UVLO}$ = $V_{STT}$ = 3V, $V_{CON}$ = 3V, $R_{RCOSC}$ = 24kΩ, $C_{CSS}$ = 10nF, $C_{RCOSC}$ = 100pF, $C_{REG9}$ = 4.7µF, $C_{REG5}$ = 4.7µF, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C. All driver, voltage-regulator, and reference outputs unconnected except for bypass capacitors.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENT (AVIN, PVIN)** | | | | | | |
| AVIN Standby Current | $I_{ASTBY}$ | $V_{AVIN}$ = $V_{PVIN}$ = 11V to 76V; $V_{STARTUP}$ = $V_{CS}$ = 0V; $V_{BST}$ = $V_{XFRMRH}$ = $V_{DRVDD}$ = $V_{REG9}$; RCFF floating | | 300 | 450 | µA |
| PVIN Standby Current | $I_{PSTBY}$ | | | 400 | 650 | µA |
| AVIN Supply Current | $I_{AVIN}$ | $V_{AVIN}$ = $V_{PVIN}$ = 11V to 76V; $V_{CS}$ = 0V; $V_{BST}$ = $V_{DRVDD}$ = $V_{REG9}$; $V_{XFRMRH}$ = 0V; STARTUP, RCFF floating | | 0.65 | 1 | mA |
| PVIN Supply Current | $I_{PVIN}$ | | | 8 | 12 | mA |
| AVIN Input Voltage Range | | Inferred from AVIN supply current test | 11 | | 76 | V |
| **+9V LDO (REG9)** | | | | | | |
| PVIN Input Voltage Range | $V_{PVIN}$ | Inferred from PVIN supply current test | 11 | | 76 | V |
| REG9 Output-Voltage Set Point | $V_{REG9}$ | $V_{PVIN}$ = 11V | 8.3 | | 9.0 | V |
| REG9 Line Regulation | | $V_{PVIN}$ = 11V to 76V | | 0.1 | | mV/V |
| REG9 Load Regulation | | $I_{REG9}$ = 0 to 80mA | | | 250 | mV |
| REG9 Dropout Voltage | | $I_{REG9}$ = 80mA | | 0.5 | | V |
| REG9 Undervoltage Lockout Threshold | | $V_{REG9}$ falling | 5.7 | | 6.7 | V |
| REG9 Undervoltage Lockout Threshold Hysteresis | | | | 750 | | mV |
| **+5V LDO (REG5)** | | | | | | |
| REG5 Output-Voltage Set Point | $V_{REG5}$ | | 4.8 | | 5.1 | V |
| REG5 Load Regulation | | $I_{REG5}$ = 0 to 40mA | | | 50 | mV |
| REG5 Dropout Voltage | | $I_{REG5}$ = 40mA, measured with respect to $V_{REG9}$ | | 0.5 | | V |

## ELECTRICAL CHARACTERISTICS (continued)

(AVIN = 12V, PVIN = 12V, $V_{UVLO}$ = $V_{STT}$ = 3V, $V_{CON}$ = 3V, $R_{RCOSC}$ = 24kΩ, $C_{CSS}$ = 10nF, $C_{RCOSC}$ = 100pF, $C_{REG9}$ = 4.7µF, $C_{REG5}$ = 4.7µF, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C. All driver, voltage-regulator, and reference outputs unconnected except for bypass capacitors.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **SOFT-START/REFERENCE (CSS)** | | | | | | |
| Reference Voltage | $V_{CSS}$ | | 1.215 | 1.235 | 1.255 | V |
| Soft-Start Pullup Current | $I_{CSS}$ | | | 70 | | µA |
| **ERROR AMPLIFIER (CSS, FB, COMP)** | | | | | | |
| FB Input Range | $V_{FB}$ | Inferred from FB offset voltage test | 0 | | 3 | V |
| FB Input Current | $I_{FB}$ | $V_{FB}$ = $V_{REF}$ | | | ±250 | nA |
| COMP Output Range | | Inferred from FB offset voltage test | 2.1 | | 6.0 | V |
| COMP Output Sink Current | | $V_{FB}$ = 3V | | 20 | | mA |
| COMP Output Source Current | | $V_{FB}$ = 0V | | 30 | | mA |
| Open-Loop Gain | $G_A$ | 2.1V < $V_{COMP}$ < 6V | | 80 | | dB |
| Unity-Gain Bandwidth | BW | $C_{COMP}$ = 50pF, $I_{COMP}$ = ±5mA | | 3 | | MHz |
| FB Offset Voltage | $V_{OS}$ | $V_{FB}$ = 0 to 3V; $V_{COMP}$ = 2.1V to 6V; $I_{COMP}$ = -5mA to +5mA | -3 | | +3 | mV |
| COMP Output Slew Rate | SR | $C_{COMP}$ = 50pF | | 1 | | V/µs |
| **PVIN UNDERVOLTAGE LOCKOUT (STT)** | | | | | | |
| PVIN Undervoltage Lockout | | $V_{PVIN}$ rising | 22 | 23.5 | 25 | V |
| STT Threshold | $V_{STT}$ | $V_{STT}$ rising | 1.18 | 1.24 | 1.30 | V |
| STT Input Impedance | $R_{STT}$ | | | 100 | | kΩ |
| **INTEGRATING FAULT PROTECTION (FLTINT)** | | | | | | |
| FLTINT Source Current | $I_{FLTINT}$ | $V_{FLTINT}$ = 0V | | 90 | | µA |
| FLTINT Shutdown Threshold | $V_{FLTINTSD}$ | $V_{FLTINT}$ = rising | | 2.9 | | V |
| FLTINT Restart Hysteresis | $V_{FLTINTHY}$ | | | 0.9 | | V |
| **OSCILLATOR (RCOSC, SYNCIN, SYNCOUT)** | | | | | | |
| PWM Period | $t_S$ | $R_{RCOSC}$ = 24kΩ, $C_{RCOSC}$ = 100pF | | 3.9 | | µs |
| Maximum PWM Duty Cycle | $D_{MAX}$ | $R_{RCOSC}$ = 24kΩ, $C_{RCOSC}$ = 100pF | | 48 | | % |
| Maximum RCOSC Frequency | $f_{RCOSCMAX}$ | | | 1 | | MHz |
| Maximum SYNCIN Frequency | $f_{SYNCIN}$ | 50% duty cycle | | 500 | | kHz |
| SYNCIN High-Level Voltage | $VH_{SYNCIN}$ | Pulse rising | 2.1 | | | V |
| SYNCIN Low-Level Voltage | $VL_{SYNCIN}$ | Pulse falling | | | 0.8 | V |
| SYNCIN Pulldown Resistor | | | | 100 | | kΩ |
| SYNCIN Rising to SYNCOUT Falling Delay | | | | 30 | | ns |
| SYNCIN Falling to SYNCOUT Rising Delay | | | | 70 | | ns |

# Parallelable, Clamped Two-Switch Power-Supply Controller IC

## ELECTRICAL CHARACTERISTICS (continued)

(AVIN = 12V, PVIN = 12V, $V_{UVLO}$ = $V_{STT}$ = 3V, $V_{CON}$ = 3V, $R_{RCOSC}$ = 24kΩ, $C_{CSS}$ = 10nF, $C_{RCOSC}$ = 100pF, $C_{REG9}$ = 4.7µF, $C_{REG5}$ = 4.7µF, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C. All driver, voltage-regulator, and reference outputs unconnected except for bypass capacitors.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| SYNCOUT Voltage High | | Sourcing 1.2mA | 4.5 | | 5.1 | V |
| SYNCOUT Voltage Low | | Sinking 2.4mA | | | 0.3 | V |
| RCOSC Peak Trip Level | $V_{TH}$ | | | 2.5 | | V |
| RCOSC Valley Trip Level | | | | 0.2 | | V |
| RCOSC Input Bias Current | | | | -0.3 | | µA |
| RCOSC Discharge MOSFET $R_{DS(ON)}$ | | Sinking 10mA | | 50 | 100 | Ω |
| RCOSC Discharge Pulse Width | | | | 50 | | ns |
| **UNDERVOLTAGE LOCKOUT (UVLO)** | | | | | | |
| UVLO Threshold | $V_{UVLO}$ | $V_{UVLO}$ rising | 1.18 | 1.24 | 1.30 | V |
| UVLO Hysteresis | $V_{HYS}$ | | | 130 | | mV |
| UVLO Input Bias Current | $I_{BUVLO}$ | $V_{UVLO}$ = 2.5V | -100 | | +100 | nA |
| **PWM COMPARATOR** | | | | | | |
| RCFF Input Voltage Range | | | 0 | | 3 | V |
| Feed-Forward Discharge MOSFET $R_{DS(ON)}$ | $R_{DS(RCFF)}$ | Sinking 10mA | | 50 | 100 | Ω |
| CON Input Voltage Range | | | 0 | | 6 | V |
| RCFF Level-Shift Voltage | $V_{CPWM}$ | | 2.2 | | 2.4 | V |
| CON Input Bias Current | $I_{CON}$ | | -2 | | +2 | µA |
| Propagation Delay to Output | $t_{dCPWM}$ | DRVH, DRVL = unconnected, overdrive = 50mV, measured from CON to DRVL | | 90 | | ns |
| **SYNCHRONOUS RECTIFIER PULSE TRANSFORMER DRIVER (LXVDD, LXH, LXL)** | | | | | | |
| High-Side MOSFET $R_{DS(ON)}$ | $R_{DSLXH}$ | LXH sourcing 10mA, $V_{LXVDD}$ = $V_{REG5}$ | 3 | 6.5 | 12 | Ω |
| Low-Side MOSFET $R_{DS(ON)}$ | $R_{DSLXL}$ | LXL sinking 10mA, $V_{LXVDD}$ = $V_{REG5}$ | 2.0 | 5 | 10 | Ω |
| LXH Rising to DRVL Rising Delay | | | | 90 | | ns |
| **CURRENT-LIMIT COMPARATOR (CS)** | | | | | | |
| Current-Limit Threshold Voltage | $V_{ILIM}$ | | 144 | 154 | 164 | mV |
| Current-Limit Input Bias Current | $I_{BILIM}$ | 0 < $V_{CS}$ < 0.3V | -2 | | +2 | µA |
| Propagation Delay to Output | $t_{dILIM}$ | DRVH, DRVL = unconnected, overdrive = 10mV, measured from CS to DRVL | | 100 | | ns |
| **LOW-SIDE MOSFET DRIVER (DRVDD, DRVL, PGND)** | | | | | | |
| Peak Source Current | | $V_{DRVL}$ = 0V, pulse width < 100ns; $V_{DRVDD}$ = $V_{REG9}$ | | 2 | | A |
| Peak Sink Current | | $V_{DRVL}$ = $V_{REG9}$, pulse width < 100ns; $V_{DRVDD}$ = $V_{REG9}$ | | 5 | | A |
| DRVL Resistance Sourcing | | $I_{DRVL}$ = 50mA, $V_{DRVDD}$ = $V_{REG9}$ | | 1.7 | 3.5 | Ω |
| DRVL Resistance Sinking | | $I_{DRVL}$ = -50mA, $V_{DRVDD}$ = $V_{REG9}$ | | 0.6 | 1.4 | Ω |

## ELECTRICAL CHARACTERISTICS (continued)

(AVIN = 12V, PVIN = 12V, $V_{UVLO}$ = $V_{STT}$ = 3V, $V_{CON}$ = 3V, $R_{RCOSC}$ = 24kΩ, $C_{CSS}$ = 10nF, $C_{RCOSC}$ = 100pF, $C_{REG9}$ = 4.7µF, $C_{REG5}$ = 4.7µF, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C. All driver, voltage-regulator, and reference outputs unconnected except for bypass capacitors.)

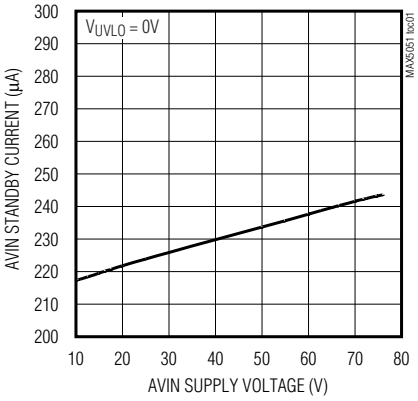
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **HIGH-SIDE MOSFET DRIVER (BST, DRVH, XFRMRH)** | | | | | | |
| Peak Source Current | | $V_{DRVH}$ = GND, pulse width < 100ns, $V_{BST}$ = $V_{REG9}$, $V_{XFRMRH}$ = 0V | | 2 | | A |
| Peak Sink Current | | $V_{DRVH}$ = $V_{BST}$, pulse width < 100ns, $V_{BST}$ = $V_{REG9}$, $V_{XFRMRH}$ = 0V | | 5 | | A |
| DRVH Resistance Sourcing | | $I_{DRVH}$ = 50mA, $V_{BST}$ = $V_{REG9}$, $V_{XFRMRH}$ = 0V | | 1.7 | 3.5 | Ω |
| DRVH Resistance Sinking | | $I_{DRVH}$ = -50mA, $V_{BST}$ = $V_{REG9}$, $V_{XFRMRH}$ = 0V | | 0.6 | 1.4 | Ω |
| Skew Between Low-Side and High-Side Drivers | | | | 0 | | ns |
| **BOOST CAPACITOR CHARGE MOSFET (DRVB)** | | | | | | |
| DRVB Resistance Sourcing | | $I_{DRVB}$ = 50mA | 8 | | 35 | Ω |
| DRVB Resistance Sinking | | $I_{DRVB}$ = 50mA | 5 | | 35 | Ω |
| Delay from Clock Fall | | | | 200 | | ns |
| One-Shot Pulse Width | | | | 300 | | ns |
| **STARTUP (STARTUP)** | | | | | | |
| Startup Threshold | $V_{STARTUP}$ | $V_{STARTUP}$ rising | 1.4 | | 2.1 | V |
| Startup Threshold Hysteresis | | | | 330 | | mV |
| Internal Pullup Current | $I_{STARTUP}$ | | | 50 | | µA |
| STARTUP Pulldown MOSFET $R_{DS(ON)}$ | | Sinking 10mA | | 50 | 100 | Ω |
| **OVERTEMPERATURE SHUTDOWN** | | | | | | |
| Shutdown Junction Temperature | | Temperature rising | | 150 | | °C |
| Hysteresis | | | | 10 | | °C |

# Parallelable, Clamped Two-Switch Power-Supply Controller IC

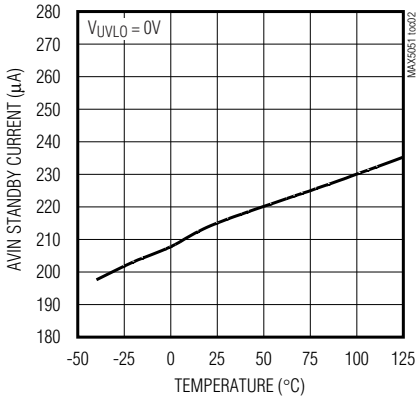
## Typical Operating Characteristics

($V_{AVIN}$ = $V_{PVIN}$ = 12V, $V_{UVLO}$ = $V_{STT}$ = 3V, $V_{CON}$ = 3V, $R_{RCOSC}$ = 24kΩ, $C_{CSS}$ = 10nF, $C_{RCOSC}$ = 100pF, $C_{REG9}$ = 4.7µF, $C_{REG5}$ = 4.7µF, $T_A$ = +25°C, unless otherwise noted.)

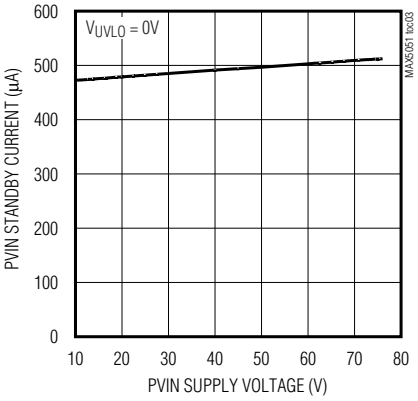
**AVIN STANDBY CURRENT vs. AVIN SUPPLY VOLTAGE**



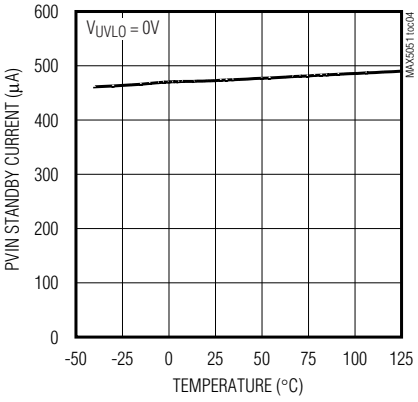

**AVIN STANDBY CURRENT vs. TEMPERATURE**



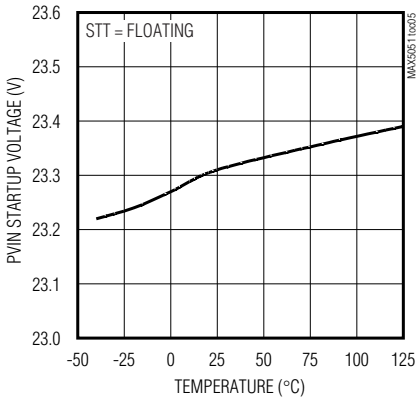

**PVIN STANDBY CURRENT vs. SUPPLY VOLTAGE**



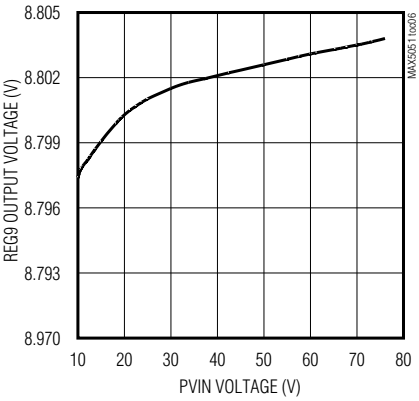

**PVIN STANDBY CURRENT vs. TEMPERATURE**



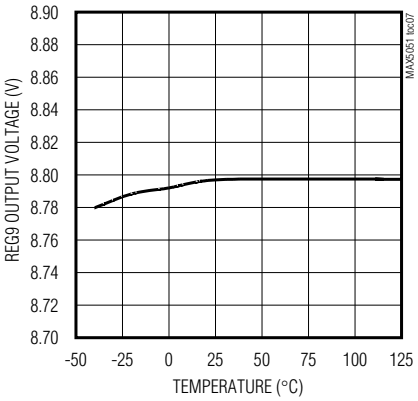

**PVIN STARTUP VOLTAGE vs. TEMPERATURE**



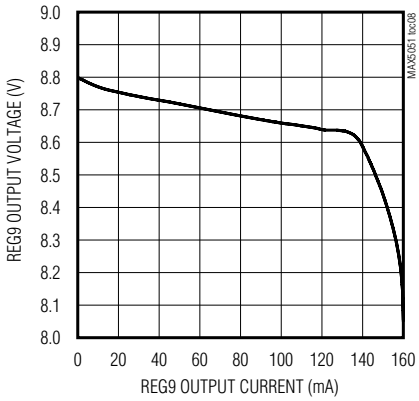

**REG9 OUTPUT VOLTAGE vs. PVIN VOLTAGE**



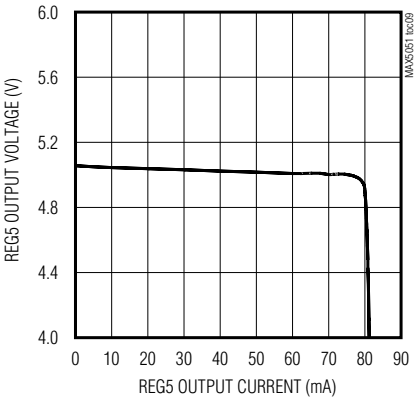

**REG9 OUTPUT VOLTAGE vs. TEMPERATURE**




**REG9 OUTPUT VOLTAGE vs. REG9 OUTPUT CURRENT**



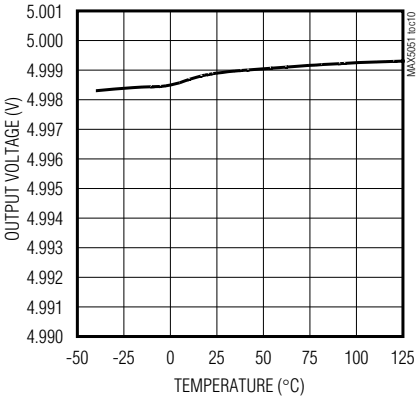

**REG5 OUTPUT VOLTAGE vs. REG5 OUTPUT CURRENT**



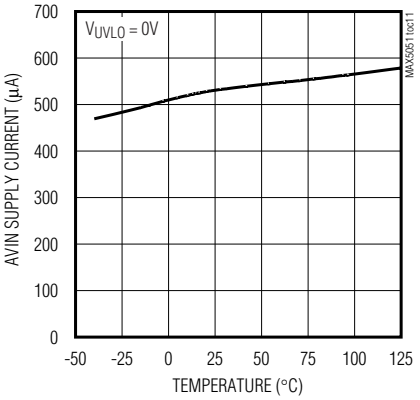
## Typical Operating Characteristics (continued)

($V_{AVIN}$ = $V_{PVIN}$ = 12V, $V_{UVLO}$ = $V_{STT}$ = 3V, $V_{CON}$ = 3V, $R_{RCOSC}$ = 24kΩ, $C_{CSS}$ = 10nF, $C_{RCOSC}$ = 100pF, $C_{REG9}$ = 4.7µF, $C_{REG5}$ = 4.7µF, $T_A$ = +25°C, unless otherwise noted.)

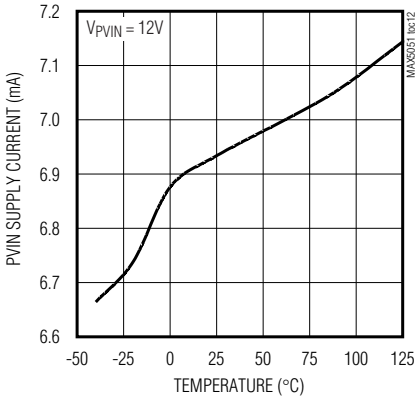
**REG5 OUTPUT VOLTAGE vs. TEMPERATURE**



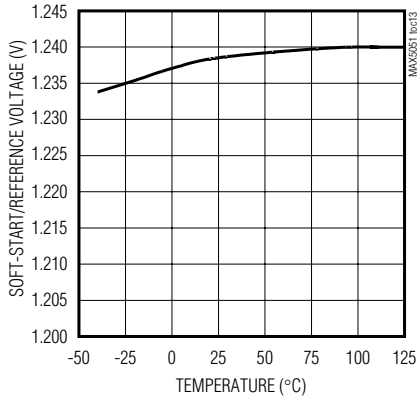

**AVIN SUPPLY CURRENT vs. TEMPERATURE**



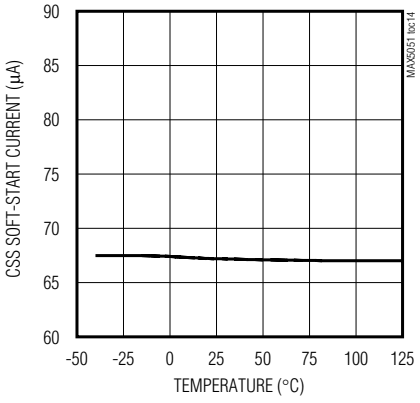

**PVIN SUPPLY CURRENT vs. TEMPERATURE**



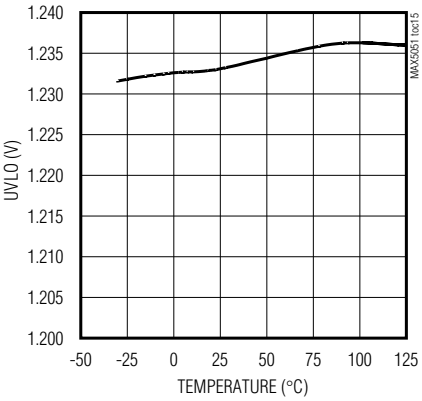

**SOFT-START/REFERENCE VOLTAGE vs. TEMPERATURE**



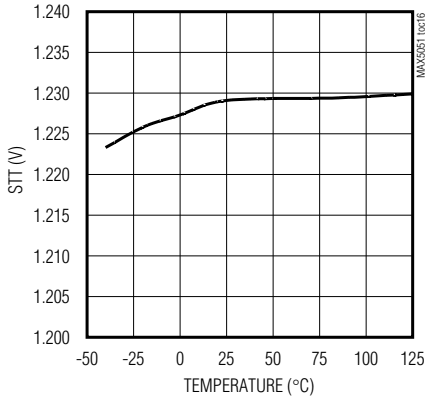

**CSS SOFT-START CURRENT vs. TEMPERATURE**



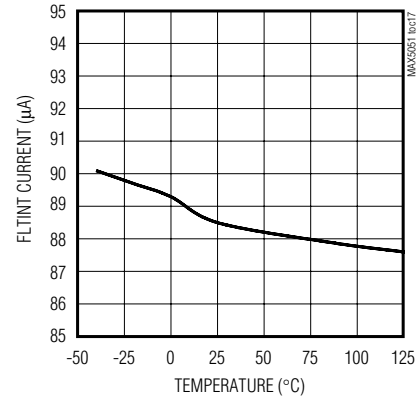

**UVLO THRESHOLD vs. TEMPERATURE**



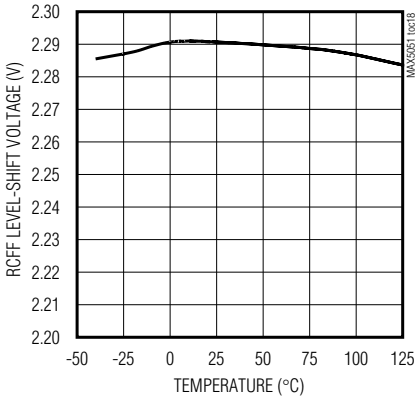

**STT STARTUP THRESHOLD vs. TEMPERATURE**




**FLTINT CURRENT vs. TEMPERATURE**




**RCFF LEVEL-SHIFT VOLTAGE vs. TEMPERATURE**

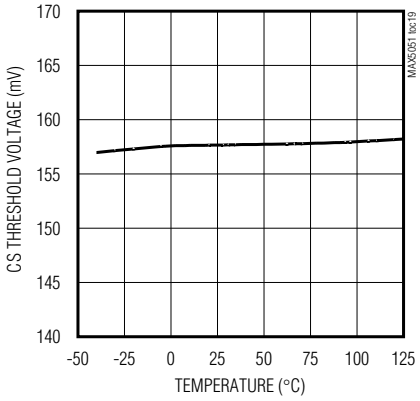


# Parallelable, Clamped Two-Switch Power-Supply Controller IC

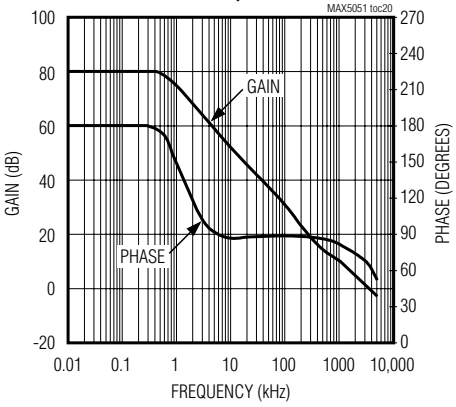
## Typical Operating Characteristics (continued)

($V_{AVIN}$ = $V_{PVIN}$ = 12V, $V_{UVLO}$ = $V_{STT}$ = 3V, $V_{CON}$ = 3V, $R_{RCOSC}$ = 24kΩ, $C_{CSS}$ = 10nF, $C_{RCOSC}$ = 100pF, $C_{REG9}$ = 4.7µF, $C_{REG5}$ = 4.7µF, $T_A$ = +25°C, unless otherwise noted.)

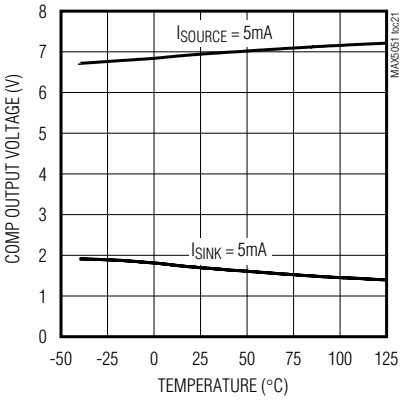
**CURRENT-LIMIT THRESHOLD vs. TEMPERATURE**



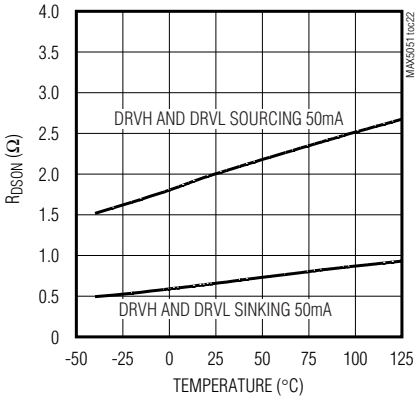

**OPEN-LOOP GAIN/PHASE vs. FREQUENCY**



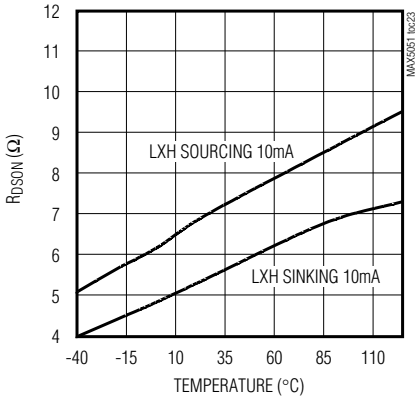

**COMP OUTPUT VOLTAGE vs. TEMPERATURE**



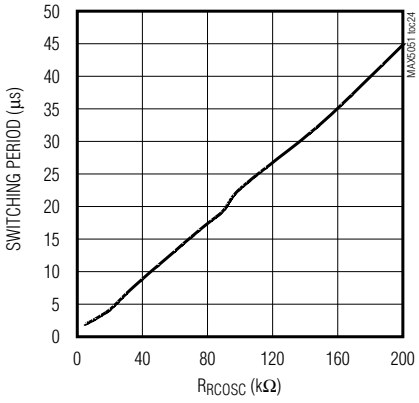

**DRVH AND DRVL $R_{DSON}$ vs. TEMPERATURE**



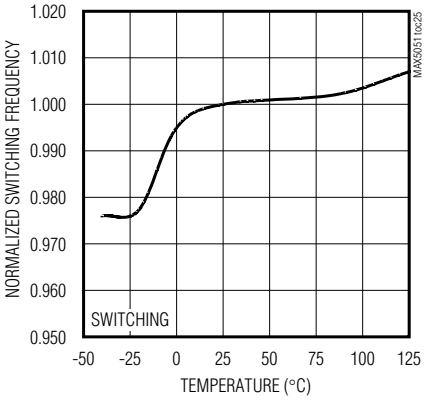

**LXL AND LXH $R_{DSON}$ vs. TEMPERATURE**



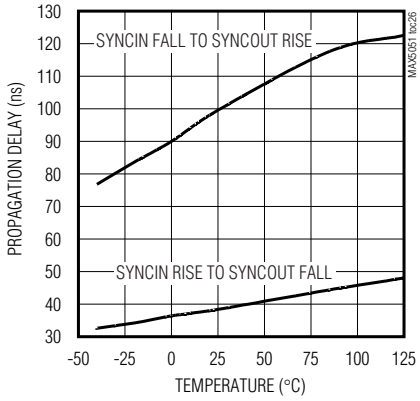

**SWITCHING PERIOD vs. $R_{RCOSC}$**



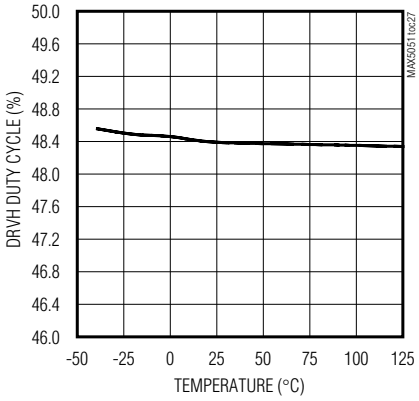

**NORMALIZED SWITCHING FREQUENCY vs. TEMPERATURE**




**SYNCIN TO SYNCOUT PROPAGATION DELAY vs. TEMPERATURE**



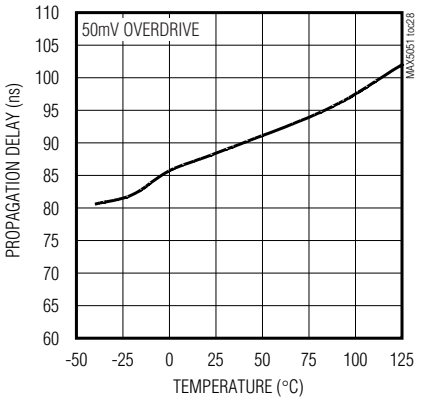

**DRVH MAXIMUM DUTY CYCLE vs. TEMPERATURE**



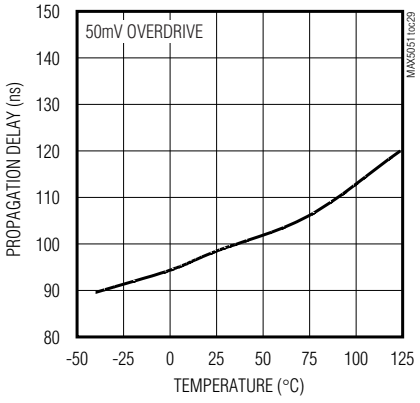
## Typical Operating Characteristics (continued)

($V_{AVIN}$ = $V_{PVIN}$ = 12V, $V_{UVLO}$ = $V_{STT}$ = 3V, $V_{CON}$ = 3V, $R_{RCOSC}$ = 24kΩ, $C_{CSS}$ = 10nF, $C_{RCOSC}$ = 100pF, $C_{REG9}$ = 4.7µF, $C_{REG5}$ = 4.7µF, $T_A$ = +25°C, unless otherwise noted.)

**CON TO DRVL PROPAGATION DELAY vs. TEMPERATURE**




**CS CURRENT LIMIT TO DRVH PROPAGATION DELAY vs. TEMPERATURE**




## Pin Description

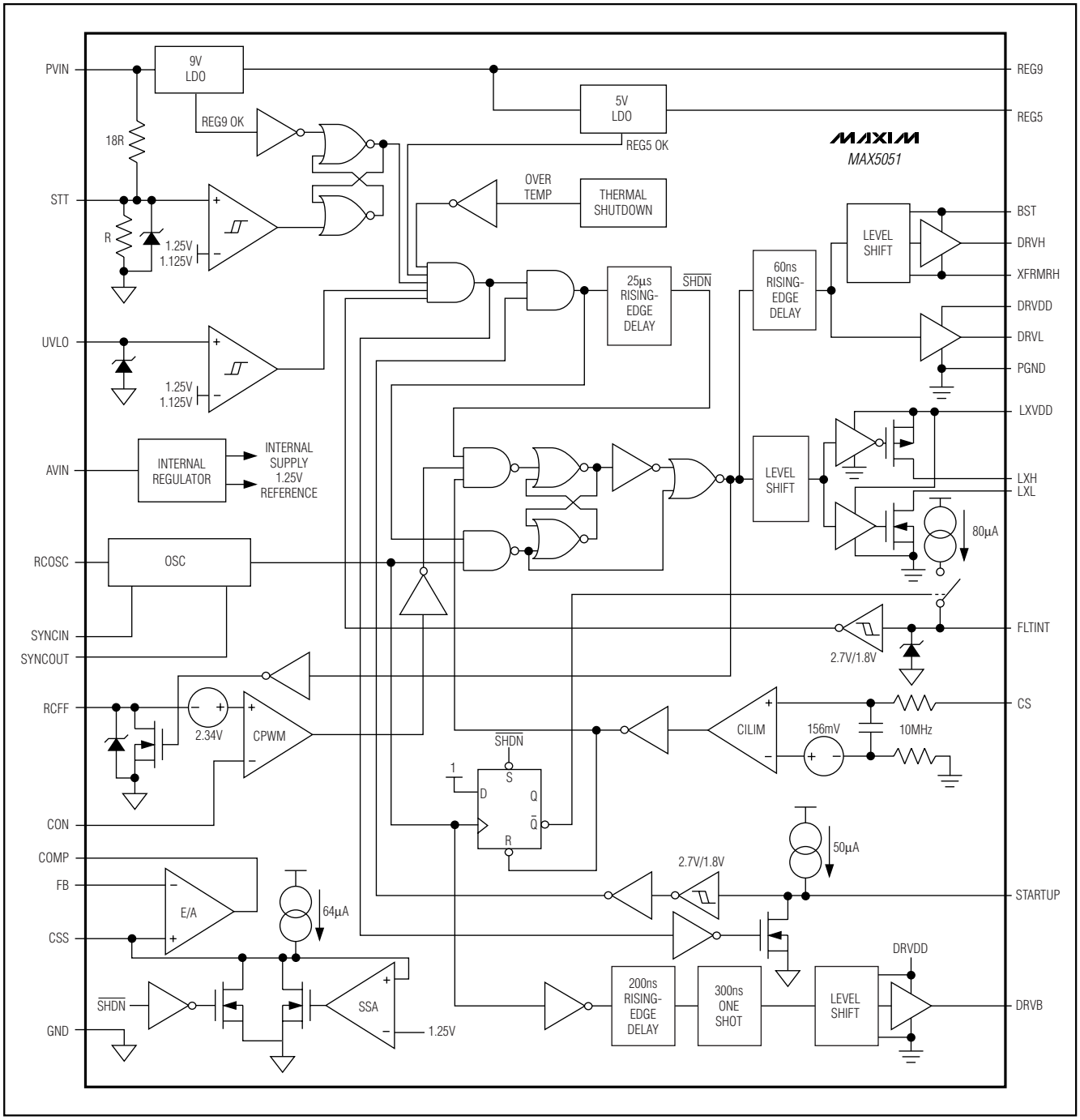
| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | RCOSC | Oscillator Frequency Set Input. Connect a resistor from RCOSC to REG5 and a capacitor from RCOSC to GND to set the oscillator frequency. Switching frequency is 1/2 the frequency of the sawtooth signal at RCOSC. |
| 2 | SYNCOUT | Synchronization Output. Synchronization signal to drive SYNCIN of a second MAX5051, if used. |
| 3 | RCFF | Feed-Forward Input. Connect a resistor from RCFF to AVIN and a capacitor from RCFF to GND. This is the PWM ramp. |
| 4 | CON | PWM Comparator Noninverting Input. Connect CON to the optocoupler output for isolated applications, or to COMP for nonisolated applications. |
| 5 | CSS | Soft-Start and Reference. Connect a 0.01µF or greater capacitor from CSS to GND. The 1.24V reference voltage appears across this capacitor. |
| 6 | COMP | Internal Error Amplifier Output |
| 7 | FB | Feedback Input. Inverting input of the internal error amplifier. The soft-started reference is connected to the noninverting input of this amplifier. |
| 8 | REG5 | 5V Linear Regulator Output. Bypass REG5 to GND with a 4.7µF ceramic capacitor. |
| 9 | REG9 | 9V Linear Regulator Output. Bypass REG9 to GND with a 4.7µF ceramic capacitor. |
| 10 | PVIN | Regulator Voltage Input. Voltage input to the internal 5V and 9V linear regulators. A high-value resistor connected from the input supply to PVIN provides the necessary current to charge up the startup capacitor, and the 400µA standby current required by the MAX5051. After startup, the output of a tertiary winding is used to provide continued bias to the controller. |
| 11 | STT | Startup Threshold Input. Leave STT floating for a default startup voltage of 24V at PVIN. STT can be modified by connecting external resistors. For high accuracy, choose external resistors with 50kΩ or less impedance looking back into the divider. |
| 12 | LXVDD | Supply Input for the Secondary-Side Synchronous Pulse Transformer or Optocoupler Driver. LXVDD is normally connected to REG5. |

# Parallelable, Clamped Two-Switch Power-Supply Controller IC

## Pin Description (continued)

| PIN | NAME | FUNCTION |
|---|---|---|
| 13 | LXH | Synchronous-Pulse Transformer Driver, PMOS Open Drain. LXH is the high-side driver for the secondary-side synchronous-pulse transformer. LXH can also drive a high-speed switching optocoupler. If not used, connect LXH to LXVDD. |
| 14 | LXL | Synchronous-Pulse Transformer Driver, NMOS Open Drain. LXL is the low-side driver for the secondary-side synchronous-pulse transformer. LXL can also drive a high-speed switching optocoupler. If not used, connect LXL to PGND. |
| 15 | CS | Current-Sense Input. The current-limit threshold is internally set to 156mV relative to PGND. The device has an internal noise filter. If necessary, connect an additional external RC filter. |
| 16 | DRVL | Gate-Drive Output for Low-Side MOSFET. DRVL is capable of sourcing and sinking approximately 2A peak current. |
| 17 | PGND | Power Ground |
| 18 | DRVDD | Supply Input for Low-Side MOSFET Driver. Bypass DRVDD locally with good quality 1µF ll 0.1µF ceramic capacitors. DRVDD is normally connected to REG9. |
| 19 | DRVB | Gate-Drive Output for Boost MOSFET. Connect the gate of a small high-voltage external FET to this pin to enable charging of the high-side boost capacitor connected between pins 20 and 22. This FET may be necessary to keep the boost capacitor charged at light loads. |
| 20 | XFRMRH | Transformer Input. Transformer primary high-side connection. |
| 21 | DRVH | Gate-Drive Output for High-Side MOSFET |
| 22 | BST | Boost Input. Boost supply connection point for the high-side MOSFET driver. Connect at least a 1µF ll 0.1µF ceramic capacitor from BST to XFRMRH with short and wide PC board traces. If the voltage across the boost capacitor falls below the high-side undervoltage lockout threshold, the DRVH output stops switching. |
| 23 | AVIN | Supply Voltage Input. Connect AVIN directly to the input supply line. |
| 24 | GND | Analog Signal Ground |
| 25 | UVLO | Undervoltage Lockout Input. An external voltage-divider from the input supply sets the startup voltage; the threshold is 1.24V with 130mV hysteresis. UVLO can also be used as a shutdown input. If unused, connect UVLO to REG5 |
| 26 | STARTUP | Startup Input. STARTUP coordinates simultaneous startup of multiple units from faults, during initial turn-on, and UVLO recovery. When paralleling the secondaries of two MAX5051's, the STARTUP inputs of each device must be connected together. |
| 27 | FLTINT | Fault Integration Input. During persistent current-limit faults, a capacitor connected to FLTINT is charged with an internal 90µA current source. Switching is terminated when the voltage reaches 2.9V. An external resistor connected in parallel discharges the capacitor. Switching resumes when the voltage drops to 2V. |
| 28 | SYNCIN | Synchronization Input. SYNCIN accepts the synchronization signal from SYNCOUT of another MAX5051 and shifts the switching of the synchronized unit by 180° allowing the reduction of input bypass capacitors. The MAX5051 switches at the same frequency at SYNCIN. SYNCIN must be 50% duty cycle. Leave SYNCIN floating if unused. |

## Functional Diagram



# Parallelable, Clamped Two-Switch Power-Supply Controller IC

## Detailed Description

The MAX5051 controller IC is designed for two-switch forward converter power-supply topologies. It incorporates an advanced set of protection features that makes it uniquely suitable when high reliability and comprehensive fault protection are required, as in power supplies intended for telecommunication equipment. The device operates over a wide 11V to 76V supply range. By using the MAX5051 with a secondary-side synchronous rectifier circuit, a very efficient low output voltage and high output-current power supply can be designed.

In a typical application, the AVIN pin is connected directly to the input supply. The PVIN pin is connected to the input supply through a bleed resistor. This is used to charge up a reservoir capacitor. When the voltage across this capacitor reaches approximately 24V, then primary switching commences. If the tertiary winding is able to supply bias to the IC, then self boot-strapping takes place and operation continues normally. If the voltage across the reservoir capacitor connected to PVIN falls below 6.2V, then switching stops and the capacitor starts charging up again until the voltage across it reaches 24V.

This device incorporates synchronization circuitry, enabling the direct paralleling of two devices for higher output power and lower input ripple current. Using a single pin, the circuitry synchronizes and shifts the phase of the second device by 180°. To enable simultaneous wakeup and shutdown, a STARTUP pin is provided. Connect all the STARTUP pins of all MAX5051 devices together to facilitate parallel operation in the primary side. When each power supply generates different output voltages, connecting the STARTUP pins is not necessary.

### Power Topology

The two-switch forward-converter topology offers outstanding robustness against faults and transformer saturation while allowing the use of SO-8 power MOSFETs with a voltage rating equal to only that of the input supply voltage.

Voltage-mode control with feed-forward compensation allows the rejection of input supply disturbances within a single cycle, similar to that of current-mode controlled topologies. This control method offers some significant benefits not possible with current-mode control. These benefits are:

- No minimum duty-cycle requirement because of current-signal blanking;
- Clean modulator ramp and higher amplitude for increased stability;
- Stable operating current of the optocoupler LED and phototransistor for maximized control-loop bandwidth (in current-mode applications, the optocoupler bias point is output-load dependent);
- Predictable loop dynamics simplifying the design of the control loop.

The two-switch power topology has the added benefit of recovering practically all magnetizing as well as the leakage energy stored in the parasitics of the isolation transformer. The lower clamped voltages on the primary power FETs allow for the use of low $R_{DS(ON)}$ devices. Figure 2 shows the schematic diagram of a 48V input 3.3V/10A output power supply built around the MAX5051.

### MOSFET Drivers

The MAX5051's integrated high- and low-side MOSFET drivers source and sink up to 2A of peak currents, resulting in very low losses even when switching high gate charge MOSFETs. The high-side gate driver requires its own bypass capacitor connected between BST and XFRMRH. Use high-quality ceramic capacitors close to these two pins for bypass. Under normal operating conditions, the energy stored in the transformer parasitics swings the XFRMRH pin to ground while the transformer is resetting. During this time, the charge on the boost capacitor connected to the BST pin is replenished. However, under certain conditions, such as when the magnetizing inductance of the transformer is very high or when using conventional rectification at the output, the duty cycle with light loads may become very small. Thus, the energy stored could be insufficient to swing XFRMRH to ground and replenish the boost capacitor. Figure 3 shows the equivalent circuit during the magnetizing inductance reset interval, assuming synchronous rectification where the output inductor is not allowed to run discontinuous.

If the magnetizing inductance is kept below the following minimum, then the boost capacitor charge will not deplete:

$$L_M \le 0.294 \; d^2 \frac{V_{IN}}{f_S^2 \; Qg_{total} + (0.005A) \; f_S}$$

where d is the duty cycle, $V_{IN}$ is the input voltage, $f_S$ is the switching frequency, and $Q_{gtotal}$ is the total gate charge for the high-side MOSFET. The above formula is only an approximation; the actual value will depend on other parasitics as well.

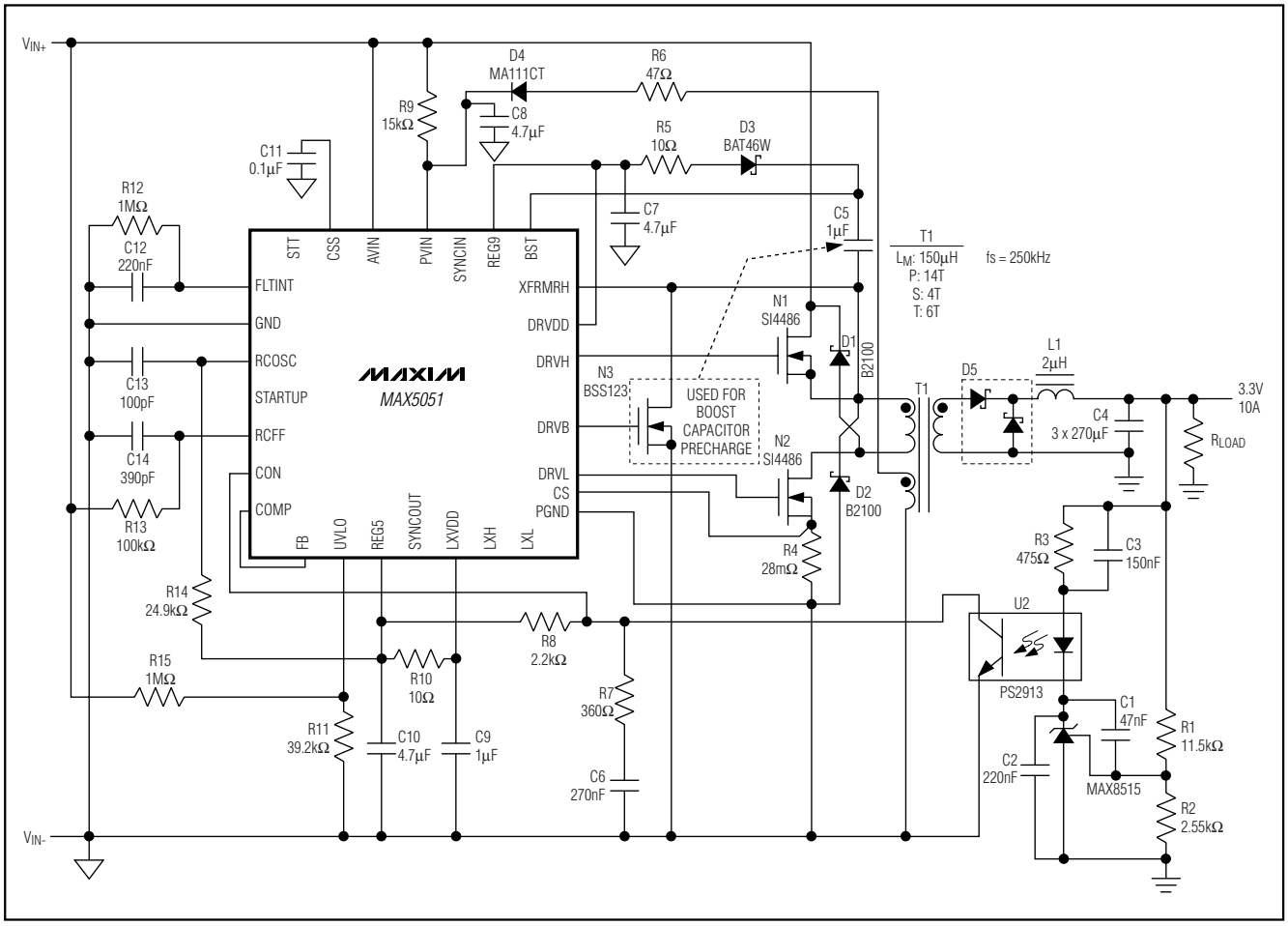



*Figure 2. Typical Application Circuit*

If the charge stored on the boost capacitor is not adequately replenished then the gate-driver lockout for the high-side MOSFET is triggered, stopping the high side from switching. The low side continues switching, eventually recharging the capacitor, at which point the high side starts switching again. To prevent this behavior, use the boost capacitor's cycle-by-cycle charging circuit to prevent unwanted shutdowns of the high side (Figure 2). Connect the gate of a small high-voltage FET (with the same voltage rating or higher as the main FETs) to the DRVB output of the MAX5051. Connect the drain of this FET to XFRMRH, and connect the source to the primary ground. DRVB will briefly (300ns) turn this FET ON every cycle after the main PWM clock terminates. This allows the boost capacitor to be replenished under all conditions, even when switching stops completely. A suitable FET for this is BSS123 or equivalent (100V, 170mA rated). The boost-capacitor charge

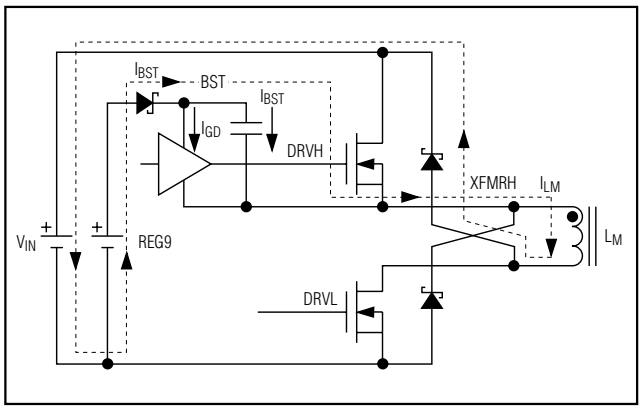



*Figure 3. Boost Capacitor Charging Path During Transformer Reset*

# Parallelable, Clamped Two-Switch Power-Supply Controller IC

diode is a high-voltage, small-signal Schottky type. It may be helpful to connect a resistor in series with this diode to minimize noise as well as reduce the peak charging currents. As in any other switching power-supply circuit, the gate-drive loops must be kept to a minimum. Plan PC board layout with the critical current carrying loops of the circuit as a starting point.

### Secondary-Side Synchronization

The MAX5051 has additional (LXH and LXL) outputs to make the driving of secondary-side synchronous rectifiers possible with a signal from the primary. These signals lead in time, the actual gate drive applied to the main power FETs, and allow the secondary-side synchronous FETs to be commutated in advance of the power pulse. The synchronizing pulse is generated approximately 90ns ahead of the main pulse that drives the two power FETs.

Synchronization is accomplished by connecting a small pulse transformer between LXH and LXL, along with some clamp diodes (D1 and D2 in Figure 4). This is a small integrated two-switch driver configuration that allows for full recovery of the stored energy in the magnetizing inductance of the pulse transformer, thereby significantly reducing the running bias current of the controller. It also allows for correct transfer of DC levels without requiring series capacitors with large time constants, assuring correct drive levels for the secondary circuit.

Select a pulse transformer, T1, so the current buildup in its magnetizing inductance is low enough not to create a significant voltage droop across the internal driver FETs. Use the following formula to calculate the approximate value of the primary magnetizing inductance of T1:

$$2.5\ \frac{R_{dsLXH}+R_{dsLXL}}{f_S} \le L_M \le \frac{t_S}{16\ C_{ds}\ f_S}$$

where $R_{dsLXH}$ and $R_{dsLXL}$ are the internal high- and low-side pulse transformer driver on-resistances, $f_S$ is the switching frequency, $L_M$ is the pulse transformer primary magnetizing inductance, $t_S$ is the transition time at the drains of these FETs (typically < 40ns), and $C_{ds}$ is the total drain-source capacitance (approximately 10pF).

Alternatively, a high-speed optocoupler (Figure 5) can be used instead of the pulse transformer. The look-ahead pulse accommodates the propagation delays of the high-speed optocoupler as well as the delays through the gate drivers of the secondary-side FETs. Choose optocouplers with propagation delays of less than 50ns.

### Error Amplifier And Reference Soft-Start

The error amplifier in the MAX5051 has an uncommitted inverting input (FB) and output (COMP). Use this amplifier when secondary isolation is not required. COMP can then be directly connected to CON (the input of the PWM comparator). The noninverting input of the error amplifier is connected to the soft-start generator and is also available externally at CSS. A capacitor connected to CSS is slewed linearly during initial startup with the 70µA internal current source (see Figure 2). This provides a linearly increasing reference to the noninverting input of the error amplifier forcing the output voltage also to slew proportionally. This method of soft-start is superior to other methods because the loop is always

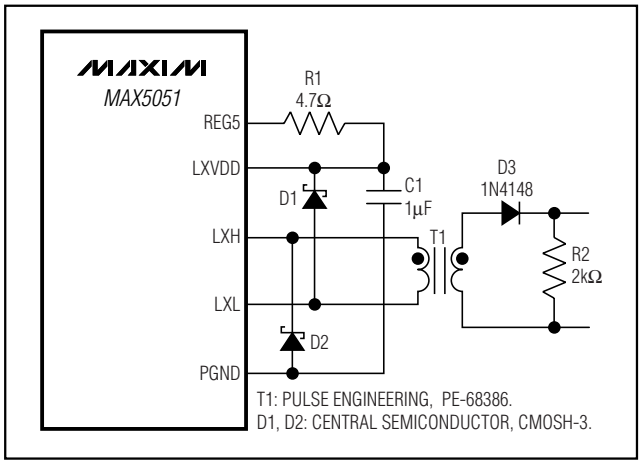



*Figure 4. Secondary-Side Synchronous Rectifier Driver Using Pulse Transformer*

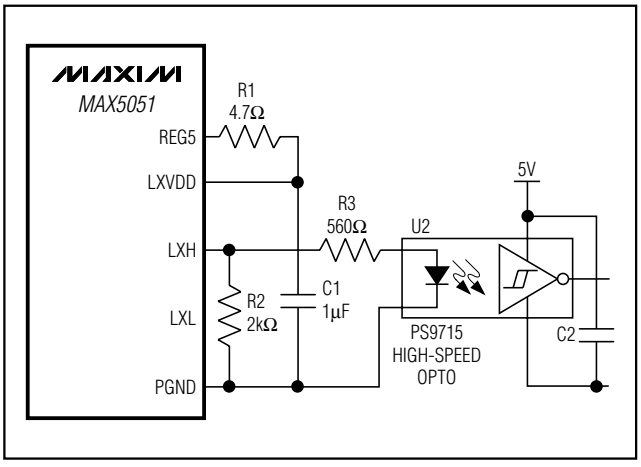



*Figure 5. Secondary-Side Synchronous Rectifier Driver Using High-Speed Optocoupler*

in control. Thus, the output-voltage slew rate is constant at light or heavy loads. Once the soft-start ends, the voltage on CSS regulates to 1.24V. Do not load CSS with external circuitry. A suitable range of capacitors connected to CSS is from 10nF to 0.1µF. Calculate the required soft-start capacitor based on the total output-voltage startup time as follows:

$$C_{CSS} = 56\mu F/s \times t_{SS}$$

where $C_{CSS}$ is the capacitor connected to CSS, $t_{SS}$ is the soft-start time required for the output voltage to rise from 0V to the rated output voltage. This only applies when this amplifier is used for output voltage regulation.

### PWM Ramp

The PWM ramp is generated at RCFF. Connect a capacitor $C_{RCFF}$ from RCFF to ground and a resistor $R_{RCFF}$ from RCFF to AVIN. The ramp generated on RCFF is internally offset by 2.3V and applied to the non-inverting input of the PWM comparator. The slope of the ramp is part of the overall loop gain. The dynamic range of RCFF is 0 to 3V, and so the ramp peak must be kept below that. Assuming the maximum duty cycle approaches 50% at minimum input voltage, use the following formula to calculate the minimum value of either the ramp capacitor or resistor:

$$R_{RCFF} C_{RCFF} \geq \frac{V_{INUVLO}}{2 f_S V_{RPP}}$$

where $V_{INUVLO}$ is the minimum input supply voltage (typically the PWM UVLO turn-on voltage), $f_S$ is the switching frequency, and $V_{RPP}$ is the peak-to-peak ramp voltage, typically 2V.

Allow the ramp peak to be as high as possible to maximize the signal-to-noise ratio. The low-frequency small-signal gain of the power stage, Gps (the gain from the inverting input of the PWM comparator to the output) can be calculated by using the following formula:

$$G_{ps} = N_{sp} R_{RCFF} C_{RCFF} f_s$$

where $N_{sp}$ is the secondary-to-primary power transformer turns ratio.

### Internal Regulators

The MAX5051 has two internal linear regulators that are used to power internal and external control circuits. The 9V regulator, REG9, is primarily used to power the high- and low-side gate drivers. Bypass REG9 with a 4.7µF ceramic capacitor or any other high-quality capacitor; use low-value ceramics in parallel as necessary. A 5V regulator also is provided, REG5, primarily used to bias the internal circuitry of the MAX5051. Bypass REG5 with a 4.7µF ceramic capacitor similar to the one used for REG9. Both of these regulators are always powered. When using bootstrapped startup through a bleed resistor, do not load these outputs while the MAX5051 is in standby as it may fail to start. Any external loading to this output should be such that the sum of their load and the standby current through PVIN of the MAX5051 is less than the current that the bleed resistor can supply.

### Startup Modes

The MAX5051 can be configured for two different startup modes, allowing operation in either bootstrapped or direct power mode.

#### Direct Power Mode

In direct power mode, AVIN and PVIN are connected directly to the input supply. This is typical in 12V to 24V systems. The undervoltage lockout set at STT needs to be adjusted down with an external resistor-divider to an appropriate level.

#### Bootstrapped Startup

In bootstrap mode, a resistor is connected from the input supply to PVIN, where a capacitor to GND is charged towards the input supply. When this voltage reaches the startup threshold, the device wakes up and begins switching. A tertiary winding from the transformer is then used to sustain operation. The MAX5051 draws little current from PVIN before reaching the threshold, which allows a large-value bootstrap resistor and reduces its power dissipation after startup. A large startup hysteresis helps the design of the bootstrap circuit by providing longer running times during startup.

After coming out of standby and before initiating the soft-start, the MAX5051 turns on the low-side FET to charge up the boost capacitor. A voltage detector has been incorporated in the high-side driver that prevents the high-side switch from turning on with insufficient voltage. It is also used to indicate when the boost capacitor has been charged. Once the capacitor is charged, soft-start commences. If the duty cycle is low, the magnetizing energy in the transformer may be insufficient to keep the bootstrap capacitor charged. DRVB (see Figure 2 dotted lines) has been provided to drive a small external FET connected between XFRMRH and PGND, and is pulsed every cycle to keep the capacitor charged.

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Normally PVIN is derived from a tertiary winding of the transformer. However, at startup there is no energy delivered through the transformer, hence, a special bootstrap sequence is required. Figure 6 shows the voltages on PVIN, REG9, and REG5 during startup. Initially, PVIN, REG9, and REG5 are 0V. After the input voltage is applied, C21 (Figure 8) charges PVIN through the startup resistor, R22, to an intermediate voltage. At this point, the internal regulators begin charging C3 and C4. The MAX5051 uses only 400µA (typ) of the current supplied by R22, and the remaining current charges C21, C3, and C4. The charging of C4 and C3 stops when their voltages reach approximately 5V and 9V, respectively, while PVIN continues rising until it reaches the wakeup level of 24V. Once PVIN exceeds this wakeup level, switching of the external MOSFETs begins and energy is transferred to the secondary and tertiary outputs. When the voltage on the tertiary output builds to higher than 9V, startup has been accomplished and operation is sustained. However, if REG9 drops below 6.2V (typ) before startup is complete, the device goes back into standby. In this case, increase the value of C21 to store enough energy allowing for voltage buildup at the tertiary winding.

### Startup Time Considerations

The PVIN bypass capacitor, C21, supplies current immediately after wakeup (see Figure 8). The size of C21 and the connection of the tertiary winding determine the number of cycles available for startup. Large values of C21 increase the startup time and supply gate charge for more cycles during initial startup. If the value of C21 is too small, REG9 drops below 6.2V because the MOSFETs did not have enough time to switch and build up sufficient voltage across the tertiary output to power the device. The device goes back into standby and will not attempt to restart until PVIN rises above 24V. Use a low-leakage capacitor for C21, C3, and C4 (see Figure 8). Generally, power supplies keep typical startup times to less than 500ms even in low-line conditions (36VDC for telecom applications). Size the startup resistor, R22 (Figure 8) to supply both the maximum startup bias of the device and the charging current for C21, C3, and C4.

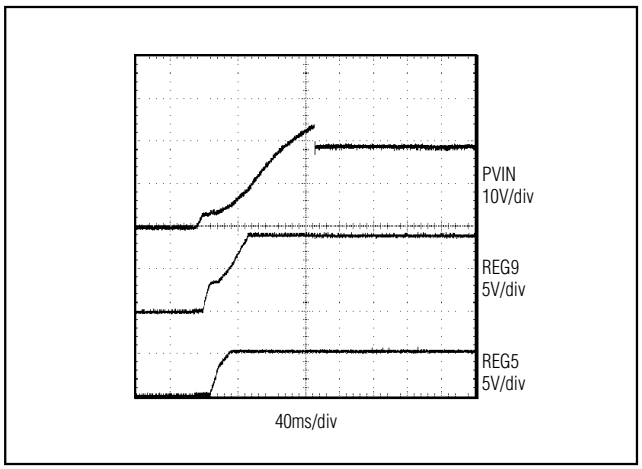



*Figure 6. PVIN, REG5, and REG9 During Startup in Bootstrapped Mode*

### Oscillator and Synchronization

The MAX5051 oscillator is externally programmable through a resistor and capacitor connected to RCOSC. The PWM frequency will be 1/2 the frequency at RCOSC with a 50% duty cycle, and is available at SYNCOUT. The maximum duty cycle is limited to < 50% by a 60ns internal blanking circuit in the power drivers in addition to the gate and driver delays.

Use the following formula to calculate the oscillator components:

$$R_{RCOSC} \cong \frac{1}{2f_S (C_{RCOSC} + C_{PCB}) \ln\left(\frac{REG5}{REG5 - V_{TH}}\right)}$$

where $C_{PCB}$ is the stray capacitance on the PC board (about 14pF), REG5 = 5V, $V_{TH}$ is the RCOSC peak trip level, and $f_S$ is the switching frequency.

The MAX5051 contains circuitry that allows it to be synchronized to an external clock whose duty cycle is 50%. For proper synchronization, the frequency of this clock should be 15% to 20% higher than half the RCOSC frequency of the MAX5051's internal oscillator. This is because the external source SYNCIN directly drives the power stage, whereas the internal clock is divided by two. The synchronization feature in the MAX5051 has been designed primarily for two devices connected to the same power source with a short physical distance between the two circuits. Under these circumstances, the SYNCOUT from one of the circuits can be connected to the SYNCIN of the other one; this forces the power cycle of the second unit to be 180° out-of-phase. To synchronize a second MAX5051, feed the SYNCOUT of the first device to the SYNCIN of the second device. If necessary, many devices can be daisy-chained in this manner. Each device will then have 180° phase difference from the device that drives it.

### Integrating Fault Protection

The integrating fault protection feature allows transient overcurrent conditions to be ignored for a programmable amount of time, giving the power supply time to behave like a current source to the load. This can happen, for example, under load-current transients when the control loop requests maximum current to keep the output voltage from going out of regulation. The fault integration time can be programmed externally by connecting a suitably sized capacitor to the FLTINT pin. Under sustained overcurrent faults, the voltage across this capacitor is allowed to ramp up towards the FLTINT shutdown threshold (2.9V, typ). Once the threshold is reached, the power supply shuts down. A high-value bleed resistor connected in parallel with the FLTINT capacitor allows it to discharge towards the restart threshold (1.8V, typ). Once this threshold is reached, the supply restarts with a new soft-started cycle.

Note that cycle-by-cycle current limiting is provided at all times by CS with a threshold of 154mV (typ). The fault integration circuit works by forcing a 90µA current out of FLTINT every time that the current-limit comparator (Figure 1, CILIM) is tripped. Use the following formula to calculate the value of the capacitor necessary for the desired shutdown time of this circuit.

$$C_{FLTINT} = \frac{I_{FLTINT} \ t_{SH}}{0.9V}$$

where $I_{FLTINT}$ = 90µA, $t_{SH}$ is the desired fault integration time after the first shutdown cycle during which current-limit events from the current-limit comparator are ignored. For example, a 0.1µF capacitor gives a fault integration time of 2.25ms.

Some testing may be required to fine-tune the actual value of the capacitor. To calculate the required bleed resistance $R_{FLTINT}$, use the following formula:

$$R_{FLTINT} = \frac{t_{RT}}{0.372 \times C_{FLTINT}}$$

where $t_{RT}$ is the desired recovery time.

Typically choose $t_{RT}$ = 10 x $t_{SH}$. Typical values for $t_{SH}$ range from a few hundred microseconds to a few milliseconds.

### Synchronizing Primary-Side STARTUP For Parallel Operation

Figure 7 shows the connection diagram of two or more MAX5051s for synchronized primary-side operation. The common connection of STARTUP ensures all paralleled modules wakeup and shutdown in tandem. This helps prevent startup conflicts when the secondaries of the power supplies are paralleled. Connecting SYNCOUT to SYNCIN is not necessary; however, when used, this minimizes the ripple current though the input bypass capacitors.

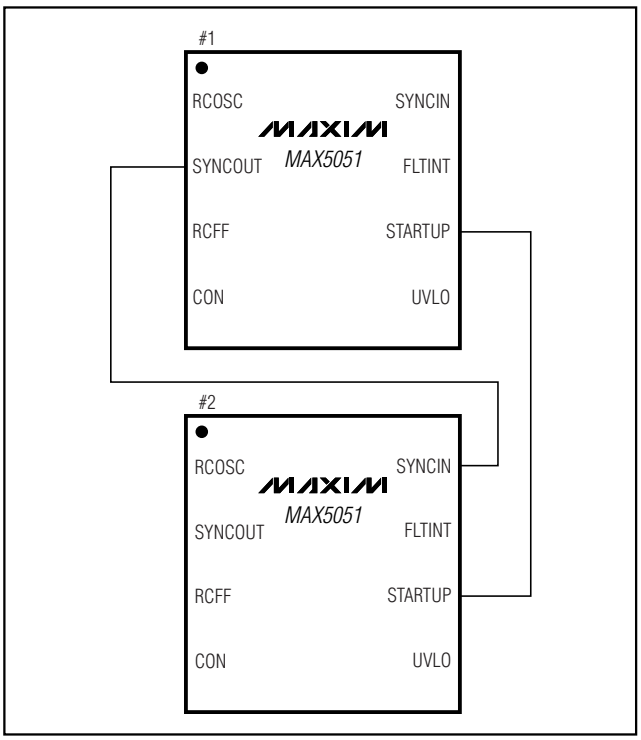



*Figure 7. Connection for Synchronized STARTUP of Two or More MAX5051s*

## Applications Information

### Isolated Telecom Power Supply

Figure 8 shows a complete design of an isolated synchronously rectified power supply with a 36V to 72V telecom voltage range. This power supply is fully protected and can sustain a continuous short circuit at its output terminals. Figures 9 though 14 show some of the performance aspects of this power-supply design. This circuit is available as a completely built and tested evaluation kit.

# Parallelable, Clamped Two-Switch Power-Supply Controller IC

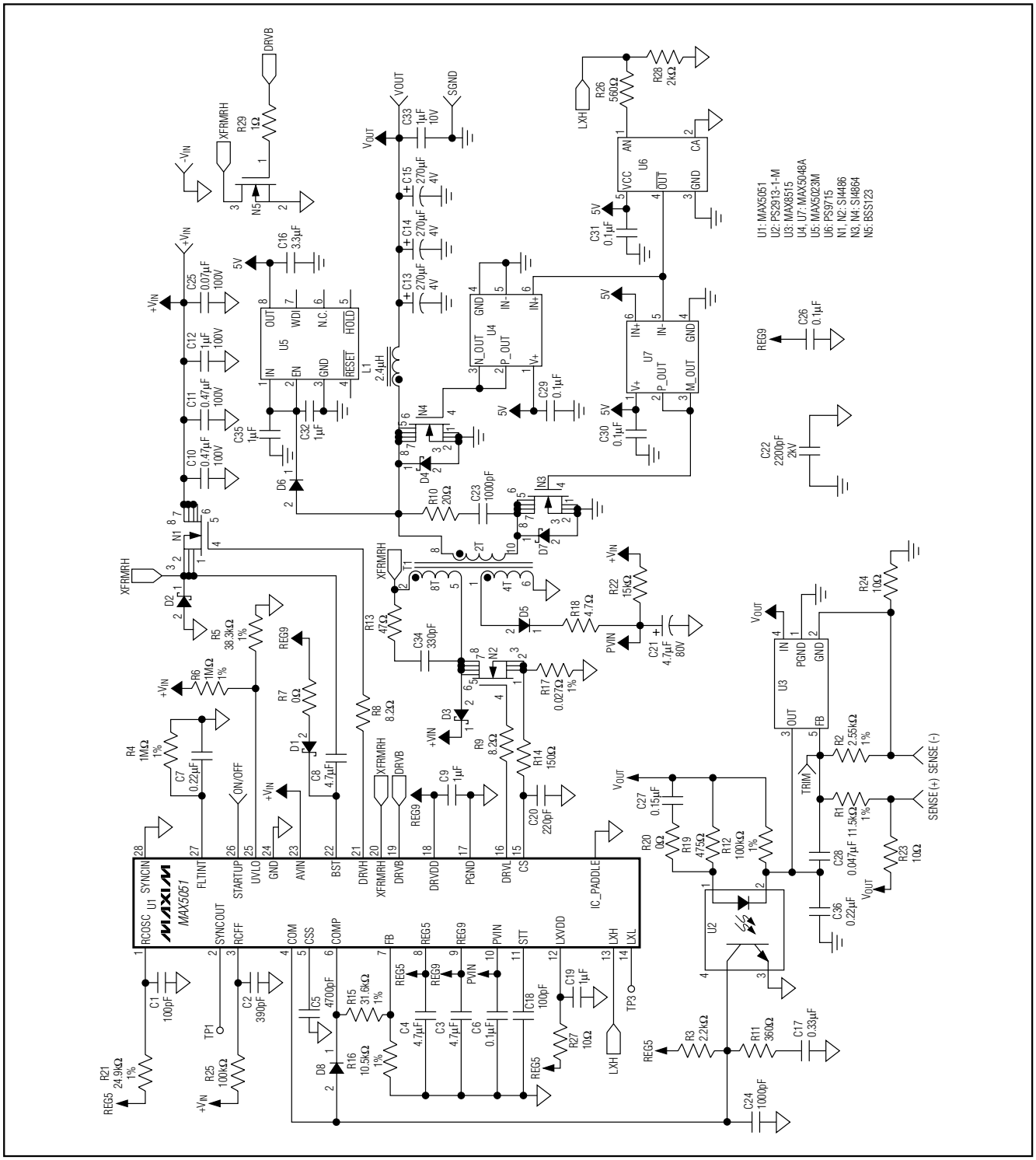



*Figure 8. Schematic of a 48V Input 3.3V at 15A Output Synchronously Rectified, Isolated Power Supply*

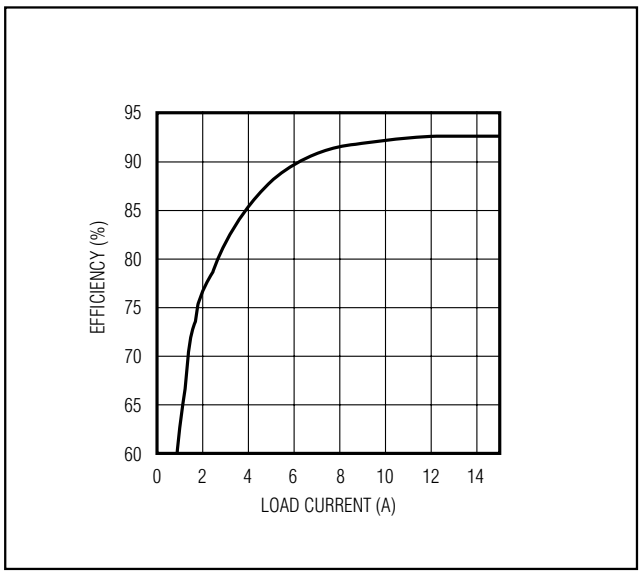



*Figure 9. Efficiency at Nominal Output Voltage vs. Load Current 48V Nominal Input Voltage*

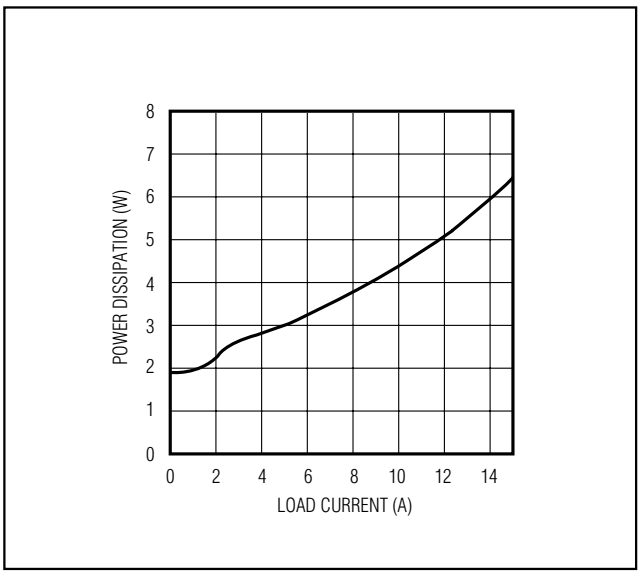



*Figure 10. Power Dissipation at Nominal Output Voltage vs. Load Current for 48V Input Voltage.*

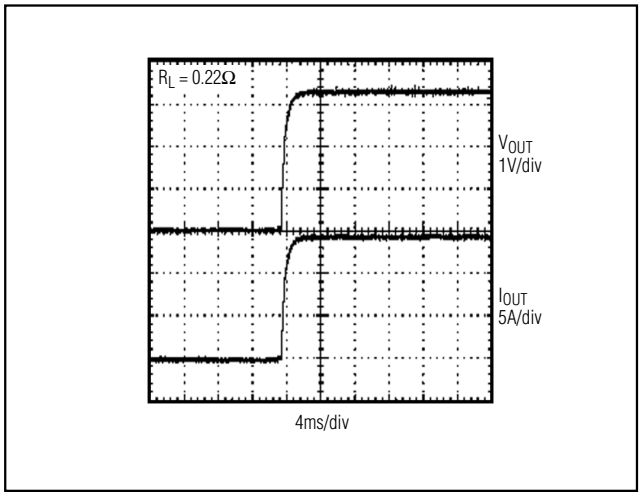



*Figure 11. Turn-On Transient at Full Load (Resistive Load)*

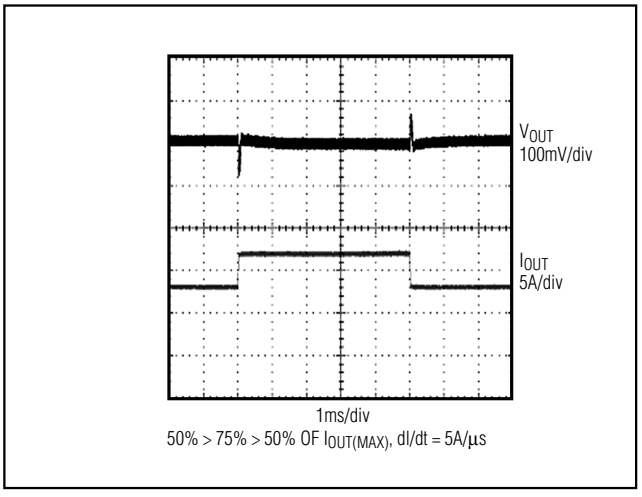



*Figure 12. Output Voltage Response to Step-Change in Load Current*

# Parallelable, Clamped Two-Switch Power-Supply Controller IC

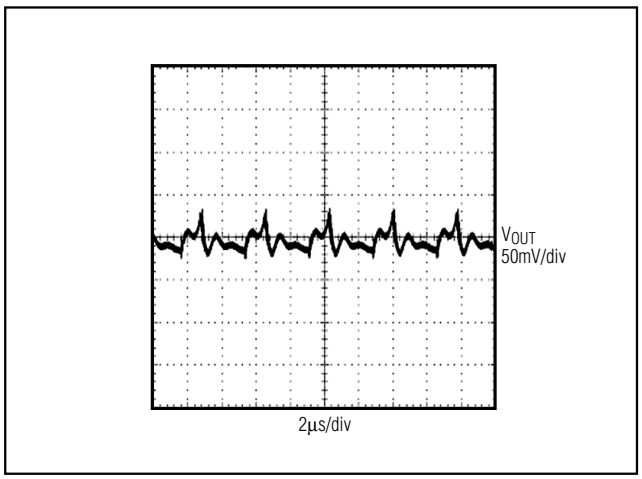



*Figure 13. Output Voltage Ripple At Nominal Input Voltage and Full Load Current (Scope Bandwidth = 20MHz)*

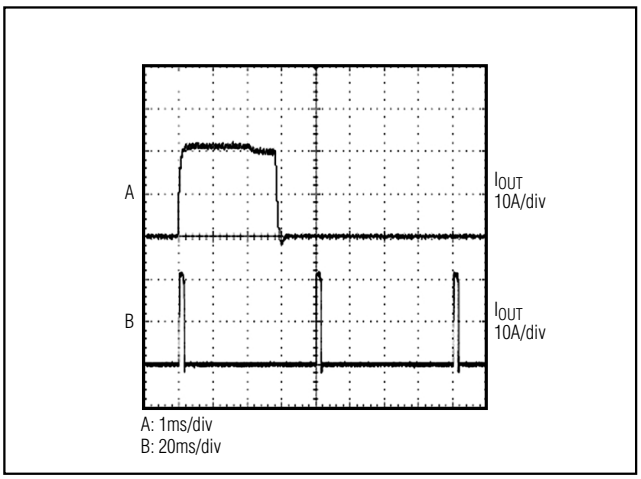
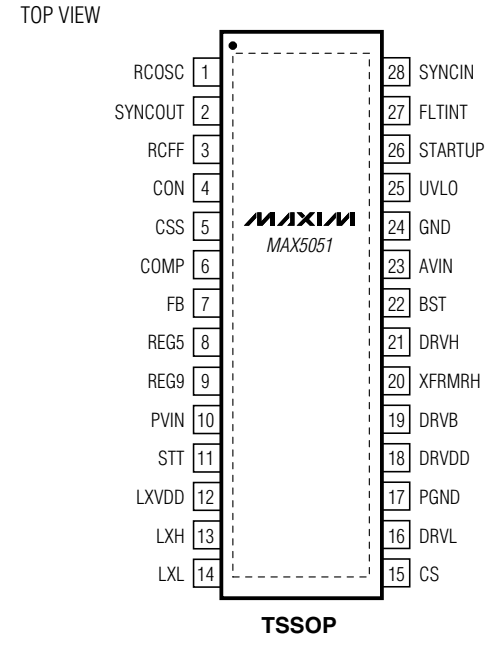



*Figure 14. Load Current (10A/div) as a Function of Time When the Converter Attempts to Turn On into a 50mΩ Short Circuit*

## Pin Configuration




**TSSOP**

EXPOSED PADDLE IS INTERNALLY CONNECTED TO GND.

## Chip Information

TRANSISTOR COUNT: 2049

PROCESS: BiCMOS/DMOS

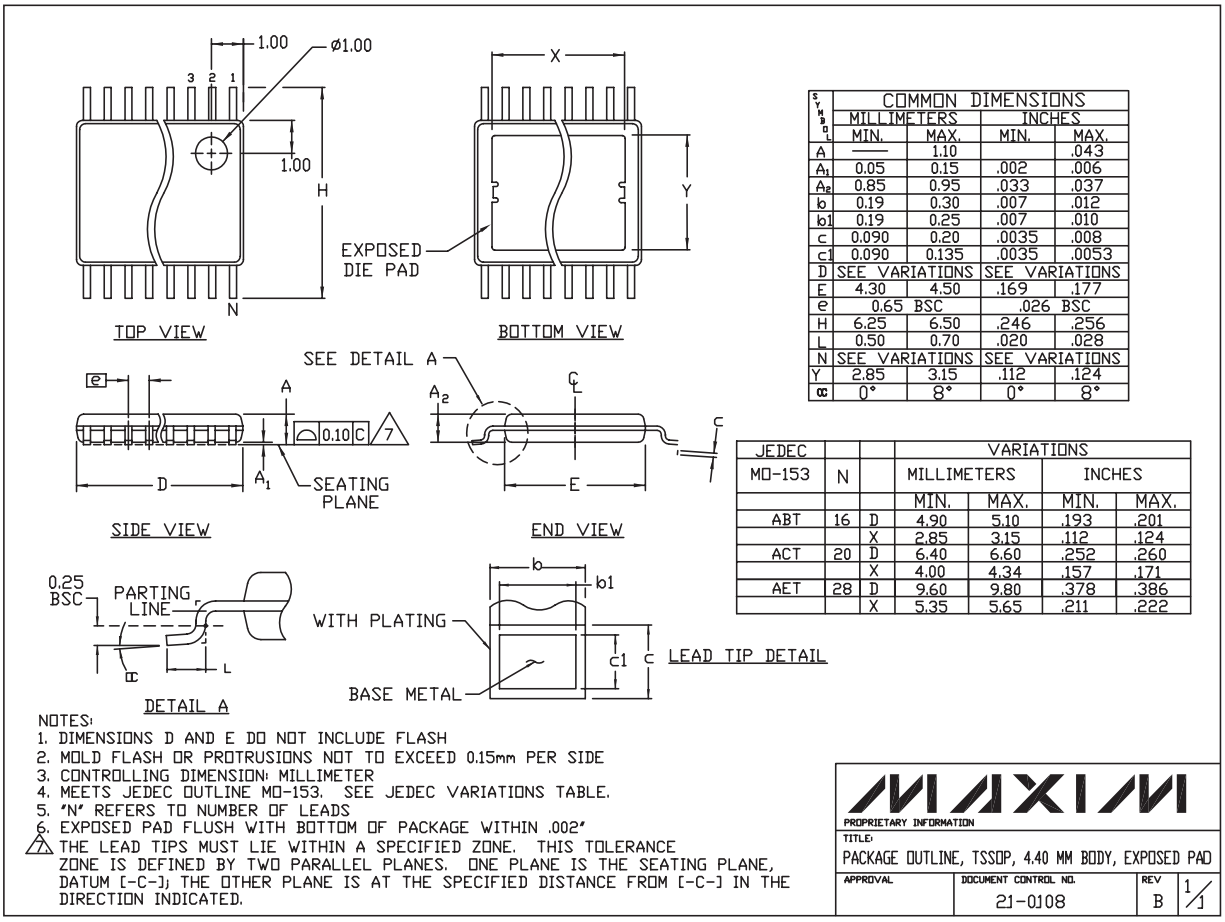
Exposed Paddle Connected to GND

# Parallelable, Clamped Two-Switch Power-Supply Controller IC

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP 4.4mm BODY.EPS




| SYMBOL | COMMON DIMENSIONS | | | |
|---|---|---|---|---|
| | MILLIMETERS | | INCHES | |
| | MIN. | MAX. | MIN. | MAX. |
| A | ——— | 1.10 | | .043 |
| $A_1$ | 0.05 | 0.15 | .002 | .006 |
| $A_2$ | 0.85 | 0.95 | .033 | .037 |
| b | 0.19 | 0.30 | .007 | .012 |
| b1 | 0.19 | 0.25 | .007 | .010 |
| c | 0.090 | 0.20 | .0035 | .008 |
| c1 | 0.090 | 0.135 | .0035 | .0053 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 4.30 | 4.50 | .169 | .177 |
| e | 0.65 BSC | | .026 BSC | |
| H | 6.25 | 6.50 | .246 | .256 |
| L | 0.50 | 0.70 | .020 | .028 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| Y | 2.85 | 3.15 | .112 | .124 |
| α | 0° | 8° | 0° | 8° |

| JEDEC | | | VARIATIONS | | | |
|---|---|---|---|---|---|---|
| MO-153 | N | | MILLIMETERS | | INCHES | |
| | | | MIN. | MAX. | MIN. | MAX. |
| ABT | 16 | D | 4.90 | 5.10 | .193 | .201 |
| | | X | 2.85 | 3.15 | .112 | .124 |
| ACT | 20 | D | 6.40 | 6.60 | .252 | .260 |
| | | X | 4.00 | 4.34 | .157 | .171 |
| AET | 28 | D | 9.60 | 9.80 | .378 | .386 |
| | | X | 5.35 | 5.65 | .211 | .222 |

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
5. "N" REFERS TO NUMBER OF LEADS
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002"
7. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-], THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY, EXPOSED PAD

| APPROVAL | DOCUMENT CONTROL NO. | REV | |
|---|---|---|---|
| | 21-0108 | B | 1/1 |