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19-0021; Rev 2; 1/94

MAXIM

# Quad 8-Bit DACs with Rail-to-Rail Voltage Outputs

MAX505/MAX506

## General Description

The MAX505 and MAX506 are CMOS, quad, 8-bit voltage-output digital-to-analog converters (DACs). The parts operate with a single +5V supply or dual ±5V supplies. Internal, precision output buffers swing rail-to-rail. The reference input range includes both supply rails.

Offset, gain, and linearity are factory calibrated to provide 1LSB total unadjusted error (TUE) over the full operating temperature range.

The MAX505 contains double-buffered logic inputs, which allow all analog outputs to be simultaneously updated using the asynchronous load DAC (LDAC) control signal. The MAX505 also has four separate reference inputs, allowing each DAC's full-scale range to be independently set.

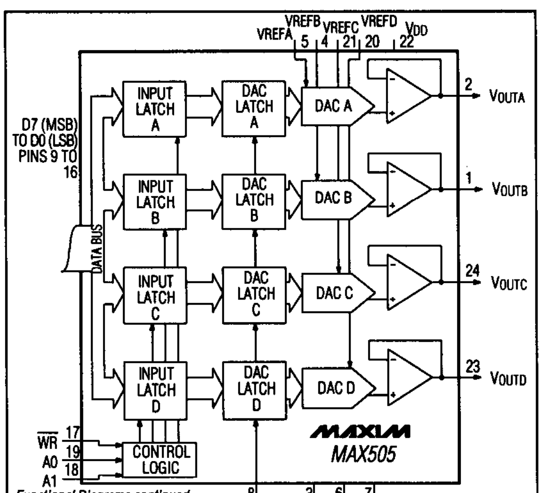
The MAX506 has separate input latches for each of its four DACs. Data is transferred to the input latches from a common 8-bit input port. The DACs are individually selected through address inputs A0 and A1, and updated by bringing WR low. All MAX506 DACs share a common reference input.

All logic inputs are TTL and +5V CMOS compatible.

## Applications

Minimum Component Count Analog Systems
Digital Offset/Gain Adjustment
Arbitrary Function Generators
Industrial Process Control
Automatic Test Equipment
Programmable Attenuators

## Functional Diagrams




Functional Diagrams continued on last page.

## Features

- ♦ Operate from Single +5V Supply or Dual ±5V Supplies
- ♦ Output Buffer Amplifiers Swing Rail-to-Rail
- ♦ Reference Input Range Includes Both Supply Rails
- ♦ Factory-Calibrated for 1LSB TUE
- ♦ Double-Buffered Digital Inputs (MAX505)
- ♦ Microprocessor and TTL/CMOS Compatible
- ♦ Require No External Adjustments
- ♦ Pin-Compatible Upgrades to MX7225/MX7226
- ♦ Now Available in Tiny SSOP Package

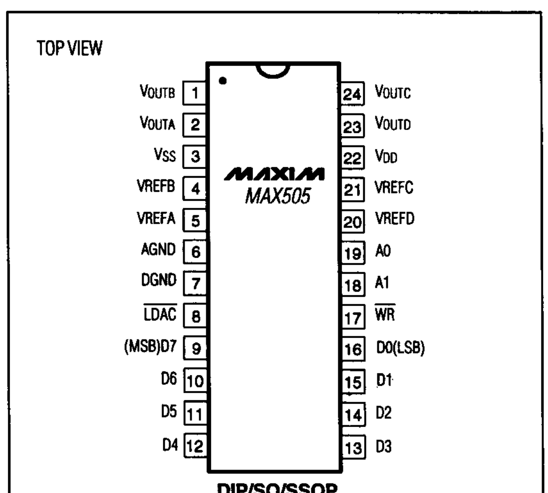
## Ordering Information

| PART | TEMP. RANGE | PIN-PACKAGE | TUE (LSBs) |
|---|---|---|---|
| MAX505ACNG | 0°C to +70°C | 24 Narrow Plastic DIP | ±1 |
| MAX505BCNG | 0°C to +70°C | 24 Narrow Plastic DIP | ±1½ |
| MAX505ACWG | 0°C to +70°C | 24 Wide SO | ±1 |
| MAX505BCWG | 0°C to +70°C | 24 Wide SO | ±1½ |
| MAX505ACAG | 0°C to +70°C | 24 SSOP | ±1 |
| MAX505BCAG | 0°C to +70°C | 24 SSOP | ±1½ |
| MAX505BC/D | 0°C to +70°C | Dice* | ±1½ |

***Ordering Information continued on last page.***

** Contact factory for dice specifications.*
***Contact factory for availability and processing to MIL-STD-883.*

## Pin Configurations




Pin Configurations continued on last page.



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# Quad 8-Bit DACs with Rail-to-Rail Voltage Outputs

## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to AGND .......... -0.3V, +8V
$V_{DD}$ to DGND .......... -0.3V, +6V
$V_{SS}$ to AGND .......... -7V, 0.3V
$V_{SS}$ to DGND .......... -7V, 0.3V
$V_{DD}$ to $V_{SS}$ .......... -0.3V, +12V
Digital Input Voltage to DGND .......... -0.3V, ($V_{DD}$ + 0.3V)
VREF .......... ($V_{SS}$ - 0.3V), ($V_{DD}$ + 0.3V)
$V_{OUT}$ (Note 1) .......... $V_{SS}$, $V_{DD}$
Continuous Power Dissipation ($T_A$ = +70°C)
MAX505
  Plastic DIP (derate 13.33mW/°C above +70°C) .... 1067mW
  Wide SO (derate 11.76mW/°C above +70°C) .......941mW
  CERDIP (derate 12.50mW/°C above +70°C) ...... 1000mW
  SSOP (derate 8mW/°C above +70°C) .......640mW
MAX506
  Plastic DIP (derate 11.11mW/°C above +70°C) ...... 889mW
  Wide SO (derate 10.00mW/°C above +70°C) ....... 800mW
  CERDIP (derate 11.11mW/°C above +70°C) ........ 889mW
Operating Temperature Ranges:
  MAX50_C_ .......... 0°C to +70°C
  MAX50_E_ .......... -40°C to +85°C
  MAX50_M_ .......... -55°C to +125°C
Storage Temperature Range .......... -65°C to +165°C
Lead Temperature (soldering, 10 sec) .......... +300°C

**Note 1:** The outputs may be shorted to $V_{DD}$, $V_{SS}$, or AGND if the package power dissipation is not exceeded. Typical short-circuit current to AGND is 50mA.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{DD}$ = +5V ±10%, $V_{SS}$ = 0V to -5.5V, AGND = DGND = 0V, VREF = 4V, $R_L$ = 10kΩ, $C_L$ = 100pF, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **STATIC ACCURACY** | | | | | | | |
| Resolution | | | | 8 | | | Bits |
| Total Unadjusted Error | TUE | VREF = +4V, $V_{SS}$ = 0V or -5V ±10% | MAX50_A | | | ±1 | LSB |
| | | | MAX50_B | | | ±1½ | |
| | | VREF = -4V, $V_{SS}$ = -5V ±10% | MAX50_A | | | ±1 | |
| | | | MAX50_B | | | ±1½ | |
| Differential Nonlinearity | DNL | Guaranteed monotonic | | | | ±1 | LSB |
| Zero-Code Error | ZCE | Code = 00 hex, $V_{SS}$ = 0V | MAX50_C | | | 14 | mV |
| | | | MAX50_E | | | 16 | |
| | | | MAX50_M | | | 20 | |
| | | Code = 00 hex, $V_{SS}$ = -5V ±10% | MAX50_C | | | ±14 | |
| | | | MAX50_E | | | ±16 | |
| | | | MAX50_M | | | ±20 | |
| Zero-Code Error Supply Rejection | | Code = 00 hex, $V_{DD}$ = 5V ±10%, $V_{SS}$ = 0V or -5V ±10% | | | 1 | 2 | mV |
| Zero-Code Temperature Coefficient | | Code = 00 hex | | | ±10 | | µV/°C |
| Full-Scale Error | | Code = FF hex | | | | ±14 | mV |
| Full-Scale Error Supply Rejection | | Code = FF hex, $V_{DD}$ = +5V ±10%, $V_{SS}$ = 0V or -5V ±10% | MAX50_C | | 1 | 4 | mV |
| | | | MAX50_E | | 1 | 8 | |
| | | | MAX50_M | | | 12 | |
| Full-Scale-Error Temperature Coefficient | | Code = FF hex | | | ±10 | | µV/°C |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = +5V ±10%, $V_{SS}$ = 0V to -5.5V, AGND = DGND = 0V, VREF = 4V, $R_L$ = 10kΩ, $C_L$ = 100pF, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **REFERENCE INPUTS** | | | | | | | |
| Input Voltage Range | | | | $V_{SS}$ | | $V_{DD}$ | V |
| Input Resistance (Note 2) | | Code = 55 hex | MAX505 | 16 | 24 | | kΩ |
| | | | MAX506 | 4 | 6 | | |
| Input Capacitance (Note 3) | | Code = 00 hex | MAX505 | | 15 | | pF |
| | | | MAX506 | | 40 | | |
| Channel-to-Channel Isolation | | MAX505 (Note 4) | | | -60 | | dB |
| AC Feedthrough | | MAX505 (Note 5) | | | -70 | | dB |
| **DAC OUTPUTS** | | | | | | | |
| Full-Scale Output Voltage | | | | $V_{SS}$ | | $V_{DD}$ | V |
| Resistive Load | | $V_{OUT}$ = 4V, load regulation ≤ 1/4LSB | | 2 | | | kΩ |
| | | $V_{OUT}$ = -4V, load regulation ≤ 1/4LSB | | 2 | | | |
| | | $V_{OUT}$ = $V_{DD}$ MAX50_C/E load regulation ≤ 1.5LSB | | 10 | | | |
| | | $V_{OUT}$ = $V_{DD}$ MAX50_M load regulation ≤ 2LSB | | 10 | | | |
| **DIGITAL INPUTS** | | | | | | | |
| Logic High | $V_{IH}$ | | | 2.4 | | | V |
| Logic Low | $V_{IL}$ | | | | | 0.8 | V |
| Input Current | | Measured at $V_{IH}$ and $V_{IL}$ | | | | ±1 | µA |
| Input Capacitance | | | | | 8 | | pF |
| Input Coding | | | | Binary | | | |
| **DYNAMIC PERFORMANCE** | | | | | | | |
| Voltage-Output Slew Rate | | Positive and negative | MAX50_C | 1.0 | | | V/µs |
| | | | MAX50_E | 0.7 | | | |
| | | | MAX50_M | 0.5 | | | |
| Output Settling Time | | To ±1/2LSB, 10kΩ II 100pF load (Note 6) | | | 6 | | µs |
| Digital Feedthrough | | Code = 00 hex, $\overline{WR}$ = $V_{DD}$, all digital inputs from 0V to $V_{DD}$ | | | 5 | | nV-s |
| Signal to (Noise + Distortion) Ratio | | VREF = 4Vp-p at 1kHz, $V_{DD}$ = 5V, $V_{SS}$ = -5V, code = FF hex | | | 87 | | dB |
| | | VREF = 4Vp-p at 20kHz, $V_{SS}$ = -5V ±10% | | | -74 | | dB |
| Multiplying Bandwidth | | VREF = 0.5Vp-p, 3dB bandwidth | | | 1 | | MHz |
| Wideband Amplifier Noise | | | | | 60 | | $\mu V_{RMS}$ |

# Quad 8-Bit DACs with Rail-to-Rail Voltage Outputs

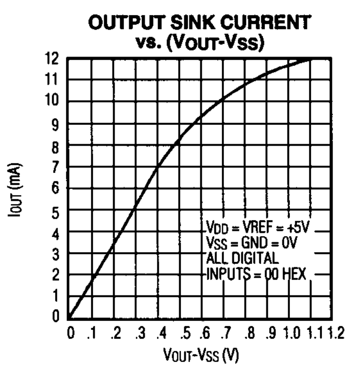
## ELECTRICAL CHARACTERISTICS (continued)

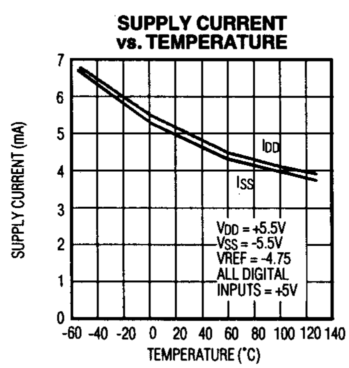
($V_{DD}$ = +5V ±10%, $V_{SS}$ = 0V to -5.5V, AGND = DGND = 0V, VREF = 4V, $R_L$ = 10kΩ, $C_L$ = 100pF, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.)

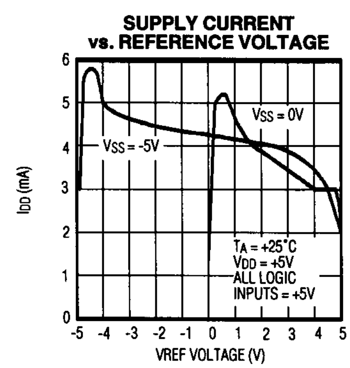
| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **POWER SUPPLIES** | | | | | | | |
| Positive Supply Voltage | $V_{DD}$ | For specified performance | | 4.5 | | 5.5 | V |
| Negative Supply Voltage | $V_{SS}$ | For specified performance | | -5.5 | | 0 | V |
| Positive Supply Current | $I_{DD}$ | Outputs unloaded, all digital inputs = 0V or $V_{DD}$ | MAX50__C/E | | 5 | 10 | mA |
| | | | MAX50_M | | 5 | 12 | |
| Negative Supply Current | $I_{SS}$ | $V_{SS}$ = -5V ±10%, outputs unloaded, all digital inputs = 0V or $V_{DD}$ | MAX50__C/E | | 5 | 10 | mA |
| | | | MAX50_M | | 5 | 12 | |
| **SWITCHING CHARACTERISTICS** | | | | | | | |
| Address to $\overline{WR}$ Setup | $t_{AS}$ | | | 5 | -8 | | ns |
| Address to $\overline{WR}$ Hold | $t_{AH}$ | | | 5 | -4 | | ns |
| Data to $\overline{WR}$ Setup | $t_{DS}$ | | | 45 | 35 | | ns |
| Data to $\overline{WR}$ Hold | $t_{DH}$ | | | 0 | -13 | | ns |
| $\overline{WR}$ Pulse Width | $t_{WR}$ | | | 40 | 20 | | ns |
| $\overline{LDAC}$ Pulse Width | $t_{LC}$ | | | 40 | 20 | | ns |

**Note 2:** Input resistance is code dependent. The lowest input resistance occurs at code = 55 hex.
**Note 3:** Input capacitance is code dependent. The highest input capacitance occurs at code = 00 hex.
**Note 4:** VREF = 10kHz, 4Vp-p. Channel-to-channel isolation is measured by setting the code of one DAC to FF hex and setting the code of all other DACs to 00 hex.
**Note 5:** VREF = 10kHz, 4Vp-p. DAC code = 00 hex.
**Note 6:** Output settling time is measured by taking the code from 00 hex to FF hex, and from FF hex to 00 hex.

## *Typical Operating Characteristics*

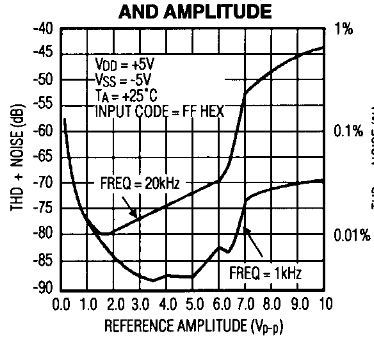


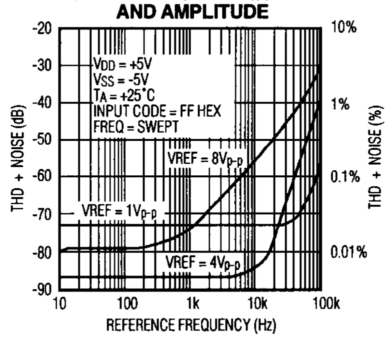



## Typical Operating Characteristics (continued)

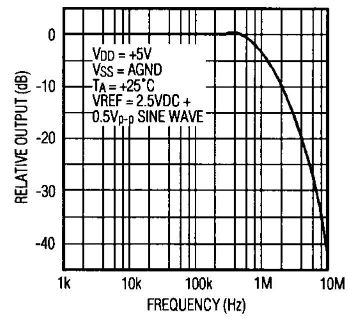
**THD + NOISE AT DAC OUTPUT vs. REFERENCE FREQUENCY AND AMPLITUDE**



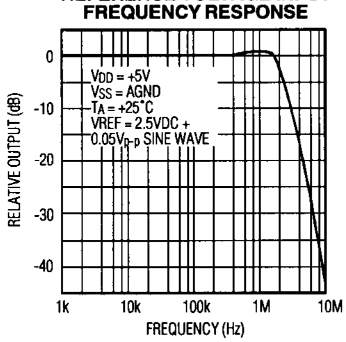

**THD + NOISE AT DAC OUTPUT vs. REFERENCE FREQUENCY AND AMPLITUDE**



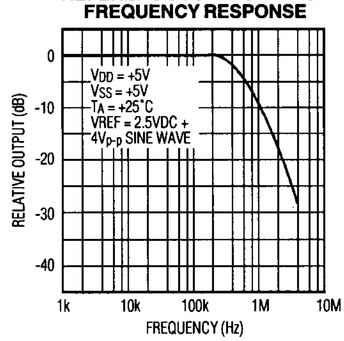

**REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE**



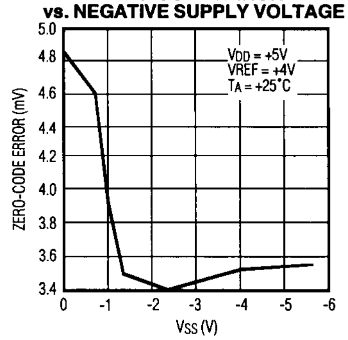

**REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE**



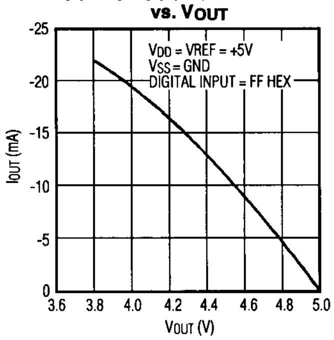

**REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE**



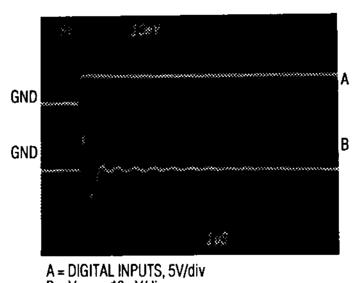

**ZERO-CODE ERROR vs. NEGATIVE SUPPLY VOLTAGE**




**OUTPUT SOURCE CURRENT vs. VOUT**



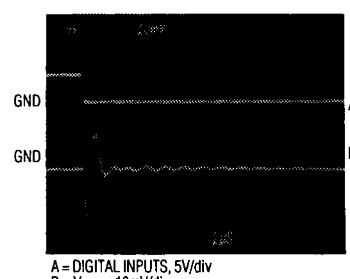

**DIGITAL FEEDTHROUGH – GLITCH IMPULSE (0 TO 1 DIGITAL TRANSITION)**




A = DIGITAL INPUTS, 5V/div
B = VOUTA, 10mV/div
TIMEBASE = 1µs

0 TO 1 DIGITAL TRANSITION ON ALL DATA BITS (WITH $\overline{WR}$ HIGH)
VREFA = AGND

**DIGITAL FEEDTHROUGH – GLITCH IMPULSE (1 TO 0 DIGITAL TRANSITION)**



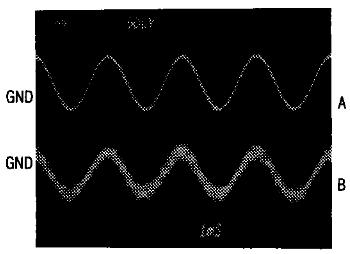

A = DIGITAL INPUTS, 5V/div
B = VOUTA, 10mV/div
TIMEBASE = 1µs

1 TO 0 DIGITAL TRANSITION ON ALL DATA BITS (WITH $\overline{WR}$ HIGH)
VREFA = AGND

# Quad 8-Bit DACs with Rail-to-Rail Voltage Outputs

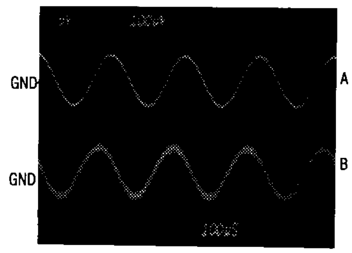
## Typical Operating Characteristics (continued)

**REFERENCE FEEDTHROUGH AT 400Hz**



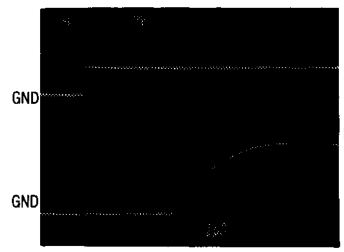

A = VREFA, $10V_{P-P}$
B = $V_{OUTA}$, 50µV/div, UNLOADED
TIMEBASE = 1ms/div
$V_{DD}$ = +5V
$V_{SS}$ = -5V
CODE = ALL 0s
LOAD = ∞

**REFERENCE FEEDTHROUGH AT 4000Hz**



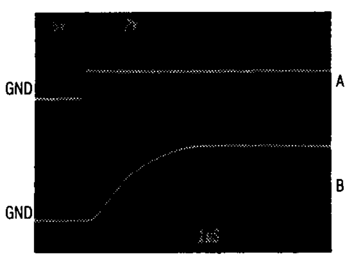

A = VREFA, $10V_{P-P}$
B = $V_{OUTA}$, 100µV/div, UNLOADED
TIMEBASE = 100µs/div
$V_{DD}$ = +5V
$V_{SS}$ = -5V
CODE = ALL 0s
LOAD = ∞

**POSITIVE SETTLING TIME ($V_{SS}$ = AGND)**



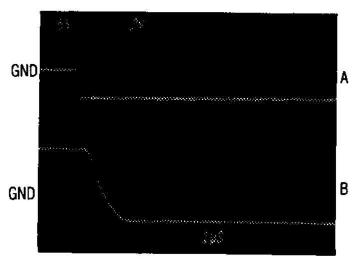

A = DIGITAL INPUT, 5V/div
B = $V_{OUTA}$, 2V/div
TIMEBASE = 1µs
$V_{DD}$ = +5V
VREFA = +5V
ALL BITS OFF TO ALL BITS ON
$R_L$ = 10kΩ, $C_L$ = 100pF

**POSITIVE SETTLING TIME ($V_{SS}$ = -5V)**



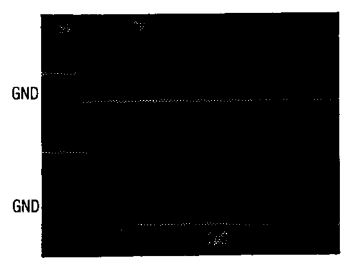

A = DIGITAL INPUT, 5V/div
B = $V_{OUTA}$, 2V/div
TIMEBASE = 1µs
$V_{DD}$ = +5V
VREFA = +5V
ALL BITS OFF TO ALL BITS ON
$R_L$ = 10kΩ, $C_L$ = 100pF

**NEGATIVE SETTLING TIME ($V_{SS}$ = AGND)**




A = DIGITAL INPUT, 5V/div
B = $V_{OUTA}$, 2V/div
TIMEBASE = 1µs
$V_{DD}$ = +5V
VREFA = +5V
ALL BITS ON TO ALL BITS OFF
$R_L$ = 10kΩ, $C_L$ = 100pF

**NEGATIVE SETTLING TIME ($V_{SS}$ = -5V)**




A = DIGITAL INPUT, 5V/div
B = $V_{OUTA}$, 2V/div
TIMEBASE = 1µs
$V_{DD}$ = +5V
VREFA = +5V
ALL BITS ON TO ALL BITS OFF
$R_L$ = 10kΩ, $C_L$ = 100pF

## Pin Description

| PIN MAX505 | PIN MAX506 | NAME | FUNCTION |
|---|---|---|---|
| 1 | 1 | $V_{OUTB}$ | DAC B Output Voltage |
| 2 | 2 | $V_{OUTA}$ | DAC A Output Voltage |
| 3 | 3 | $V_{SS}$ | Negative Power Supply |
| 4 | | VREFB | Reference Voltage Input for DAC B |
| | 4 | VREF | Reference Voltage Input for DAC A to DAC D |
| 5 | | VREFA | Reference Voltage Input for DAC A |
| 6 | 5 | AGND | Analog Ground |
| 7 | 6 | DGND | Digital Ground |
| 8 | | $\overline{LDAC}$ | Load DAC Input (active low). Driving this asynchronous input low transfers the contents of each input latch to its respective DAC latch. |
| 9 | 7 | D7 | Data Bit 7 (MSB) |
| 10 | 8 | D6 | Data Bit 6 |
| 11 | 9 | D5 | Data Bit 5 |
| 12 | 10 | D4 | Data Bit 4 |
| 13 | 11 | D3 | Data Bit 3 |
| 14 | 12 | D2 | Data Bit 2 |
| 15 | 13 | D1 | Data Bit 1 |
| 16 | 14 | D0 | Data Bit 0 (LSB) |
| 17 | 15 | $\overline{WR}$ | Write Input (active low). Used to load data into the DAC input latch selected by A0 and A1. |
| 18 | 16 | A1 | DAC Address select bit (MSB) |
| 19 | 17 | A0 | DAC Address select bit (LSB) |
| 20 | | VREFD | Reference Voltage Input for DAC D |
| 21 | | VREFC | Reference Voltage Input for DAC C |
| 22 | 18 | $V_{DD}$ | Positive Supply Voltage |
| 23 | 19 | $V_{OUTD}$ | DAC D Output Voltage |
| 24 | 20 | $V_{OUTC}$ | DAC C Output Voltage |

## Detailed Description

### Digital-to-Analog Section

The MAX505/MAX506 contain four matched voltage-output DACs. The DACs are inverted R-2R ladder networks that convert 8-bit digital words into equivalent analog output voltages in proportion to the applied reference voltage(s). Each DAC in the MAX505 has a separate reference input, while all four DACs in the MAX506 share a common reference input. Figure 1 shows a simplified functional diagram of one of the DACs.

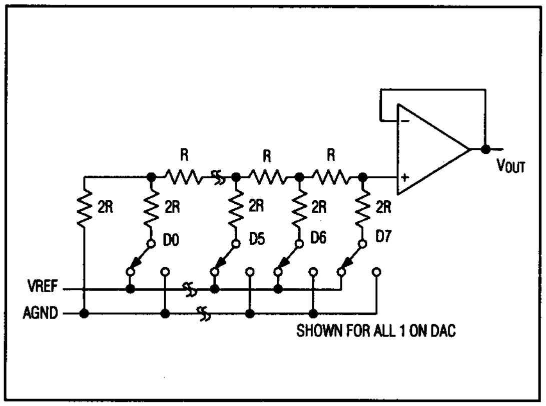



*Figure 1. DAC Simplified Circuit Diagram*

### Power Supplies and Reference Input

The MAX505/MAX506 can be used for multiplying applications. The reference accepts both DC and AC signals. The voltage at each VREF input sets the full-scale output voltage for its respective DAC. The VREF input impedance is code dependent, with the lowest value (16kΩ for the MAX505 and 4kΩ for the MAX506) occuring when the input code is 55 hex. The maximum value, essentially infinity, occurs when the input code is 00 hex. Since the VREF input impedance is code dependent, the DACs' reference sources must have a low output impedance (no more than 32Ω for the MAX505 and 8Ω for the MAX506) to maintain output linearity. The VREF input capacitance is also code dependent: 15pF maximum for the MAX505 and 40pF maximum for the MAX506.

The output voltage for any DAC can be represented by a digitally programmable voltage source as:

$$V_{OUT} = (N_B \times VREF) / 256$$

where $N_B$ is the numeric value of the DAC's binary input code.

### Output Buffer Amplifiers

All MAX505/MAX506 voltage outputs are internally buffered by precision unity-gain followers that slew at 1V/µs. With a 0V to +4V (or +4V to 0V) output transition, the amplifier outputs will settle to 1/2LSB in typically 6µs when loaded with 10kΩ in parallel with 100pF.

The buffer amplifiers are stable with any combination of resistive loads ≥ 2kΩ and capacitive loads ≤ 300pF.

### Digital Inputs and Interface Logic

The digital inputs are compatible with both TTL and 5V CMOS logic. However, the power-supply current ($I_{DD}$) depends on the input logic levels. Supply current is specified for CMOS input levels (best case). Supply current increases by about 2mA when driven with TTL logic levels.

Address lines A0 and A1 select which DAC receives data from the data bus as shown in Table 1. When $\overline{WR}$ is low, the addressed DAC's input latch is transparent. Data is latched when $\overline{WR}$ is high. Figure 2 shows the MAX505/MAX506 input control logic.

The MAX506 DAC outputs represent the data held in the four 8-bit input latches. The MAX505 has double-buffered inputs; in addition to the input registers, there are individual DAC latches (see *Functional Diagrams*).

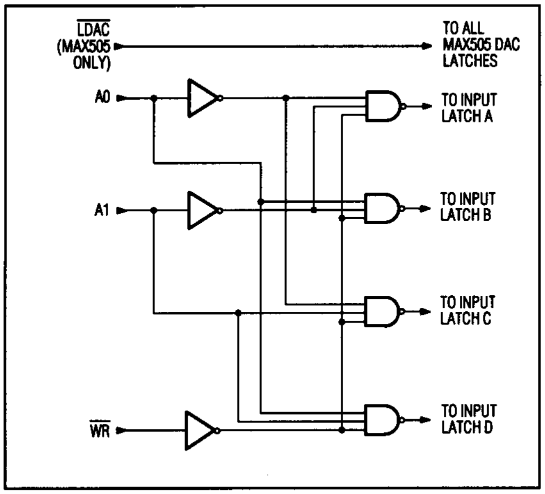



*Figure 2. MAX505/MAX506 Input Control Logic*

In the MAX505, data is transferred from the input latches to the DAC latches by pulling the $\overline{\text{LDAC}}$ control input low. This operation simultaneously updates all four outputs. Since $\overline{\text{LDAC}}$ is asynchronous with respect to $\overline{\text{WR}}$, be sure that incorrect data is not latched to the output. Table 1a is the write-cycle truth table for the MAX505. Table 1b is the write-cycle truth table for the MAX506. Figure 3 shows the MAX505/MAX506 write-cycle timing. If simultaneous updating is not required, tie $\overline{\text{LDAC}}$ low to keep the DAC latches transparent. To avoid output glitches, insure that data is valid before $\overline{\text{WR}}$ goes low (MAX506). This also applies to the MAX505 if $\overline{\text{WR}}$ and $\overline{\text{LDAC}}$ are low simultaneously.

On power-up, all MAX505/MAX506 latches are internally preset with all 0s.

### Table 1a. MAX505 DAC Addressing (partial list)

| $\overline{\text{LDAC}}$ | $\overline{\text{WR}}$ | A1 | A0 | LATCH STATE |
|---|---|---|---|---|
| H | H | X | X | Input and DAC data latched |
| H | L | L | L | DAC A input latch transparent |
| L | H | X | X | All 4 DACs' DAC latches transparent |
| L | L | L | L | DAC A input registers transparent and all 4 DACs' DAC latches transparent |
| H | L | L | H | DAC B input latch transparent |
| H | L | H | L | DAC C input latch transparent |
| H | L | H | H | DAC D input latch transparent |

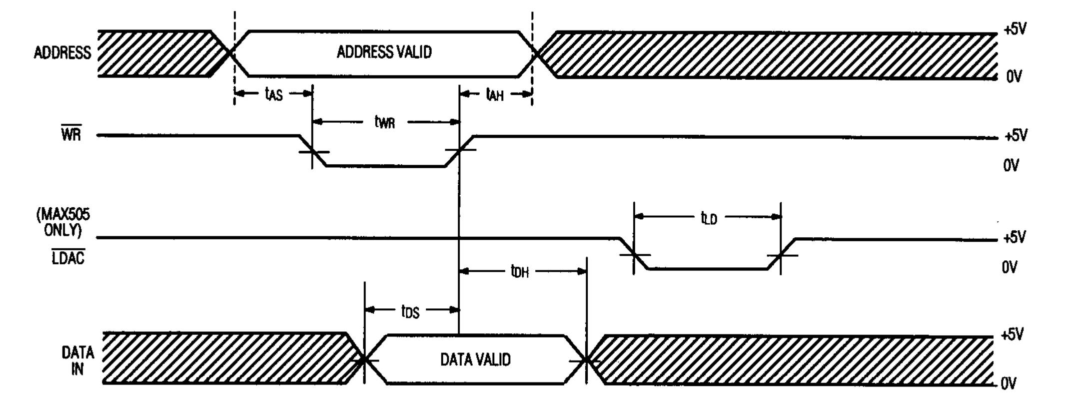
H = High State, L = Low State, X = Don't Care

### Table 1b. MAX506 DAC Addressing (partial list)

| $\overline{\text{WR}}$ | A1 | A0 | LATCH STATE |
|---|---|---|---|
| H | X | X | Input data latched |
| L | L | L | DAC A input latch transparent |
| L | L | H | DAC B input latch transparent |
| L | H | L | DAC C input latch transparent |
| L | H | H | DAC D input latch transparent |

H = High State, L = Low State, X = Don't Care

# Quad 8-Bit DACs with Rail-to-Rail Voltage Outputs




NOTES:
ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V, $t_r = t_f = 5ns$ OVER $V_{DD}$ RANGE.
TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{INH} + V_{INL}}{2}$.
IF $\overline{LDAC}$ (MAX505 ONLY) IS ACTIVATED PRIOR TO $\overline{WR}$'S RISING EDGE, IT MUST STAY LOW FOR $t_{LD}$ (OR LONGER) AFTER $\overline{WR}$ GOES HIGH.

*Figure 3. MAX505/MAX506 Write-Cycle Timing Diagram*

## Applications Information

### Power Supply and Reference Operating Ranges

The MAX505/MAX506 are fully specified to operate with $V_{DD}$ = 5V ±10% and $V_{SS}$ = 0V to -5.5V. 8-bit performance is guaranteed for both single- and dual-supply operation. The zero-code output error is guaranteed to be less than 14mV when operating from a single +5V supply.

The DACs work well with reference voltages from $V_{SS}$ to $V_{DD}$.

$V_{SS}$ should never be more positive than either AGND or DGND. No input should be more positive than $V_{DD}$.

### Power-Supply Bypassing and Ground Management

In single-supply operation (AGND = DGND = $V_{SS}$ = 0V), AGND, DGND, and $V_{SS}$ should be connected together in a "star" ground at the chip. This ground should then return to the highest quality ground available. Bypass $V_{DD}$ with a 0.1µF capacitor, located as close to $V_{DD}$ and AGND as possible.

In dual-supply operation, where DGND = AGND, $V_{DD}$ and $V_{SS}$ should be bypassed with 0.1µF capacitors to AGND. These capacitors should be placed as close to the supply pins as possible. To minimize digital noise on AGND, DGND and AGND should have separate return paths to the highest quality ground available.

Careful PCB layout minimizes crosstalk between DAC outputs, reference inputs, and digital inputs. Figures 4 and 5 show suggested circuit board layouts to minimize crosstalk.

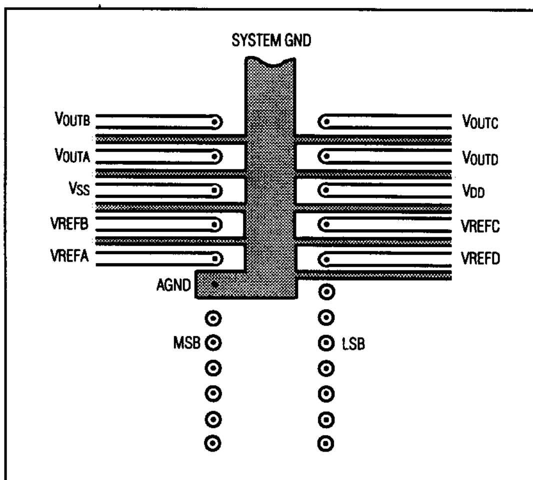



*Figure 4. Suggested MAX505 PCB Layout for Minimizing Crosstalk*

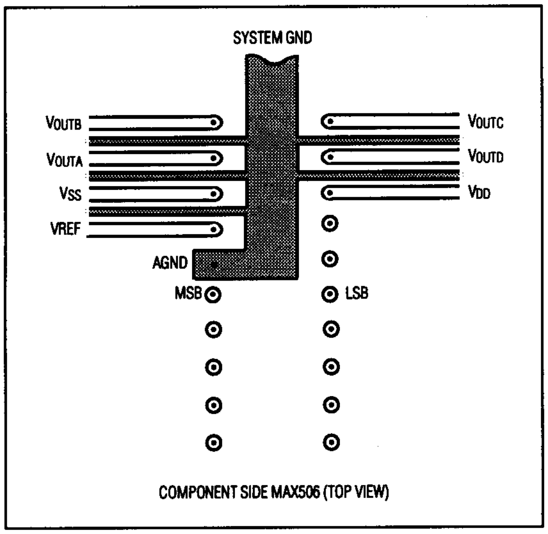



*Figure 5. Suggested MAX506 PCB Layout for Minimizing Crosstalk*

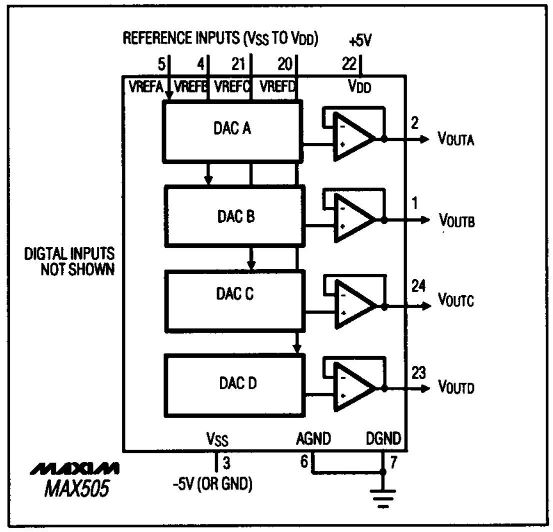



*Figure 6. MAX505 Unipolar Output Circuit*

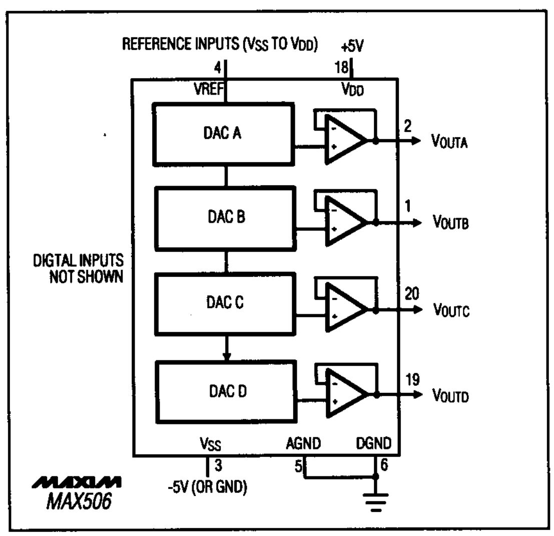



*Figure 7. MAX506 Unipolar Output Circuit*

### Unipolar Output, 2-Quadrant Multiplication

In unipolar operation, the output voltages and the reference input(s) are the same polarity. Figures 6 and 7 show the MAX505/MAX506 unipolar configurations. If the reference inputs are positive, both devices can be operated from a single supply. If dual supplies are used, the reference input can vary from $V_{SS}$ to $V_{DD}$. Table 2 is the unipolar code table.

### Bipolar Output, 2-Quadrant Multiplication

Bipolar output 2-quadrant multiplication is achieved by offsetting AGND positively or negatively.

#### Offsetting AGND Positively - Single or Dual Supplies

AGND can be biased above DGND to provide an arbitrary nonzero output voltage for a 0 input code, as shown in Figure 8. The output voltage at $V_{OUTA}$ is:

$$V_{OUTA} = V_{BIAS} + (N_B/256)(V_{IN}),$$

where $N_B$ represents the digital input word. Since AGND is common to all four DACs, all outputs will be offset by $V_{BIAS}$ in the same manner. AGND should not be biased more than +1V above DGND.

# Quad 8-Bit DACs with Rail-to-Rail Voltage Outputs

### Table 2. Unipolar Code Table

| DAC CONTENTS MSB | LSB | ANALOG OUTPUT |
|---|---|---|
| 1111 | 1111 | $+VREF\left(\frac{255}{256}\right)$ |
| 1000 | 0001 | $+VREF\left(\frac{129}{256}\right)$ |
| 1000 | 0000 | $+VREF\left(\frac{128}{256}\right) = +\frac{VREF}{2}$ |
| 0111 | 1111 | $+VREF\left(\frac{127}{256}\right)$ |
| 0000 | 0001 | $+VREF\left(\frac{1}{256}\right)$ |
| 0000 | 0000 | 0V |

**Note:** $1LSB = (VREF)(2^{-8}) = +VREF\left(\frac{1}{256}\right)$

### *Offsetting AGND Negatively - Dual Supplies*

An alternate method of generating bipolar outputs uses Figure 9's circuits. In these circuits, AGND is biased negatively (up to -2.5V with respect to DGND) to provide an arbitrary negative output voltage for a 0 input code. The output voltage at $V_{OUTA}$ is:

$$V_{OUTA} = -(R2/R1)(2.5V) + (N_B/256)(2.5V)(R2/R1 + 1)$$

where $N_B$ represents the digital input word. Since AGND is common to all four DACs, all outputs will be offset by $V_{BIAS}$ in the same manner. Table 3, with VREF = 2.5V, shows the digital code vs. output voltage for Figure 9's circuits with R1 = R2.

### *4-Quadrant Multiplication*

Each DAC output may be configured for 4-quadrant multiplication using Figure 10's circuit. One op amp and two resistors are required per channel. With R1 = R2:

$$V_{OUT} = VREF\,[(2)(N_B/256) - 1],$$

where $N_B$ represents the digital word in DAC register A.

Recommended values for resistors R1 and R2 are 330kΩ (±0.1%). Table 3 shows the digital code vs. output voltage for Figure 10's circuit.

### Table 3. Bipolar Code Table

| DAC CONTENTS MSB | LSB | ANALOG OUTPUT |
|---|---|---|
| 1111 | 1111 | $VREF\left(\frac{127}{128}\right)$ |
| 1000 | 0001 | $VREF\left(\frac{1}{128}\right)$ |
| 1000 | 0000 | 0V |
| 0111 | 1111 | $-VREF\left(\frac{1}{128}\right)$ |
| 0000 | 0001 | $-VREF\left(\frac{127}{128}\right)$ |
| 0000 | 0000 | $-VREF\left(\frac{128}{128}\right) = -VREF$ |

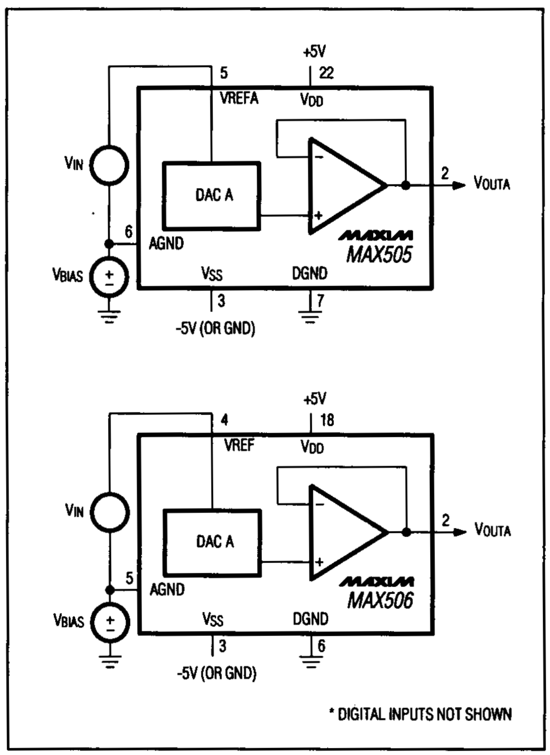



*Figure 8. AGND Bias Circuits (Positive Offset)*

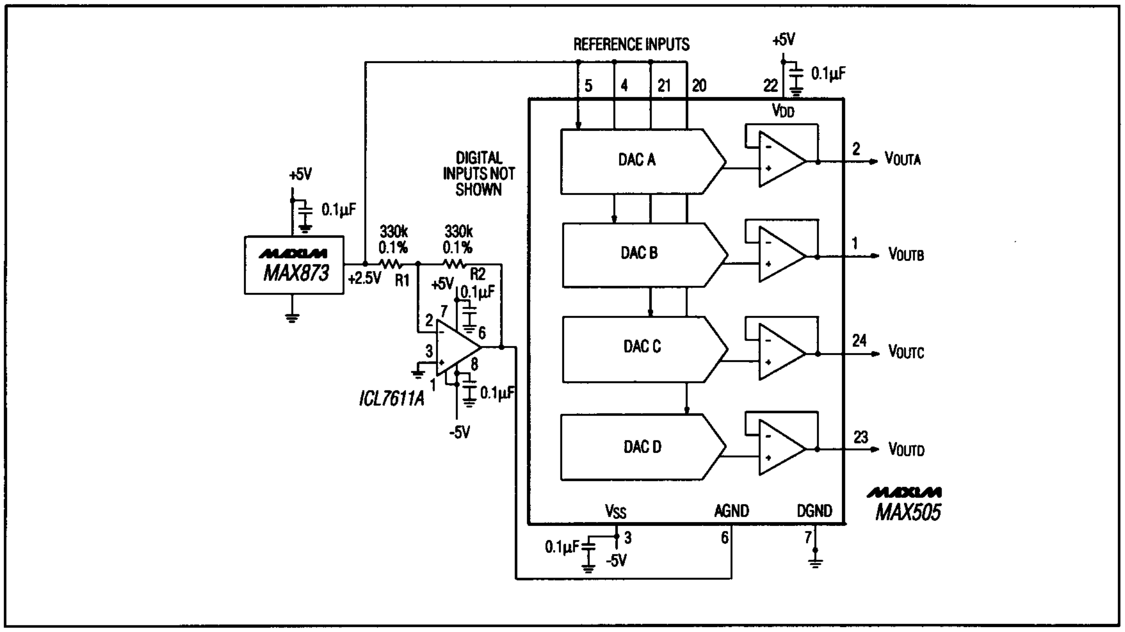



*Figure 9a. MAX505 AGND Bias Circuit (Negative Offset)*

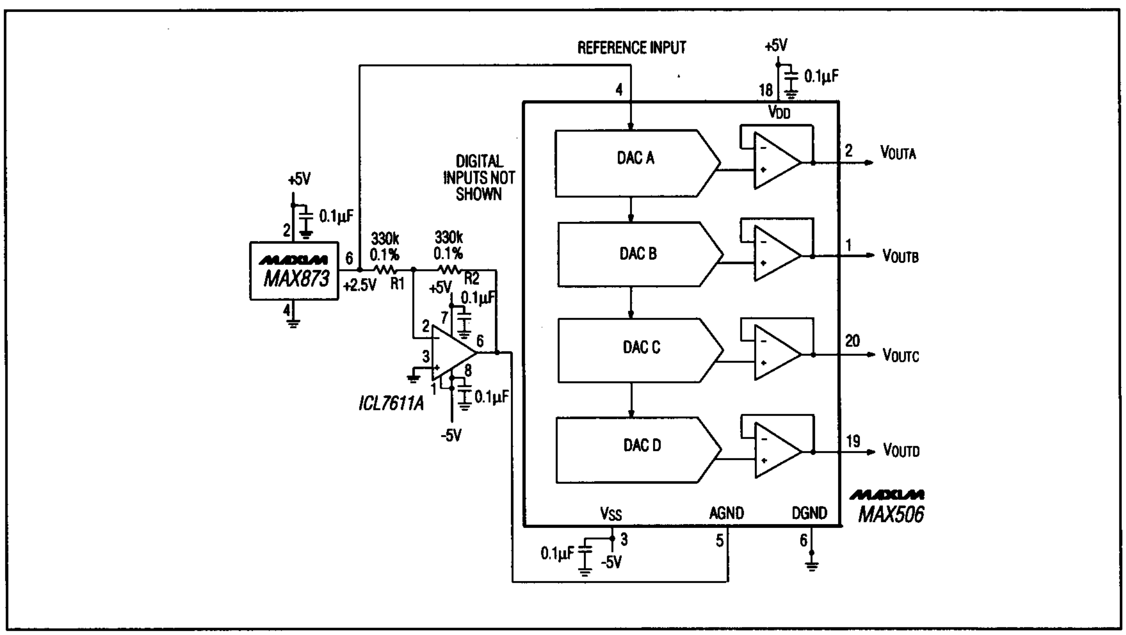



*Figure 9b. MAX506 AGND Bias Circuit (Negative Offset)*

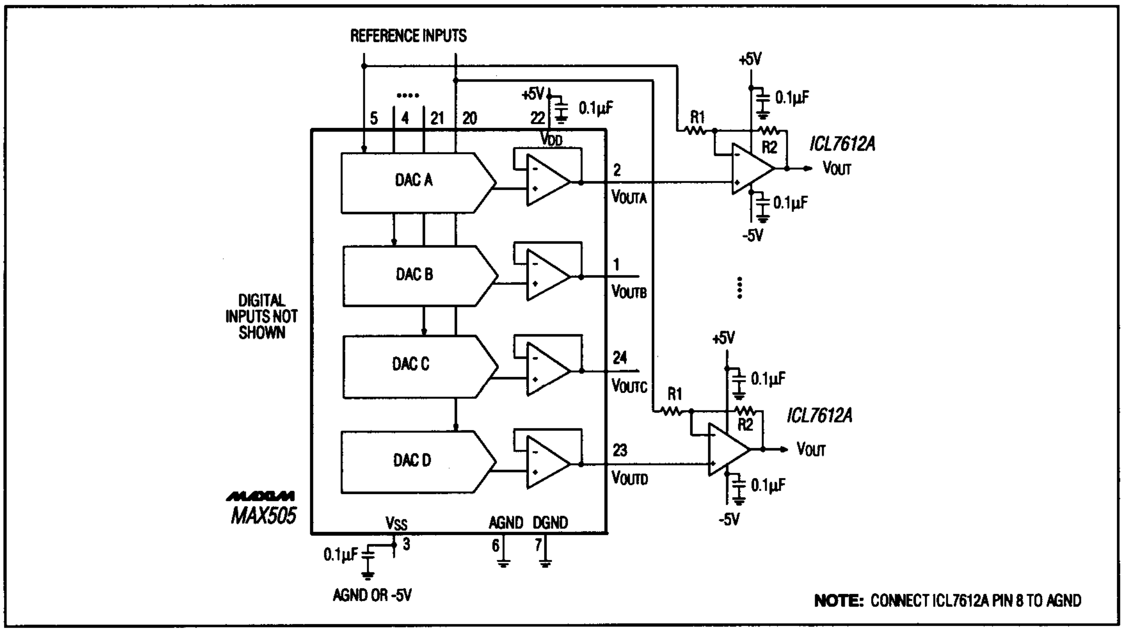



*Figure 10a. MAX505 Bipolar Output Circuit*

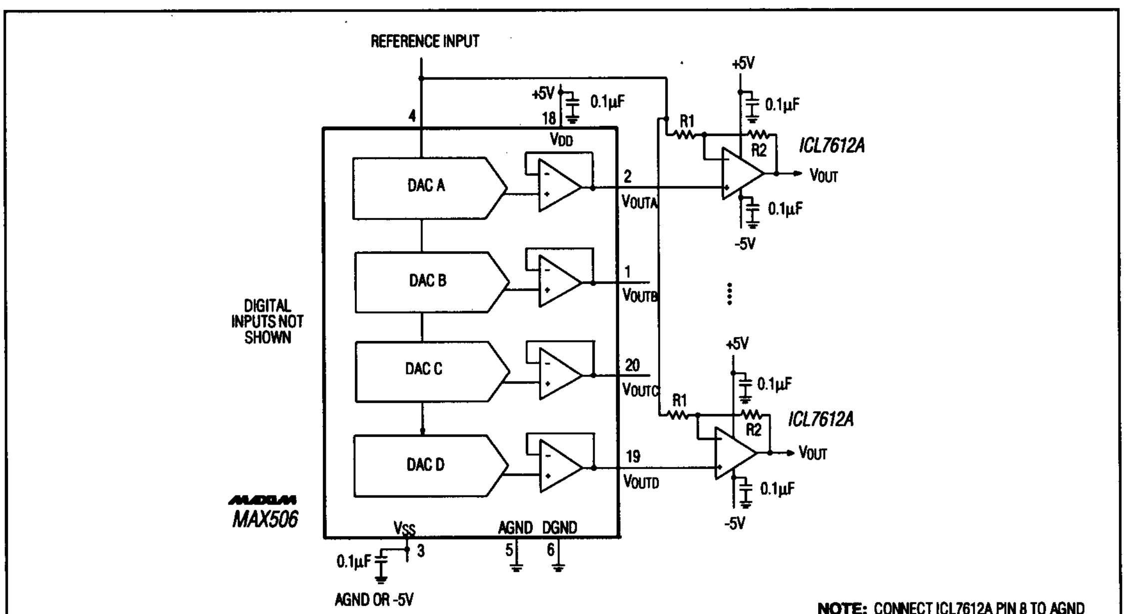
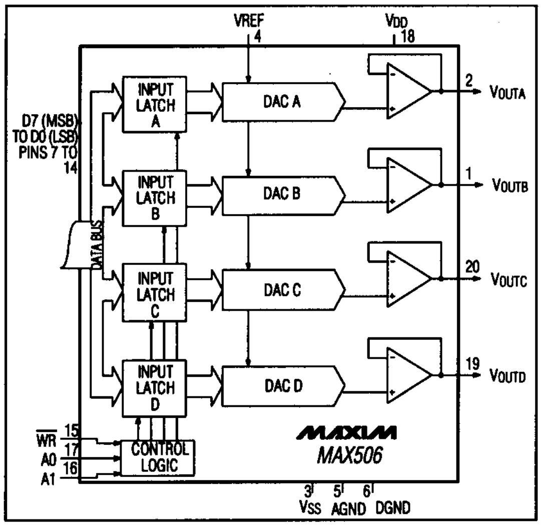
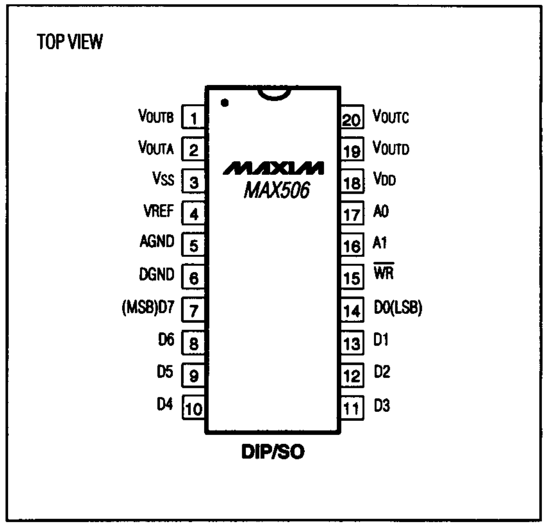



*Figure 10b. MAX506 Bipolar Output Circuit*

## Functional Diagrams (continued)




## Pin Configurations (continued)




## Ordering Information

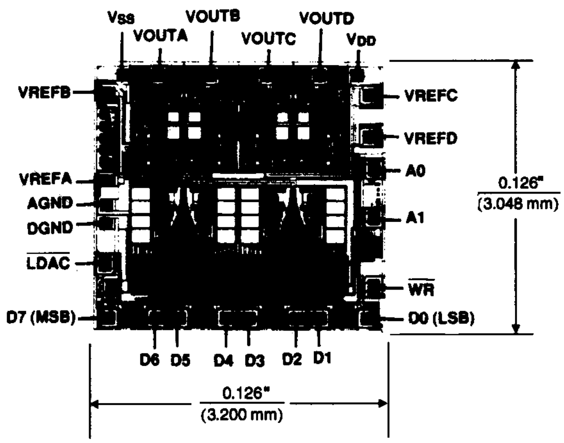
| PART | TEMP. RANGE | PIN-PACKAGE | TUE (LSBs) |
|---|---|---|---|
| MAX505AENG | -40°C to +85°C | 24 Narrow Plastic DIP | ±1 |
| MAX505BENG | -40°C to +85°C | 24 Narrow Plastic DIP | ±1½ |
| MAX505AEWG | -40°C to +85°C | 24 Wide SO | ±1 |
| MAX505BEWG | -40°C to +85°C | 24 Wide SO | ±1½ |
| MAX505AEAG | -40°C to +85°C | 24 SSOP | ±1 |
| MAX505BEAG | -40°C to +85°C | 24 SSOP | ±1½ |
| MAX505AMRG | -55°C to +125°C | 24 Narrow CERDIP** | ±1 |
| MAX505BMRG | -55°C to +125°C | 24 Narrow CERDIP** | ±1½ |
| MAX506ACPP | 0°C to +70°C | 20 Plastic DIP | ±1 |
| MAX506BCPP | 0°C to +70°C | 20 Plastic DIP | ±1½ |
| MAX506ACWP | 0°C to +70°C | 20 Wide SO | ±1 |
| MAX506BCWP | 0°C to +70°C | 20 Wide SO | ±1½ |
| MAX506BC/D | 0°C to +70°C | Dice* | ±1½ |
| MAX506AEPP | -40°C to +85°C | 20 Plastic DIP | ±1 |
| MAX506BEPP | -40°C to +85°C | 20 Plastic DIP | ±1½ |
| MAX506AEWP | -40°C to +85°C | 20 Wide SO | ±1 |
| MAX506BEWP | -40°C to +85°C | 20 Wide SO | ±1½ |
| MAX506AMJP | -55°C to +125°C | 20 CERDIP** | ±1 |
| MAX506BMJP | -55°C to +125°C | 20 CERDIP** | ±1½ |

** Contact factory for dice specifications.*
***Contact factory for availability and processing to MIL-STD-883.*

# Quad 8-Bit DACs with Rail-to-Rail Voltage Outputs

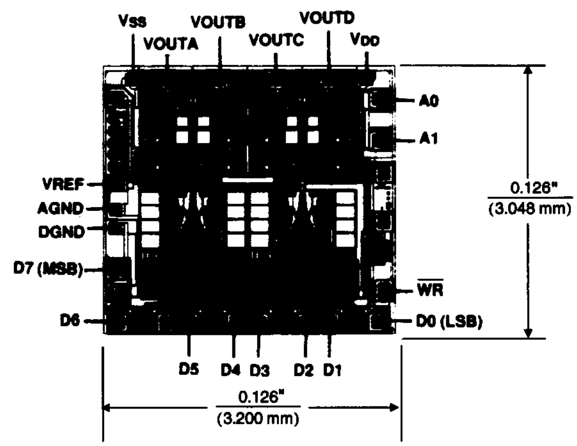
## Chip Topographies

MAX505



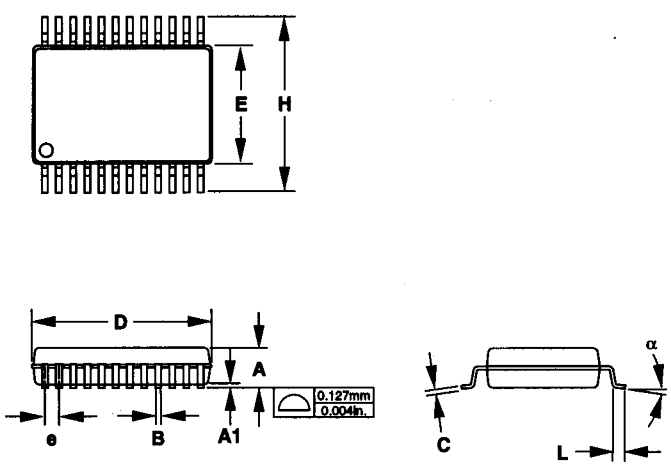

TRANSISTOR COUNT: 1717;
SUBSTRATE CONNECTED TO VDD.

MAX506




TRANSISTOR COUNT: 1717;
SUBSTRATE CONNECTED TO VDD.

## Package Information




| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 0.068 | 0.078 | 1.73 | 1.99 |
| A1 | 0.002 | 0.008 | 0.05 | 0.21 |
| B | 0.010 | 0.015 | 0.25 | 0.38 |
| C | 0.005 | 0.009 | 0.13 | 0.22 |
| D | 0.278 | 0.328 | 7.07 | 8.33 |
| E | 0.205 | 0.212 | 5.20 | 5.38 |
| e | 0.0256 BSC | | 0.65 BSC | |
| H | 0.301 | 0.311 | 7.65 | 7.90 |
| L | 0.022 | 0.037 | 0.55 | 0.95 |
| α | 0° | 8° | 0° | 8° |

21-0002A

**24-PIN PLASTIC SHRINK SMALL-OUTLINE PACKAGE**

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