19-3582; Rev 1; 5/06

MAXIM

Overvoltage Protection Controllers with Reverse Polarity Protection

General Description

The MAX4864L/MAX4865L/MAX4866L/MAX4867/MAX4865/MAX4866 overvoltage protection controllers protect low-voltage systems against high-voltage faults up to +28V, and negative voltages down to -28V. These devices drive a low-cost complementary MOSFET. If the input voltage exceeds the overvoltage threshold, these devices turn off the n-channel MOSFET to prevent damage to the protected components. If the input voltage drops below ground, the devices turn off the p-channel MOSFET to prevent damage to the protected components. An internal charge pump eliminates the need for external capacitors and drives the MOSFET GATEN for a simple, robust solution.

The overvoltage thresholds are preset to +7.4V (MAX4864L), +6.35V (MAX4865L), +5.8V (MAX4866L), and +4.65V (MAX4867). When the input voltage drops below the undervoltage lockout (UVLO) threshold, the devices enter a low-current standby mode (8.5µA). Also in shutdown ($\overline{EN}$ set to logic-high), the current is reduced further (0.4µA). The MAX4864L/MAX4865L/MAX4866L have a +2.85V UVLO threshold, and the MAX4867 has a +2.5V UVLO threshold. The MAX4865/MAX4866 have a 4.15V UVLO threshold.

In addition, a ±15kV ESD protection is provided to the input when bypassed with a 1µF capacitor to ground. All devices are offered in a small 6-pin SOT23 and a 6-pin, 2mm x 2mm µDFN package, and are specified for operation over the -40°C to +85°C temperature range.

Applications

Cell Phones
Digital Still Cameras
PDAs and Palmtop Devices
MP3 Players

Features

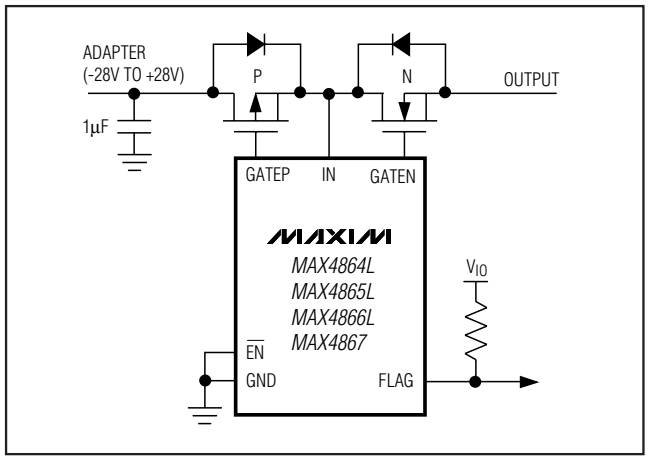
- **Overvoltage Protection Up to +28V**
- **Reverse Polarity Protection Down to -28V**
- **Preset Overvoltage (OV) Trip Level (7.4V, 6.35V, 5.8V, 4.65V)**
- **Drive Low-Cost Complementary MOSFET**
- **Internal 50ms Startup Delay**
- **Internal Charge Pump**
- **8.5µA Standby Current (In UVLO Mode)**
- **0.4µA Shutdown Current**
- **Overvoltage Fault FLAG Indicator**
- **6-Pin (2mm x 2mm) µDFN and 6-Pin SOT23 Packages**

Ordering Information

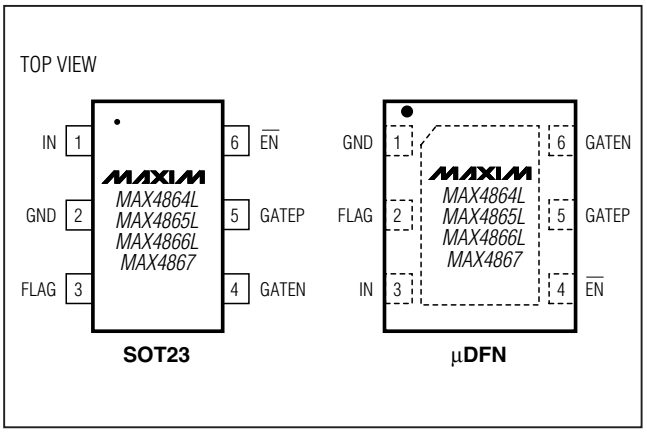
PART	PIN-PACKAGE	OV TRIP LEVEL (V)	TOP MARK	PKG CODE
MAX4864LEUT-T	6 SOT23-6	7.40	ABVO	—
MAX4864LELT	6 µDFN	7.40	AAE	L622-1
MAX4865LEUT-T	6 SOT23-6	6.35	ABVP	—
MAX4865LELT	6 µDFN	6.35	AAF	L622-1
MAX4866LEUT-T	6 SOT23-6	5.80	ABVQ	—
MAX4866LELT	6 µDFN	5.80	AAG	L622-1
MAX4867EUT-T	6 SOT23-6	4.65	ABVN	—
MAX4867ELT	6 µDFN	4.65	AAD	L622-1

Note: *All devices are specified over the -40°C to +85°C operating range.*

Typical Operating Circuit



Pin Configurations



Functional Diagram appears at end of data sheet.

Overvoltage Protection Controllers with Reverse Polarity Protection

ABSOLUTE MAXIMUM RATINGS

IN to GND .....-0.3V to +30V
GATEN, GATEP to GND .....-0.3V to +12V
IN to GATEP .....-0.3V to +20V
FLAG, $\overline{EN}$ to GND .....-0.3V to +6V
Continuous Power Dissipation (T_A = +70°C)
6-Pin µDFN (2mm x 2mm) (derate 2.1mW/°C above +70°C) 168mW
6-Pin SOT23 (derate 8.7mW/°C above +70°C).....696mW

Operating Temperature Range .....-40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +5V (MAX4864L/MAX4865L/MAX4866L), V_{IN} = +4V (MAX4867), T_A = -40°C to +85°C, C_{GATEN} = 500pF, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}			1.2		28.0	V
Overvoltage Trip Level	OVLO	V_{IN} rising	MAX4864L	7.0	7.4	7.8	V
			MAX4865L	5.95	6.35	6.75	
			MAX4866L	5.45	5.8	6.15	
			MAX4867	4.35	4.65	4.95	
Overvoltage Lockout Hysteresis		MAX4864L			75		mV
		MAX4865L			65		
		MAX4866L			55		
		MAX4867			50		
Undervoltage Lockout Threshold	UVLO	V_{IN} falling	MAX4864L/MAX4865L/MAX4866L	2.65	2.85	3.05	V
			MAX4867	2.3	2.5	2.7	
Undervoltage Lockout Hysteresis		MAX4864L/MAX4865L/MAX4866L			44		mV
		MAX4867			25		
IN Supply Current	I_{IN}	$\overline{EN}$ = GND	MAX4864L/MAX4865L/MAX4866L		77	120	µA
			MAX4867		68	110	
UVLO Supply Current	I_{UVLO}	$\overline{EN}$ = GND	MAX4864L/MAX4865L/MAX4866L, V_{IN} = +2.6V		8.5	22	µA
			MAX4867, V_{IN} = +2.2V		8	18	
Shutdown Supply Current	I_{SHD}	$\overline{EN}$ = 1.6V	MAX4864L/MAX4865L/MAX4866L, V_{IN} = 3.6V		0.4	2	µA
			MAX4867, V_{IN} = 3.6V		0.4	2	
GATEN Voltage	V_{GATEN}	1µA load	MAX4864L/MAX4865L/MAX4866L	9	9.83	10	V
			MAX4867	7.5	7.85	8.0	
GATEN Pulldown Current	I_{PD}	V_{IN} > OVLO, V_{GATEN} = +5.5V		12	32	65	mA
GATEP Clamp Voltage	V_{CLAMP}			13.5	16.5	19.5	V
GATEP Pulldown Resistor	R_{GATEP}			32	48	64	kΩ
FLAG Output-Low Voltage	V_{OL}	I_{SINK} = 1mA				0.4	V
FLAG Leakage Current		V_{FLAG} = +5.5V				1	µA
$\overline{EN}$ Input-High Voltage	V_{IH}			1.5			V
$\overline{EN}$ Input-Low Voltage	V_{IL}					0.4	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +5V (MAX4864L/MAX4865L/MAX4866L), V_{IN} = +4V (MAX4867), T_A = -40°C to +85°C, C_{GATEN} = 500pF, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{EN}$ Input Leakage Current	I_{LKG}	$\overline{EN}$ = GND or +5.5V			1	µA
TIMING						
Startup Delay	t_{START}	V_{IN} > UVLO to V_{GATEN} > 0.3V, Figure 1	20	50	80	ms
FLAG Blanking Time	t_{BLANK}	V_{GATEN} > 0.3V to V_{FLAG} < 0.3V, Figure 1	20	50	80	ms
GATEN Turn-On Time	t_{GON}	C_{GATEN} = 500pF, V_{GATEN} = 0.3V to +8V (MAX4864L/MAX4865L/MAX4866L) V_{GATEN} = 0.3V to +7V (MAX4867), Figure 1		10		ms
GATEN Turn-Off Time	t_{Goff}	V_{IN} rising at 3V/µs from +5V to +8V (MAX4864L/MAX4865L/MAX4866L), or from +4V to +7V (MAX4867) V_{GATEN} = 0.3V, C_{GATEN} = 500pF, Figure 2		7	20	µs
FLAG Assertion Delay	t_{FLAG}	V_{IN} rising at 3V/µs from 5V to 8V (MAX4864L/MAX4865L/MAX4866L), or from +4V to +7V (MAX4867), V_{FLAG} = 0.3V, Figure 2		3.5		µs
Initial Overvoltage Fault Delay	t_{OVP}	V_{IN} rising at 3V/µs from 0V to +9V, time from V_{IN} = 5V to I_{GATEN} = 80% of I_{PD} (GATEN pulldown current), Figure 3		1.5		µs
Disable Time	t_{DIS}	$V_{\overline{EN}}$ = +2.4V, V_{GATEN} = 0.3V, Figure 4		2		µs

Note 1: All parts are 100% tested at +25°C. Electrical limits across the full temperature range are guaranteed by design and correlation.

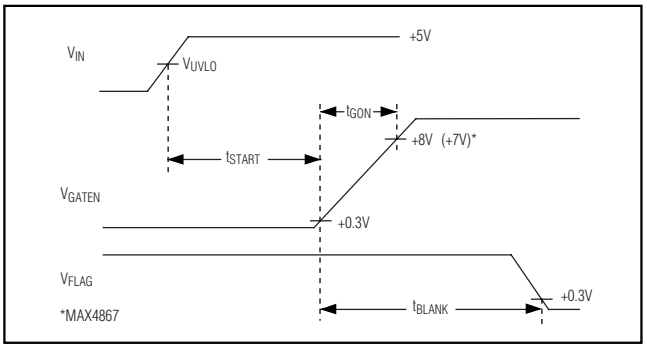


Figure 1. Startup Timing Diagram

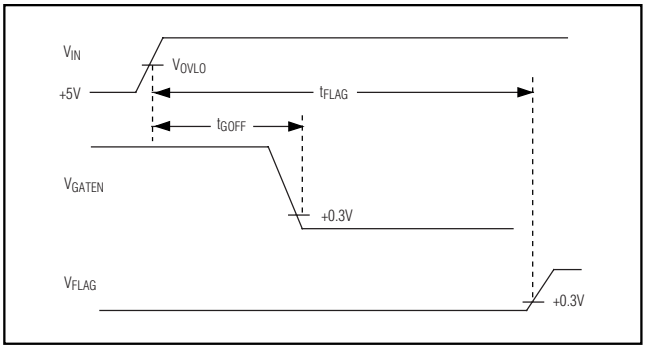


Figure 2. Shutdown Timing Diagram

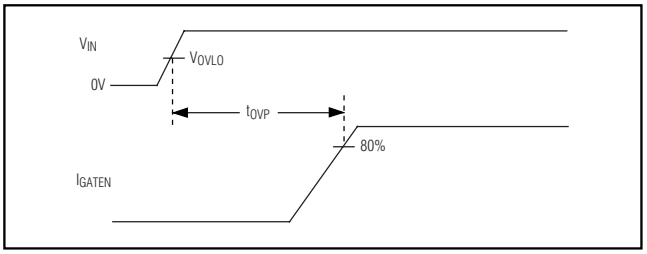


Figure 3. Power-Up Overvoltage Timing Diagram

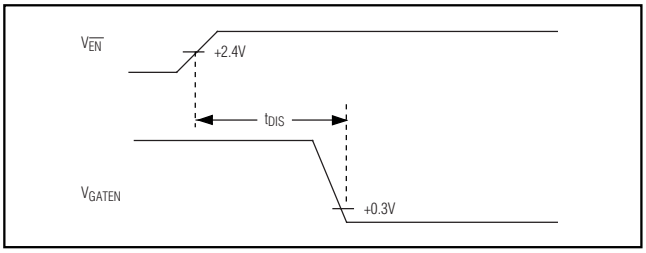


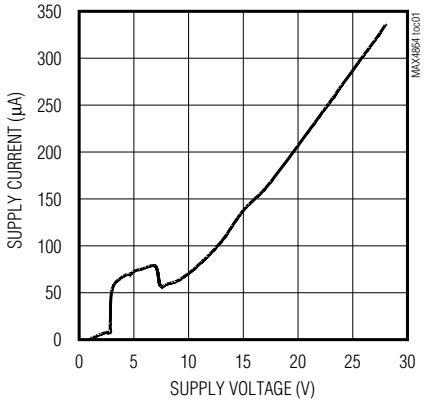
Figure 4. Disable Timing Diagram

Overvoltage Protection Controllers with Reverse Polarity Protection

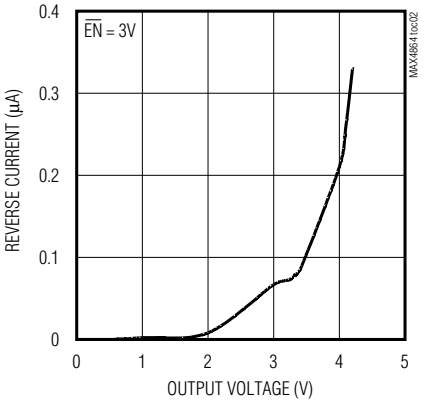
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

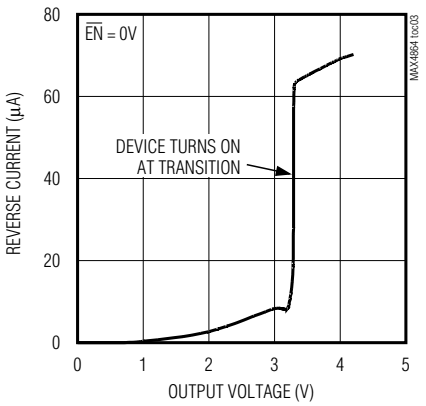
SUPPLY CURRENT vs. SUPPLY VOLTAGE (MAX4864L)



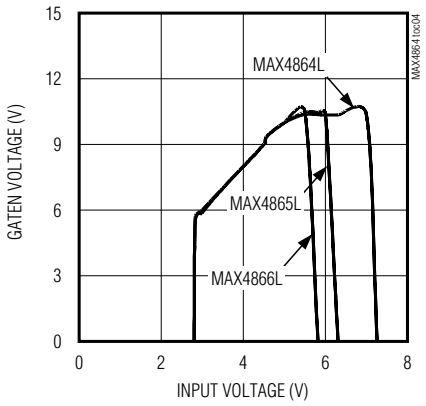
REVERSE CURRENT vs. OUTPUT VOLTAGE (MAX4864L)



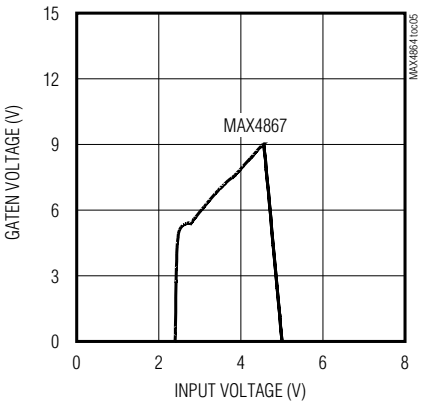
REVERSE CURRENT vs. OUTPUT VOLTAGE (MAX4864L)



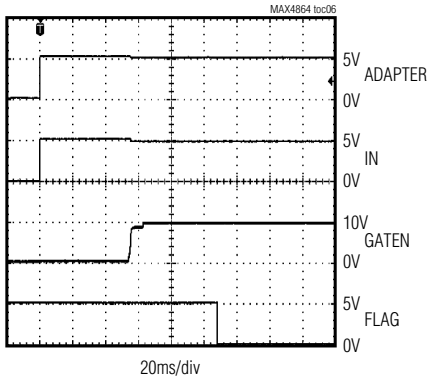
MAX4864L/MAX4865L/MAX4866L GATEN VOLTAGE vs. INPUT VOLTAGE



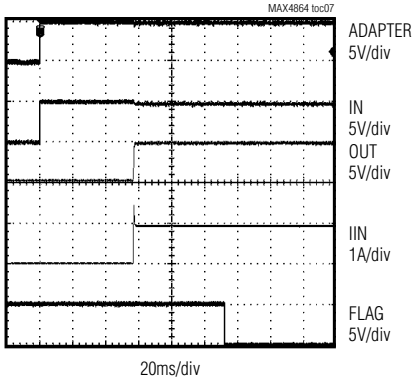
MAX4867 GATEN VOLTAGE vs. INPUT VOLTAGE



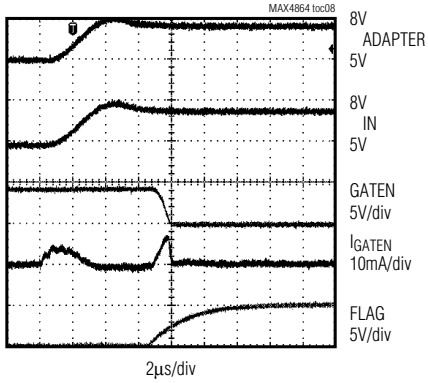
POWER-UP RESPONSE



POWER-UP RESPONSE



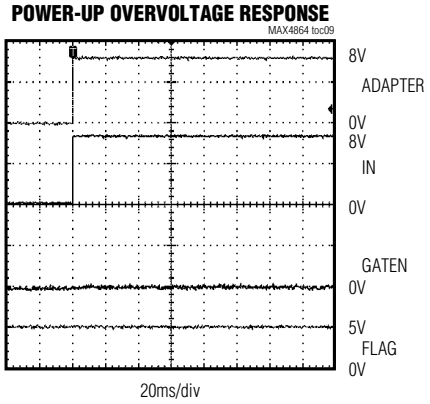
OVERVOLTAGE RESPONSE



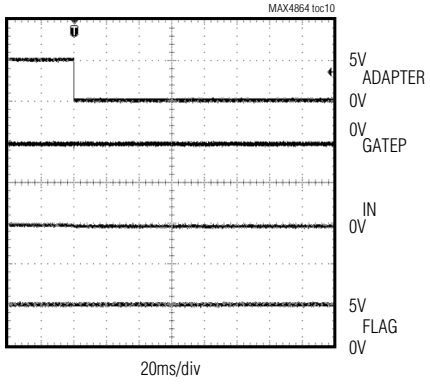
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

POWER-UP OVERVOLTAGE RESPONSE



NEGATIVE VOLTAGE RESPONSE



Pin Description

PIN		NAME	FUNCTION
MAX4864LEUT/ MAX4865LEUT/ MAX4866LEUT/ MAX4867EUT	MAX4864LELT/ MAX4865LELT/ MAX4866LELT/ MAX4867ELT		
1	3	IN	Voltage Input. IN is both the power-supply input and the overvoltage sense input.
2	1	GND	Ground
3	2	FLAG	Fault-Indication Output. When $\overline{EN}$ goes high, FLAG becomes high-impedance. FLAG is asserted high during undervoltage lockout and overvoltage lockout conditions. FLAG is deasserted during normal operation. FLAG is an open-drain output.
4	6	GATEN	n-Channel MOSFET Gate-Drive Output. GATEN is the output of an on-chip charge pump. When $V_{UVLO} < V_{IN} < V_{OVLO}$, GATEN is driven high to turn on the external n-channel MOSFET.
5	5	GATEP	p-Channel MOSFET Gate-Drive Output. GATEP is always on when input is above ground and off when input drops below ground.
6	4	$\overline{EN}$	Active-Low Enable Input. Connect to ground in normal operation. Drive $\overline{EN}$ high to disable device and enter shutdown mode.

Overvoltage Protection Controllers with Reverse Polarity Protection

Detailed Description

The MAX4864L/MAX4865L/MAX4866L/MAX4867 provide up to +28V overvoltage and negative voltage protection for low voltage systems. When the input voltage exceeds the overvoltage trip level, the MAX4864L/MAX4865L/MAX4866L/MAX4867 turn off a low-cost external n-channel MOSFET to prevent damage to the protected components. The devices also drive an external p-channel MOSFET to protect against negative voltage inputs. An internal charge-pump (see the *Functional Diagram*), drives the MOSFET GATEN for a simple, robust solution. On power-up, the device waits for 50ms before driving GATEN high. The open-drain FLAG output is kept at a high impedance for an additional 50ms after GATEN goes high before deasserting. The FLAG output asserts high immediately to an overvoltage fault.

Undervoltage Lockout (UVLO)

The MAX4864L/MAX4865L/MAX4866L/MAX4867 have a fixed +2.85V typical UVLO level, and the MAX4867 has +2.5V UVLO level. When V_{IN} is less than the UVLO, the GATEN driver is held low and FLAG is asserted.

Overvoltage Lockout (OVLO)

The MAX4864L has a +7.4V typical OVLO threshold; the MAX4865L has +6.35V typical OVLO threshold; the MAX4866L has a +5.8V typical OVLO threshold; and the MAX4867 has a +4.65V typical OVLO threshold. When V_{IN} is greater than OVLO, the GATEN driver is held low and FLAG is asserted.

FLAG Output

The open-drain FLAG output is used to signal to the host system when there is a fault with the input voltage. On power-up, FLAG is held high for 50ms after GATEN turns on, before deasserting. FLAG asserts immediately to overvoltage and undervoltage faults. When the fault condition is removed, FLAG deasserts 50ms after GATEN turns on. Connect a pullup resistor from FLAG to the logic I/O voltage of the host system.

GATEN Driver

An on-chip charge pump is used to drive GATEN above IN, allowing the use of a low-cost n-channel MOSFET. The charge pump operates from the internal +5.5V regulator.

The actual GATEN output voltage tracks approximately two times V_{IN} until V_{IN} exceeds +5.5V, or the OVLO trip level is exceeded, whichever comes first. The MAX4864L has a +7.4V typical OVLO, therefore GATEN remains relatively constant at approximately +10.5V for +5.5V < V_{IN} < +7.4V. The MAX4866L has a +5.8V typical OVLO, but this can be as low as +5.5V. The GATEN output voltage is a function of input voltage, as shown in the *Typical Operating Characteristics*.

GATEP Driver

When the input voltage drops below ground, GATEP goes high turning the external p-channel MOSFET off. When the input voltage goes above ground, GATEP pulls low and turns on the p-channel MOSFET. An internal clamp protects the p-channel MOSFET by insuring that the GATEP-to-IN voltage does not exceed +16V when the input (IN) rises to +28V.

Device Operation

The MAX4864L/MAX4865L/MAX4866L/MAX4867 have an on-board state machine to control device operation. A flowchart is shown in Figure 5. On initial power-up, if V_{IN} < UVLO or if V_{IN} > OVLO, GATEN is held at 0V and FLAG is high.

If UVLO < V_{IN} < OVLO, the device enters startup after a 50ms internal delay. The internal charge pump is enabled, and GATEN begins to be driven above V_{IN} by the internal charge pump. FLAG is held high during startup until the FLAG blanking period expires, typically 50ms after the GATEN starts going high. At this point, the device is in its on-state.

At any time if V_{IN} drops below UVLO, FLAG is driven high and GATEN is driven to ground.

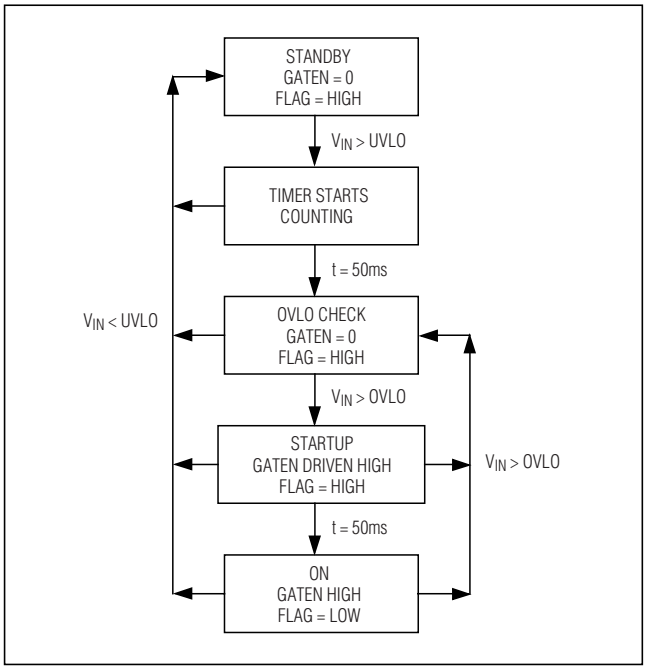


Figure 5. State Diagram

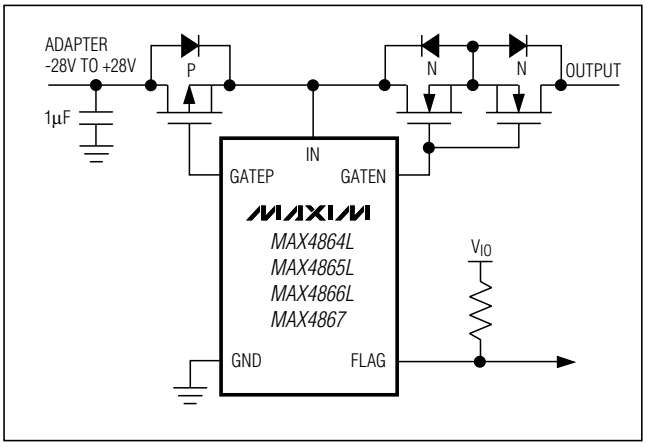


Figure 6. Back-to-Back External MOSFET Configuration

Applications Information

MOSFET Configuration

The MAX4864L/MAX4865L/MAX4866L/MAX4867 can be used with either a complementary MOSFET configuration as shown in the *Typical Operating Circuit*, or can be configured with a single p-channel MOSFET and back-to-back n-channel MOSFETs as shown in Figure 6.

The MAX4864L/MAX4865L/MAX4866L/MAX4867 can drive either a complementary MOSFET or a single p-channel MOSFET and back-to-back n-channel MOSFETs. The back-to-back configuration has almost zero reverse current when the adapter is not present or when the adapter voltage is below the UVLO threshold.

If reverse current leakage is not a concern, a single MOSFET can be used. This approach has half the loss of the back-to-back configuration when used with similar MOSFET types and is a lower cost solution. Note that if the input is actually pulled low, the output will also be pulled low due to the parasitic body diode in the MOSFET. If this is a concern, then the back-to-back configuration should be used.

MOSFET Selection

The MAX4864L/MAX4865L/MAX4866L/MAX4867 are designed for use with a complementary MOSFET or single p-channel and dual back-to-back n-channel MOSFETs. In most situations, MOSFETs with RDS(ON) specified for a VGS of 4.5V work well. Also the V_{DS} should be +30V for the MOSFET to withstand the full +28V IN range of the MAX4864L/MAX4865L/MAX4866L/MAX4867. Table 1 shows a selection of MOSFETs which are appropriate for use with the MAX4864L/MAX4865L/MAX4866L/MAX4867.

IN Bypass Considerations

For most applications, bypass ADAPTER to GND with a 1µF ceramic capacitor. If the power source has significant inductance due to long lead length, take care to prevent overshoots due to the LC tank circuit and provide protection if necessary to prevent exceeding the +30V absolute maximum rating on IN.

ESD Test Conditions

ESD performance depends on a number of conditions. The MAX4864L/MAX4865L/MAX4866L/MAX4867 are specified for +/-15kV typical ESD resistance on IN when ADAPTER is bypassed to ground with a 1µF ceramic capacitor.

Human Body Model

Figure 7 shows the Human Body Model, and Figure 8 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

Table 1. MOSFET Suggestions

PART	CONFIGURATION/ PACKAGE	V_{GS} MAX (V)	V_{DS} MAX (V)	R_{ON} AT 4.5V (mΩ)	MANUFACTURER
Si5504DC	Complementary MOSFET/1206-8	±20	+30	143 (n-MOSFET)	Vishay Siliconix
			-30	290 (p-MOSFET)	
Si5902DC	Dual/1206-8	±20	+30	143 (n-MOSFET)	
Si1426DH	Single/µDFN-6	±20	+30	115 (n-MOSFET)	
Si5435DC	Single/1206-8	±20	-30	80 (p-MOSFET)	
FDC6561AN	Dual/SSOT-6	±20	+30	145 (n-MOSFET)	Fairchild Semiconductor
FDG315N	Single/µDFN-6	±20	+30	160 (n-MOSFET)	
FDC658P	Single/SSOT-6	±20	-30	75 (p-MOSFET)	
FDC654P	Single/SSOT-6	±20	-30	125 (p-MOSFET)	

Overvoltage Protection Controllers with Reverse Polarity Protection

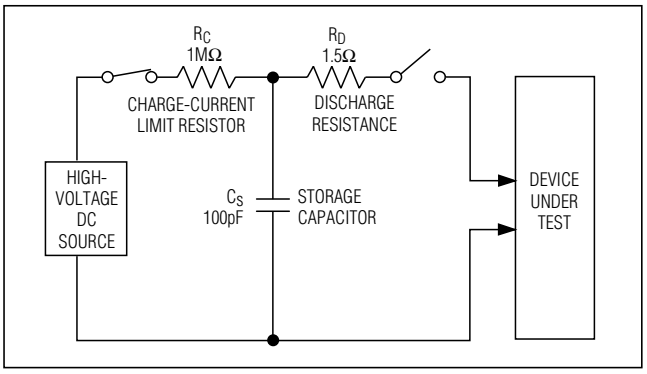


Figure 7. Human Body ESD Test Model

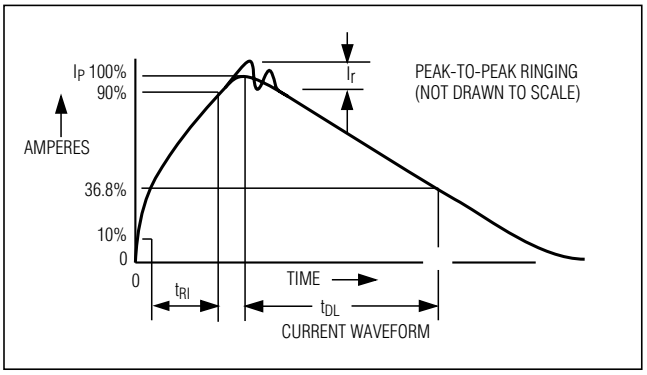


Figure 8. Human Body Current Waveform

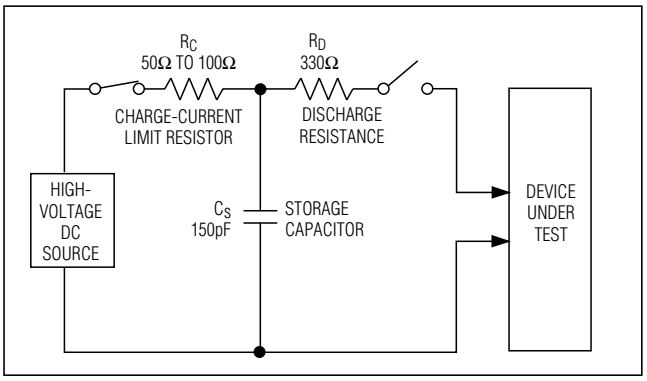


Figure 9. IEC 1000-4-2 ESD Test Model

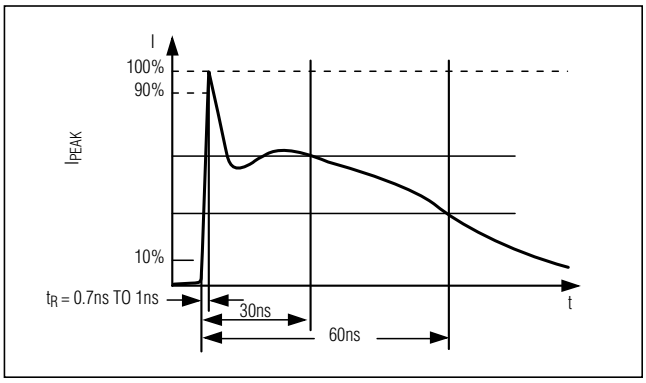


Figure 10. IEC 1000-4-2 ESD Generator Current Waveform

IEC 1000-4-2

Since January 1996, all equipment manufactured and/or sold in the European Union has been required to meet the stringent IEC 1000-4-2 specification. The IEC 1000-4-2 standard covers ESD testing and performance of finished equipment. It does not specifically refer to ICs. The MAX4864L/MAX4865L/MAX4866L/MAX4867 help users design equipment that meets Level 3 of IEC 1000-4-2, without additional ESD-protection components.

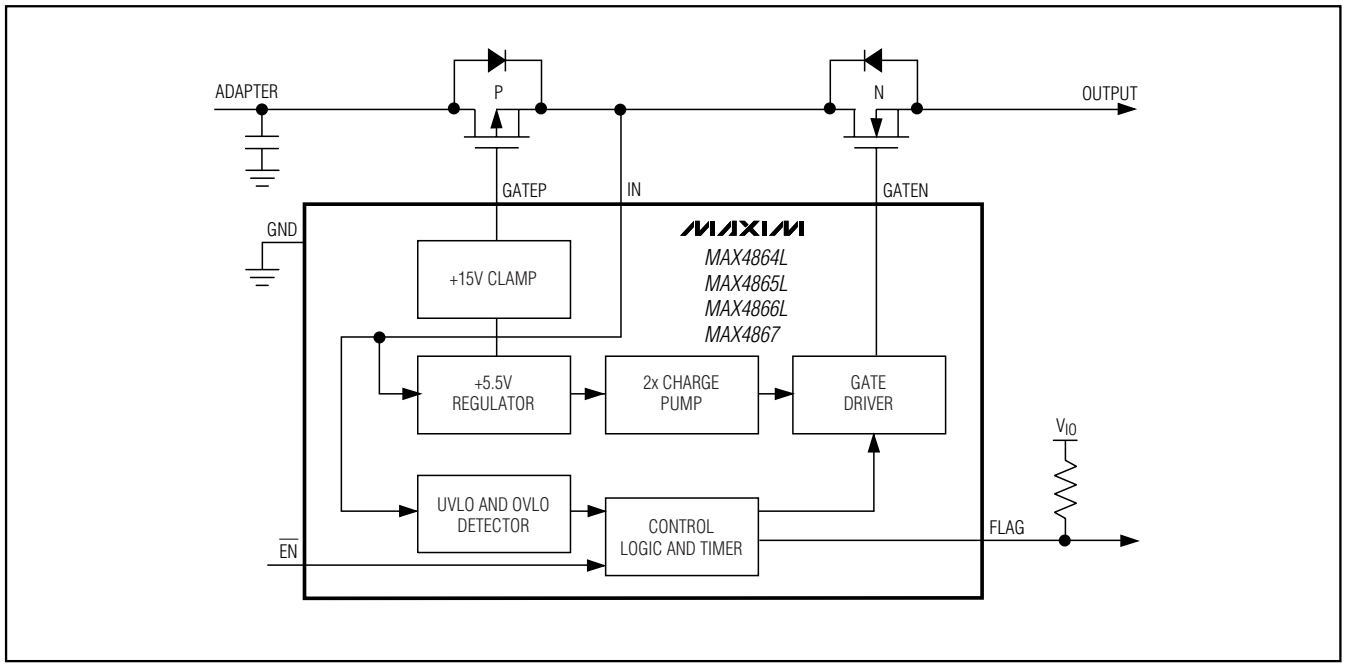
The main difference between tests done using the Human Body Model and IEC 1000-4-2 is higher peak current in IEC 1000-4-2. Because series resistance is lower in the IEC 1000-4-2 ESD test model (Figure 9), the ESD-withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 10 shows the current waveform for the ±8kV IEC 1000-4-2 Level 4 ESD Contact Discharge test. The Air-Gap test involves approaching the device with a charger probe. The Contact Discharge method connects the probe to the device before the probe is energized.

Chip Information

TRANSISTOR COUNT: 727

PROCESS TECHNOLOGY: BiCMOS

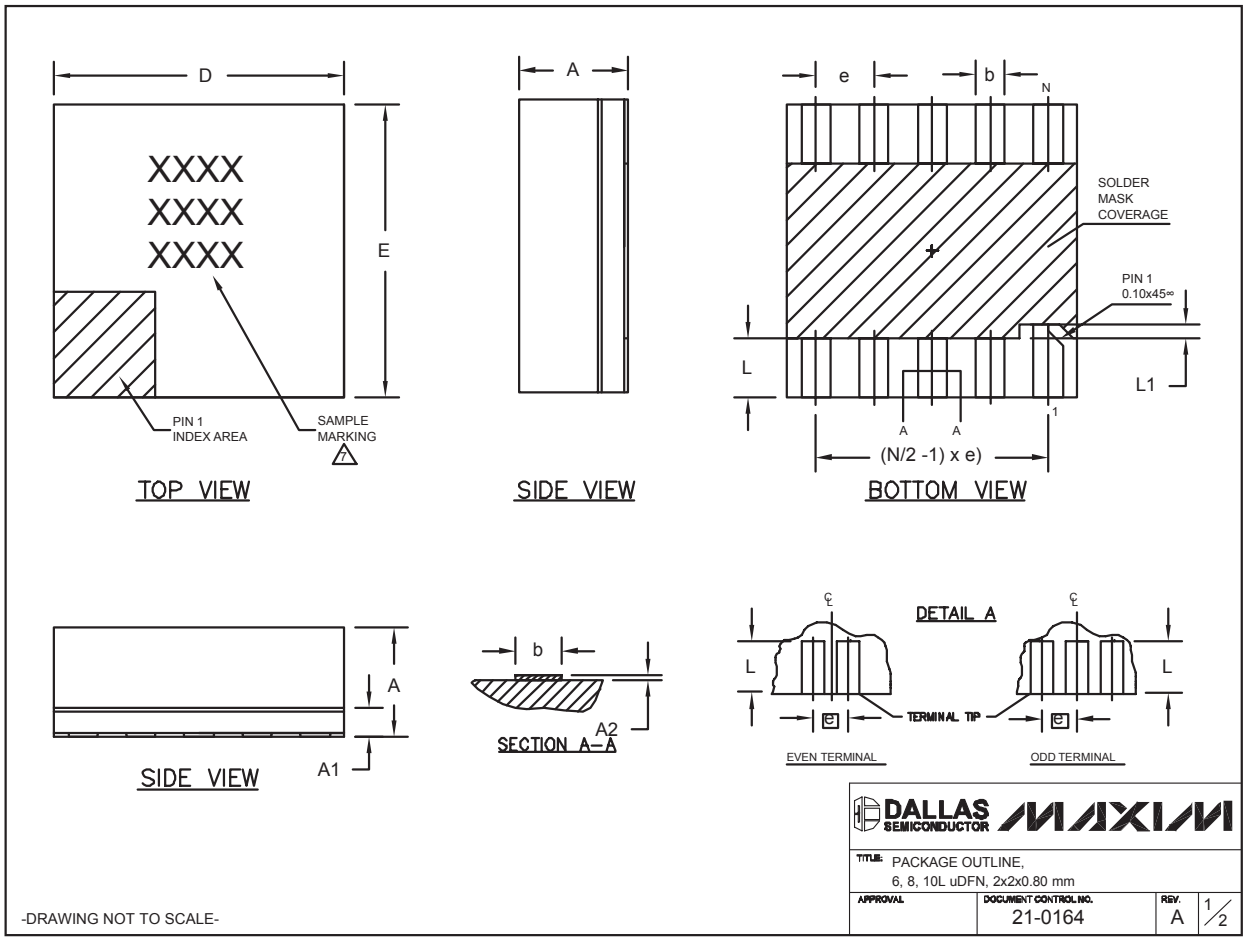
Functional Diagram



Overvoltage Protection Controllers with Reverse Polarity Protection

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS			
SYMBOL	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.15	0.20	0.25
A2	0.020	0.025	0.035
D	1.95	2.00	2.05
E	1.95	2.00	2.05
L	0.30	0.40	0.50
L1	0.10 REF.		

PACKAGE VARIATIONS				
PKG. CODE	N	e	b	(N/2 -1) x e
L622-1	6	0.65 BSC	0.30±0.05	1.30 REF.
L822-1	8	0.50 BSC	0.25±0.05	1.50 REF.
L1022-1	10	0.40 BSC	0.20±0.03	1.60 REF.

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08mm.
3. WARPAGE SHALL NOT EXCEED 0.10mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. "N" IS THE TOTAL NUMBER OF LEADS.
6. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
7. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6, 8, 10L uDFN, 2x2x0.80 mm

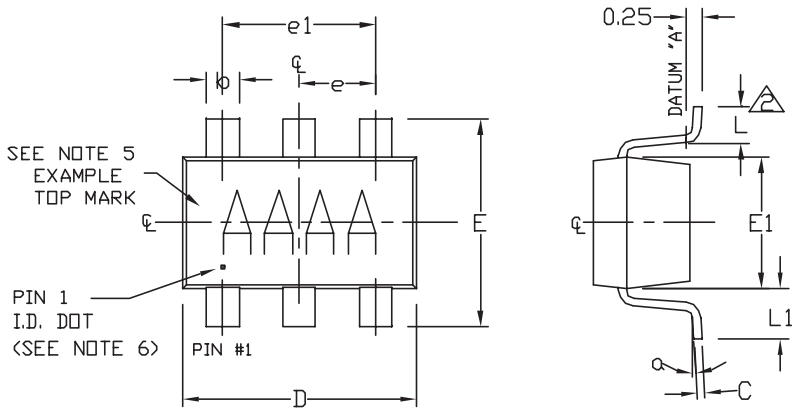
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0164	A	2/2

Overvoltage Protection Controllers with Reverse Polarity Protection

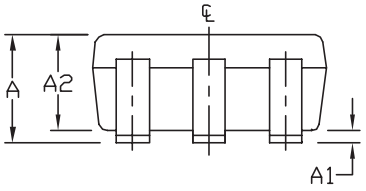
Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

6LSOT.EPS



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.60
L1	0.60 REF.	
e1	1.90 BSC.	
e	0.95 BSC.	
a	0°	10°



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25 MM.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT. (SEE EXAMPLE TOP MARK)
6. PIN 1 I.D. DOT IS 0.3 MM ø MIN. LOCATED ABOVE PIN 1.
7. MEETS JEDEC MO178, VARIATION AB.
8. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEADTIP.
9. LEAD TO BE COPLANAR WITHIN 0.1 MM.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, SOT 6L BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0058	G	1/1

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