February 1999



## **USB10H**

### **Dual P-Channel 2.5V Specified PowerTrench™ MOSFET**

### **General Description**

These P-Channel 2.5V specified MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain low gate charge for superior switching performance.

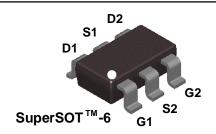
These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the bigger more expensive SO-8 and TSSOP-8 packages are impractical.

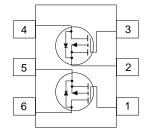
### **Applications**

- Load switch
- Battery protection
- Power management

### **Features**

- -1.9 A, -20 V.  $R_{DS(on)} = 0.170~\Omega~@V_{GS} = -4.5~V$   $R_{DS(on)} = 0.250\Omega~@V_{GS} = -2.5~V$
- Low gate charge (3 nC typical).
- · Fast switching speed.
- $\bullet \;\;$  High performance trench technology for extremely low  $R_{\text{\tiny DS/IONI}}.$
- SuperSOT<sup>TM</sup>-6 package: small footprint (72% smaller than standard SO-8); low profile (1mm thick).





### Absolute Maximum Ratings T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units	
V <sub>DSS</sub>	Drain-Source Voltage		-20	V
V <sub>GSS</sub>	Gate-Source Voltage		±8	V
I <sub>D</sub>	Drain Current - Continuous	(Note 1a)	-1.9	Α
	- Pulsed		-5	
P <sub>D</sub>	Power Dissipation for Single Operation	(Note 1a)	0.96	W
		(Note 1b)	0.9	7
		(Note 1c)	0.7	7
T <sub>J</sub> , T <sub>stg</sub>	Operating and Storage Junction Temperatu	-55 to +150	°C	

### **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	130	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	60	°C/W

**Package Outlines and Ordering Information** 

Device Marking	Device	Reel Size	Tape Width	Quantity	
.306	USB10H	7"	8mm	3000 units	

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Symbol	Parameter	Test Conditions	Min	qyT	Max	Units
Off Char	acteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$	-20			V
ABVDSS ATJ	Breakdown Voltage Temperature Coefficient	$I_D$ = -250 $\mu$ A, Referenced to 25°C		-18		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$			-1	μΑ
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 8 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	$V_{GS} = -8 \text{ V}, V_{DS} = 0 \text{ V}$			-100	nA
On Char	acteristics (Note 2)					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250  \mu A$	-0.4	-0.9	-1.5	V
ΔVGS(th) ΔT <sub>J</sub>	Gate Threshold Voltage Temperature Coefficient	$I_D$ = -250 $\mu$ A, Referenced to 25°C		3		mV/°C
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	$V_{GS} = -4.5 \text{ V}, I_D = -1.9 \text{ A}$ $V_{GS} = -4.5 \text{ V}, I_D = -1.9 \text{ A}$ @125°C $V_{GS} = -2.5 \text{ V}, I_D = -1.7 \text{ A}$		0.127 0.182 0.194	0.170 0.270 0.250	Ω
I <sub>D(on)</sub>	On-State Drain Current	V <sub>GS</sub> = -4.5 V, V <sub>DS</sub> =- 5 V	-5			Α
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = -5 \text{ V}, I_{D} = -1.9 \text{ A}$		4		S
Dvnamic	Characteristics					
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0 V,		441		pF
Coss	Output Capacitance	f = 1.0 MHz		127		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			67		pF
Switchin	g Characteristics (Note 2)					
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = -10 \text{ V}, I_D = -1 \text{ A},$		6	12	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = -4.5 \text{ V}, R_{GEN} = 6 \Omega$		9	18	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			14	25	ns
t <sub>f</sub>	Turn-Off Fall Time			3	9	ns
Qg	Total Gate Charge	$V_{DS} = -10 \text{ V}, I_{D} = -1.9 \text{ A},$		3	4.2	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = -4.5 V		0.7		nC
$Q_{gd}$	Gate-Drain Charge			0.8		nC
Drain-So	ource Diode Characteristics and	d Maximum Ratings				
I <sub>S</sub>	Maximum Continuous Drain-Source Did				-0.8	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = -0.8 \text{ A} \text{ (Note 2)}$		-0.8	-1.2	V

#### Notes:

R<sub>B,JA</sub> is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface
of the drain pins. R<sub>B,JC</sub> is guaranteed by design while R<sub>B,JA</sub> is determined by the user's board design.Both devices are assumed to be operating and
sharing the dissipated heat energy equally.



a) 130 °C/W when mounted on a 0.125 in² pad of 2 oz. copper.



b) 140 °C/W when mounted on a 0.005 in² pad of 2 oz. copper.

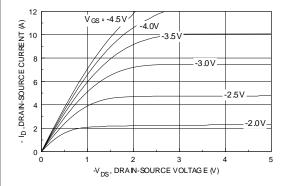


c) 180 °C/W when mounted on a 0.0015 in² pad of 2 oz. copper.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width  $\leq 300~\mu\text{s},~\text{Duty Cycle} \leq 2.0\%$ 

## **Typical Characteristics**



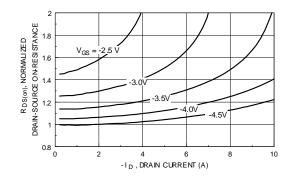
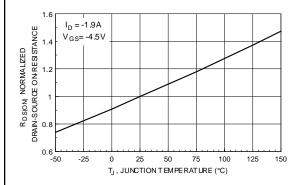


Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.



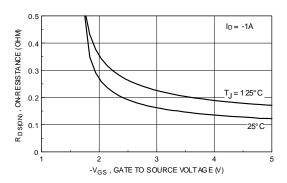
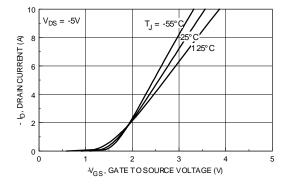


Figure 3. On-Resistance Variation with Temperature.

Figure 4. On-Resistance Variation with Gate-to-Source Voltage.



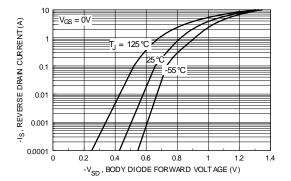
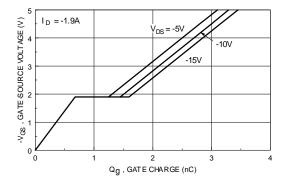


Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

### Typical Characteristics (continued)



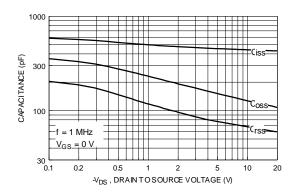
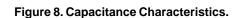
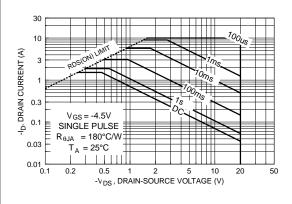


Figure 7. Gate-Charge Characteristics.





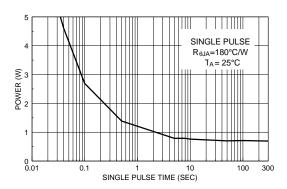


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

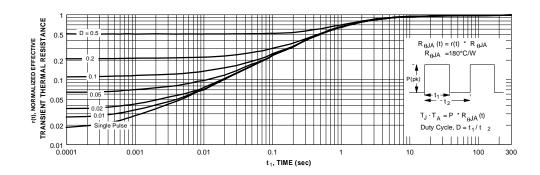
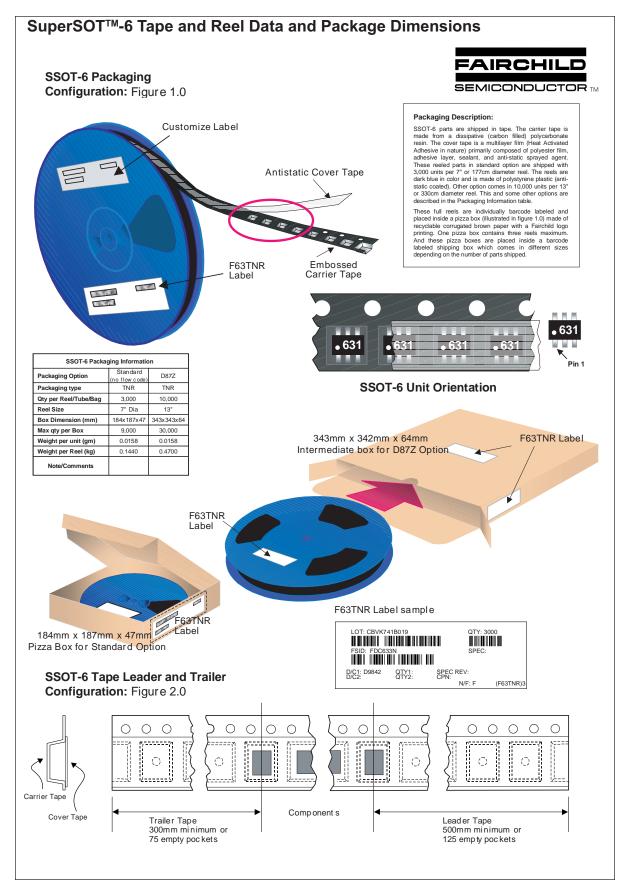
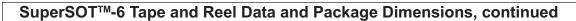


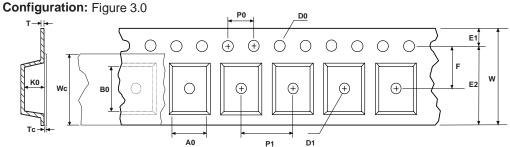
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient themal response will change depending on the circuit board design.





### **SSOT-6 Embossed Carrier Tape**



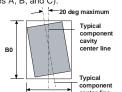


Dimensions are in millimeter														
Pkg type	Α0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	т	Wc	Тс
SSOT-6 (8mm)	3.23 +/-0.10	3.18 +/-0.10	8.0 +/-0.3	1.55 +/-0.05	1.125 +/-0.125	1.75 +/-0.10	6.25 min	3.50 +/-0.05	4.0 +/-0.1	4.0 +/-0.1	1.37 +/-0.10	0.255 +/-0.150	5.2 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation

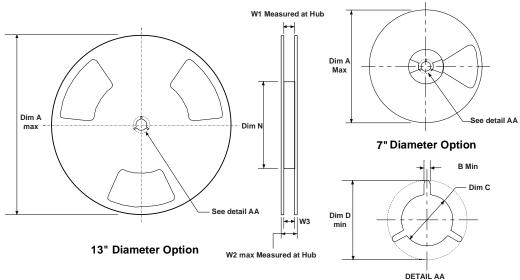


Sketch B (Top View)
Component Rotation



Sketch C (Top View)
Component lateral movement

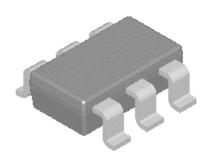
## **SSOT-6 Reel Configuration:** Figure 4.0

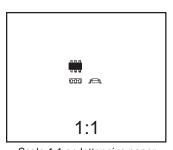


Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
8mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10.9
8mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10.9

## SuperSOT™-6 Tape and Reel Data and Package Dimensions, continued

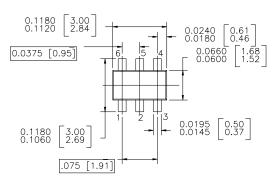
# SuperSOT -6 (FS PKG Code 31, 33)

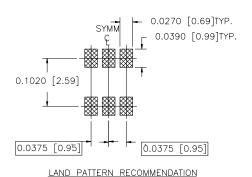




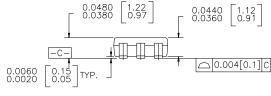
Scale 1:1 on letter size paper
Dimensions shown below are in:
inches [millimeters]

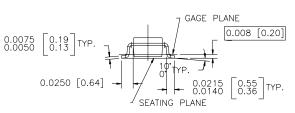
Part Weight per unit (gram): 0.0158





CONTROLLING DIMENSION IS INCH VALUES IN [ ] ARE MILLIMETERS





NOTES: UNLESS OTHERWISE SPECIFIED

1.0 STANDARD LEAD FINISH: 150 MICROINCHES 93.81 MICROMETERS) MINIMUM TIN / LEAD (SOLDER) ON COPPER.

 $2.0\ \mathsf{NO}\ \mathsf{JEDEC}\ \mathsf{REGISTRATION}\ \mathsf{AS}\ \mathsf{OF}\ \mathsf{JULY}\ 1996$ 

SUPER SOT 6 LEADS

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