



October 1987
Revised January 2004

MM74C08 Quad 2-Input AND Gate

General Description

The MM74C08 employs complementary MOS (CMOS) transistors to achieve wide power supply operating range, low power consumption and high noise margin, these gates provide basic functions used in the implementation of digital integrated circuit systems. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swing essentially equal to the supply voltage. No DC power other than that caused by leakage current is consumed during static condition. All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

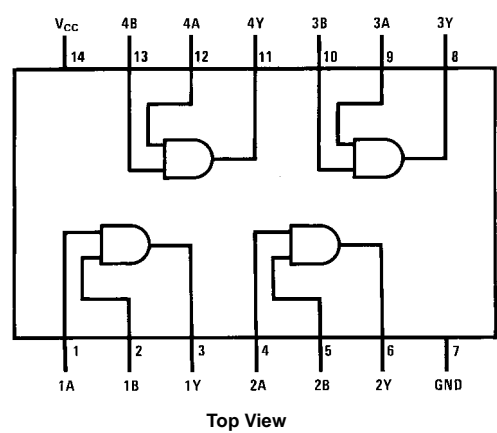
Features

- Wide supply voltage range: 3.0V to 15V
- Guaranteed noise margin: 1.0V
- High noise immunity: 0.45 V_{CC} (typ.)
- Low power TTL compatibility:
Fan out of 2 driving 74L
- Low power consumption: 10 nW/package (typ.)

Ordering Code:

| Order Number | Package Number | Package Description |
|--------------|----------------|--|
| MM74CD8N | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Connection Diagram



Truth Table

| Inputs | | Outputs |
|--------|---|---------|
| A | B | Y |
| L | L | L |
| L | H | L |
| H | L | L |
| H | H | H |

H = HIGH Level
L = LOW Level

MM74C08 Quad 2-Input AND Gate

Absolute Maximum Ratings(Note 1)

| | |
|---|--------------------------|
| Voltage at Any Pin | -0.3V to $V_{CC} + 0.3V$ |
| Operating Temperature Range | -55°C to +125°C |
| Storage Temperature Range | -65°C to +150°C |
| Power Dissipation (P_D) | |
| Dual-In-Line | 700 mW |
| Small Outline | 500 mW |
| Operating V_{CC} Range | 3.0V to 15V |
| Absolute Maximum V_{CC} | 18V |
| Lead Temperature (Soldering, 10 seconds) | 260°C |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics table provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across the guaranteed temperature range, unless otherwise noted

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|--------------------------------------|---|----------------|--------|-----|---------|
| CMOS TO CMOS | | | | | | |
| $V_{IN(1)}$ | Logical "1" Input Voltage | $V_{CC} = 5.0V$ | 3.5 | | | V |
| | | $V_{CC} = 10V$ | 8.0 | | | |
| $V_{IN(0)}$ | Logical "0" Input Voltage | $V_{CC} = 5.0V$ | | | 1.5 | V |
| | | $V_{CC} = 10V$ | | | 2.0 | |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | $V_{CC} = 5.0V, I_O = -10 \mu A$ | 4.5 | | | V |
| | | $V_{CC} = 10V, I_O = -10 \mu A$ | 9.0 | | | |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | $V_{CC} = 5.0V, I_O = 10 \mu A$ | | | 0.5 | V |
| | | $V_{CC} = 10V, I_O = 10 \mu A$ | | | 1.0 | |
| $I_{IN(1)}$ | Logical "1" Input Current | $V_{CC} = 15V, V_{IN} = 15V$ | | 0.005 | 1.0 | μA |
| $I_{IN(0)}$ | Logical "0" Input Current | $V_{CC} = 15V, V_{IN} = 0V$ | -1.0 | -0.005 | | μA |
| I_{CC} | Supply Current | $V_{CC} = 15V$ | | 0.01 | 15 | μA |
| CMOS/LPTTL INTERFACE | | | | | | |
| $V_{IN(1)}$ | Logical "1" Input Voltage | 74C, $V_{CC} = 4.75V$ | $V_{CC} - 1.5$ | | | V |
| $V_{IN(0)}$ | Logical "0" Input Voltage | 74C, $V_{CC} = 4.75V$ | | | 0.8 | V |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | 74C, $V_{CC} = 4.75V, I_O = -360 \mu A$ | 2.4 | | | V |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | 74C, $V_{CC} = 4.75V, I_O = 360 \mu A$ | | | 0.4 | V |
| OUTPUT DRIVE (see Family Characteristics Data Sheet) $T_A = 25^\circ C$ (short circuit current) | | | | | | |
| I_{SOURCE} | Output Source Current (P-Channel) | $V_{CC} = 5.0V, V_{OUT} = 0V$ | -1.75 | -3.3 | | mA |
| I_{SOURCE} | Output Source Current (P-Channel) | $V_{CC} = 10V, V_{OUT} = 0V$ | -8.0 | 15 | | mA |
| I_{SINK} | Output Sink Current (N-Channel) | $V_{CC} = 5.0V, V_{OUT} = V_{CC}$ | 1.75 | 3.6 | | mA |
| I_{SINK} | Output Sink Current (N-Channel) | $V_{CC} = 10V, V_{OUT} = V_{CC}$ | 8.0 | 16 | | mA |

AC Electrical Characteristics (Note 2)

(MM74C08) $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, unless otherwise specified

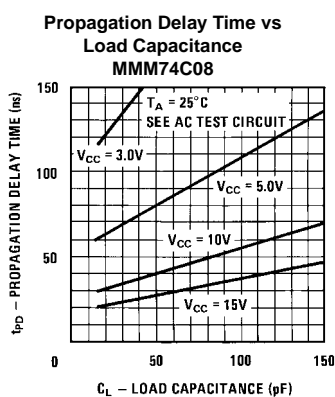
| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------------|--|------------------------|-----|-----|-----|-------|
| t_{pd0} , t_{pd1} | Propagation Delay Time to Logical "1" or "0" | $V_{CC} = 5.0\text{V}$ | | 80 | 140 | ns |
| | | $V_{CC} = 10\text{V}$ | | 40 | 70 | |
| C_{IN} | Input Capacitance | (Note 3) | | 5.0 | | pF |
| C_{PD} | Power Dissipation Capacitance | (Note 4) Per Gate | | 14 | | pF |

Note 2: AC Parameters are guaranteed by DC correlated testing.

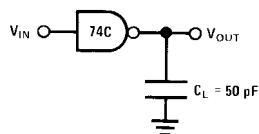
Note 3: Capacitance is guaranteed by periodic testing.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics Application Note—AN-90.

Typical Performance Characteristics

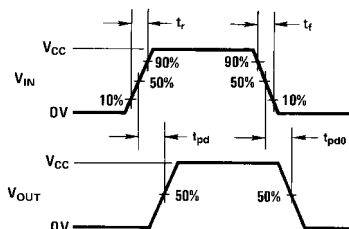


AC Test Circuit

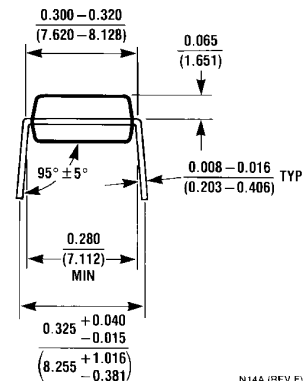
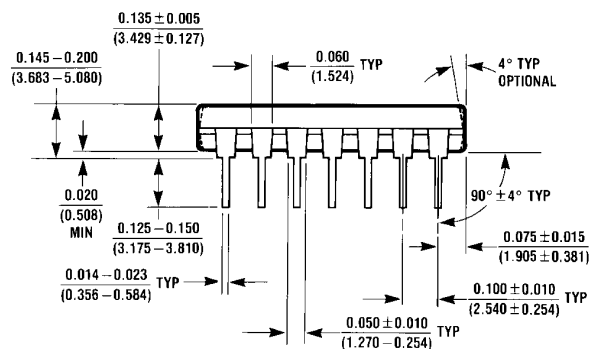
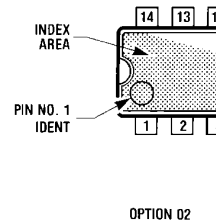
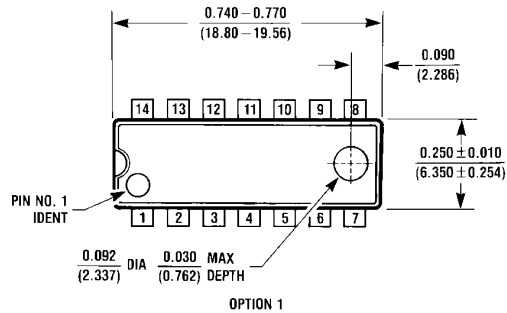


Note: Delays measured with input t_r , $t_f = 20\text{ ns}$

Switching Time Waveforms



Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

N14A (REV F)

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com