

March 2000 Revised March 2000

FST16861 20-Bit Bus Switch

General Description

The Fairchild Switch FST16861 provides 20-Bits of highspeed CMOS TTL-compatible bus switching. The low ON resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device is organized as a 10-bit or 20-Bit bus switch. When $\overline{\text{OE}}_1$ is LOW, the switch is ON and Port 1A is connected to Port 1B. When $\overline{\text{OE}}_2$ is LOW, Port 2A is connected to Port 2B. When $\overline{\text{OE}}_X$ is HIGH, a high impedance state exists between the A and B Ports.

Features

- \blacksquare 4 Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.

Ordering Code:

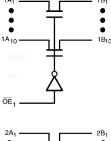
Order Number	Package Number	Package Description
FST16861MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

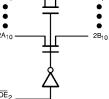
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Logic Diagram





Pin Descriptions

Pin Name	Description			
$\overline{OE}_1, \overline{OE}_2$	Bus Switch Enables			
1A, 2A	Bus A			
1B, 2B	Bus B			

Truth Table

Inp	uts	Inputs/Outputs				
ŌE ₁	OE ₂	1A, 1B	2A, 2B			
L	L	1A = 1B	2A = 2B			
L	Н	1A = 1B	Z			
Н	L	Z	2A = 2B			
Н	Н	Z	Z			

Absolute Maximum Ratings(Note 1)

Supply Voltage (V _{CC})	0.5V to +7.0V
DC Switch Voltage (V _S) (Note 2)	-0.5V to +7.0V
DC Input Voltage (V _{IN}) (Note 3)	-0.5V to +7.0V
DC Input Diode Current (I _{IK}) V _{IN} <0V	-50mA
DC Output (I _{OUT}) Current	128mA
DC V _{CC} /GND Current (I _{CC} /I _{GND})	±100mA
Storage Temperature Range (T _{STG})	-65°C to +150 °C

Recommended Operating Conditions (Note 4)

 $\begin{array}{ll} \mbox{Power Supply Operating (V_{CC})} & 4.0 \mbox{V to } 5.5 \mbox{V} \\ \mbox{Input Voltage (V_{IN})} & 0 \mbox{V to } 5.5 \mbox{V} \\ \mbox{Output Voltage (V_{OUT})} & 0 \mbox{V to } 5.5 \mbox{V} \\ \mbox{Input Rise and Fall Time (t_f, t_f)} \end{array}$

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions

for actual device operation.

Note 2: V_{S} is the voltage observed/applied at either the A or B Ports across the switch.

Note 3: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 4: Unused control inputs must be held high or low. They may not float.

DC Electrical Characteristics

	Parameter	V _{CC} (V)	$T_A = -40 ^{\circ}\text{C} \text{ to } +85 ^{\circ}\text{C}$				
Symbol			Min	Typ (Note 5)	Max	Units	Conditions
V _{IK}	Clamp Diode Voltage	4.5			-1.2	V	I _{IN} = -18mA
V _{IH}	HIGH Level Input Voltage	4.0-5.5	2.0			V	
V _{IL}	LOW Level Input Voltage	4.0-5.5			0.8	V	
I	Input Leakage Current	5.5			±1.0	μΑ	0 ≤ V _{IN} ≤ 5.5V
		0			±1.0	μΑ	V _{IN} = 5.5V
I _{OZ}	OFF-STATE Leakage Current	5.5			±1.0	μΑ	0 ≤ A, B ≤ V _{CC}
R _{ON}	Switch On Resistance	4.5		4	7	Ω	V _{IN} = 0V, I _{IN} = 64mA
	(Note 6)	4.5		4	7	Ω	V _{IN} = 0V, I _{IN} = 30mA
		4.5		7	12	Ω	V _{IN} = 2.4V, I _{IN} = 15mA
		4.0		11	20	Ω	V _{IN} = 2.4V, I _{IN} = 15mA
I _{CC}	Quiescent Supply Current	5.5			3	μΑ	V _{IN} = V _{CC} or GND, I _{OUT} = 0
ΔI _{CC}	Increase in I _{CC} per Input	5.5			2.5	mA	One input at 3.4V
							Other inputs at V _{CC} or GND

Note 5: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 6: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40$ °C to +85 °C, $C_L = 50$ pF, RU = RD = 500Ω						
		V _{CC} = 4.5 - 5.5V		V _{CC} = 4.0V		Units	Conditions	Figure No.
		Min	Max	Min	Max			
t _{PHL} ,t _{PLH}	Prop Delay Bus-to-Bus (Note 7)		0.25		0.25	ns	V _I = OPEN	Figure 1, Figure 2
t _{PZH} , t _{PZL}	Output Enable Time	1.0	5.0		5.3	ns	$V_I = 7V$ for t_{PZL} $V_I = OPEN$ for t_{PZH}	Figure 1, Figure 2
t _{PHZ} , t _{PLZ}	Output Disable Time	1.0	6.0		6.3		$V_I = 7V$ for t_{PLZ} $V_I = OPEN$ for t_{PHZ}	Figure 1, Figure 2

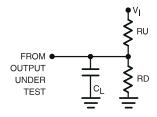
Note 7: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 8)

Symbol Parameter		Тур	Max	Units	Conditions
C _{IN}	Control Pin Input Capacitance	3		pF	$V_{CC} = 5.0V, V_{IN} = 0V$
C _{I/O}	Input/Output Capacitance "OFF State"	6		pF	V_{CC} , $\overline{OE} = 5.0V$, $V_{IN} = 0V$

Note 8: T_A = +25°C, f = 1 Mhz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50Ω source terminated in 50Ω Note: C_L includes load and stray capacitance Note: Input PRR = 1.0 MHz, T_W = 500 ns

FIGURE 1. AC Test Circuit

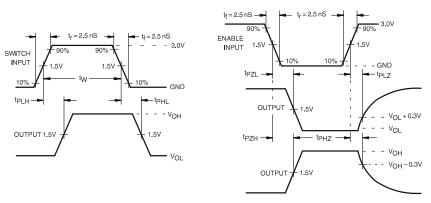
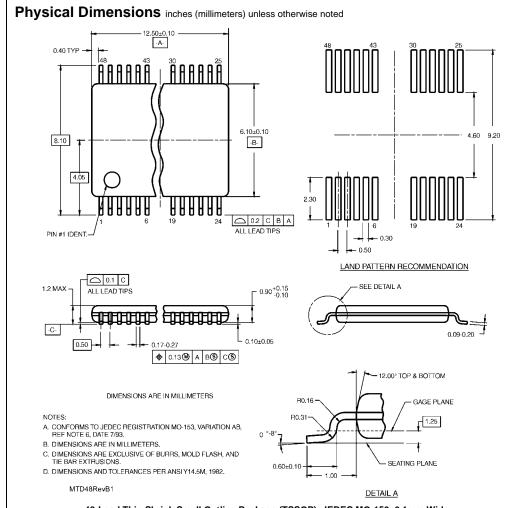


FIGURE 2. AC Waveforms



48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384(FST3384) bus switch product.

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