

March 2000

## FDP5645/FDB5645

#### 60V N-Channel PowerTrench® MOSFET

#### **General Description**

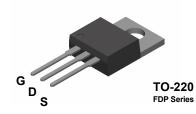
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable  $R_{\text{DS(ON)}}$  specifications.

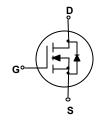
The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

#### **Features**

- 80 A, 60 V.  $R_{DS(ON)} = 0.0095 \ \Omega \ @V_{GS} = 10 \ V$  $R_{DS(ON)} = 0.011 \ \Omega \ @V_{GS} = 6 \ V.$
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- High performance trench technology for extremely low R<sub>DS/(ON)</sub>.
- 175°C maximum junction temperature rating.







S TO-263AB
FDB Series

**Absolute Maximum Ratings** T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	FDP5645 FDB5645	Units
V <sub>DSS</sub>	Drain-Source Voltage	60	V
V <sub>GSS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Maximum Drain Current – Continuous (note 3)	80	А
	– Pulsed	300	7
P <sub>D</sub>	Total Power Dissipation @ T <sub>C</sub> = 25°C	125	W
	Derate above 25°C	0.83	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	-65 to +175	°C
TL	Maximum lead termperature for soldering purposes, 1/8" from case for 5 seconds	+275	°C

### **Thermal Characteristics**

R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	1.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	°C/W

**Package Marking and Ordering Information** 

FDB5645 FDB5645 13"	0.4	000 ''
1 000000	24mm	800 units
FDP5645 FDP5645 note 2		

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Drain-Sc	ource Avalanche Ratings (Note 1	1)				
W <sub>DSS</sub>	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 40 \text{ V}, \qquad I_D = 80 \text{ A}$			800	mJ
lar	Maximum Drain-Source Avalanche Current				80	Α
Off Char	racteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	60			V
<u>ΔBV dss</u> ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , Referenced to 25°C		64		mV/°C
DSS	Zero Gate Voltage Drain Current	$V_{DS} = 48 \text{ V},  V_{GS} = 0 \text{ V}$			1	μА
GSSF	Gate-Body Leakage, Forward	$V_{GS} = 20 \text{ V}, \qquad V_{DS} = 0 \text{ V}$			100	nA
IGSSR	Gate-Body Leakage, Reverse	$V_{GS} = 20 \text{ V},  V_{DS} = 0 \text{ V}$			-100	nA
On Char	acteristics (Note 1)					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{CS}, I_D = 250 \mu\text{A}$	2		4	V
ΔV GS(th) ΔT <sub>J</sub>	Gate Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , Referenced to $25^{\circ}\text{C}$		-7.8		mV/°C
R <sub>DS(on)</sub>	Static Drain–Source On–Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 40 A V <sub>GS</sub> =10V, I <sub>D</sub> = 40 A, T <sub>J</sub> =125°C V <sub>GS</sub> = 6 V, I <sub>D</sub> = 38 A		8 13 9	9.5 18 11	mΩ
I <sub>D(on)</sub>	On-State Drain Current	$V_{GS} = 10 \text{ V}, \qquad V_{DS} = 10 \text{ V}$	60			Α
<b>g</b> FS	Forward Transconductance	$V_{DS} = 5 \text{ V}, \qquad I_{D} = 40 \text{ A}$		88		S
Dvnamio	Characteristics					
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 30 \text{ V}, \qquad V_{GS} = 0 \text{ V},$		4468		pF
Coss	Output Capacitance	f = 1.0 MHz		810		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			198		pF
Switchin	ng Characteristics (Note 2)			I.	ı	I.
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = 30 \text{ V}, \qquad I_{D} = 1 \text{ A},$		21	30	ns
t <sub>r</sub>	Turn–On Rise Time	$V_{GS} = 10 \text{ V}, \qquad R_{GEN} = 6 \Omega$		13	20	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	1		77	90	ns
t <sub>f</sub>	Turn-Off Fall Time			42	50	ns
Qg	Total Gate Charge	$V_{DS} = 30 \text{ V}, \qquad I_{D} = 80 \text{ A},$		76	107	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 10 V		18		nC
Q <sub>gd</sub>	Gate-Drain Charge			21		nC
	ource Diode Characteristics a	and Maximum Ratings				
ls	Maximum Continuous Drain–Source				80	Α
ls s	Maximum Pulsed Drain-Source Diod			ĺ	300	Α
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	$V_{GS} = 0 \text{ V},  I_S = 40 \text{ A}$		0.9	1.3	V

#### Notes

- 1. Pulse Test: Pulse Width <  $300\mu$ s, Duty Cycle < 2.0%
- 2. TO-220 package is supplied in tube / rail @ 45 pieces per rail.
- 3. Calculated continuous current based on maximum allowable junction temperature. Actual maximum continuous current limited by package constraints to 75A

## **Typical Characteristics**

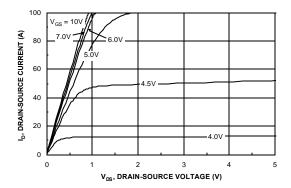


Figure 1. On-Region Characteristics.

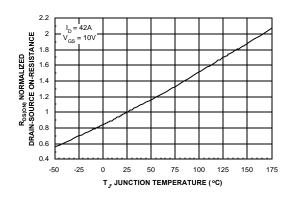


Figure 3. On-Resistance Variation withTemperature.

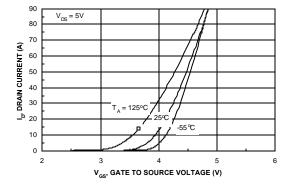


Figure 5. Transfer Characteristics.

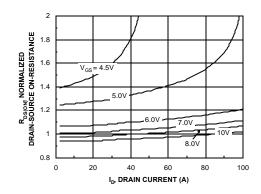


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

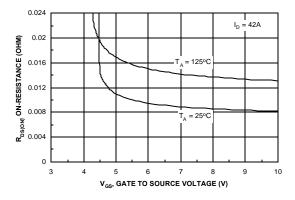


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

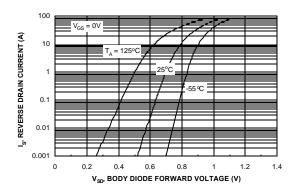
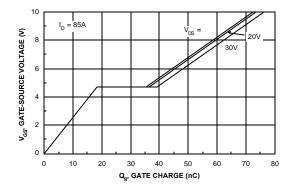


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## **Typical Characteristics**



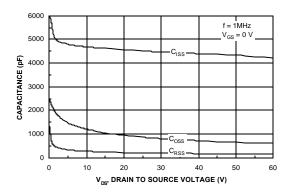
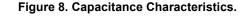
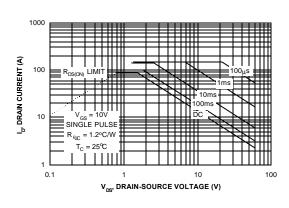


Figure 7. Gate Charge Characteristics.





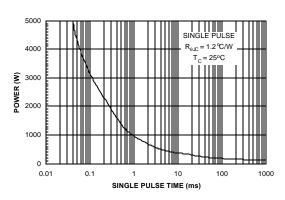


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

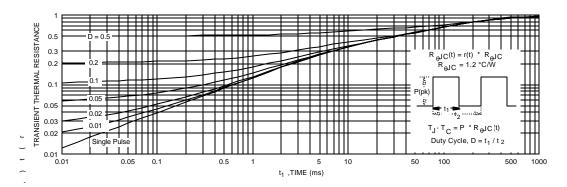
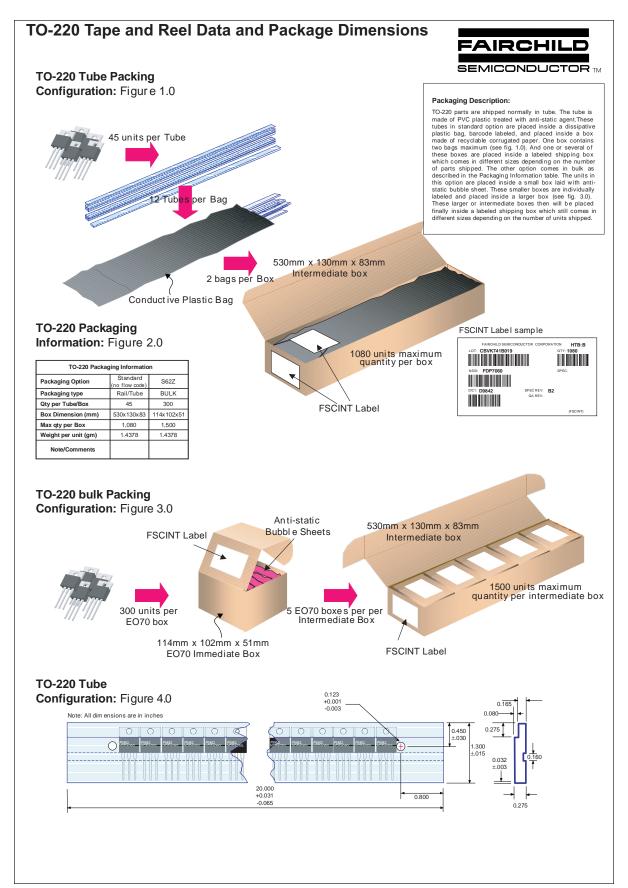


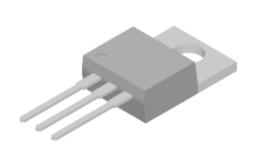
Figure 11. Transient Thermal Response Curve.

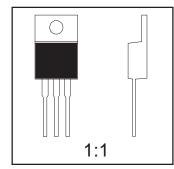
Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.



## TO-220 Tape and Reel Data and Package Dimensions, continued

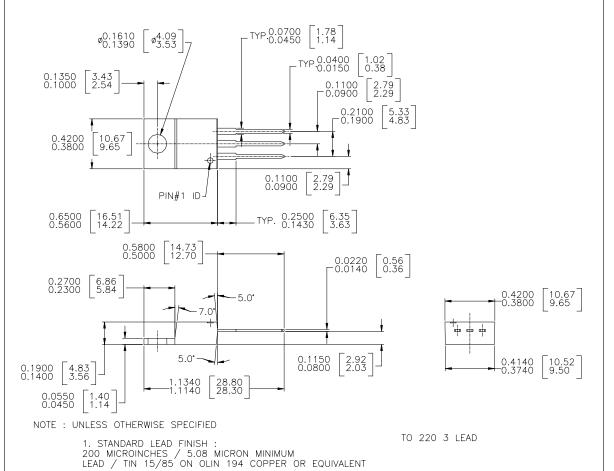
## TO-220 (FS PKG Code 37)

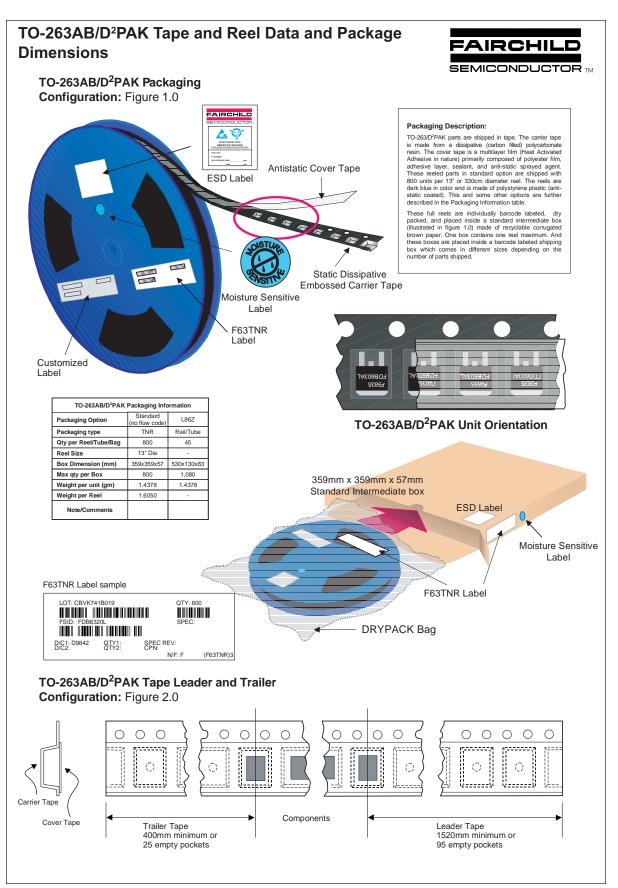




Scale 1:1 on letter size paper
Dimensions shown below are in:
inches [millimeters]

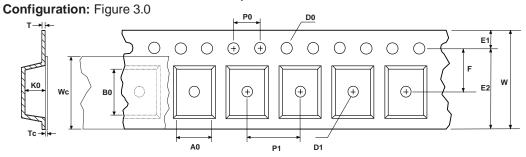
Part Weight per unit (gram): 1.4378





## TO-263AB/D<sup>2</sup>PAK Tape and Reel Data and Package Dimensions, continued

### TO-263AB/D<sup>2</sup>PAK Embossed Carrier Tape



## User Direction of Feed

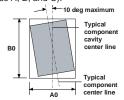
Dimensions are in millimeter														
Pkg type	Α0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	Т	Wc	Тс
TO263AB/ D <sup>2</sup> PAK (24mm)	10.60 +/-0.10	15.80 +/-0.10	24.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	22.25 min	11.50 +/-0.10	16.0 +/-0.1	4.0 +/-0.1	4.90 +/-0.10	0.450 +/-0.150	21.0 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)

Component Rotation

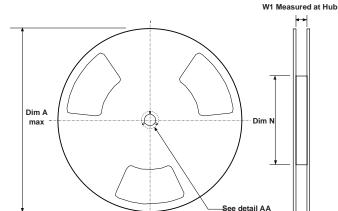


Sketch B (Top View)
Component Rotation

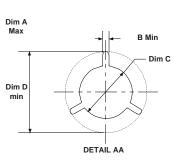


Sketch C (Top View)
Component lateral movement

# **TO-263AB/D<sup>2</sup>PAK Reel Configuration:** Figure 4.0



13" Diameter Option



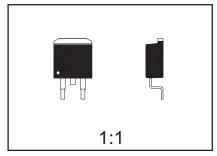
W2 max Measured at Hub

Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
24mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.961 +0.078/-0.000 24.4 +2/0	1.197 30.4	0.941 - 0.1.079 23.9 - 27.4

## TO-263AB/D<sup>2</sup>PAK Tape and Reel Data and Package Dimensions, continued

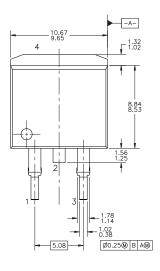
## TO-263AB/D<sup>2</sup>PAK (FS PKG Code 45)

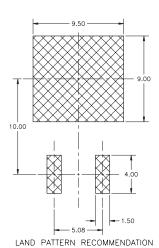


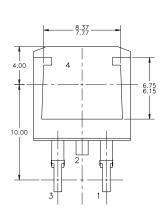


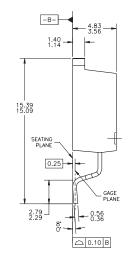
Scale 1:1 on letter size paper Dimensions shown below are in: inches [millimeters]

Part Weight per unit (gram): 1.4378









- NOTES: UNLESS OTHERWISE SPECIFIED

  A) ALL DIMENSIONS ARE IN MILLIMETERS.
  B) STANDARD LEAD FINISH:
  200 MICROINCHES / 5.08 MICROMETERS MIN.
  LEAD/TIN 15/85 ON OLIN 194 COPPER OR
  EQUIVALENT.
  C) MAXIMUM YERTICAL BURR ON HEATSINK NOT
  TO EXCEED 0.003 INCH / 0.05mm.
  D) NO PACKAGE CHIPS, CRACKS OR SURFACE
  IDENTIFICATION ALLOWED AFTER FORMING.
  E) REFERENCE JEDEC, TO—265, ISSUE C,
  VARIATION AB, DATED 2/92.

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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