Switching Waveforms Of The L²FET: A 5 Volt Gate-Drive Power MOSFET

Application Note | October 1999 | AN-7501

The switching waveforms of a series of power MOSFET devices called Logic Level FETs (L²FETs) and featuring a 5V gate drive are presented and contrasted with those of the more conventional 10V gate drive devices. A new method of characterizing MOSFET switching performance is discussed in which the MOSFET is treated as a vertical JFET driven in cascade from a low voltage lateral MOS. The 2:1 advantage in rise and fall time and the 4:1 reduction in switching "dynamic $V_{(SAT)}$" dissipation with constant drive power of the L²FET over the 10V MOSFET are demonstrated and discussed.

Background

A series of power MOSFET devices called Logic Level FETs, or L²FETs, is compatible with the 5V power supply used for logic circuitry. L²FETs retain the on resistance, drain current, and blocking voltage ratings of their 10V predecessors, but operate from a much less costly 5V supply.

The reduction in gate drive voltage is the result of halving the thickness of the gate insulator from the industry standard 100nm to 50nm (500Å). Since the surface inversion of the MOS channel is determined by the gate insulator voltage field, halving the insulator thickness halves the required gate voltage to achieve the same surface inversion thereby not compromising drain characteristics.

The apparent conclusion from a study of the switching waveforms of the new device that halving the gate oxide thickness would double the gate capacitance and halve the switching speed does not prove true. Measurements demonstrate empirically a 2:1 increase in switching speed for the L²FET over its 100nm predecessor, where gate drive power is the same for both devices. The "dynamic $V_{(SAT)}$" dissipation is lowered by a factor of four. The apparent anomalies are explained with the aid of a new method of switching characterization developed by treating the power MOSFET as a grounded gate, depletion mode, vertical JFET driven in cascade by a grounded source, enhancement mode, lateral MOS. The waveforms and switching characterization methods are described in detail below.

L²FET Characteristics Compared to Standard Types - A Brief Review

A large number of power MOSFETs of the L²FET structure have been announced. These devices were designed to be totally interchangeable with the standard power MOSFET with respect to output characteristics, while offering twice the gate sensitivity, as shown in Figures 1, 2, and 3, which are comparisons of the industry standard RFM10N15 with its Logic Level FET counterpart, the RFM10N15L. (Although the L suffix notation in the type number will ultimately be valid for the entire product matrix, the L²FET product currently available is available in both p-channel and n-channel devices handling 200V or less, with 50A ratings or less.)

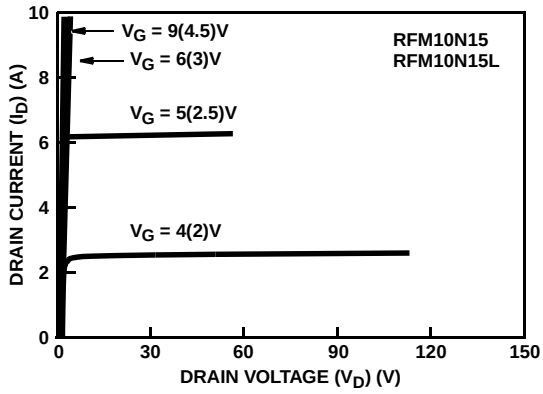


FIGURE 1. DRAIN CURRENT vs. DRAIN VOLTAGE CURVES FOR REPRESENTATIVE STANDARD AND L²FET DEVICES

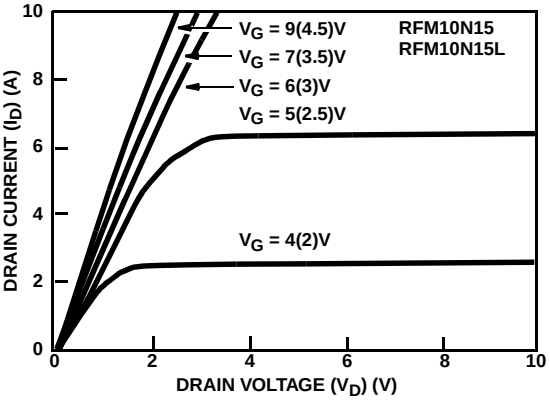


FIGURE 2. DRAIN CURRENT vs. LOW DRAIN VOLTAGE CURVES FOR REPRESENTATIVE STANDARD AND L²FET DEVICES DEMONSTRATING THAT R_{ON} HAS NOT BEEN SACRIFICED IN THE L²FET

Figures 1 and 2 are plots of drain current versus drain voltage with gate voltage as the running parameter. The L²FET gate voltage is in parenthesis. The low drain voltage curves of Figure 2 demonstrate that $r_{DS(ON)}$ has not been sacrificed in the L²FET. Figure 3 is the transfer characteristic comparison for three different temperatures. The abscissa has two scales to reflect the different gate sensitivities; again, the logic level part values are in parenthesis. It is evident from the curve that:

1. The threshold voltage is scaled down by a factor of two for the L²FET.
2. The threshold voltage temperature coefficient in mV/°C is scaled down.
3. The current level for zero temperature coefficient is unchanged.
4. The transconductance is scaled up by a factor of two.

All other L^2FETs have similar relationships to their respective predecessors.

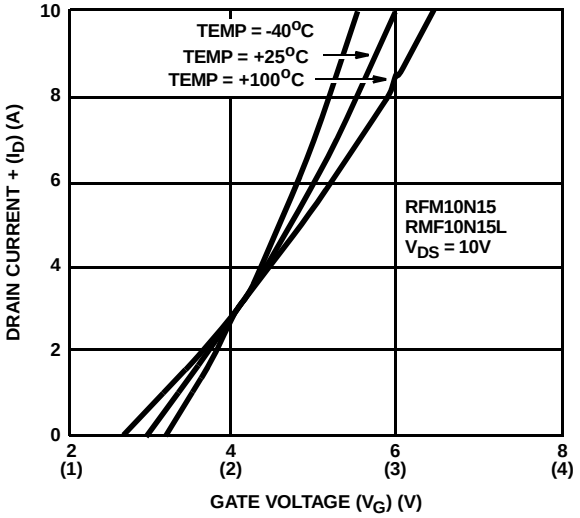


FIGURE 3. TRANSFER CHARACTERISTIC

Switching Waveforms with Conventional Drive

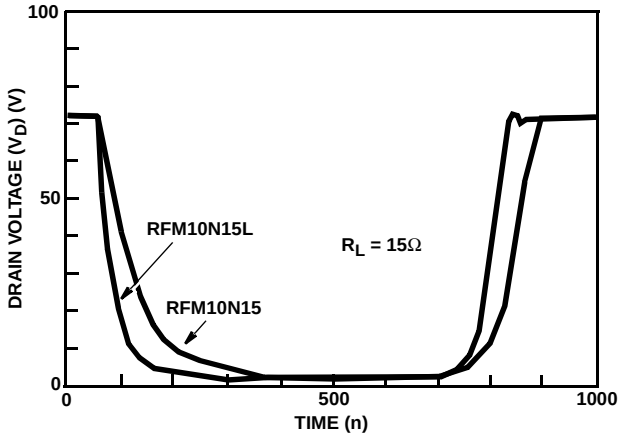
The first concern when comparing devices with such a large difference of transfer sensitivity is one of "other things being equal". If the standard device is driven between zero and ten volts with an R_G of 25Ω, impedance transformation dictates that the L^2FET should be driven between zero and five volts with an R_G of $6^1/_4$ Ω, thereby transforming open circuit voltage and short circuit current by factors of 2 (or $^1/_2$). With these parameters, either drive system will supply a peak P_G, or generator dissipation, of one watt.

Figure 4 displays the drain voltage versus time of the RFM10N15 and the RFM10N15L when each is driven as described above with a 5A, 75V resistive load line. The time scale is 100ns per division. The table under the graph compares on delay time, rise time, off delay time, and fall time for each device. The times are measured in the normal manner, that is, involving the 10% and 90% points of the input voltage and output voltage waveforms.

Note that:

1. The rise and fall times are not symmetrical
2. The L^2FET is faster
3. There is a "dynamic $V_{(SAT)}$" type of behavior
4. The "dynamic $V_{(SAT)}$" is of a lesser amplitude for the L^2FET

These observations are discussed below.



TYPE	GATE DRIVE	R_G (Ω)	$t_{D(ON)}$ (ns)	$t_{(RISE)}$ (ns)	$t_{D(OFF)}$ (ns)	$t_{(FALL)}$ (ns)
RFM10N15 (100nm)	0-10V	25	15	120	123	73
RFM10N15L (50nm)	0-5V	6.25	11	57	104	62

FIGURE 4. DRAIN VOLTAGE vs. TIME CURVES FOR REPRESENTATIVE STANDARD AND L^2FET DEVICES

Switching Waveforms with Constant Current Drive

The power MOSFET is a current driven device during transitions due to the charging or discharging of capacitances. In actual applications, most drive circuits exhibit a first order approximation to a constant current where the voltage compliance is determined by the ground potential or the drive circuit power supply voltage. The on current may not equal the off current; this situation is addressed below.

Figure 5 presents the curves for the RFM10N15 and RFM10N15L when each is driven from a current generator whose $I_{G1} = I_{G2}$, with gate voltage limits of zero and 10 or (5) volts. The drive current is kept the same for both devices in this case even though the L^2FET receives less drive power or energy. The value for I_{G1} and I_{G2} was chosen as 5mA; the time scale is 1µs/division.

Note that:

1. The rise and fall times of a given device are the same with current drive.
2. The two devices have similar output waveforms in most regions.
3. There is a persistent "dynamic $V_{(SAT)}$" even at slow switching speeds.
4. The "dynamic $V_{(SAT)}$" curves are symmetrical during the low drain voltage portion of the turn on and turn off portion.
5. The "dynamic $V_{(SAT)}$" curves are lower in amplitude by a factor of approximately two for the L^2FET.

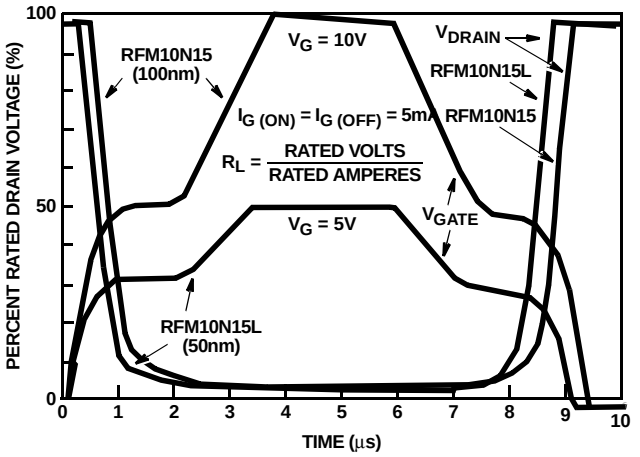


FIGURE 5. CHARACTERIZATION CURVES FOR REPRESENTATIVE DEVICES DRIVEN FROM A CURRENT GENERATOR

Large Signal Equivalent Circuit of the MOSFET

If we are to understand the differences and similarities of the L^2FET relative to the conventional power MOSFET, the conventional power MOSFET must first be understood. Figure 6 shows a properly proportioned cross sectional view of the power MOSFET.

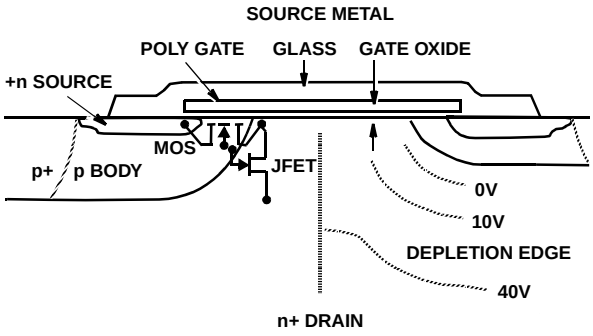


FIGURE 6. CROSS SECTION OF POWER MOSFET

When the drain voltage is very low and the gate is forward biased, an accumulation layer exists for the n- region beneath the gate. This layer may be thought of as serving the function of the drain for the lateral MOS. In addition, it serves as a source for a vertical depletion mode JFET. The gate of the JFET is formed by the body diffusion, particularly in the neck region. The JFET drain is the n+ region usually though of as being the MOSFET drain. This situation is shown in Figure 6, where the cross sectional view of the MOSFET is shown. The lateral MOS and the vertical JFET are schematically implied by the left half of Figure 6. The right half indicates the edge of the depletion width for several drain voltages. Note how the JFET pinches off, such that increased drain voltage is supported predominately by the JFET. This structure is schematically represented as shown in Figure 7. Note that the third quadrant diode is caused by the p-n junction associated with the gate and drain characteristic (common to all JFETs). A parasitic n-p-n transistor is not shown, nor is it discussed in this Note. Voltage node (4) is within the device, and is not precisely a single node, as represented.

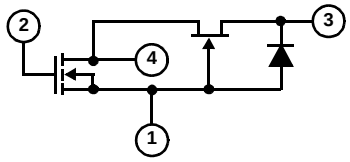


FIGURE 7. SCHEMATIC REPRESENTATION OF THE CROSS SECTION OF FIGURE 6

Interelectrode Capacitance

The equivalent circuit of Figure 7 contains four voltage nodes. Therefore, six capacitors will exist to couple these nodes. The switching waveforms are determined by these capacitors and the small signal equivalent circuit of the MOS and JFET. Of course, the MOS and JFET small signal equivalent circuits are nonlinear functions of voltage and current and invariant with frequency. Similarly, the capacitors are nonlinear with voltage and current.

Industry data sheets show three terminal characterization of this four node network at zero drain current. Under this condition, the transconductance and output resistance are zero and infinity for both the MOS and the JFET. This condition reduces the power MOSFET to the capacitor network of Figure 8, which may be replaced by three capacitors. Note that this situation is valid only when no MOSFET current flows.

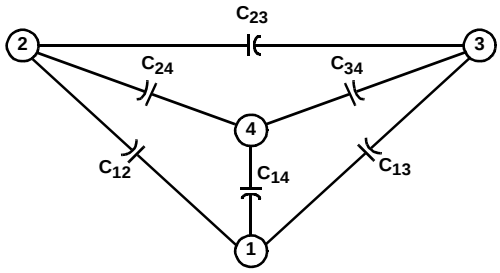


FIGURE 8. CAPACITOR NETWORK REPRESENTATION OF THE POWER MOSFET

When current does flow, node (4) of Figure 7 is a low impedance node due to the source follower characteristic of the JFET. Similarly, nodes (1) and (3) are generally low impedance nodes by virtue of the ground reference and the load resistance. Therefore, capacitive currents will usually be significant only to the input node, (2). Capacitors C_{12}, C_{23}, and C_{24} are examined below over most of the switching regime when current is flowing.

Gate to Source Capacitance, C_{12}

When all of the die except the actual MOSFET cells are ignored, Figure 6 shows that the gate to source capacitance (C_{12}) is that from the poly gate upward through the thick

oxide to the source metal. In addition, there is a contribution from the poly gate to the n+ source through the thin gate oxide. Additionally a fringing capacitance exists at the edge of the polysil gate. These components of C_{12} are invariant with voltage and current. There is a fourth component from the poly gate to a region about half way along the MOS channel through the gate oxide. This component is actually distributed, and varies somewhat with current and voltage.

Gate to Drain Capacitance, C_{23}

Capacitor C_{23} exists only when no accumulation layer is present beneath the poly gate. Otherwise, the accumulation layer acts as an electrostatic shield. This layer exists whenever the drain voltage immediately beneath the gate oxide is essentially negative relative to the poly gate. In addition, the capacitive coupling from drain to gate diminishes greatly when the JFET is pinched off. Therefore, C_{23} exists for only a small range of drain voltage. In addition, it should decrease rapidly as the pinch-off voltage level is approached because the effective area of concern is closed off similarly to the aperture of a camera (for a hex cell).

Gate to Internal Electrode Capacitance, C_{24}

Capacitor C_{24} is rather large for positive gate voltages. It is made up of that area between the poly gate and the accumulation layer, plus some of the area between the poly gate and the middle of the MOS channel. In both cases, the dielectric is the thin gate oxide. So long as the gate voltage is positive relative to the n- layer beneath the poly gate, the accumulation layer exists and C_{24} is invariant. This accumulation layer ceases to exist when the external drain voltage minus the IR drop through the n- neck region approximately equals the gate voltage. The area associated with the accumulation layer (JFET cathode) rapidly decreases with increased drain voltage. In addition, a depletion layer may now form, leading to a further reduction of C_{24}.

Waveforms Expected from the Model

The following discussion relates the prior model discussion to the waveforms of Figure 5. The discussion begins with the gate voltage at +5V or +10V and the gate current equal to zero. This condition corresponds to saturated behavior, where the drain current is approximately equal to $I_{D(max)}$ and the drain voltage equals $I_{D(max)}$ times $r_{DS(ON)}$.

Gate Voltage Slope - t_{OFF} Delay

As time progresses, I_G = -5mA, which must flow through C_{12} + C_{23} + C_{24} of Figure 8 because the MOS and JFET are both heavily biased into conduction. Therefore, dV_4/dt = dV_3/dt = nearly 0. With large positive gate bias and drain voltage near zero, C_{23} is zero and C_{12} and C_{24} are constant. As a result, the gate voltage should be a straight line with a slope equal to:

$$dV_G/dt = I_G/(C_{12} = C_{24}) \quad \text{(EQ. 1)}$$

Gate Voltage Plateau

As the gate voltage decreases, the drain voltage will increase imperceptibly at first until the gate voltage drops enough to bias the MOS into its constant current mode. At this point, the very high transconductance of the MOS is consistent with very little change in gate voltage to reduce the current by several percent. Several percent change in drain current corresponds to many volts in drain voltage. As a result, the gate current no longer flows from C_{12} during the constant gate voltage plateau.

Drain Voltage Shallow Slope

Since C_{23} is still zero, all gate current must flow from C_{24}. Assuming that the gate voltage is plateaued and that the JFET is still heavily forward biased, node 4 of Figure 7 must ramp at linear rate. Therefore, the JFET must also ramp at this same rate.

$$dV_D/dt = I_G/C_{24} \quad \text{(EQ. 2)}$$

Again this curve will approximate a straight line.

Drain Transition Voltage

As mentioned above, C_{24} rapidly decreases once the drain voltage is slightly greater than the gate voltage. (Actually, this voltage is the n- voltage directly beneath the gate oxide, and differs from the drain voltage by an amount nearly equal to I_D $r_{DS(ON)}$.)

Since the drain voltage is still fairly low and the drain current has not changed much, the gate plateau voltage still exists. Equation 2 still applies except that the value of C_{24} has materially decreased and C_{23} has become finite. This situation results in a substantial increase in dV_D/dt.

JFET Pinch Off Voltage - Drain Voltage Steep Slope

As the drain voltage approaches the pinch off voltage of the JFET, the JFET comes out of saturation and starts to support MOSFET drain voltage. The voltage gain of the active JFET permits large changes in the JFET drain voltage for small changes in its source-to-gate voltage. But the JFET source-to-gate voltage is the lateral MOS drain-to-source voltage, which is dominated by equation 2 (but for low values of C_{24}).

Gate Voltage Curvature from Plateau

As the drain voltage increases, the drain current decreases. This condition requires significant decrease in gate voltage until the gate threshold is approached. A significant portion of the gate current must now flow through C_{12}. This flow produces a gradual transition in the gate voltage and some slowing of the drain voltage waveform.

Gate Voltage Slope - $t_{(ON)}$ Delay

When the drain is totally off, most of the gate current flows from C_{12}. Again, this capacitance is constant, so that the waveform is a straight line with a slope equal to:

$$dV_G/dt = I_G/C_{12} \quad \text{(EQ. 3)}$$

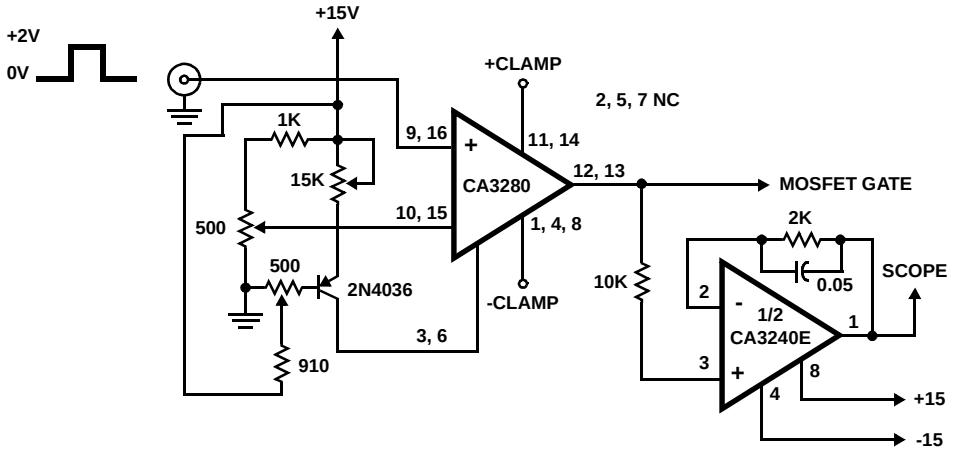


FIGURE 9. TEST CIRCUIT

New Switching Characterization for Power MOSFETs

The above discussion suggests that a new method of characterization may be provided for resistive switching with power MOSFETs, where constant current gate drive is employed during the transition time.[1] The below method bears some similarity to the gate charge concept.[2] The state of the gate charge is a continuous plot in this work, however, rather than a single point. This approach permits a knowledge of all waveforms with any drive circuitry, rather than just the total elapsed time. In addition, the total elapsed time is fixed (at just under 50 microseconds) by choosing the required value of constant gate current. Circuit designers are usually more comfortable with milliamperes and microseconds (although the product is charged in nanocoulombs).

Test Circuit - Drive

A test circuit is shown in Figure 9. The heart of this circuit is the Fairchild CA3280 integrated circuit. This is an operational transconductance amplifier (OTA) operated as a comparator. An OTA is a current output circuit where the output current and output transconductance are programmed by the amplifier bias current (I_{ABC}). Internal chip circuit feedback assures an extremely high output impedance within a compliance range established by the supply voltages. The circuit of Figure 9 is actually two OTA's in parallel. The linearizing diodes on this chip are not used.

A value of I_{ABC} is established from the collector of the 2N4036. The current into the load (the gate of the MOSFET under test) may be varied between $+I_{ABC}$ and $-I_{ABC}$ times a constant of proportionality (approximately 0.9). The actual value depends upon the input differential input voltage. As a comparator, the differential voltage is large resulting in saturated behavior of $\pm I_{ABC}$. If the gate voltage comes within a volt of the rail voltages, this current goes to zero, producing a clamping voltage. For the purposes of this Note, these supply voltages are adjusted to clamp 0 volts and +10 volts for the normal n-channel MOSFET. The behavior of this IC is excellent from submicroamperes to about 2.5mA. Higher current may be achieved by stacking many CA3280 packages one on top of another and soldering the leads parallel to the chips rather than wiring many sockets. However, this arrangement may require an increase in the bypass capacitor values.

A CA3240E MOS input op amp is used as a unity gain follower. Otherwise, the 1mΩ or 10mΩ shunting impedance of the scope would load the high impedance circuitry associated with the MOSFET gate.

Testing Conditions

A pulse generator is set for 50µs on time duration and approximately 25ms repetition rate (about 0.2% duty cycle). The ± clamp voltages are set to the appropriate values. The power MOSFET load resistor is chosen to equal the maximum rated voltage divided by the maximum rated current.

With a low value of drain supply voltage, observe the gate voltage while adjusting I_{ABC}. A convenient set of conditions occurs when a short dwell time of several µs exists at the +10V level. Minor adjustments may be desired for I_{ABC} as the drain supply voltage is increased to maximum rated value. The L^2FETs would be tested at +5V gate clamp.

Figure 10 exhibits the pertinent waveforms for an RFM15N15. All power MOSFETs have similar waveforms. Figure 10(A) is the 3V signal to the CA3280. Figure 10(B) is the power MOSFET gate current. In this example, the amplitude is ±1mA with a third state of 0mA. Figure 10(C) displays the gate voltage and the drain voltage, 10V peak-to-peak and 150V peak-to-peak. Figure 10(D) is a piece wise linear approximation of Figure 10(C). The datum line is zero volts and applies to both waveforms. The time scale of the waveforms of Figure 10 is 100µs full scale.

There are some features of the gate and drain voltage waveforms that should be noted. These features are consistent with the equivalent model discussion.

1. The waveforms during the positive gate current time are symmetrical to those during the negative gate current time. Exceptions will occur for very fast or very slow switching, and for nonsymetrical current drive. These exceptions are discussed in the following.

2. The drain voltage waveform contains a rather steep slope with a fairly constant dv/dt over most of the drain voltage excursion.
3. The drain voltage contains a rather shallow slope with a fairly constant dv/dt over the remainder of the drain voltage excursion.
4. The drain transition voltage (defined as the intercept of the above two near straight lines) typically occurs when the drain voltage equals the sum of the gate voltage (at that instant of time) plus the product of the drain current times $r_{DS}(on)$.
5. The gate voltage waveform contains three near straight line segments during the positive gate current transition time.

FIGURE 10A. 3V SIGNAL TO THE CA3280

FIGURE 10B. POWER MOSFET GATE CURRENT

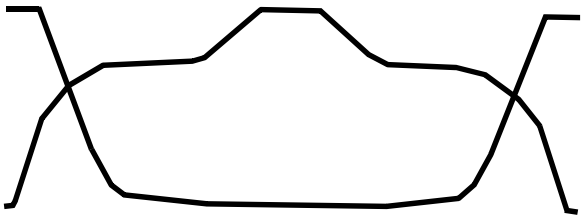


FIGURE 10C. GATE AND DRAIN VOLTAGE

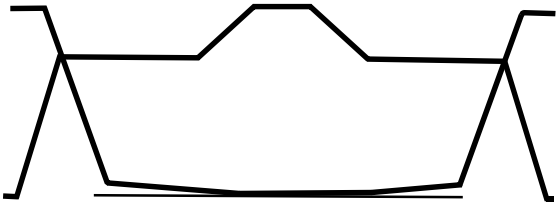


FIGURE 10D. PIECE WISE LINEAR APPROXIMATION OF FIGURE 10C

Application of the Switching Data

Figure 11 is a family of curves similar to Figure 10(C), where the drain supply voltage is fixed at four values. Note that the ordinate is 10V full scale for the gate voltage, while it is normalized to 100% of maximum-rated drain voltage for the drain-voltage curves. All four sets of curves are taken with a predetermined gate current, $\pm I_{T(REF)}$. The abscissa is also normalized to 100 ($I_{T(REF)}/I_G$) microseconds full scale, where I_G is the actual gate drive current. With this characteristic curve, switching behavior may be readily predicted for almost any driving circuit, provided the load is resistive.

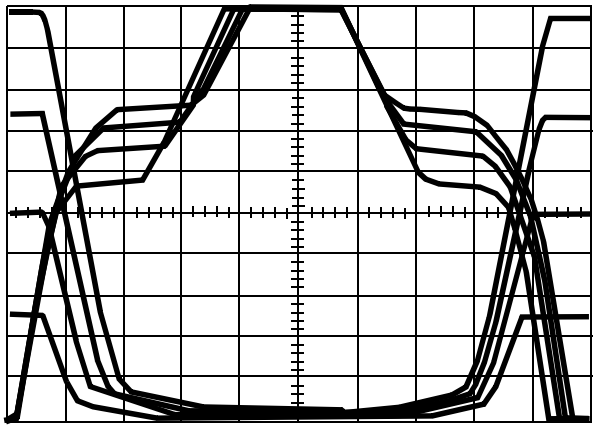


FIGURE 11. CURVES SIMILAR TO THOSE OF FIGURE 10(C) WITH DRAIN SUPPLY VOLTAGE FIXED AT FOUR VALUES

Symmetrical Current Drive

Waveforms of Figure 11 will scale in an inverse manner with gate current. Driving current was varied from ±200mA to ±2µA for the device of Figure 11. Measurements of delay time (on), rise time, delay time (off), and fall time are plotted in Figure 12 and compared to the inverse scaling suggested by Figure 11.

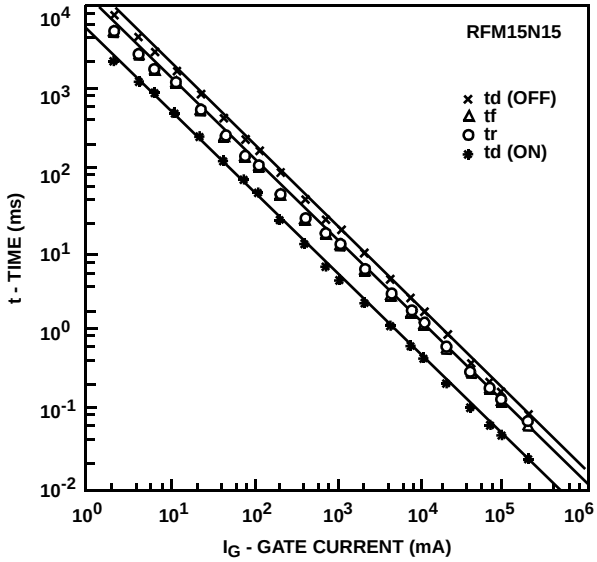


FIGURE 12. VARIOUS TIME MEASUREMENTS COMPARED TO THE INVERSE SCALING SUGGESTED BY FIGURE 11.

It is anticipated that very slow switching (in the millisecond region) will result in the chip thermally tracking the power dissipation, which would cause some deviation from the inverse scaling. This condition was not noted on Figure 12 for gate currents as low as ±2µA.

Large gate currents result in very fast switching waveforms. The gate of each hex cell is accessed through a gate pad and gate runners, which are of a low resistivity metal followed by buried polysilicon of a moderate resistivity. As a result, the high gate currents cause a propagation delay to exist for those cells far removed from the gate runners. This effect is not seen in Figure 12, even though the gate current was increased to ±200mA.

Asymmetrical Current Drive

The positive and negative gate drive will often be dissimilar. Of course, the scaling must reflect this situation. At other times the gate current varies with amplitude. This condition is always true when driving from a pulse generator of fixed resistance. Piecewise linear methods will yield the gate current, which will permit the proper piecewise linear scaling. This calculation could be done in the following manner:

1. Mark eleven small x's along the gate waveform of Figure 11 dividing it into 10 equal voltage segments; for example, V_G = 0, 1, 2, . . . 9, 10V.
2. Draw a vertical line through each x the full height of the figure, creating 10 time segments.
3. If the driving-pulse amplitude is 0 to 10 volts with an internal resistance of 100 ohms, calculate the piecewise linear gate current for each time segment. I_{G1} = (10 - 0.5)/100 = 95mA, I_{G2} = (10 -1.5)/100 = 85mA, etc.
4. Then scale each waveform within the pertinent time segment by the proper gate current.
5. Smooth the curves.
6. Create 10 more time segments for the right half of Figure 11 corresponding to an average gate voltage of 9.5, 8.5, . . . 1.5, 0.5 volts. Call these segments 11, 12,... 19, 20.
7. In that the pulse-generator voltage is now zero volts, calculate I_G as:
   I_{G11} = (0-9.5)/100 = -95mA, I_{G12} = (0-8.5)/100 = -85mA, etc.
8. Repeat 4 and 5. L^2FETs would be treated with smaller voltage segments.

Generally, the gate-voltage plateau of Figure 11 will not be located at the middle of the pulse-generator amplitude (5 volts). As a result, rise and fall times measured this way experience differing gate currents and are "nonsymetrical". This type of measurement will also lead one to observe temperature sensitivities, load-current sensitivities, and device-to-device variability, all of which are more circuit dependent than device dependent.

Source-Lead Inductance

The gate-voltage waveforms may be corrected by the voltage across the source-lead inductance and external inductance, which may be mutually common to the input and output current loops. This voltage, L di/dt, may be approximated and applied to the gate-voltage waveform after scaling Figure 12 for the actual gate currents. Generally, this effect is not appreciable for gate current small relative to ±100mA. A very loose circuit wiring arrangement with inches of mutually common source wire will exaggerate this effect.

Gate Voltage Propagation Effects

Most power MOSFET applications need switch no faster than tenths of a microsecond, but should faster switching be required, this section will become important. It must be understood that the power MOSFET appears as a distributed network of many cells when used for very fast switching.

The thousands of individual MOSFET cells are connected in parallel with highly conductive metal for the sources and drains. However, the gates are paralleled with a moderately conductive film of doped polysilicon. As a result, a very steep voltage waveform applied to the gate pad will bias those cells close by, but a delay will occur for turn on or turn off. Because of the nonlinear "input capacitance" of each cell, the delay cannot be characterized by a pure number of so many nanoseconds.

Presently, most manufacturers characterize typical switching speed for a single test condition. The test conditions are usually chosen to present the most favorable result, usually near the upper limit of usefulness.

Figures 13(A), (B), and (C) show the increasing effect of gate voltage propagation. The gate waveform is the only one shown because the drain is not affected so drastically. This is true because some cells are overdriven, offsetting the effect of the starved cells. Care must be exercised when operating with large gate effects similar to those of Figure 13(C).

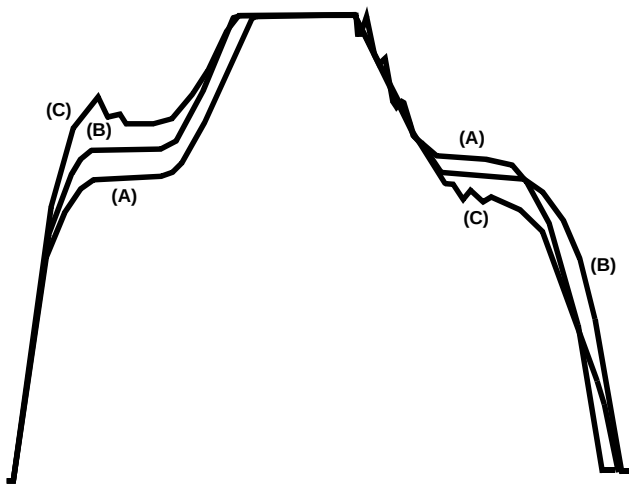


FIGURE 13. CURVES SHOWING THE INCREASING EFFECT OF GATE VOLTAGE PROPAGATION

Gate-propagation effects may be reduced by the following design methods:

1. Many gate runners.
2. More conductive polysilicon.
3. Silicide rather than polysilicon gates.
4. Less cells (resulting in lower transconductance and higher $r_{DS(ON)}$).
5. Substantially different lateral and vertical structure.
6. High-frequency packaging.

None of the above methods will yield “breakthrough” devices unless used in combination.

Any of the previous methods require trade-offs which would not be attractive to the needs of most components users. These trade-offs are in the realm of:

1. Reduction of $r_{DS(ON)}$ per unit area.
2. Decreased yield.
3. Added cost (beyond the cost of yield impact).
4. RFI, self-oscillation, and other problems characteristic of very fast devices.

References

[1] “Power MOSFET Switching Waveforms - A New Insight,” H. R. Ronan, Jr., and C. F. Wheatley, Jr., Proc. Powercon 11, April 1984.

[2] “Correlating the Charge-Transfer Characteristics of Power MOSFETs with Switching Speed,” E. Oxner, Proc. Powercon 9, April 1982.

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FAST ®	MICROWIRE™	SILENT SWITCHER ®	UHC™
Bottomless™	FASTr™	OPTOLOGIC ®	SMART START™	UltraFET ®
CoolFET™	FRFET™	OPTOPLANAR™	SPM™	VCX™
CROSSVOLT™	GlobalOptoisolator™	PACMAN™	STAR*POWER™	
DenseTrench™	GTO™	POP™	Stealth™	
DOME™	HiSeC™	Power247™	SuperSOT™-3	
EcoSPARK™	I^2C™	PowerTrench ®	SuperSOT™-6	
E^2CMOS^{TM}	ISOPLANAR™	QFET™	SuperSOT™-8	
$EnSigna^{TM}$	LittleFET™	QS™	SyncFET™	
FACT™	MicroFET™	QT Optoelectronics™	TinyLogic™	
FACT Quiet Series™	MicroPak™	Quiet Series™	TruTranslation™	

STAR*POWER is used under license

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.
As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.