FAIRCHILD SEMICONDUCTOR TM

April 1988
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# 74F02
# Quad 2-Input NOR Gate

## General Description

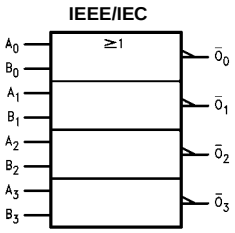
This device contains four independent gates, each of which performs the logic NOR function.

## Ordering Code:

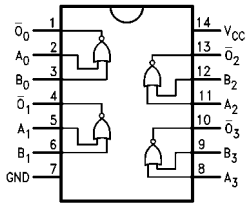
| Order Number | Package Number | Package Description |
|---|---|---|
| 74F02SC | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow |
| 74F02SJ | M14D | 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74F02PC | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Logic Symbol




## Connection Diagram




## Unit Loading/Fan Out

| Pin Names | Description | U.L. HIGH/LOW | Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$ |
|---|---|---|---|
| $A_n$, $B_n$ | Inputs | 1.0/1.0 | 20 μA/–0.6 mA |
| $\overline{O}_n$ | Outputs | 50/33.3 | –1 mA/20 mA |

## Absolute Maximum Ratings(Note 1)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature under Bias | −55°C to +125°C |
| Junction Temperature under Bias | −55°C to +150°C |
| $V_{CC}$ Pin Potential to Ground Pin | −0.5V to +7.0V |
| Input Voltage (Note 2) | −0.5V to +7.0V |
| Input Current (Note 2) | −30 mA to +5.0 mA |
| Voltage Applied to Output | |
| in HIGH State (with $V_{CC}$ = 0V) | |
| Standard Output | −0.5V to $V_{CC}$ |
| 3-STATE Output | −0.5V to +5.5V |
| Current Applied to Output | |
| in LOW State (Max) | twice the rated $I_{OL}$ (mA) |

## Recommended Operating Conditions

| | |
|---|---|
| Free Air Ambient Temperature | 0°C to +70°C |
| Supply Voltage | +4.5V to +5.5V |

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

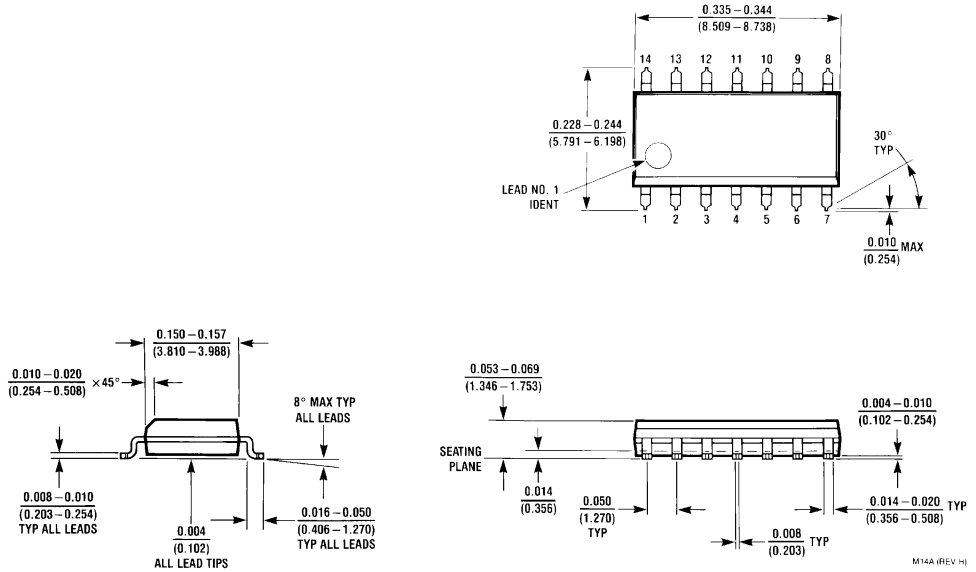
## DC Electrical Characteristics

| Symbol | Parameter | | Min | Typ | Max | Units | $V_{CC}$ | Conditions |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V | | Recognized as a HIGH Signal |
| $V_{IL}$ | Input LOW Voltage | | | | 0.8 | V | | Recognized as a LOW Signal |
| $V_{CD}$ | Input Clamp Diode Voltage | | | | −1.2 | V | Min | $I_{IN}$ = −18 mA |
| $V_{OH}$ | Output HIGH Voltage | 10% $V_{CC}$ | 2.5 | | | V | Min | $I_{OH}$ = −1 mA |
| | | 5% $V_{CC}$ | 2.7 | | | | | $I_{OH}$ = −1 mA |
| $V_{OL}$ | Output LOW Voltage | 10% $V_{CC}$ | | | 0.5 | V | Min | $I_{OL}$ = 20 mA |
| $I_{IH}$ | Input HIGH Current | | | | 5.0 | µA | Max | $V_{IN}$ = 2.7V |
| $I_{BVI}$ | Input HIGH Current Breakdown Test | | | | 7.0 | µA | Max | $V_{IN}$ = 7.0V |
| $I_{CEX}$ | Output HIGH Leakage Current | | | | 50 | µA | Max | $V_{OUT}$ = $V_{CC}$ |
| $V_{ID}$ | Input Leakage Test | | 4.75 | | | V | 0.0 | $I_{ID}$ = 1.9 µA<br>All other pins grounded |
| $I_{OD}$ | Output Leakage Circuit Current | | | | 3.75 | µA | 0.0 | $V_{IOD}$ = 150 mV<br>All other pins grounded |
| $I_{IL}$ | Input LOW Current | | | | −0.6 | mA | Max | $V_{IN}$ = 0.5V |
| $I_{OS}$ | Output Short-Circuit Current | | −60 | | −150 | mA | Max | $V_{OUT}$ = 0V |
| $I_{CCH}$ | Power Supply Current | | | 3.7 | 5.6 | mA | Max | $V_O$ = HIGH |
| $I_{CCL}$ | Power Supply Current | | | 8.7 | 13.0 | mA | Max | $V_O$ = LOW |

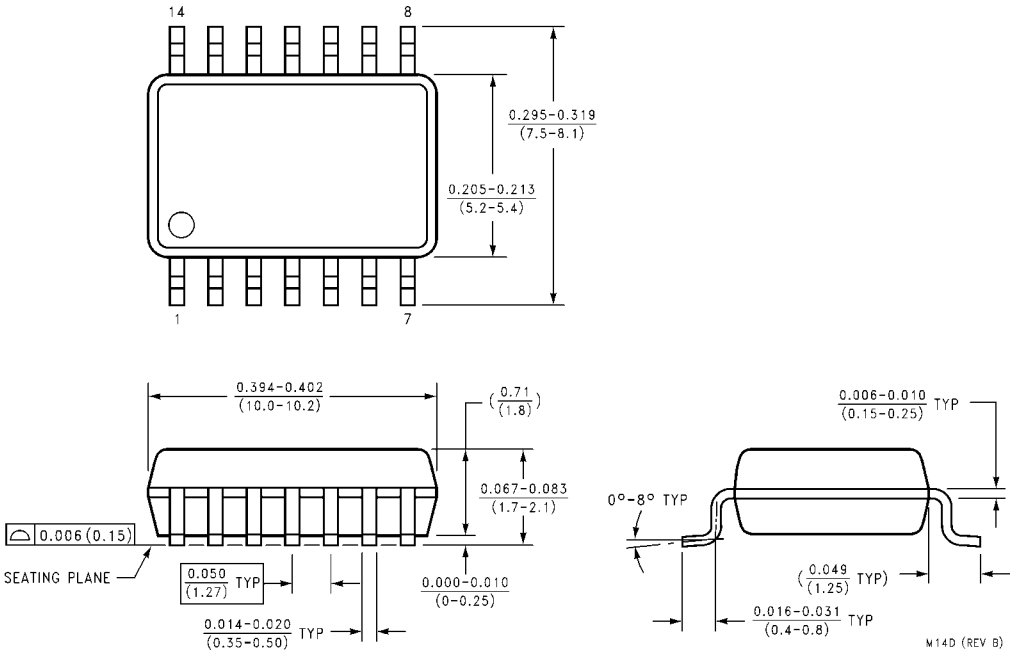
## AC Electrical Characteristics

| Symbol | Parameter | $T_A$ = +25°C, $V_{CC}$ = +5.0V, $C_L$ = 50 pF | | | $T_A$ = −55°C to +125°C, $V_{CC}$ = +5.0V, $C_L$ = 50 pF | | $T_A$ = 0°C to +70°C, $V_{CC}$ = +5.0V, $C_L$ = 50 pF | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Max | Min | Max | |
| $t_{PLH}$ | Propagation Delay | 2.5 | 4.4 | 5.5 | 2.5 | 7.5 | 2.5 | 6.5 | ns |
| $t_{PHL}$ | $A_n$, $B_n$ to $\overline{O}_n$ | 1.5 | 3.2 | 4.3 | 1.5 | 6.5 | 1.5 | 5.3 | |

## Physical Dimensions inches (millimeters) unless otherwise noted

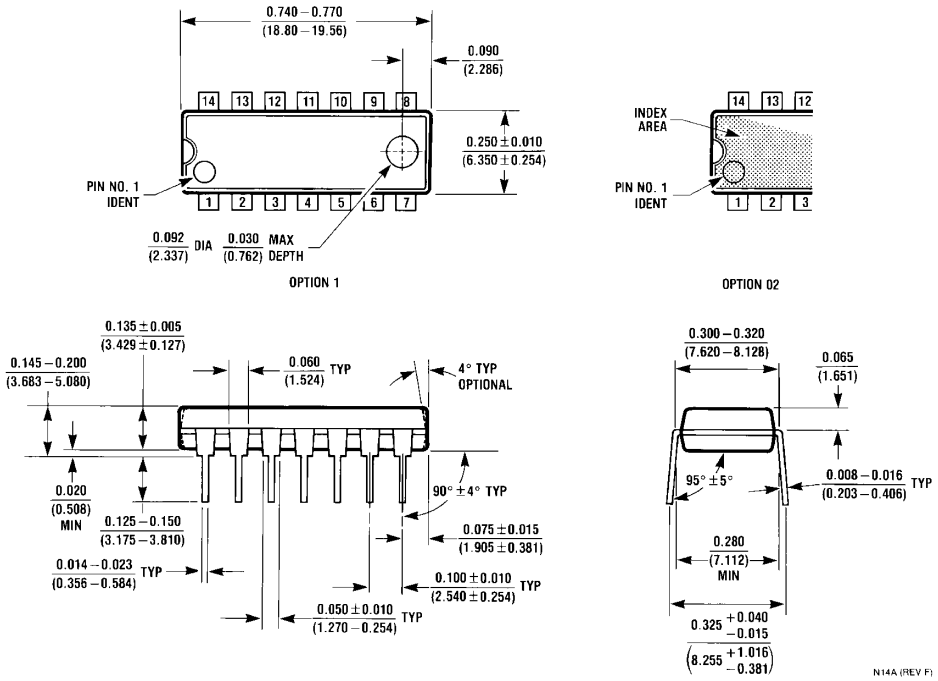



**14-Lead Small Outline Integrated Circuit (SOC), JEDEC MS-120, 0.150 Narrow**
**Package Number M14A**




**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**
**Package Number M14D**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide**
**Package Number N14A**



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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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