

Atmel AVR Microcontroller Family - Product Selection Guide

DEVICE	90S1200	90S2313	90S2343	90S4414	90S8515	90S2333	90S8535	MEGA603	MEGA103
ON-CHIP MEMORY									
FLASH (Bytes)	1K	2K	2K	4K	8K	2K	8K	64K	128K
EEPROM (Bytes)	64	128	128	256	512	128	512	2K	4K
SRAM (Bytes)	0	128	128	256	512	128	512	4K	4K
In-System Programmable (ISP)	YES	YES	YES	YES	YES	YES	YES	YES	YES
HARDWARE FEATURES									
I/O Pins	15	15	5	32	32	20	32	32I/O, 8O, 8I	32I/O, 8O, 8I
On-chip RC Oscillator	YES	NO	YES	NO	NO	NO	NO	NO	NO
Real Time Clock (RTC)	NO	NO	NO	NO	NO	NO	NO	YES	YES
SPI Port	NO	NO	NO	YES	YES	YES	YES	YES	YES
Full Duplex Serial UART	NO	YES	NO	YES	YES	YES	YES	1	1
Watchdog Timer	YES	YES	YES	YES	YES	YES	YES	YES	YES
Timer/Counters	1	2	2	2	2	2	2	3	3
PWM Channels (10-bit)	-	1	-	2	2	1	TBA	2	2
Analogue Comparator	YES	YES	NO	NO	NO	NO	NO	NO	NO
ADC	NO	NO	NO	NO	NO	6CH/10BIT	8CH/10BIT	8CH/10BIT	8CH/10BIT
IDLE and Power Down modes	YES	YES	YES	YES	YES	YES	YES	YES	YES
Interrupts	4	11	3	13	13	14	17	24	24
MISCELLANEOUS									
AVR Instructions	89	118	118	118	118	118	120	121	121
Max External Clock Frequency	12MHz	10MHz	10MHz	8MHz	8MHz	8MHz	8MHz	6MHz	6MHz
Vcc Voltage Range (V)	4.0-6.0V	4.0-6.0V	4.0-6.0V	4.0-6.0V	4.0-6.0V	4.0-6.0V	4.0-6.0V	4.0-6.0V	4.0-6.0V
EQUINOX SUPPORT TOOLS									
AVR Starter System	ISP/PAR	ISP/PAR	ISP/PAR	ISP/PAR	ISP/PAR	ISP/PAR	ISP only	ACT-UPG1	ACT-UPG1
AVR Development System	ZIF-ISP	ZIF-ISP	ZIF-ISP	ZIF-ISP	ZIF-ISP	ZIF-ISP	ZIF-ISP	UISP-UPG1	UISP-UPG1
Micro-ISP Series IV Programmer	ISP only	ISP only	ISP only	ISP only	ISP only	ISP only	ISP only	ISP only	ISP only
Micro-ISP Series IV LV Prog.	ISP only	ISP only	ISP only	ISP only	ISP only	ISP only	ISP only	ISP only	ISP only
Micro-Pro Device Programmer	PAR only	PAR only	-	ZIF-ISP	ZIF-ISP	-	-	-	-
AllWriter Universal Programmer	PAR	PAR	-	PAR	PAR	-	-	-	-
AVR BASIC LITE	YES (1K)	-	-	-	-	-	-	-	-
AVR BASIC FULL	YES	YES	YES	YES	YES	YES	YES	YES	YES
AT90S8515 Socket Stealer (DIL-40)	NO	NO	NO	YES	YES	NO	NO	NO	NO

* Max speed depends on Vcc voltage. Frequencies and Currents listed are for Vcc = 5.0V & T = 25°C

Please verify correct part codes for low voltage parts before ordering.

Key

- SRAM** - Static RAM
- ISP** - In-System Programmable
- I/O** - Input/Output
- ADC** - Analogue to Digital Converter
- SPI** - Serial Peripheral Interface
- PWM** - Pulse Width Modulation
- PAR** - Parallel programming mode
- FLASH** - Reprogrammable Code Memory
- EEPROM** - Parallel programming mode

Farnell Order Code	Equinox Order Code
111-806	EQ-8051-ST1 (UK)
302-2249	AVR-DV1 (UK)
302-2286	UISP-S4
302-2298	UISP-LV4
111-715	MPW-PLUS (UK)
302-2225	SG-ALLWRITER
111-788	AVR-BAS-LIT
302-2330	AVR-BAS-FULL
302-2365	SS-90S8515-P

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Continued....

Device	90S1200	90S2313	90S2343	90S4414	90S8515	90S2333	90S8535	MEGA603	MEGA103	Farnell Order Code	Equinox Order Code
EQUINOX SUPPORT TOOLS											
AT90S8515 Socket Stealer (PLCC)	NO	NO	NO	YES	YES	NO	NO	NO	NO	303-1068	SS-90S8515-J
DOBOX-MOD1	YES	YES	YES	YES	YES	NO	YES	NO	NO	121-022	UC-PM1
PACKAGE TYPES (Farnell Codes)											
6AC	-	-	-	-	-	-	-	120-984	120-972		
8JC	-	-	-	111-480	111-508	-	120-959	-	-		
8PC	-	-	-	111-478	111-491	-	120-960	-	-		
10PC	-	111-454	111-430	-	-	-	-	-	-		
10SC	-	111-466	111-442	-	-	-	-	-	-		
12PC	690-752	-	-	-	-	-	-	-	-		
12SC	690-934	-	-	-	-	-	-	-	-		

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Errata

- Lock Bits at High V_{CC}
- Reset During EEPROM Write
- Verifying EEPROM in System
- Serial Programming at Voltages Below 3.0 Volts

4. Lock Bits at High V_{CC}

On some devices, the lock bits will not erase at high V_{CC} . In this situation, it will not be possible to reprogram the devices when the lock bits are set.

Problem Fix/Workaround

Lower V_{CC} below 4.0V before you perform a chip-erase. Then the device will unlock, and it will be possible to reprogram the device at any V_{CC} .

3. Reset During EEPROM Write

If reset is activated during EEPROM write the result is not what should be expected. The EEPROM write cycle completes as normal, but the address registers are reset to 0. The result is that both the address written and address 0 in the EEPROM can be corrupted.

Problem Fix/Workaround

Avoid using address 0 for storage, unless you can guarantee that you will not get a reset during EEPROM write.

2. Verifying EEPROM in System

EEPROM verify in In-System Programming mode cannot operate with maximum clock frequency. This is independent of the SPI clock frequency.

Problem Fix/Workaround

Reduce the clock speed, or avoid using the EEPROM verify feature.

1. Serial Programming at Voltages Below 3.0 Volts

At voltages below 3.0 Volts, serial programming might fail.

Problem Fix/Workaround

Keep V_{CC} above 3.0 Volts during in-system programming.



8-Bit AVR[®]
Microcontroller
with 2K bytes
In-System
Programmable
Flash

AT90S2313
Rev. B
Errata Sheet





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Features

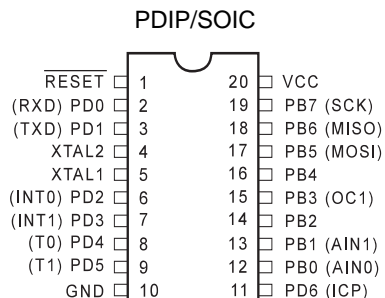
- Utilizes the AVR[®] RISC Architecture
- AVR - High-performance and Low-power RISC Architecture
 - 118 Powerful Instructions - Most Single Clock Cycle Execution
 - 32 x 8 General Purpose Working Registers
 - Up to 10 MIPS Throughput at 10 MHz
- Data and Nonvolatile Program Memory
 - 2K Bytes of In-System Programmable Flash
Endurance 1,000 Write/Erase Cycles
 - 128 Bytes of SRAM
 - 128 Bytes of In-System Programmable EEPROM
Endurance: 100,000 Write/Erase Cycles
 - Programming Lock for Flash Program and EEPROM Data Security
- Peripheral Features
 - One 8-bit Timer/Counter with Separate Prescaler
 - One 16-bit Timer/Counter with Separate Prescaler,
Compare, Capture Modes and 8-, 9- or 10-bit PWM
 - On-chip Analog Comparator
 - Programmable Watchdog Timer with On-chip Oscillator
 - SPI Serial Interface for In-System Programming
 - Full Duplex UART
- Special Microcontroller Features
 - Low-power Idle and Power Down Modes
 - External and Internal Interrupt Sources
- Specifications
 - Low-power, High-speed CMOS Process Technology
 - Fully Static Operation
- Power Consumption at 4 MHz, 3V, 25°C
 - Active: 2.8 mA
 - Idle Mode: 0.8 mA
 - Power Down Mode: <1 µA
- I/O and Packages
 - 15 Programmable I/O Lines
 - 20-pin PDIP and SOIC
- Operating Voltages
 - 2.7 - 6.0V (AT90S2313-4)
 - 4.0 - 6.0V (AT90S2313-10)
- Speed Grades
 - 0 - 4 MHz (AT90S2313-4)
 - 0 - 10 MHz (AT90S2313-10)

Description

The AT90S2313 is a low-power CMOS 8-bit microcontroller based on the AVR RISC architecture. By executing powerful instructions in a single clock cycle, the

(continued)

Pin Configuration



8-bit **AVR**[®]
Microcontroller
with 2K bytes
In-System
Programmable
Flash

AT90S2313

Rev. 0839ES-04/99

Note: This is a summary document. For the complete 87 page document, please visit our web site at www.atmel.com or e-mail at literature@atmel.com and request literature #0839E.

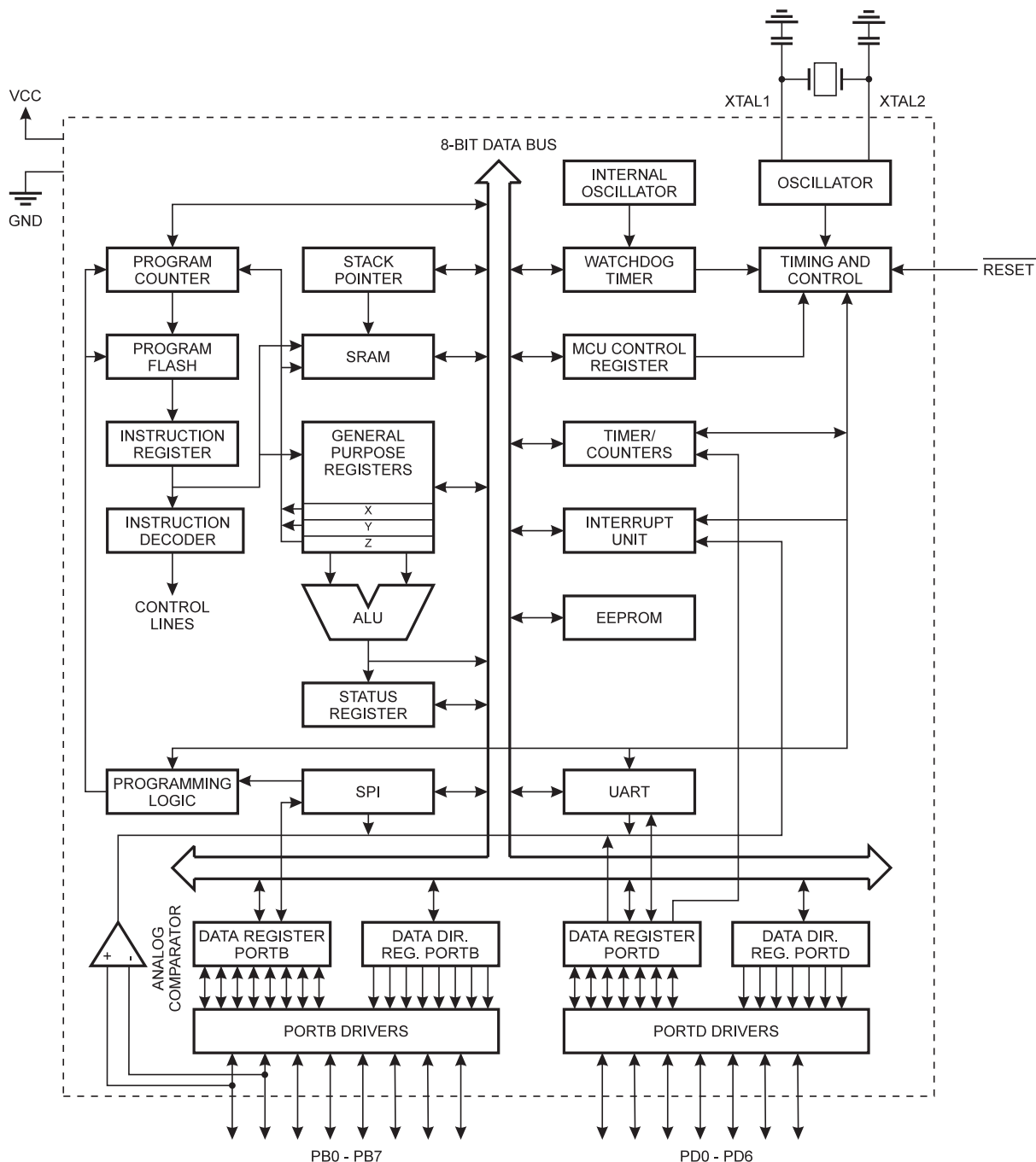


AT90S2313 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

Block Diagram

Figure 1. The AT90S2313 Block Diagram



The AT90S2313 provides the following features: 2K bytes of In-System Programmable Flash, 128 bytes EEPROM, 128 bytes SRAM, 15 general purpose I/O lines, 32 general purpose working registers, flexible timer/counters with compare modes, internal and external interrupts, a programmable serial UART, programmable Watchdog Timer with internal oscillator, an SPI serial port for Flash Memory downloading and two software selectable power saving modes. The Idle Mode stops the CPU while allowing the SRAM, timer/counters, SPI port and interrupt system to continue functioning. The power down mode saves the register contents but freezes the oscillator, disabling all other chip functions until the next external interrupt or hardware reset.

The device is manufactured using Atmel's high density nonvolatile memory technology. The on-chip In-System Programmable Flash allows the program memory to be reprogrammed in-system through an SPI serial interface or by a conventional nonvolatile memory programmer. By combining an enhanced RISC 8-bit CPU with In-System Programmable Flash on a monolithic chip, the Atmel AT90S2313 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The AT90S2313 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

Pin Descriptions

VCC

Supply voltage pin.

GND

Ground pin.

Port B (PB7..PB0)

Port B is an 8-bit bi-directional I/O port. Port pins can provide internal pull-up resistors (selected for each bit). PB0 and PB1 also serve as the positive input (AIN0) and the negative input (AIN1), respectively, of the on-chip analog comparator. The Port B output buffers can sink 20mA and can drive LED displays directly. When pins PB0 to PB7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not active.

Port D (PD6..PD0)

Port D has seven bi-directional I/O port with internal pull-up resistors, PD6..PD0. The Port D output buffers can sink 20 mA. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not active.

RESET

Reset input. A low level on this pin for more than 50 ns will generate a reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a reset.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

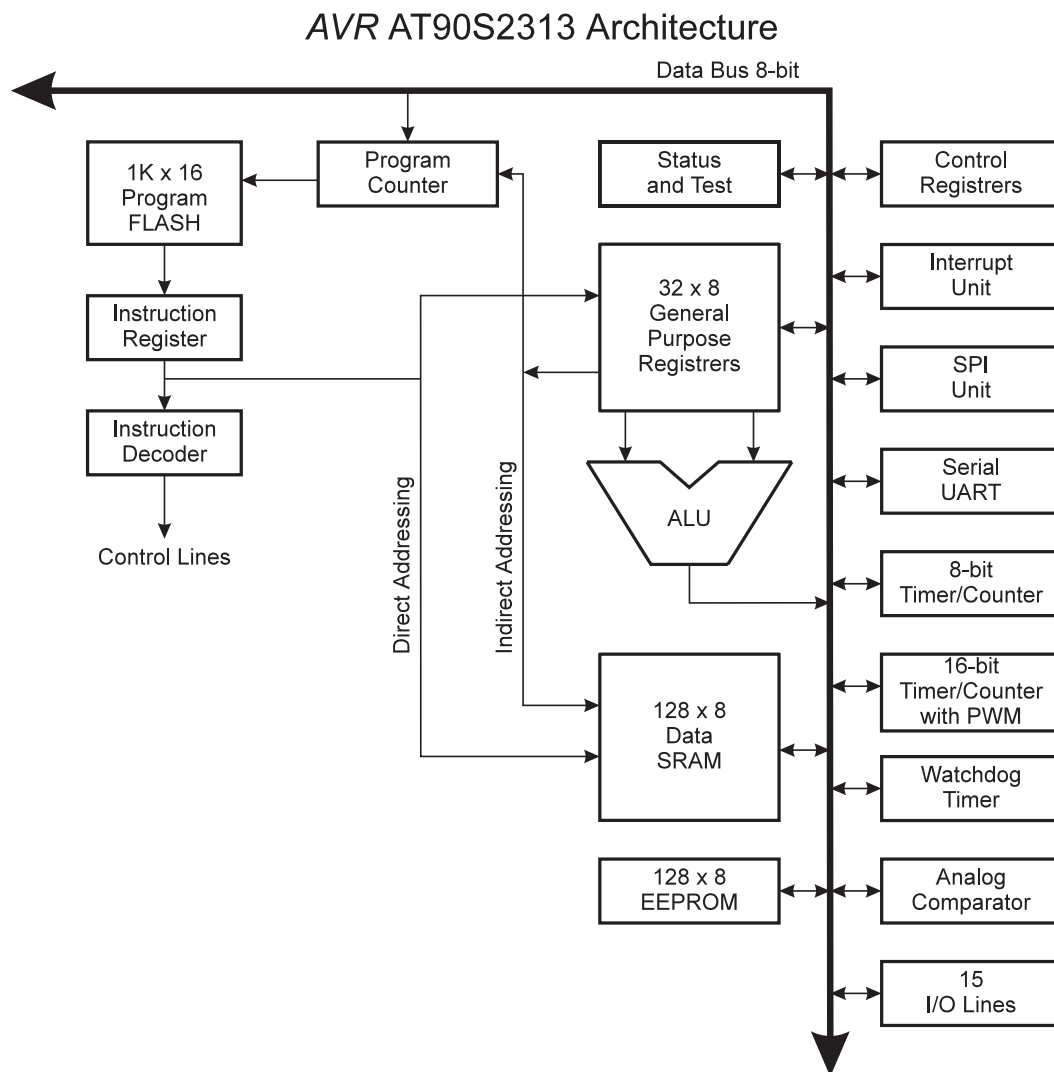
XTAL2

Output from the inverting oscillator amplifier

Architectural Overview

The fast-access register file concept contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This means that during one single clock cycle, one ALU (Arithmetic Logic Unit) operation is executed. Two operands are output from the register file, the operation is executed, and the result is stored back in the register file - in one clock cycle.

Figure 2. The AT90S2313 AVR RISC Architecture



Six of the 32 registers can be used as three 16-bits indirect address register pointers for Data Space addressing - enabling efficient address calculations. One of the three address pointers is also used as the address pointer for the constant table look up function. These added function registers are the 16-bits X-register, Y-register and Z-register.

The ALU supports arithmetic and logic functions between registers or between a constant and a register. Single register operations are also executed in the ALU. Figure 2 shows the AT90S2313 AVR RISC microcontroller architecture.

In addition to the register operation, the conventional memory addressing modes can be used on the register file as well. This is enabled by the fact that the register file is assigned the 32 lowermost Data Space addresses (\$00 - \$1F), allowing them to be accessed as though they were ordinary memory locations.

The I/O memory space contains 64 addresses for CPU peripheral functions as Control Registers, Timer/Counters, A/D-converters, and other I/O functions. The I/O memory can be accessed directly, or as the Data Space locations following those of the register file, \$20 - \$5F.

The AVR has Harvard architecture - with separate memories and buses for program and data. The program memory is accessed with a two stage pipeline. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is In-system Programmable Flash memory.

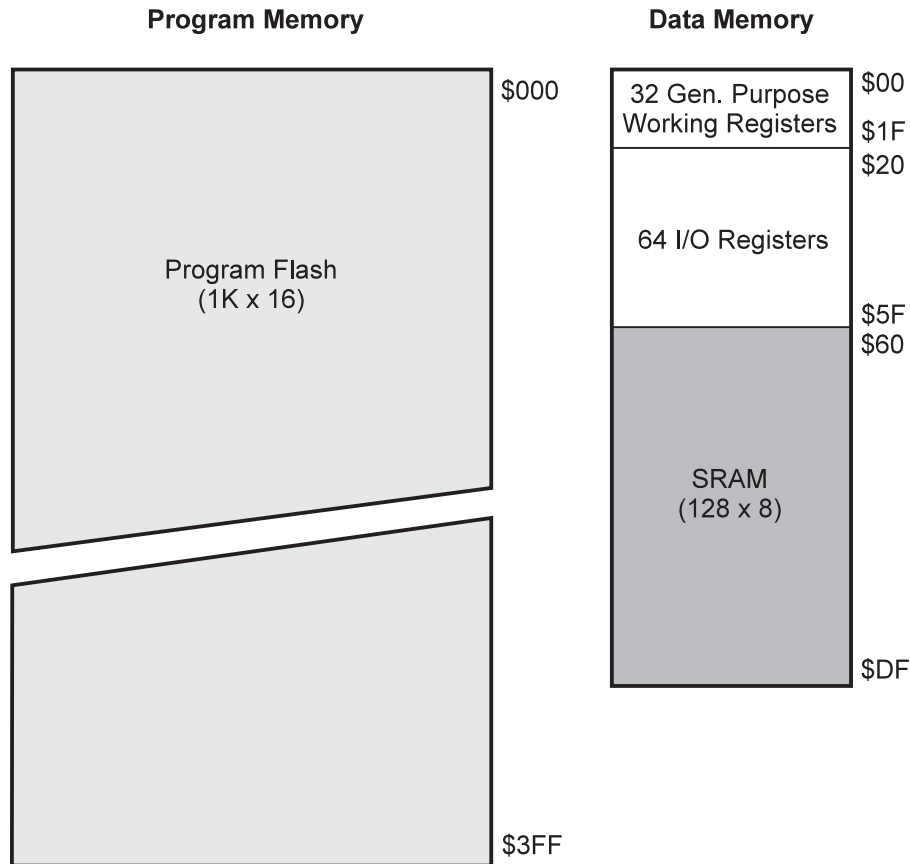
With the relative jump and call instructions, the whole 1K address space is directly accessed. Most AVR instructions have a single 16-bit word format. Every program memory address contains a 16- or 32-bit instruction.

During interrupts and subroutine calls, the return address program counter (PC) is stored on the stack. The stack is effectively allocated in the general data SRAM, and consequently the stack size is only limited by the total SRAM size and the usage of the SRAM. All user programs must initialize the SP in the reset routine (before subroutines or interrupts are executed). The 8-bit stack pointer SP is read/write accessible in the I/O space.

The 128 bytes data SRAM + register file and I/O registers can be easily accessed through the five different addressing modes supported in the AVR architecture.

The memory spaces in the AVR architecture are all linear and regular memory maps.

Figure 3. Memory Mapss



A flexible interrupt module has its control registers in the I/O space with an additional global interrupt enable bit in the status register. All the different interrupts have a separate interrupt vector in the interrupt vector table at the beginning of the program memory. The different interrupts have priority in accordance with their interrupt vector position. The lower the interrupt vector address the higher the priority.



Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
\$3F (\$5F)	SREG	I	T	H	S	V	N	Z	C	19
\$3E (\$5E)	Reserved									
\$3D (\$5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	20
\$3C (\$5C)	Reserved									
\$3B (\$5B)	GIMSK	INT1	INT0	-	-	-	-	-	-	25
\$3A (\$5A)	GIFR	INTF1	INTF0							26
\$39 (\$59)	TIMSK	TOIE1	OCIE1A	-	-	TICIE1	-	TOIE0	-	26
\$38 (\$58)	TIFR	TOV1	OCF1A	-	-	ICF1	-	TOV0	-	27
\$37 (\$57)	Reserved									
\$36 (\$56)	Reserved									
\$35 (\$55)	MCUCR	-	-	SE	SM	ISC11	ISC10	ISC01	ISC00	28
\$34 (\$54)	Reserved									
\$33 (\$53)	TCCR0	-	-	-	-	-	CS02	CS01	CS00	31
\$32 (\$52)	TCNT0	Timer/Counter0 (8 Bit)								31
\$31 (\$51)	Reserved									
\$30 (\$50)	Reserved									
\$2F (\$4F)	TCCR1A	COM1A1	COM1A0	-	-	-	-	PWM11	PWM10	33
\$2E (\$4E)	TCCR1B	ICNC1	ICES1	-	-	CTC1	CS12	CS11	CS10	34
\$2D (\$4D)	TCNT1H	Timer/Counter1 - Counter Register High Byte								35
\$2C (\$4C)	TCNT1L	Timer/Counter1 - Counter Register Low Byte								35
\$2B (\$4B)	OCR1AH	Timer/Counter1 - Compare Register High Byte								36
\$2A (\$4A)	OCR1AL	Timer/Counter1 - Compare Register Low Byte								36
\$29 (\$49)	Reserved									
\$28 (\$48)	Reserved									
\$27 (\$47)	Reserved									
\$26 (\$46)	Reserved									
\$25 (\$45)	ICR1H	Timer/Counter1 - Input Capture Register High Byte								36
\$24 (\$44)	ICR1L	Timer/Counter1 - Input Capture Register Low Byte								36
\$23 (\$43)	Reserved									
\$22 (\$42)	Reserved									
\$21 (\$41)	WDTCSR	-	-	-	WDTOE	WDE	WDP2	WDP1	WDP0	38
\$20 (\$40)	Reserved									
\$1F (\$3F)	Reserved									
\$1E (\$3E)	EEAR	-	EEPROM Address Register							40
\$1D (\$3D)	EEDR	EEPROM Data register								40
\$1C (\$3C)	EECR	-	-	-	-	-	EEMWE	EEWE	EERE	40
\$1B (\$3B)	Reserved									
\$1A (\$3A)	Reserved									
\$19 (\$39)	Reserved									
\$18 (\$38)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	50
\$17 (\$37)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	50
\$16 (\$36)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	50
\$15 (\$35)	Reserved									
\$14 (\$34)	Reserved									
\$13 (\$33)	Reserved									
\$12 (\$32)	PORTD	-	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	55
\$11 (\$31)	DDRD	-	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	55
\$10 (\$30)	PIND	-	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	55
...	Reserved									
\$0C (\$2C)	UDR	UART I/O Data Register								44
\$0B (\$2B)	USR	RXC	TXC	UDRE	FE	OR	-	-	-	45
\$0A (\$2A)	UCR	RXCIE	TXCIE	UDRIE	RXEN	TXEN	CHR9	RXB8	TXB8	45
\$09 (\$29)	UBRR	UART Baud Rate Register								47
\$08 (\$28)	ACSR	ACD	-	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	48
...	Reserved									
\$00 (\$20)	Reserved									

- Notes:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
 2. Some of the status flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers \$00 to \$1F only.

Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add two Registers	$Rd \leftarrow Rd + Rr$	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
ADIW	Rdl,K	Add Immediate to Word	$Rdh:Rdl \leftarrow Rdh:Rdl + K$	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	$Rd \leftarrow Rd - Rr$	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	$Rd \leftarrow Rd - K$	Z,C,N,V,H	1
SBIW	Rdl,K	Subtract Immediate from Word	$Rdh:Rdl \leftarrow Rdh:Rdl - K$	Z,C,N,V,S	2
SBC	Rd, Rr	Subtract with Carry two Registers	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	$Rd \leftarrow Rd - K - C$	Z,C,N,V,H	1
AND	Rd, Rr	Logical AND Registers	$Rd \leftarrow Rd \cdot Rr$	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	$Rd \leftarrow Rd \cdot K$	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	$Rd \leftarrow Rd \vee Rr$	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	$Rd \leftarrow Rd \vee K$	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	$Rd \leftarrow Rd \oplus Rr$	Z,N,V	1
COM	Rd	One's Complement	$Rd \leftarrow \$FF - Rd$	Z,C,N,V	1
NEG	Rd	Two's Complement	$Rd \leftarrow \$00 - Rd$	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	$Rd \leftarrow Rd \vee K$	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \cdot (\$FF - K)$	Z,N,V	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \cdot Rd$	Z,N,V	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V	1
SER	Rd	Set Register	$Rd \leftarrow \$FF$	None	1
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
IJMP		Indirect Jump to (Z)	$PC \leftarrow Z$	None	2
RCALL	k	Relative Subroutine Call	$PC \leftarrow PC + k + 1$	None	3
ICALL		Indirect Call to (Z)	$PC \leftarrow Z$	None	3
RET		Subroutine Return	$PC \leftarrow STACK$	None	4
RETI		Interrupt Return	$PC \leftarrow STACK$	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if $(Rd = Rr)$ $PC \leftarrow PC + 2$ or 3	None	1 / 2
CP	Rd,Rr	Compare	$Rd - Rr$	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	$Rd - Rr - C$	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	$Rd - K$	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if $(Rr(b)=0)$ $PC \leftarrow PC + 2$ or 3	None	1 / 2
SBRs	Rr, b	Skip if Bit in Register is Set	if $(Rr(b)=1)$ $PC \leftarrow PC + 2$ or 3	None	1 / 2
SBIC	P, b	Skip if Bit in I/O Register Cleared	if $(P(b)=0)$ $PC \leftarrow PC + 2$ or 3	None	1 / 2
SBIS	P, b	Skip if Bit in I/O Register is Set	if $(P(b)=1)$ $PC \leftarrow PC + 2$ or 3	None	1 / 2
BRBS	s, k	Branch if Status Flag Set	if $(SREG(s) = 1)$ then $PC \leftarrow PC + k + 1$	None	1 / 2
BRBC	s, k	Branch if Status Flag Cleared	if $(SREG(s) = 0)$ then $PC \leftarrow PC + k + 1$	None	1 / 2
BREQ	k	Branch if Equal	if $(Z = 1)$ then $PC \leftarrow PC + k + 1$	None	1 / 2
BRNE	k	Branch if Not Equal	if $(Z = 0)$ then $PC \leftarrow PC + k + 1$	None	1 / 2
BRCS	k	Branch if Carry Set	if $(C = 1)$ then $PC \leftarrow PC + k + 1$	None	1 / 2
BRCC	k	Branch if Carry Cleared	if $(C = 0)$ then $PC \leftarrow PC + k + 1$	None	1 / 2
BRSH	k	Branch if Same or Higher	if $(C = 0)$ then $PC \leftarrow PC + k + 1$	None	1 / 2
BRLO	k	Branch if Lower	if $(C = 1)$ then $PC \leftarrow PC + k + 1$	None	1 / 2
BRMI	k	Branch if Minus	if $(N = 1)$ then $PC \leftarrow PC + k + 1$	None	1 / 2
BRPL	k	Branch if Plus	if $(N = 0)$ then $PC \leftarrow PC + k + 1$	None	1 / 2
BRGE	k	Branch if Greater or Equal, Signed	if $(N \oplus V = 0)$ then $PC \leftarrow PC + k + 1$	None	1 / 2
BRLT	k	Branch if Less Than Zero, Signed	if $(N \oplus V = 1)$ then $PC \leftarrow PC + k + 1$	None	1 / 2
BRHS	k	Branch if Half Carry Flag Set	if $(H = 1)$ then $PC \leftarrow PC + k + 1$	None	1 / 2
BRHC	k	Branch if Half Carry Flag Cleared	if $(H = 0)$ then $PC \leftarrow PC + k + 1$	None	1 / 2
BRTS	k	Branch if T Flag Set	if $(T = 1)$ then $PC \leftarrow PC + k + 1$	None	1 / 2
BRTC	k	Branch if T Flag Cleared	if $(T = 0)$ then $PC \leftarrow PC + k + 1$	None	1 / 2
BRVS	k	Branch if Overflow Flag is Set	if $(V = 1)$ then $PC \leftarrow PC + k + 1$	None	1 / 2
BRVC	k	Branch if Overflow Flag is Cleared	if $(V = 0)$ then $PC \leftarrow PC + k + 1$	None	1 / 2
BRIE	k	Branch if Interrupt Enabled	if $(I = 1)$ then $PC \leftarrow PC + k + 1$	None	1 / 2
BRID	k	Branch if Interrupt Disabled	if $(I = 0)$ then $PC \leftarrow PC + k + 1$	None	1 / 2

Instruction Set Summary (Continued)

Mnemonics	Operands	Description	Operation	Flags	#Clocks
DATA TRANSFER INSTRUCTIONS					
MOV	Rd, Rr	Move Between Registers	$Rd \leftarrow Rr$	None	1
LDI	Rd, K	Load Immediate	$Rd \leftarrow K$	None	1
LD	Rd, X	Load Indirect	$Rd \leftarrow (X)$	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	$Rd \leftarrow (X), X \leftarrow X + 1$	None	2
LD	Rd, -X	Load Indirect and Pre-Dec.	$X \leftarrow X - 1, Rd \leftarrow (X)$	None	2
LD	Rd, Y	Load Indirect	$Rd \leftarrow (Y)$	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	$Rd \leftarrow (Y), Y \leftarrow Y + 1$	None	2
LD	Rd, -Y	Load Indirect and Pre-Dec.	$Y \leftarrow Y - 1, Rd \leftarrow (Y)$	None	2
LDD	Rd, Y+q	Load Indirect with Displacement	$Rd \leftarrow (Y + q)$	None	2
LD	Rd, Z	Load Indirect	$Rd \leftarrow (Z)$	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	$Rd \leftarrow (Z), Z \leftarrow Z + 1$	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	$Z \leftarrow Z - 1, Rd \leftarrow (Z)$	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	$Rd \leftarrow (Z + q)$	None	2
LDS	Rd, k	Load Direct from SRAM	$Rd \leftarrow (k)$	None	2
ST	X, Rr	Store Indirect	$(X) \leftarrow Rr$	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	$(X) \leftarrow Rr, X \leftarrow X + 1$	None	2
ST	-X, Rr	Store Indirect and Pre-Dec.	$X \leftarrow X - 1, (X) \leftarrow Rr$	None	2
ST	Y, Rr	Store Indirect	$(Y) \leftarrow Rr$	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	$(Y) \leftarrow Rr, Y \leftarrow Y + 1$	None	2
ST	-Y, Rr	Store Indirect and Pre-Dec.	$Y \leftarrow Y - 1, (Y) \leftarrow Rr$	None	2
STD	Y+q, Rr	Store Indirect with Displacement	$(Y + q) \leftarrow Rr$	None	2
ST	Z, Rr	Store Indirect	$(Z) \leftarrow Rr$	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	$(Z) \leftarrow Rr, Z \leftarrow Z + 1$	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	$Z \leftarrow Z - 1, (Z) \leftarrow Rr$	None	2
STD	Z+q, Rr	Store Indirect with Displacement	$(Z + q) \leftarrow Rr$	None	2
STS	k, Rr	Store Direct to SRAM	$(k) \leftarrow Rr$	None	2
LPM		Load Program Memory	$R0 \leftarrow (Z)$	None	3
IN	Rd, P	In Port	$Rd \leftarrow P$	None	1
OUT	P, Rr	Out Port	$P \leftarrow Rr$	None	1
PUSH	Rr	Push Register on Stack	$STACK \leftarrow Rr$	None	2
POP	Rd	Pop Register from Stack	$Rd \leftarrow STACK$	None	2
BIT AND BIT-TEST INSTRUCTIONS					
SBI	P, b	Set Bit in I/O Register	$I/O(P, b) \leftarrow 1$	None	2
CBI	P, b	Clear Bit in I/O Register	$I/O(P, b) \leftarrow 0$	None	2
LSL	Rd	Logical Shift Left	$Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$	Z, C, N, V	1
LSR	Rd	Logical Shift Right	$Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$	Z, C, N, V	1
ROL	Rd	Rotate Left Through Carry	$Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$	Z, C, N, V	1
ROR	Rd	Rotate Right Through Carry	$Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$	Z, C, N, V	1
ASR	Rd	Arithmetic Shift Right	$Rd(n) \leftarrow Rd(n+1), n=0..6$	Z, C, N, V	1
SWAP	Rd	Swap Nibbles	$Rd(3..0) \leftarrow Rd(7..4), Rd(7..4) \leftarrow Rd(3..0)$	None	1
BSET	s	Flag Set	$SREG(s) \leftarrow 1$	SREG(s)	1
BCLR	s	Flag Clear	$SREG(s) \leftarrow 0$	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	$T \leftarrow Rr(b)$	T	1
BLD	Rd, b	Bit load from T to Register	$Rd(b) \leftarrow T$	None	1
SEC		Set Carry	$C \leftarrow 1$	C	1
CLC		Clear Carry	$C \leftarrow 0$	C	1
SEN		Set Negative Flag	$N \leftarrow 1$	N	1
CLN		Clear Negative Flag	$N \leftarrow 0$	N	1
SEZ		Set Zero Flag	$Z \leftarrow 1$	Z	1
CLZ		Clear Zero Flag	$Z \leftarrow 0$	Z	1
SEI		Global Interrupt Enable	$I \leftarrow 1$	I	1
CLI		Global Interrupt Disable	$I \leftarrow 0$	I	1
SES		Set Signed Test Flag	$S \leftarrow 1$	S	1
CLS		Clear Signed Test Flag	$S \leftarrow 0$	S	1
SEV		Set Twos Complement Overflow	$V \leftarrow 1$	V	1
CLV		Clear Twos Complement Overflow	$V \leftarrow 0$	V	1
SET		Set T in SREG	$T \leftarrow 1$	T	1
CLT		Clear T in SREG	$T \leftarrow 0$	T	1
SEH		Set Half Carry Flag in SREG	$H \leftarrow 1$	H	1
CLH		Clear Half Carry Flag in SREG	$H \leftarrow 0$	H	1
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	3
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1

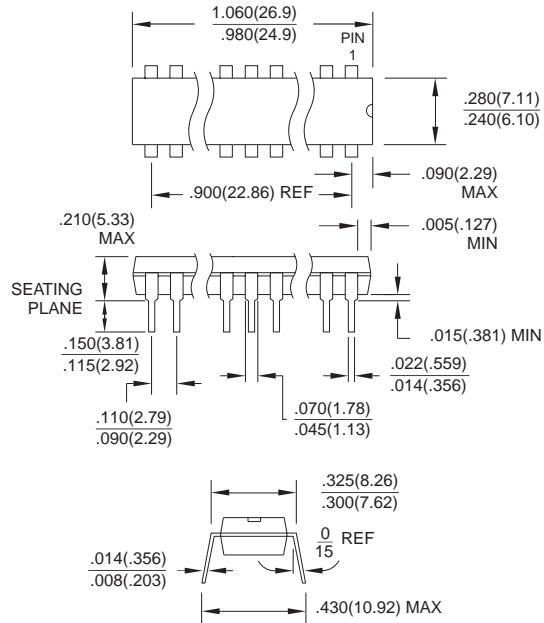
Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
4	2.7 - 6.0V	AT90S2313-4PC	20P3	Commercial (0°C to 70°C)
		AT90S2313-4SC	20S	
		AT90S2313-4PI	20P3	Industrial (-40°C to 85°C)
		AT90S2313-4SI	20S	
10	4.0 - 6.0V	AT90S2313-10PC	20P3	Commercial (0°C to 70°C)
		AT90S2313-10SC	20S	
		AT90S2313-10PI	20P3	Industrial (-40°C to 85°C)
		AT90S2313-10SI	20S	

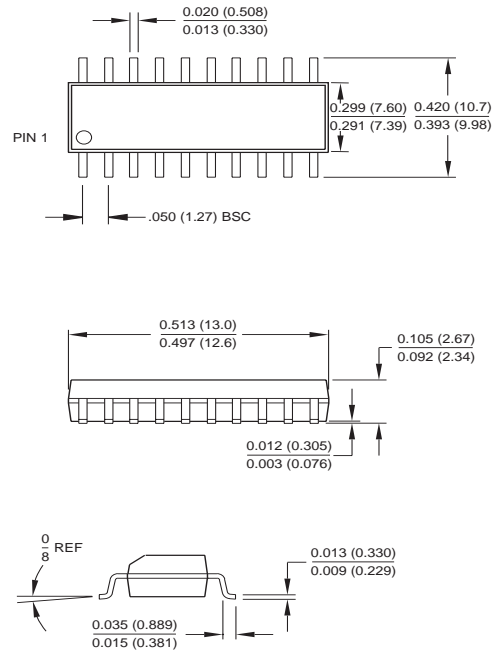
Package Type	
20P3	20-lead, 0.300" Wide, Plastic Dual In-Line Package (PDIP)
20S	20-lead, 0.300" Wide, Plastic Gull-Wing Small Outline (SOIC)

Packaging Information

20P3, 20-lead, 0.300" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-001 BA



20S, 20-lead, 0.300" Wide,
Plastic Gull-Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)





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