Precision Rail-to-Rail Input & Output Operational Amplifiers

OP184/OP284/OP484

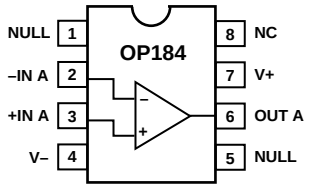
FEATURES
Single-Supply Operation
Wide Bandwidth: 4 MHz
Low Offset Voltage: 65 μV
Unity-Gain Stable
High Slew Rate: 4.0 V/μs
Low Noise: 3.9 nV/√Hz

APPLICATIONS
Battery Powered Instrumentation
Power Supply Control and Protection
Telecom
DAC Output Amplifier
ADC Input Buffer

PIN CONFIGURATIONS

8-Lead Epoxy DIP
(P Suffix)

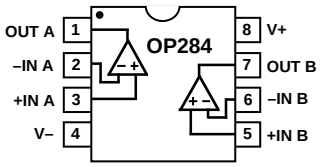
8-Lead SO
(S Suffix)



NC = NO CONNECT

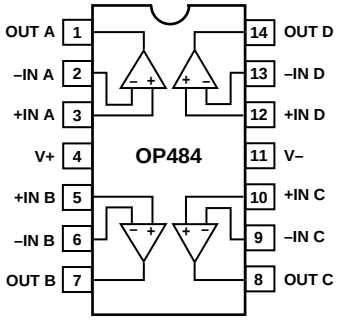
8-Lead Epoxy DIP
(P Suffix)

8-Lead SO
(S Suffix)



14-Lead Epoxy DIP
(P Suffix)

14-Lead Narrow-Body SO
(S Suffix)



GENERAL DESCRIPTION

The OP184/OP184/OP284/OP484 are single, dual and quad single-supply, 4 MHz bandwidth amplifiers featuring rail-to-rail inputs and outputs. They are guaranteed to operate from +3 to +36 (or ±1.5 to ±18) volts and will function with a single supply as low as +1.5 volts.

These amplifiers are superb for single supply applications requiring both ac and precision dc performance. The combination of bandwidth, low noise and precision makes the OP184/OP284/OP484 useful in a wide variety of applications, including filters and instrumentation.

Other applications for these amplifiers include portable telecom equipment, power supply control and protection, and as amplifiers or buffers for transducers with wide output ranges. Sensors requiring a rail-to-rail input amplifier include Hall effect, piezo electric, and resistive transducers.

The ability to swing rail-to-rail at both the input and output enables designers to build multistage filters in single-supply systems and maintain high signal-to-noise ratios.

The OP184/OP284/OP484 are specified over the HOT extended industrial (–40°C to +125°C) temperature range. The single and dual are available in 8-pin plastic DIP plus SO surface mount packages. The quad OP484 is available in 14-pin plastic DIPs and 14-lead narrow-body SO packages.

REV. 0

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Tel: 617/329-4700 **Fax: 617/326-8703**

OP184/OP284/OP484–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = +5.0 V, V_{CM} = 2.5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage "OP184/284E" Grade	V_{OS}	(Note 1)			65	µV
		–40°C ≤ T_A ≤ +125°C			165	µV
Offset Voltage "OP184/284F" Grade	V_{OS}				125	µV
		–40°C ≤ T_A ≤ +125°C			350	µV
Offset Voltage "484E" Grade	V_{OS}				75	µV
		–40°C ≤ T_A ≤ +125°C			175	µV
Offset Voltage "484F" Grade	V_{OS}				150	µV
		–40°C ≤ T_A ≤ +125°C			450	µV
Input Bias Current	I_B			60	300	nA
		–40°C ≤ T_A ≤ +125°C			500	nA
Input Offset Current	I_{OS}			2	50	nA
		–40°C ≤ T_A ≤ +125°C			50	nA
Input Voltage Range			0		+5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 5 V	60			dB
Common-Mode Rejection Ratio	CMRR	V_{CM} = 1.0 V to 4.0 V, –40°C ≤ T_A ≤ +125°C	86			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, 1 V ≤ V_O ≤ 4 V	50	240		V/mV
		R_L = 2 kΩ, –40°C ≤ T_A ≤ +125°C	25			V/mV
Bias Current Drift	$\Delta I_B/\Delta T$			150		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1.0 mA	+4.85			V
Output Voltage Low	V_{OL}	I_L = 1.0 mA			125	mV
Output Currrent	I_{OUT}		±6.5			mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = +2.0 V to +10 V, –40°C ≤ T_A ≤ +125°C	76			dB
Supply Current/Amplifier	I_{SY}	V_O = 2.5 V, –40°C ≤ T_A ≤ +125°C			1.25	mA
Supply Voltage Range	V_S		+3		+36	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	1.65	2.4		V/µs
Settling Time	t_s	To 0.01%, 1.0 V Step		2.5		µs
Gain Bandwidth Product	GBP			3.25		MHz
Phase Margin	Øo			45		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.3		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		3.9		nV/√Hz
Current Noise Density	i_n			0.4		pA/√Hz

NOTES

[1]Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_S = +3.0 V, V_{CM} = 1.5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage "OP184/284E" Grade	V_{OS}	(Note 1)			65	µV
		–40°C ≤ T_A ≤ +125°C			165	µV
Offset Voltage "OP184/284F" Grade	V_{OS}				125	µV
		–40°C ≤ T_A ≤ +125°C			350	µV
Offset Voltage "484E" Grade	V_{OS}				100	µV
		–40°C ≤ T_A ≤ +125°C			200	µV
Offset Voltage "484F" Grade	V_{OS}				150	µV
		–40°C ≤ T_A ≤ +125°C			450	µV
Input Bias Current	I_B			60	300	nA
		–40°C ≤ T_A ≤ +125°C			500	nA
Input Offset Current	I_{OS}	–40°C ≤ T_A ≤ +125°C			50	nA
Input Voltage Range			0		+3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 3 V	60			dB
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 3 V, –40°C ≤ T_A ≤ +125°C	56			dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1.0 mA	+2.85			V
Output Voltage Low	V_{OL}	I_L = 1.0 mA			125	mV
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±1.25 V to ±1.75 V	76			dB
Supply Current/Amplifier	I_{SY}	V_O = 1.5 V, –40°C ≤ T_A ≤ +125°C			1.15	mA
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBP			3		MHz
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		3.9		nV/√Hz

NOTES

[1]Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_S = ±15.0 V, V_{CM} = 0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage "OP184/284E" Grade	V_{OS}	(Note 1)			100	µV
		–40°C ≤ T_A ≤ +125°C			200	µV
Offset Voltage "284F" Grade	V_{OS}				175	µV
		–40°C ≤ T_A ≤ +125°C			375	µV
Offset Voltage "484E" Grade	V_{OS}				150	µV
		–40°C ≤ T_A ≤ +125°C			300	µV
Offset Voltage "484F" Grade	V_{OS}				250	µV
		–40°C ≤ T_A ≤ +125°C			500	µV
Input Bias Current	I_B			80	300	nA
		–40°C ≤ T_A ≤ +125°C			500	nA
Input Offset Current	I_{OS}	–40°C ≤ T_A ≤ +125°C			50	nA
Input Voltage Range			–15		+15	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = –14.0 V to +14.0 V, –40°C ≤ T_A ≤ +125°C	86	90		dB
Common-Mode Rejection Ratio	CMRR	V_{CM} = –15.0 V to +15.0 V	80			dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, –10 V ≤ V_O ≤ 10 V	150	1000		V/mV
		R_L = 2 kΩ, –40°C ≤ T_A ≤ +125°C	75			V/mV
Offset Voltage Drift "E" Grade	$\Delta V_{OS}/\Delta T$			0.2	2.00	µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			150		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1.0 mA	+14.8			V
Output Voltage Low	V_{OL}	I_L = 1.0 mA			–14.875	V
Output Current	I_{OUT}		±10			mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.0 V to ±18 V, –40°C ≤ T_A ≤ +125°C	90			dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V, –40°C ≤ T_A ≤ +125°C			1.75	mA
Supply Current/Amplifier	I_{SY}	V_S = ±18 V, –40°C ≤ T_A ≤ +125°C			2.0	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ	2.4	4.0		V/µs
Full-Power Bandwidth	BW_p	1% Distortion, R_L = 2 kΩ, V_O = 29 V p-p		35		kHz
Settling Time	t_S	To 0.01%, 10 V Step		4		µs
Gain Bandwidth Product	GBP			4.25		MHz
Phase Margin	Øo			50		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.3		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		3.9		nV/√Hz
Current Noise Density	i_n			0.4		pA/√Hz

NOTES
[1]Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.
Specifications subject to change without notice.

WAFER TEST LIMITS (@ V_S = +5.0 V, V_{CM} = 2.5 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Limit	Units
Offset Voltage OP284	V_{OS}		65	µV max
Offset Voltage OP484	V_{OS}		75	µV max
Input Bias Current	I_B		300	nA max
Input Offset Current	I_{OS}		50	nA max
Input Voltage Range	V_{CM}		V– to V+	V min
Common-Mode Rejection Ratio	CMRR	V_{CM} = +1 V to +4 V	86	dB min
Power Supply Rejection Ratio	PSRR	V_S = ±2 V to ±18 V	90	dB min
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ	50	V/mV min
Output Voltage High	V_{OH}	I_L = 1.0 mA	4.85	V min
Output Voltage Low	V_{OL}	I_L = 1.0 mA	125	mV max
Supply Current/Amplifier	I_{SY}	V_O = 0 V, R_L = ∞	1.25	mA max

NOTE
Electrical tests and wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS[1]

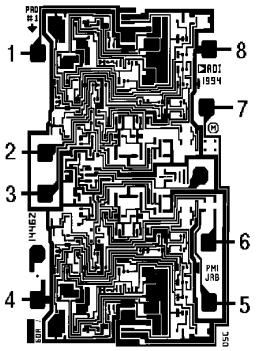
Supply Voltage . . . . . ±18 V
Input Voltage . . . . . ±18 V
Differential Input Voltage[2] . . . . . ±0.6 V
Output Short-Circuit Duration to GND[3] . . . . . Indefinite
Storage Temperature Range
P, S Packages . . . . . –65°C to +150°C
Operating Temperature Range
OP184/OP284/OP484E, F . . . . . –40°C to +125°C
Junction Temperature Range
P, S Packages . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
8-Pin Plastic DIP (P)	103	43	°C/W
8-Pin SOIC (S)	158	43	°C/W
14-Pin Plastic DIP (P)	83	39	°C/W
14-Pin SOIC (S)	92	27	°C/W

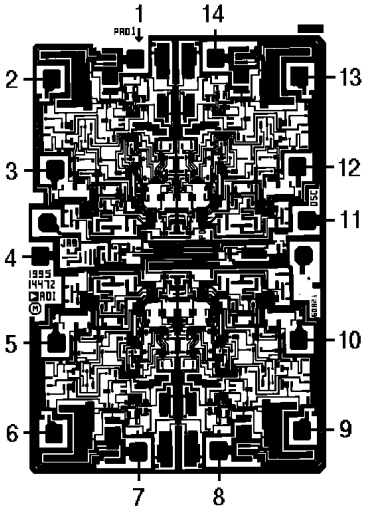
NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]For input voltages greater than 0.6 volts the input current should be limited to less than 5 mA to prevent degradation or destruction of the input devices.
[3]θ_{JA} is specified for the worst case conditions; i.e., θ_{JA} is specified for device in socket for cerdip, and P-DIP packages, θ_{JA} is specified for device soldered in circuit board for SOIC package.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP184EP	–40°C to +125°C	8-Pin Plastic DIP	N-8
OP184ES	–40°C to +125°C	8-Pin SOIC	SO-8
OP184FP	–40°C to +125°C	8-Pin Plastic DIP	N-8
OP184FS	–40°C to +125°C	8-Pin SOIC	SO-8
OP284EP	–40°C to +125°C	8-Pin Plastic DIP	N-8
OP284ES	–40°C to +125°C	8-Pin SOIC	SO-8
OP284FP	–40°C to +125°C	8-Pin Plastic DIP	N-8
OP284FS	–40°C to +125°C	8-Pin SOIC	SO-8
OP484EP	–40°C to +125°C	14-Pin Plastic DIP	N-14
OP484ES	–40°C to +125°C	14-Pin SOIC	SO-14
OP484FP	–40°C to +125°C	14-Pin Plastic DIP	N-14
OP484FS	–40°C to +125°C	14-Pin SOIC	SO-14



OP284 Die Size 0.065 × 0.092 Inch, 5,980 Sq. Mils Substrate (Die Backside) Is Connected to V–. Transistor Count, 62.



OP484 Die Size 0.080 × 0.110 Inch, 8,800 Sq. Mils Substrate (Die Backside) Is Connected to V–. Transistor Count, 120.

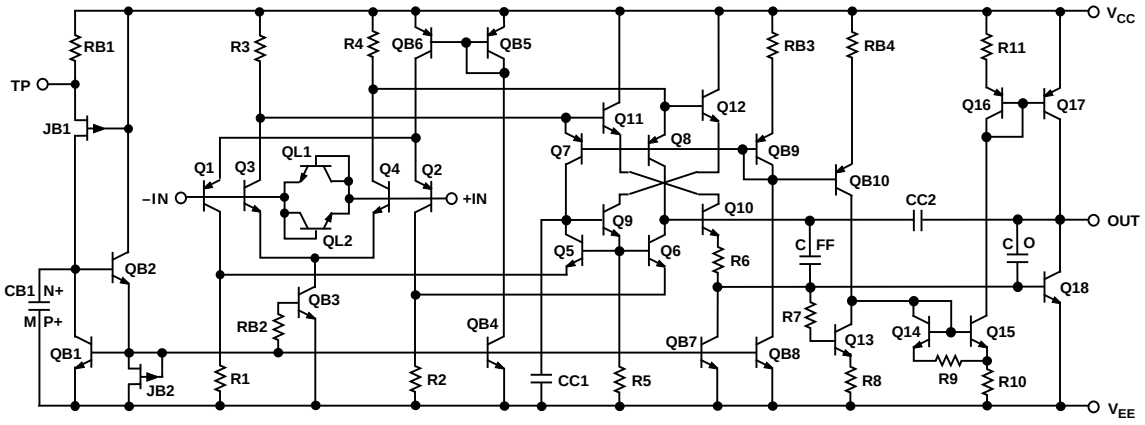


Figure 1. Simplified Schematic

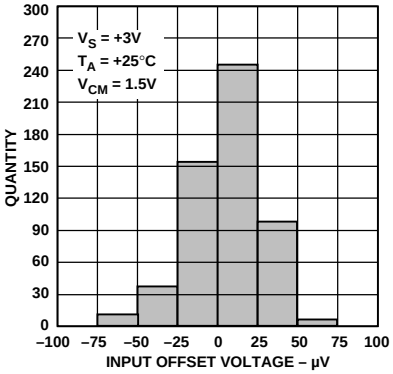


Figure 2. Input Offset Voltage Distribution

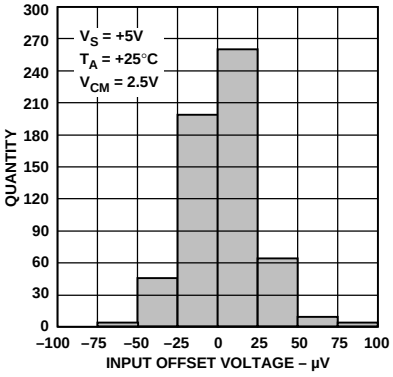


Figure 3. Input Offset Voltage Distribution

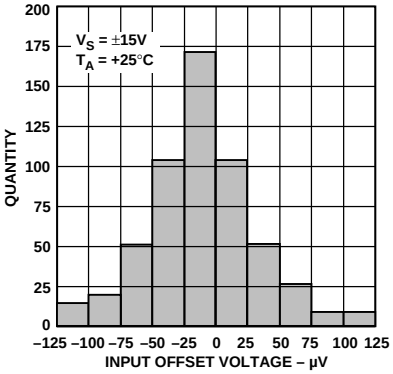


Figure 4. Input Offset Voltage Distribution

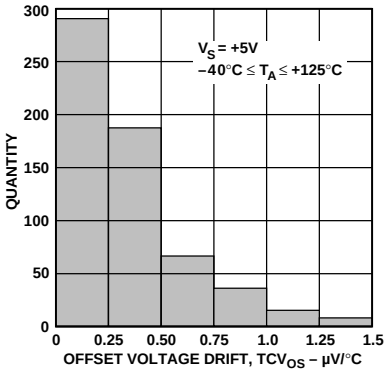


Figure 5. Input Offset Voltage Drift Distribution

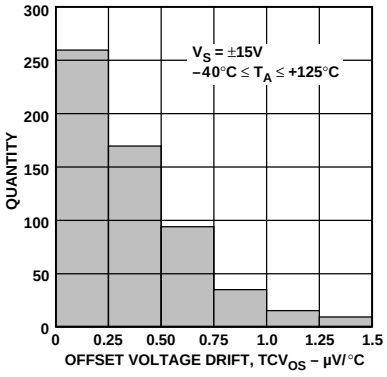


Figure 6. Input Offset Voltage Drift Distribution

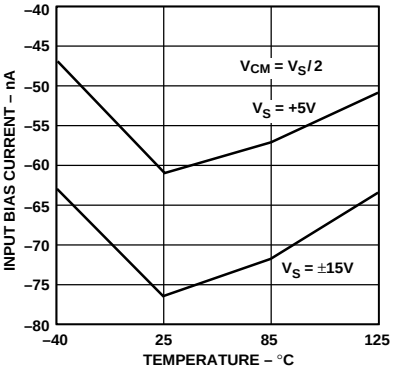


Figure 7. Bias Current vs. Temperature

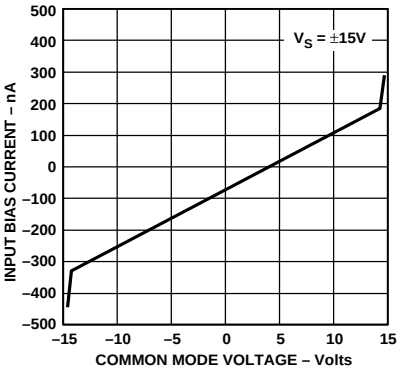


Figure 8. Input Bias Current vs. Common-Mode Voltage

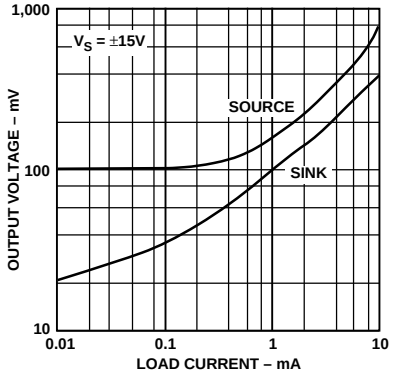


Figure 9. Output Voltage to Supply Rail vs. Load Current

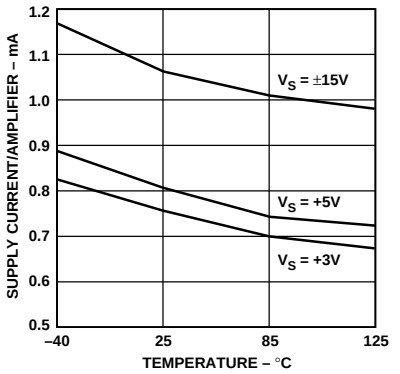


Figure 10. Supply Current vs. Temperature

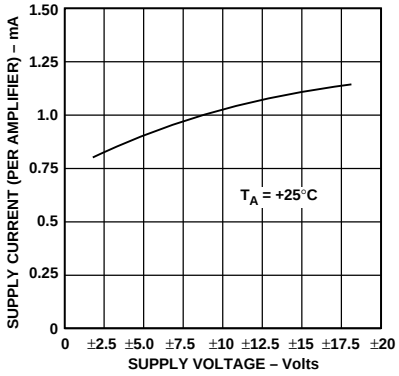


Figure 11. Supply Current vs. Supply Voltage

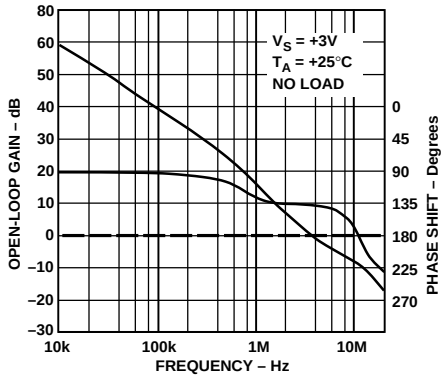


Figure 14. Open-Loop Gain and Phase vs. Frequency (No Load)

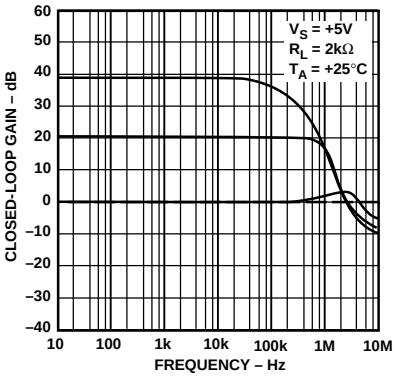


Figure 17. Closed-Loop Gain vs. Frequency (2 kΩ Load)

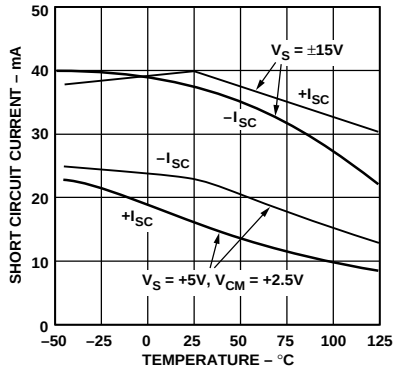


Figure 12. Short Circuit Current vs. Temperature

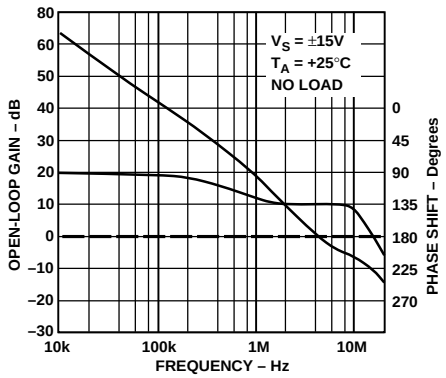


Figure 15. Open-Loop Gain and Phase vs. Frequency (No Load)

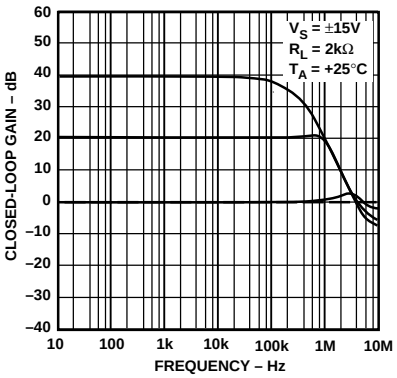


Figure 18. Closed-Loop Gain vs. Frequency (2 kΩ Load)

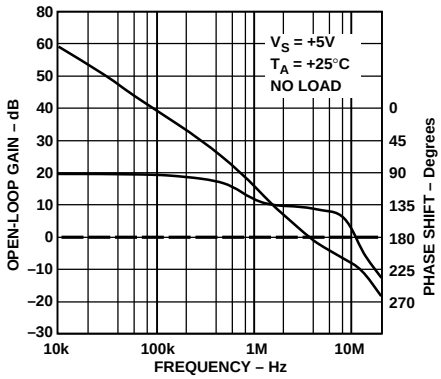


Figure 13. Open-Loop Gain and Phase vs. Frequency (No Load)

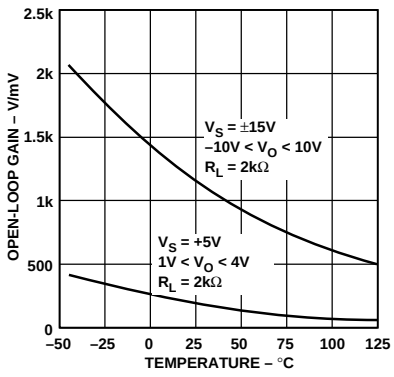


Figure 16. Open-Loop Gain vs. Temperature

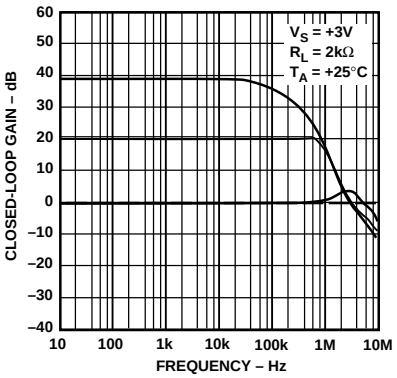


Figure 19. Closed-Loop Gain vs. Frequency (2 kΩ Load)

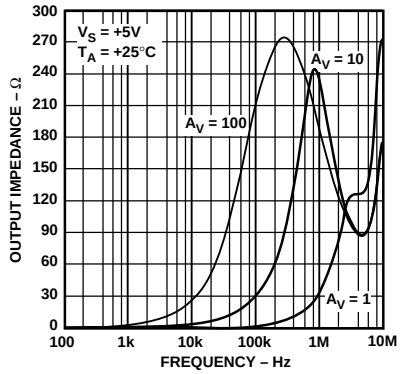


Figure 20. Output Impedance vs. Frequency

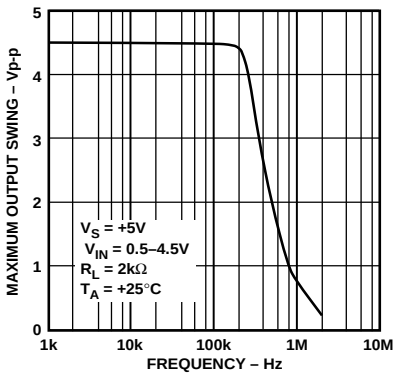


Figure 23. Maximum Output Swing vs. Frequency

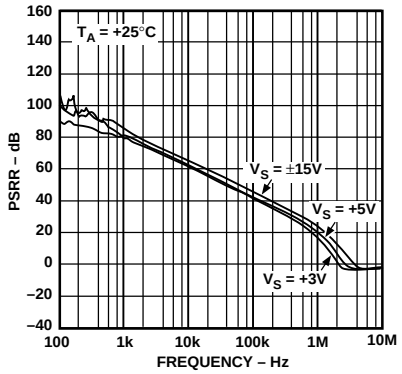


Figure 26. PSRR vs. Frequency

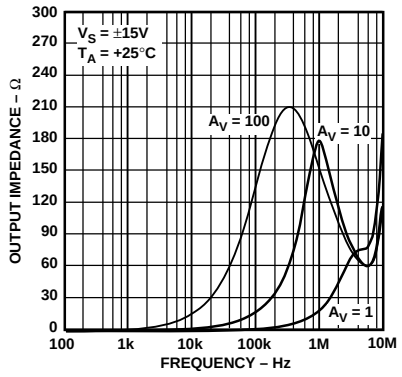


Figure 21. Output Impedance vs. Frequency

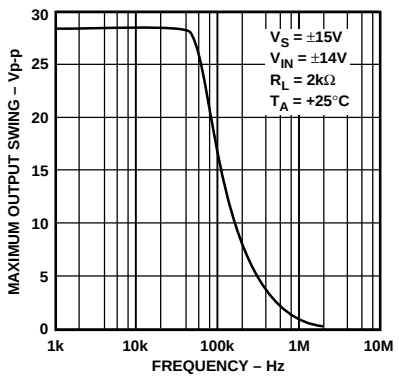


Figure 24. Maximum Output Swing vs. Frequency

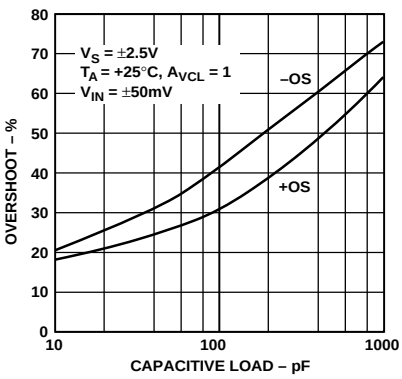


Figure 27. Small Signal Overshoot vs. Capacitive Load

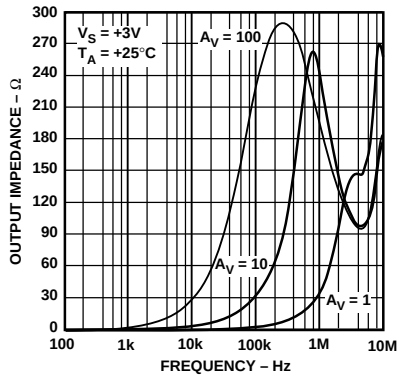


Figure 22. Output Impedance vs. Frequency

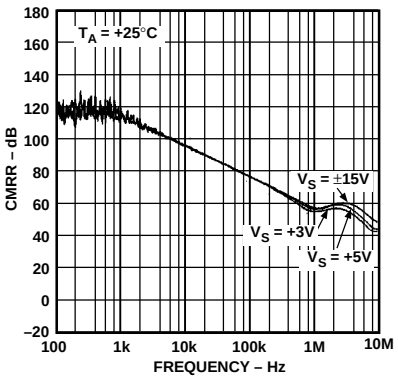


Figure 25. CMRR vs. Frequency

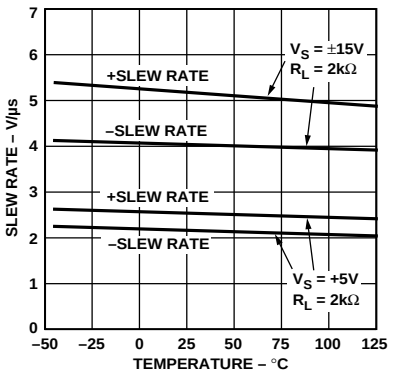


Figure 28. Slew Rate vs.Temperature

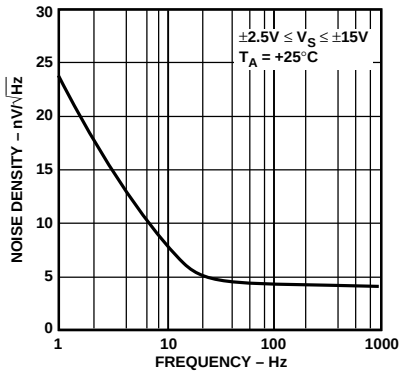


Figure 29. Voltage Noise Density vs. Frequency

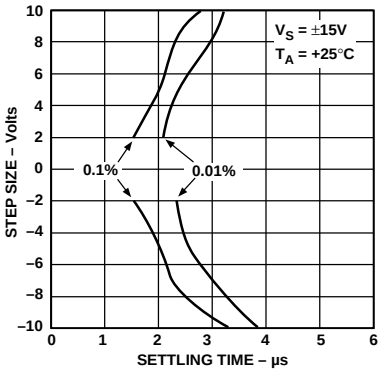


Figure 32. Settling Time vs. Step Size

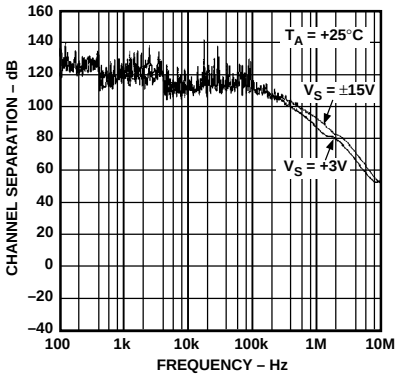


Figure 35. Channel Separation vs. Frequency

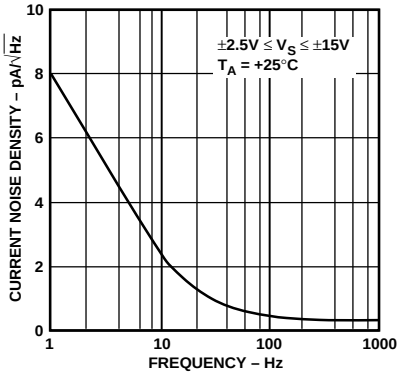


Figure 30. Current Noise Density vs. Frequency

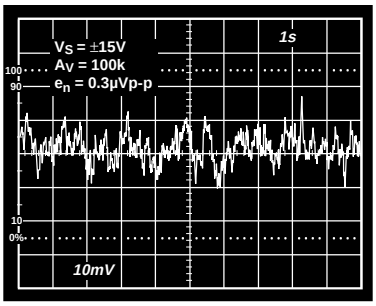


Figure 33. 0.1 Hz to 10 Hz Noise

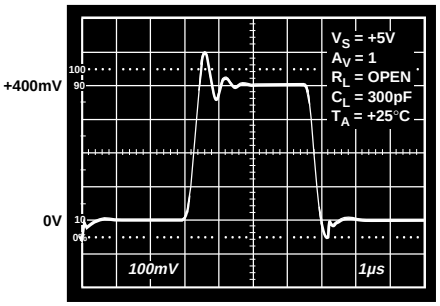


Figure 36. Small Signal Transient Response

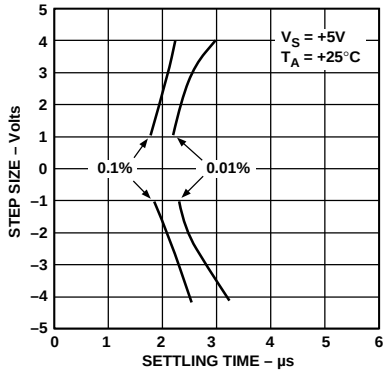


Figure 31. Settling Time vs. Step Size

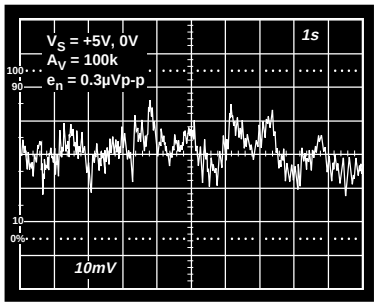


Figure 34. 0.1 Hz to 10 Hz Noise

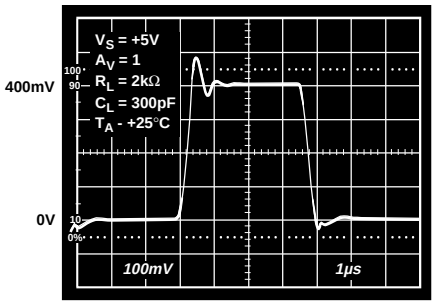


Figure 37. Small Signal Transient Response

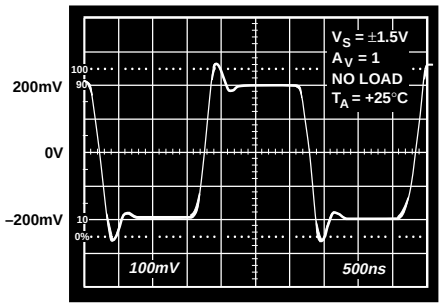


Figure 38. Small Signal Transient Response

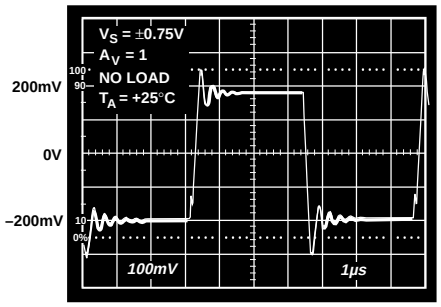


Figure 39. Small Signal Transient Response

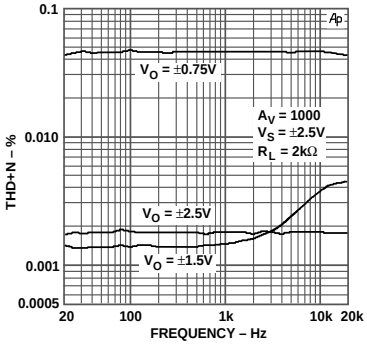


Figure 40. Total Harmonic Distortion vs. Frequency

APPLICATIONS

Functional Description

The OP284 and OP484 are precision single-supply, rail-to-rail operational amplifiers. Intended for the portable instrumentation marketplace, the OP184/OP284/OP484 combines the attributes of precision, wide bandwidth, and low noise to make it a superb choice in those single supply applications that require both ac and precision dc performance. Other low supply voltage applications for which the OP284 is well suited are active filters, audio microphone preamplifiers, power supply control, and telecom. To combine all of these attributes with rail-to-rail input/output operation, novel circuit design techniques are used.

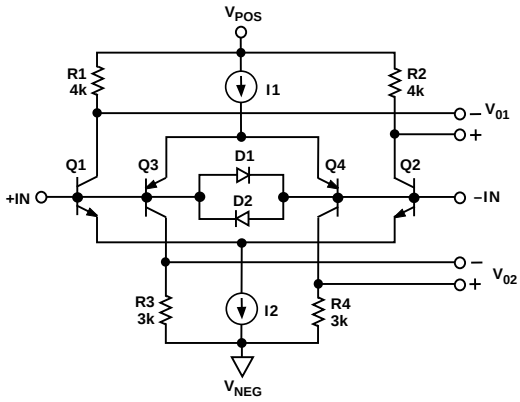


Figure 41. OP284 Equivalent Input Circuit

For example, Figure 41 illustrates a simplified equivalent circuit for the OP184/OP284/OP484's input stage. It is comprised of an NPN differential pair, Q1-Q2, and a PNP differential pair, Q3-Q4, operating concurrently. Diode network D1-D2 serves to clamp the applied differential input voltage to the OP284, thereby protecting the input transistors against avalanche damage. Input stage voltage gains are kept low for input rail-to-rail operation. The two pairs of differential output voltages are connected to the OP284's second stage which is a compound folded cascode gain stage. It is also in the second gain stage where the two pairs of differential output voltages are combined into a single-ended output signal voltage used to drive the output stage. A key issue in the input stage is the behavior of the input bias currents over the input common-mode voltage range. Input bias currents in the OP284 are the arithmetic sum of the base currents in Q1-Q3 and in Q2-Q4. As a result of this design approach, the input bias currents in the OP284 not only exhibit different amplitudes, but also exhibit different polarities. This effect is best illustrated in Figure 8. It is, therefore, of paramount importance that the effective source impedances connected to the OP284's inputs be balanced for optimum dc and ac performance.

In order to achieve rail-to-rail output, the OP284 output stage design employs a unique topology for both sourcing and sinking current. This circuit topology is illustrated in Figure 42. As previously mentioned, the output stage is voltage-driven from the second gain stage. The signal path through the output stage is inverting; that is, for positive input signals, Q1 provides the base current drive to Q6 so that it conducts (sinks) current. For negative input signals, the signal path via Q1-Q2-D1-Q4-Q3 provides the base current drive for Q5 to conduct (source) current. Both amplifiers provide output current until they are forced into saturation which occurs at approximately 20 mV from negative rail and 100 mV from the positive supply rail.

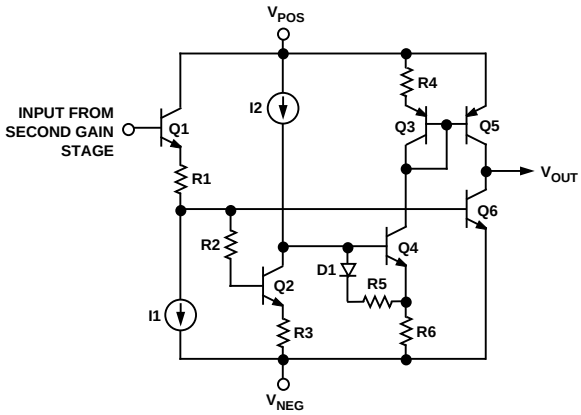


Figure 42. OP284 Equivalent Output Circuit

Thus, the saturation voltage of the output transistors sets the limit on the OP284's maximum output voltage swing. Output short circuit current limiting is determined by the maximum signal current into the base of Q1 from the second gain stage. Under output short circuit conditions, this input current level is approximately 100 μA. With transistor current gains around 200, the short circuit current limits are typically 20 mA. The output stage also exhibits voltage gain. This is accomplished by use of common-emitter amplifiers, and as a result the voltage gain of the output stage (thus, the open-loop gain of the device) exhibits a dependence to the total load resistance at the output of the OP284.

Input Overvoltage Protection

As with any semiconductor device, if conditions exist where the applied input voltages to the device exceed either supply voltage, then the device's input overvoltage I-V characteristic must be considered. When an overvoltage occurs, the amplifier could be damaged depending on the magnitude of the applied voltage and the magnitude of the fault current. Figure 43 illustrates the over voltage I-V characteristic of the OP284. This graph was generated with the supply pins connected to GND and a curve tracer's collector output drive connected to the input.

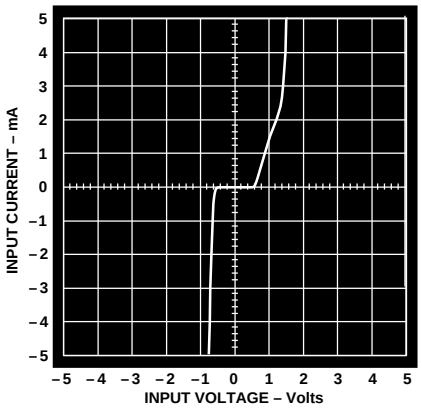


Figure 43. Input Overvoltage I-V Characteristics of the OP284

As shown in the figure, internal p-n junctions to the OP284 energize and permit current flow from the inputs to the supplies when the input is 1.8 V more positive and 0.6 V more negative than the respective supply rails. As illustrated in the simplified equivalent circuit shown in Figure 41, the OP284 does not have any internal current limiting resistors; thus, fault currents can quickly rise to damaging levels.

This input current is not inherently damaging to the device, provided that it is limited to 5 mA or less. For the OP284, once the input exceeds the negative supply by 0.6 V, the input current quickly exceeds 5 mA. If this condition continues to exist, an external series resistor should be added at the expense of additional thermal noise. Figure 44 illustrates a typical noninverting configuration for an overvoltage protected amplifier where the series resistance, R_S, is chosen such that:

$$R_S = \frac{V_{IN\,(MAX)} - V_{SUPPLY}}{5\,mA}$$

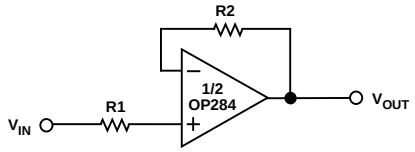


Figure 44. A Resistance in Series with an Input Limits Overvoltage Currents to Safe Values

For example, a 1 kΩ resistor will protect the OP284 against input signals up to 5 V above and below the supplies. For other configurations where both inputs are used, then each input should be protected against abuse with a series resistor. Again, in order to ensure optimum dc and ac performance, it is recommended to balance source impedance levels. For more information on the general overvoltage characteristics of amplifiers, please refer to the *1993 System Applications Guide*, Section 1, pages 56-69. This reference textbook is available from the Analog Devices Literature Center.

Output Phase Reversal

Some operational amplifiers designed for single-supply operation exhibit an output voltage phase reversal when their inputs are driven beyond their useful common-mode range. Typically for single-supply bipolar op amps, the negative supply determines the lower limit of their common-mode range. With these devices, external clamping diodes, with the anode connected to ground and the cathode to the inputs, prevent input signal excursions from exceeding the device's negative supply (i.e., GND), preventing a condition that could cause the output voltage to change phase. JFET-input amplifiers may also exhibit phase reversal, and, if so, a series input resistor is usually required to prevent it.

The OP284 is free from reasonable input voltage range restrictions provided that the input voltages no greater than the supply voltages are applied. Although the device's output will not change phase, large currents can flow through the input protection diodes, as was shown in Figure 43. Therefore, the technique recommended in the Input Overvoltage Protection section should be applied in those applications where the likelihood of input voltages exceeding the supply voltages is high.

Designing Low Noise Circuits in Single Supply Applications

In single supply applications, devices like the OP284 extend the dynamic range of the application through the use of rail-to-rail operation. In fact, the OP284 family is the first of its kind to combine single supply, rail-to-rail operation and low noise in one device. It is the first device in the industry to exhibit an input noise voltage spectral density of less than 4 nV/$\sqrt{\text{Hz}}$ at 1 kHz. It was also designed specifically for low-noise, single-supply applications, and as such some discussion on circuit noise concepts in single supply applications is appropriate.

Referring to the op amp noise model circuit configuration illustrated in Figure 45, the expression for an amplifier's total equivalent input noise voltage for a source resistance level R_S is given by:

$$e_{nT} = \sqrt{2\left[\left(e_{nR}\right)^2 + \left(i_{nOA} \times R\right)^2\right] + \left(e_{nOA}\right)^2},\ units\ in\ \frac{V}{\sqrt{Hz}}$$

where $R_S = 2R$ = Effective, or equivalent, circuit source resistance,
$(e_{nOA})^2$ = Op amp equivalent input noise voltage spectral power (1 Hz BW),
$(i_{nOA})^2$ = Op amp equivalent input noise current spectral power (1 Hz BW),
$(e_{nR})^2$ = Source resistance thermal noise voltage power = (4kTR),
k = Boltzmann's constant = 1.38×10^{-23} J/K, and
T = Ambient temperature of the circuit, in Kelvin, = 273.15 + T_A (°C)

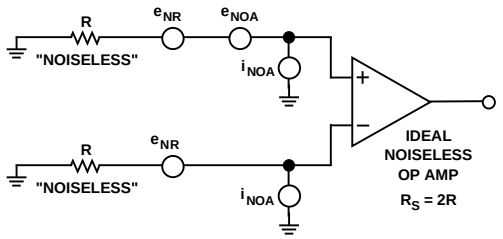


Figure 45. Op Amp Noise Circuit Model Used to Determine Total Circuit Equivalent Input Noise Voltage and Noise Figure

As a design aid, Figure 46 illustrates the total equivalent input noise of the OP284 and the total thermal noise of a resistor for comparison. Note that for source resistance less than 1 kΩ, the equivalent input noise voltage of the OP284 is dominant.

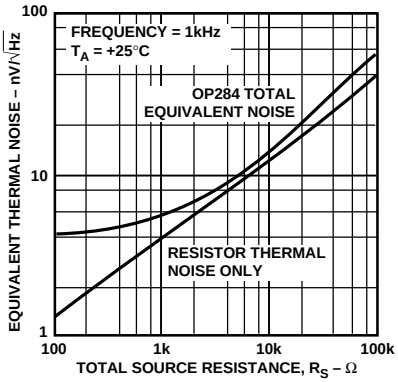


Figure 46. OP284 Total Noise vs. Source Resistance

Since circuit SNR is the critical parameter in the final analysis, many times the noise behavior of a circuit is expressed in terms of its noise figure, NF. Noise figure is defined to be the ratio of a circuit's output signal-to-noise to its input signal-to-noise. An expression for a circuit's NF in dB and in terms of the operational amplifier's voltage and current noise parameters defined previously is given by:

$$NF\ (dB) = 10 \log \left[1 + \left(\frac{\left(e_{nOA}\right)^2 + \left(i_{nOA}\ R_S\right)^2}{\left(e_{nRS}\right)^2}\right)\right]$$

where $NF\ (dB)$ = Noise figure of the circuit, expressed in dB,
R_S = Effective, or equivalent, source resistance presented to amplifier,
$(e_{nOA})^2$ = OP284 noise voltage spectral power (1 Hz BW),
$(i_{nOA})^2$ = OP284 noise current spectral power (1 Hz BW),
$(e_{nRS})^2$ = Source resistance thermal noise voltage power = ($4kTR_S$),

Circuit noise figure is straightforward to calculate because the signal level in the application is not required to determine it. However, many designers using NF calculations as the basis for achieving optimum SNR believe that low noise figure is equal to low total noise. In fact, the opposite is true, as illustrated in Figure 47. Here, the noise figure of the OP284 is expressed as a function of the source resistance level. Note that the lowest noise figure for the OP284 occurs at a source resistance level of 10 kΩ. However, Figure 46 shows that this source resistance level and the OP284 generate approximately 14 nV/√Hz of total equivalent circuit noise. Signal levels in the application would invariably be increased to maximize circuit SNR—not an option in low voltage, single supply applications.

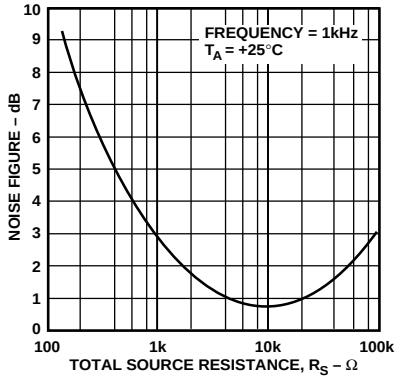


Figure 47. OP284 Noise Figure vs. Source Resistance

In single supply applications, it is, therefore, recommended for optimum circuit SNR to choose an operational amplifier with the lowest equivalent input noise voltage and to choose source resistance levels consistent in maintaining low total circuit noise.

Overdrive Recovery

The overdrive recovery time of an operational amplifier is the time required for the output voltage to recover to its linear region from a saturated condition. The recovery time is important in applications where the amplifier must recover quickly after a large transient event. The circuit shown in Figure 48 was used to evaluate the OP284's overload recovery time. The OP284 takes approximately 2 µs to recover from positive saturation and approximately 1 µs to recover from negative saturation.

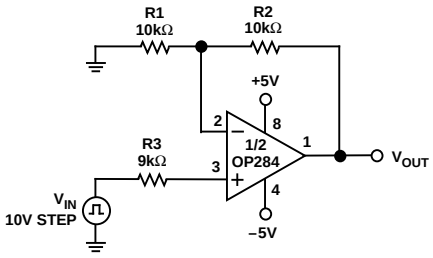


Figure 48. Output Overload Recovery Test Circuit

A Single-Supply, +3 V Instrumentation Amplifier

The OP284's low noise, wide bandwidth, and rail-to-rail input/output operation makes it ideal for low supply voltage applications, such as in an two op amp instrumentation amplifier as shown in Figure 49. The circuit utilizes the classic two op amp instrumentation amplifier topology, with four resistors to set the gain. The transfer equation of the circuit is identical to that of a noninverting amplifier. Resistors R2 and R3 should be closely matched to each other as well as resistors (R1 + P1) and R4 to ensure good common-mode rejection performance. Resistor networks should be used in this circuit for R2 and R3 because they exhibit the necessary relative tolerance matching for good performance. Matched networks also exhibit tight relative resistor temperature coefficients for good circuit temperature stability. Trimming potentiometer P1 is used for optimum dc CMR adjustment, and C1 is used to optimize ac CMR. With the circuit values as shown, circuit CMR is better than 80 dB over the frequency range of 20 Hz to 20 kHz. Circuit RTI (Referred-to-Input) noise in the 0.1 Hz to 10 Hz band is an impressively low 0.45 µV p-p. Resistors RP1 and RP2 serve to protect the OP284's inputs against input overvoltage abuse. Capacitor C2 can be included to the limit circuit bandwidth and, therefore, wide bandwidth noise in sensitive applications. The value of this capacitor should be adjusted depending on the required closed-loop bandwidth of the circuit. The R4-C2 time constant creates a pole at a frequency equal to:

$$f(3\,dB) = \frac{1}{2\pi R4\,C2}$$

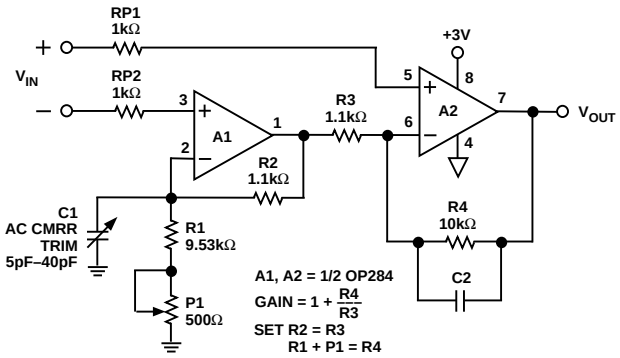


Figure 49. A Single Supply, +3 V Low Noise Instrumentation Amplifier

A +2.5 V Reference from a +3 V Supply

In many single-supply applications, the need for a 2.5 V reference often arises. Many commercially available monolithic 2.5 V references require at least a minimum operating supply of 4 V. The problem is exacerbated when the minimum operating supply voltage is +3 V. The circuit illustrated in Figure 50 is an example of a +2.5 V reference that operates from a single +3 V supply. The circuit takes advantage of the OP284's rail-to-rail input/output voltage ranges to amplify an AD589's 1.235 V output to +2.5 V. The OP284's low TCV_{OS} of 1.5 µV/°C helps to maintain an output voltage temperature coefficient which is dominated by the temperature coefficients of R2 and R3. In this circuit with 100 ppm/°C TCR resistors, the output voltage exhibits a temperature coefficient of 200 ppm/°C. Lower tempco resistors are recommended for more accurate performance over temperature.

One measure of the performance of a voltage reference is its capability to recover from sudden changes in load current. While sourcing a steady-state load current of 1 mA, this circuit recovers to 0.01% of the programmed output voltage in 1.5 µs for a total change in load current of ±1 mA.

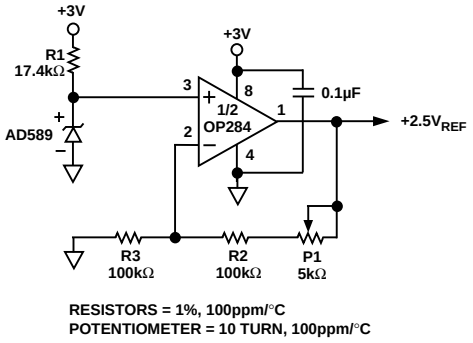


Figure 50. A +2.5 V Reference that Operates on a Single +3 V Supply

A +5 V Only, 12-Bit DAC Swings Rail-to-Rail

The OP284 is ideal for use with a CMOS DAC to generate a digitally-controlled voltage with a wide output range. Figure 51 shows a DAC8043 used in conjunction with the AD589 to generate a voltage output from 0 V to 1.23 V. The DAC is actually operating in "voltage switching" mode where the reference is connected to the current output, I_{OUT}, and the output voltage is taken from the V_{REF} pin. This topology is inherently noninverting as opposed to the classic current output mode, which is inverting and not usable in single supply applications.

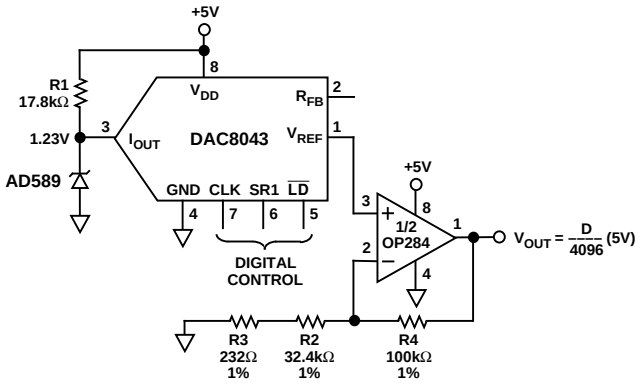


Figure 51. A +5 V Only, 12-Bit DAC Swings Rail-to-Rail

In this application the OP284 serves two functions. First, it buffers the high output impedance of the DAC's V_{REF} pin, which is on the order of 10 kΩ. The op amp provides a low impedance output to drive any following circuitry. Second, the op amp amplifies the output signal to provide a rail-to-rail output swing. In this particular case, the gain is set to 4.1 so that the circuit generates a 5 V output when the DAC output is at full scale. If other output voltage ranges are needed, such as 0 V ≤ V_{OUT} ≤ 4.095 V, the gain can easily be changed by adjusting the values of R2 and R3.

A High-Side Current Monitor

In the design of power supply control circuits, a great deal of design effort is focused on ensuring a pass transistor's long-term reliability over a wide range of load current conditions. As a result, monitoring and limiting device power dissipation is of prime importance in these designs. The circuit illustrated in Figure 52 is an example of a +3 V, single-supply high-side current monitor that can be incorporated into the design of a voltage regulator with fold-back current limiting or a high current power supply with crowbar protection. This design uses an OP284's rail-to-rail input voltage range to sense the voltage drop across a 0.1 Ω current shunt. A p-channel MOSFET used as the feedback element in the circuit converts the op amp's differential input voltage into a current. This current is then applied to R2 to generate a voltage that is a linear representation of the load current. The transfer equation for the current monitor is given by:

$$Monitor\ Output = R2 \times \left(\frac{R_{SENSE}}{R1} \right) \times I_L$$

For the element values shown, the Monitor Output's transfer characteristic is 2.5 V/A.

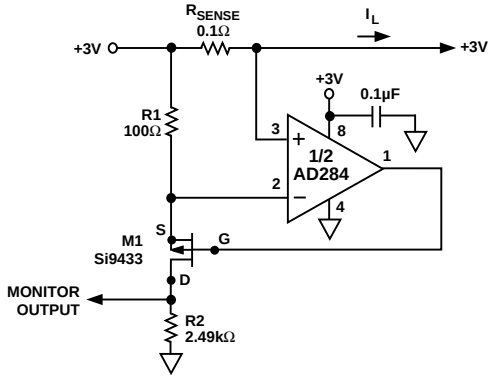


Figure 52. A High-Side Load Current Monitor

Capacitive Load Drive Capability

The OP284 exhibits excellent capacitive load driving capabilities. It can drive up to 1 nF as shown in Figure 27. However, even though the device is stable, a capacitive load does not come without penalty in bandwidth. The bandwidth is reduced to under 1 MHz for loads greater than 2 nF. A "snubber" network on the output doesn't increase the bandwidth, but it does significantly reduce the amount of overshoot for a given capacitive load. A snubber consists of a series R-C network (R_S, C_S), as shown in Figure 53, connected from the output of the device to ground. This network operates in parallel with the load capacitor, C_L, to provide the necessary phase lag compensation. The value of the resistor and capacitor is best determined empirically.

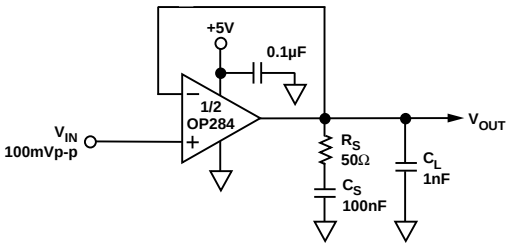


Figure 53. Snubber Network Compensates for Capacitive Load

The first step is to determine the value of the resistor R_S. A good starting value is 100 Ω (typically, the optimum value will be less than 100 Ω). This value is reduced until the small-signal transient response is optimized. Next, C_S is determined—10 µF is a good starting point. This value is reduced to the smallest value for acceptable performance (typically, 1 µF). For the case of a 10 nF load capacitor on the OP284, the optimal snubber network is a 20 Ω in series with 1 µF. The benefit is immediately apparent as shown in the scope photo in Figure 54. The top trace was taken with a 1 nF load, and the bottom trace was taken with the 50 Ω, 100 nF snubber network in place. The amount of overshoot and ringing is dramatically reduced. Table I below illustrates a few sample snubber networks for large load capacitors.

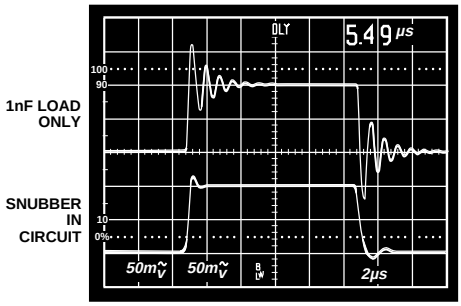


Figure 54. Overshoot and Ringing Is Reduced by Adding a "Snubber" Network in Parallel with the 1 nF Load

Table I. Snubber Networks for Large Capacitive Loads

Load Capacitance (C_L)	Snubber Network (R_S, C_S)
1 nF	50 Ω, 100 nF
10 nF	20 Ω, 1 µF
100 nF	5 Ω, 10 µF

A Low Dropout Regulator with Current Limiting

Many circuits require stable regulated voltages relatively close in potential to an unregulated input source. This "low dropout" type of regulator is readily implemented with a rail-to-rail output op amp such as the OP284, because the wide output swing allows easy drive to a low saturation voltage pass device. Furthermore, it is particularly useful when the op amp also enjoys a rail-rail input feature, as this factor allows it to perform high-side current sensing for positive rail current limiting. Typical examples are voltages developed from 3 V to 9 V range system sources, or anywhere where low dropout performance is required for power efficiency. The 4.5 V case here works from 5 V nominal sources, with worst-case levels down to 4.6 V or less.

Figure 55 shows such a regulator set up using an OP284 plus a low $R_{DS(ON)}$, P-channel MOSFET pass device. Part of the low dropout performance of this circuit is provided by Q1, which has a rating of 0.11 Ω with a gate drive voltage of only 2.7 V. This relatively low gate drive threshold allows operation of the regulator on supplies as low as 3 V without compromise to overall performance.

The circuit's main voltage control loop operation is provided by U1B, half of the OP284. This voltage control amplifier amplifies the 2.5 V reference voltage produced by three terminal U2, a REF192. The regulated output voltage V_{OUT} is then:

$$V_{OUT} = V_{OUT2}\left(1+\frac{R2}{R3}\right)$$

For the example here, a V_{OUT} of 4.5 V with V_{OUT2} = 2.5 V requires a U1B gain of 1.8 times, so R3 and R2 are chosen for a ratio of 1.2:1, or 10.0 kΩ:8.06 kΩ (using closest 1% values). Note that for the lowest V_{OUT} dc error, R2‖R3 should be maintained equal to R1 (as here), and the R2-R3 resistors should be stable, close tolerance metal film types. The table in Figure 55 summarizes R1-R3 values for some popular voltages. However, note that in general the output can be anywhere between V_{OUT2} to the 12 V maximum rating of Q1.

While the low voltage saturation characteristic of Q1 is a key part of the low dropout, another component is a low current sense comparison threshold with good dc accuracy. Here, this is provided by current sense amplifier U1A, which is provided a 20 mV reference from the 1.235 V AD589 reference diode D2 and the R7-R8 divider. When the product of the output current and the R_S value matches this voltage threshold, the current control loop is activated, and U1A drives Q1's gate through D1. This causes the overall circuit operation to enter current mode control, with a current limit I_{LIMIT} defined as:

$$I_{LIMIT} = \left(\frac{V_{R(D2)}}{R_S}\right)\left(\frac{R7}{R7+R8}\right)$$

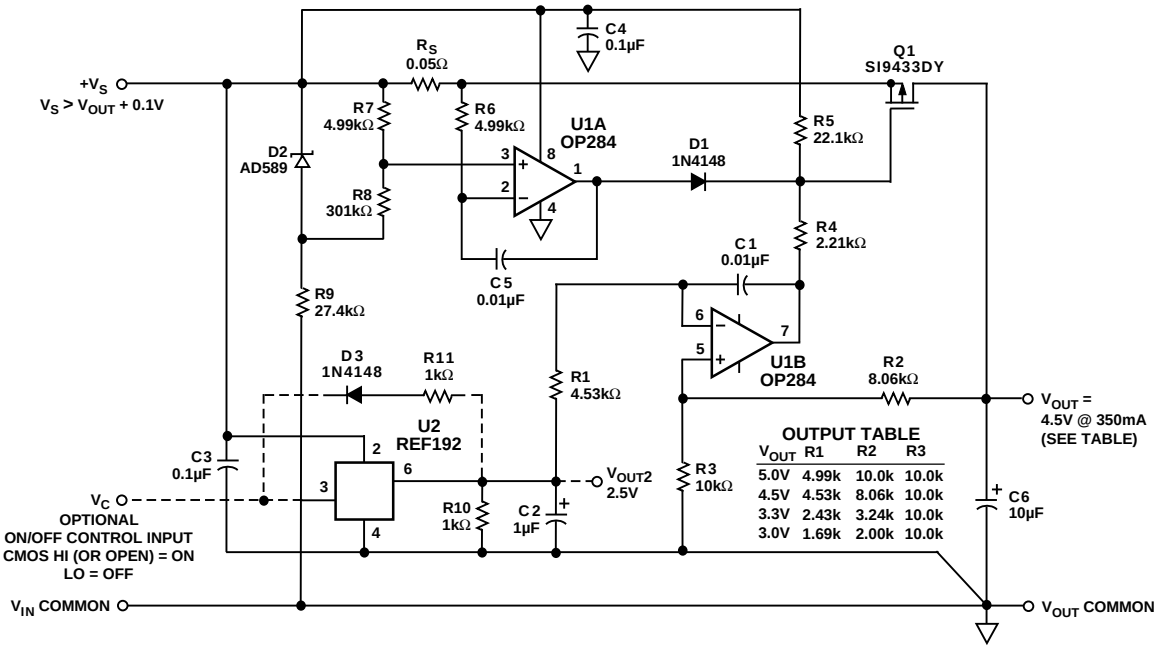


Figure 55. A Low Dropout Regulator with Current Limiting

Obviously, it is desirable to keep this comparison voltage small, since it becomes a significant portion of the overall dropout voltage. Here, the 20 mV reference, is higher than the typical offset of the OP284, but still reasonably low as a percentage of V_{OUT} (< 0.5%). In adapting the limiter for other I_{LIMIT} levels, sense resistor R_S should be adjusted along with R7-R8, to maintain this threshold voltage between 20 mV and 50 mV.

Performance of the circuit is excellent. For the 4.5 V output version, the measured dc output change for a 225 mA load change was on the order of a few microvolts, while the dropout voltage at this same current level was about 30 mV. The current limit as shown is 400 mA, which allows the circuit to be used at levels up to 300 mA or more. While the Q1 device can actually support currents of several amperes, a practical current rating takes into account the SO-8 device's 2.5 W, 25°C dissipation. A short circuit current of 400 mA at an input level of 5 V will cause a 2 W dissipation in Q1, so other input conditions should be considered carefully in terms of Q1's potential overheating. Of course, if higher powered devices are used for Q1, this circuit can support outputs of tens of amperes as well as the higher V_{OUT} levels noted above.

The circuit shown can be used either as a standard low dropout regulator, or it can also be used with ON/OFF control. By driving Pin 3 of U1 with the optional logic control signal V_C, the output is switched between ON and OFF. Note that when the output is OFF in this circuit, it is still active (i.e., not an open circuit). This is because the OFF state simply reduces the voltage input to R1, leaving the U1A/B amplifiers and Q1 still active.

When ON/OFF control is used, resistor R10 should be used with U1, to speed ON-OFF switching, and to allow the output of the circuit to settle to a nominal zero voltage. Components D3 and R11 also aid in speeding up the ON-OFF transition, by providing a dynamic discharge path for C2. OFF-ON transition time is less than 1 ms, while the ON-OFF transition is longer, but under 10 ms.

A +3 V, 50 Hz/60 Hz Active Notch Filter with False Ground

To process signals in a single-supply system, it is often best to use a false ground biasing scheme. A circuit that uses this approach is illustrated in Figure 56. In this circuit, a false-ground circuit biases an active notch filter used to reject 50 Hz/60 Hz power line interference in portable patient monitoring equipment. Notch filters are quite commonly used to reject power line frequency interference which often obscures low frequency physiological signals, such as heart rates, blood pressure readings, EEGs, EKGs, et cetera. This notch filter effectively squelches 60 Hz pickup at a filter Q of 0.75. Substituting 3.16 kΩ resistors for the 2.67 kΩ in the twin-T section (R1 through R5) configures the active filter to reject 50 Hz interference.

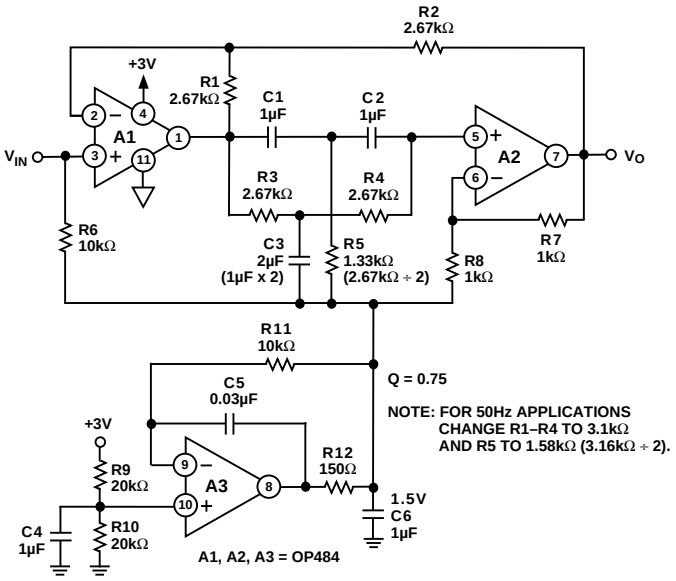


Figure 56. A +3 V Single Supply, 50/60 Hz Active Notch Filter with False Ground

Amplifier A3 is the heart of the false-ground bias circuit. It simply buffers the voltage developed at R9 and R10 and is the reference for the active notch filter. Since the OP484 exhibits a rail-to-rail input common-mode range, R9 and R10 are chosen to split the +3 V supply symmetrically. An in-the-loop compensation scheme is used around the OP484 that allows the op amp to drive C6, a 1 µF capacitor, without oscillation. C6 maintains a low impedance ac ground over the operating frequency range of the filter.

The filter section uses a OP484 in a twin-T configuration whose frequency selectivity is very sensitive to the relative matching of the capacitors and resistors in the twin-T section. Mylar is the material of choice for the capacitors, and the relative matching of the capacitors and resistors determines the filter's pass band symmetry. Using 1% resistors and 5% capacitors produces satisfactory results.

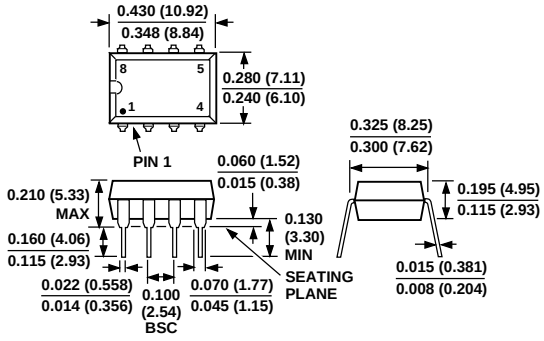
```
*OP284 SPICE Macro-model          9/94 / Rev. A
*                                       ARG/ADI
*
* Copyright 1995 by Analog Devices
*
* Refer to "README.DOC" file for License Statement. Use of this model
* indicates your acceptance of the terms and provisions in the License
* Statement.
*
* Node assignments
*                                  noninverting input
*                                  |  inverting input
*                                  |  |  positive supply
*                                  |  |  |  negative supply
*                                  |  |  |  |  output
*                                  |  |  |  |  |
.SUBCKT OP284                      1  2  99 50 45
*
* INPUT STAGE
*
Q1      5     2     3     QIN 1
Q2      6     11    3     QIN 1
Q3      7     2     4     QIP 1
Q4      8     11    4     QIP 1
DC1     2     11    DC
DC2     11    2     DC
Q5      4     9     99    QIP 1
Q6      9     9     99    QIP 1
Q7      3     10    50    QIN 1
Q8      10    10    50    QIN 1
R1      99    5     4E3
R2      99    6     4E3
R3      7     50    4E3
R4      8     50    4E3
IREF    9     10    50.5E-6
EOS     1     11    POLY(2) (22,98) (14,98) -25E-6 1E-2 1
IOS     2     1     5E-9
CIN     1     2     2E-12
GN1     98    1     (17,98) 1E-3
GN2     98    2     (23,98) 1E-3
*
* VOLTAGE NOISE SOURCE WITH FLICKER NOISE
*
VN1     13    98    DC 2
VN2     98    15    DC 2
DN1     13    14    DEN
DN2     14    15    DEN
*
* CURRENT NOISE SOURCE WITH FLICKER NOISE
*
VN3     16    98    DC 2
VN4     98    18    DC 2
DN3     16    17    DIN
DN4     17    18    DIN
*
* 2ND CURRENT NOISE SOURCE WITH FLICKER NOISE
*
VN5     19    98    DC 2
VN6     98    24    DC 2
DN5     19    23    DIN
DN6     23    24    DIN
*
* GAIN STAGE
*
EREF    98    0     POLY(2) (99,0) (50,0) 0 0.5 0.5
G1      98    20    POLY(2) (6,5) (8,7) 0 0.5E-3 0.5E-3
R9      20    98    1E3
*
* COMMON MODE STAGE WITH ZERO AT 100Hz
*
ECM     98    21    POLY(2) (1,98) (2,98) 0 0.5 0.5
R10     21    22    1
R11     22    98    100E-6
C4      21    22    1.592E-3
*
* NEGATIVE ZERO AT 20MHz
*
E1      27    98    (20,98) 1E6
R17     27    28    1
R18     28    98    1E-6
C8      25    26    7.958E-9
ENZ     25    98    (27,28) 1
VNZ     26    98    DC 0
FNZ     27    28    VNZ -1
*
* POLE AT 40MHz
*
G4      98    29    (28,98) 1
R19     29    98    1
C9      29    98    3.979E-9
*
* POLE AT 40MHz
*
G5      98    30    (29,98) 1
R20     30    98    1
C10     30    98    3.979E-9
*
* OUTUT STAGE
*
ISY     99    50    0.276E-3
GIN     50    31    POLY(1) (30,98) .862574E-6 505.879E-6
RIN     31    50    2.75E6
VB      99    32    0.7
Q11     32    31    33    QON 1
R21     33    34    4.5E3
I1      34    50    50E-6
R22     99    35    6E3
Q12     36    36    35    QOP 1
I2      36    50    50E-6
R23     99    37    2.6E3
R24     34    38    5E3
Q13     39    36    37    QOP 1
Q14     39    38    40    QON 1.5
R25     40    50    40
Q15     39    39    41    QON 1
R26     41    42    1E3
R27     99    43    220
Q16     44    44    43    QOP 1.5
Q17     44    39    42    QON 1
R28     42    50    2E3
VSCP    99    97    DC 0
```

```
FSCP    46    99    VSCP 1
RSCP    46    99    40
Q20     44    46    99    QOP 1
Q18     45    44    97    QOP 4.5
Q19     45    34    51    QON 4.5
VSCN    51    50    DC 0
FSCN    50    47    VSCN 1
RSCN    47    50    40
Q21     34    47    50    QON 1
CC2     31    45    20E-12
CF1     31    34    15E-12
CF2     31    42    15E-12
CO1     34    45    15E-12
CO2     42    45    5E-12
D3      45    99    DX
D4      50    45    DX
.MODEL DC D(IS=130E-21)
.MODEL DX D()
.MODEL DEN D(RS=100 KF=12E-15 AF=1)
.MODEL DIN D(RS=5.358 KF=56E-15 AF=1)
.MODEL QIN NPN(BF=200 VA=200 IS=0.5E-16)
.MODEL QIP PNP(BF=100 VA=60 IS=0.5E-16)
.MODEL QON NPN(BF=200 VA=200 IS=0.5E-16 RC=50)
.MODEL QOP PNP(BF=200 VA=200 IS=0.5E-16 RC=160)
.ENDS
```

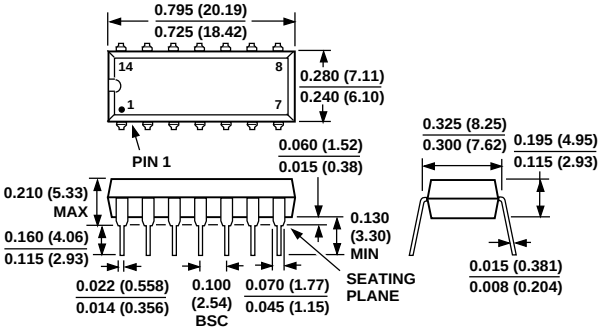
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

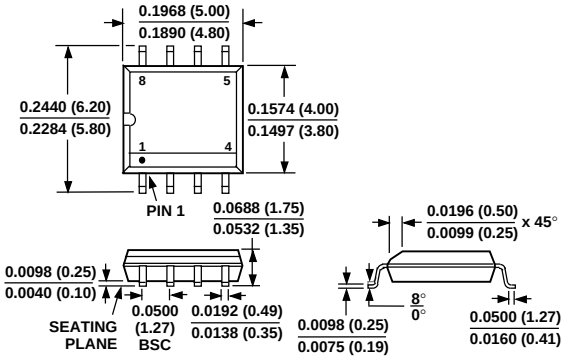
8-Lead Epoxy DIP (P Suffix)



14-Lead Epoxy DIP (P Suffix)



8-Lead SO (S Suffix)



14-Lead Narrow-Body SO (S Suffix)