Thermal Sensor (ALTTEMP_SENSE) Megafunction User Guide

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This user guide describes the features and behavior of the ALTTEMP_SENSE megafunction that you can configure through the MegaWizard™ interface in the Quartus® II software. This user guide also includes a design example that instantiates the temperature sensing diode (TSD) block using the ALTTEMP_SENSE megafunction.

This user guide assumes that you are familiar with megafunctions and how to create them. If you are unfamiliar with Altera megafunctions or the MegaWizard Plug-In Manager, refer to the *Megafunction Overview User Guide*.

Introduction

Altera® provides the temperature measurement feature through the TSD block. The TSD block includes an 8-bit analog to digital converter (ADC), a clock divider, comparator, decoder, and a temperature sensing diode that performs temperature measurement of an FPGA.

The TSD block is set and implemented in your design using the ALTTEMP_SENSE megafunction.

Device Family Support

The ALTTEMP_SENSE megafunction is only available for Stratix® IV device family, and its corresponding HardCopy® device family.

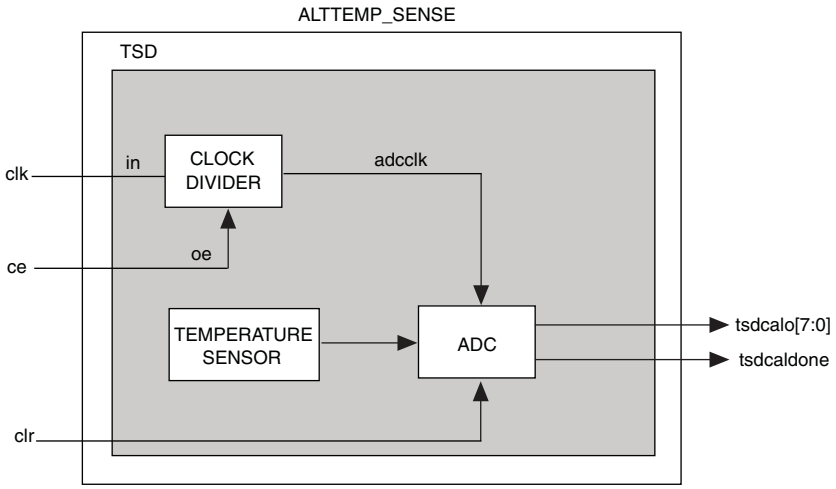
Temperature Sensing Operation

To utilize the TSD block, you must provide three signals to the ALTTEMP_SENSE megafunction block—`clk`, `ce`, and `clr` signals. There are two output ports—`tsdcalo[7:0]` and `tsdcaldone`. The `ce` and `clr` signals are optional. By default, the `ce` signal is connected to VCC and the `clr` signal is connected to GND.

For more information about the input and output ports, refer to "Ports and Parameters" on page 6.

Figure 1 shows the top-level ports and the basic building blocks of the ALTTEMP_SENSE megafunction.

Figure 1. Input and Output Ports of the ALTTEMP_SENSE Megafunction



The ALTTEMP_SENSE megafunction runs at the frequency of the `clk` signal. The allowable frequency for the `clk` signal is 1 MHz or 40 MHz. In the TSD block, the clk signal is divided down to 1 MHz or 500 kHz to feed the ADC (refer to the `adcclk` signal in Figure 1). You can select the value of the clock divider using the ALTTEMP_SENSE MegaWizard interface.

The TSD block operates whenever the `ce` signal is high. When the `ce` signal goes low, the ADC is disabled, and the `tsdcalo[7..0]` and `tsdcaldone` signals maintain their previous values unless the `clr` signal is asserted, or the device is reset. The `clr` signal is asynchronous, and must be asserted at least one clock cycle of the `adcclk` signal to clear the output ports.

The `ce` signal is connected by default to VCC when there is no `ce` port generated. In this case, the ADC circuitry is always enabled. Altera recommends to disable the ADC when the ADC is not in use to reduce power consumption.

During device power-up or when the asynchronous `clr` signal is asserted, the `tsdcaldone` port is set to `0` and the `tsdcalo[7:0]` signal is set to `11010101`. After 10 clock cycles of the `adcclk` signal, the `tsdcaldone` signal is asserted to indicate that the temperature sensing operation is complete and that the value of the `tsdcalo[7:0]` signal is valid. The value of the `tsdcalo[7:0]` signal corresponds to the device temperature range shown in Table 4 on page 7. To start another temperature sensing operation, assert the `clr` signal for at least one clock cycle of the `adcclk` signal, or reset the device.

The `clr` signal is connected by default to GND when there is no `clr` port generated. In this case, you need to reset the device to clear the output signals or start a temperature sensing operation. Altera recommends to generate the `clr` port if you are planning to run the temperature sensing operation more than once.

ALTTEMP_SENSE MegaWizard Interface

This section provides descriptions of the options available on the **Parameter Settings**, **EDA**, and **Summary** pages of the ALTTEMP_SENSE MegaWizard interface. The ALTTEMP_SENSE megafunction is listed under the **I/O** category in the MegaWizard Plug-In Manager.

For an introduction to megafunctions and more information on how to create them, refer to *Megafunction Overview User Guide* on the Altera website.

The options on page 2 and page 2a of the MegaWizard Plug-In Manager are the same for all supported device families. For more information, refer to the "Device Family Support" section of the *Megafunction Overview User Guide*.

Table 1 describes the options that you can find on the **Parameter Settings** page of the ALTTEMP_SENSE MegaWizard interface.

Table 1. ALTTEMP_SENSE Megafunction Options and Descriptions

Option	Description
What is the input frequency?	This is the input frequency of the `clk` signal. The frequency can only be **1** MHz or **40** MHz.
What is the clock divider value?	Specify the clock divider value. The `clk` signal that feeds the ADC. You can choose **40** or **80**. Altera recommends clocking the ADC with a 500 kHz signal (clock divider value equals to **80**). This option is only enabled when the `clk` signal frequency is **40** MHz.
Create a clock enable port	If selected, the `ce` port is created. If not selected, the default value is VCC
Create an asynchronous clear port	If selected, the `clr` port is created. If not selected, the default value is GND

For detailed descriptions of the ports described in Table 1, refer to "Ports and Parameters" on page 6.

The **EDA** page allows you to specify options for simulation and timing and resource estimation. This page normally lists the simulation libraries that are required for functional simulation by third-party tools. However, the ALTTEMP_SENSE megafunction does not have simulation model files, and cannot be simulated.

The **Summary** page allows you to specify the generated file types. The Variation file contains wrapper code in the HDL you specified on page 2a of the MegaWizard Plug-In Manager. You can optionally generate Pin Planner ports PPF file (**.ppf)**, AHDL Include file (<*function name*>**.inc**), VHDL component declaration file (<*function name*>**.cmp)**, Quartus II symbol file (<*function name*>**.bsf**), Instantiation template file (<*function name*>**.v)**, and Verilog HDL black box file (<*function name*>_bb**.v**). If you select the Generate netlist option on the **EDA** page, the file for the synthesis area and timing estimation netlist (<*function name*>_syn**.v**) is also available. A gray checkmark indicates that a file is automatically generated.

Design Example

This section describes a design example that uses the ALTTEMP_SENSE megafunction to control the TSD block in your targeted device. This example uses the MegaWizard Plug-In Manager in the Quartus II software. Each page of the MegaWizard interface is described in detail.

Design Files

The design files are available on the Literature and Technical Documentation page of the Altera website. The files are located under the following sections:

- On the Quartus II Development Software Literature page, expand the **Using Megafunctions** section and then expand the **I/O** section
- Literature: User Guides section

Example: Temperature Sensing Operation in Stratix IV

This design example uses the TSD block in the Stratix IV device (EP4SGX180DF29C3) to perform temperature measurement operation. This design example illustrates the parameters that you must set in the ALTTEMP_SENSE MegaWizard interface.

In this example, complete the following steps:

1. Instantiate the ALTTEMP_SENSE megafunction using the MegaWizard Plug-In Manager with the following specifications:
   - The input clock to the TSD block is 40 MHz
   - The ADC is clocked with a 500 kHz signal
   - An asynchronous signal is used to reset the TSD block
   - An asynchronous signal is used to enable or disable the TSD block
2. Compile the project.
3. Analyze the design netlist using the Netlist Viewers.

Restoring the Quartus II Project Archive

To restore the project archive of the design example, perform the following steps:

1. Open the **alttemp_sense_ ex1.zip** file and extract the Quartus II archive project **alttemp_sense_ex1.qar**.
2. In the Quartus II software, open **alttemp_sense_ex1.qar** file and restore the archive file into your working directory.
3. Open the top-level file **alttemp_sense_ex1.bdf**.
4. The file **alttemp_sense_ex1.bdf** is an incomplete file that you can complete in this example. The ALTTEMP_SENSE block that you create in this example is added to the top-level file.

Generating an ALTTEMP_SENSE Block

To generate the ALTTEMP_SENSE block, perform the following steps:

1. Double click on a blank area in the block design file **alttemp_sense_ex1.bdf**. The Symbol window appears.
2. In the Symbol window, click **MegaWizard Plug-In Manager**. Page 1 of the MegaWizard Plug-In Manager appears.
3. Select **Create a new custom megafunction variation**.
4. Click **Next**. Page 2a of the MegaWizard Plug-In Manager appears.
5. On the MegaWizard Plug-In Manager pages, select or verify the configuration settings shown in Table 2 on page 5. Click **Next** to advance from one page to the next.

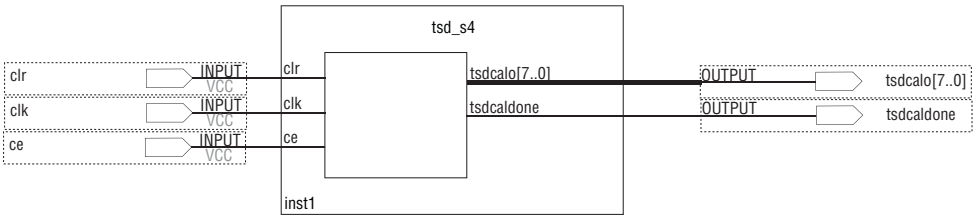
Table 2. Configuration Settings for Design Example

MegaWizard Plug-In Manager Page	MegaWizard Plug-In Manager Configuration Setting	Value
2a	Megafunction	Under I/O category, select **ALTTEMP_SENSE**
	Device family	**Stratix IV**
	Output file type	**Verilog HDL**
	Output file name	tsd_s4
	Return to this page for another create operation	Not selected
3	Currently selected device family	**Stratix IV**
	Match project/default	Selected
	What is the input frequency?	**40** MHz
	What is the clock divider value?	**80**
	Create a clock enable port	Selected
	Create an asynchronous clear port	Selected
4	Generate netlist	Not selected
5	Variation file (**.v**)	Selected
	Quartus II IP file (**.qip**)	Selected
	Quartus II symbol file (**.bsf**)	Selected
	Instantiation template file (**.v**)	Selected
	Verilog HDL block-box file (**.v**)	Selected
	AHDL include file (**.inc**)	Selected
	VHDL component declaration file (**.cmp**)	Selected

6. Click **Finish**. The **tsd_s4** module is generated.
7. Click **OK**.

8. Place the **tsd_s4** symbol in the top-level **alttemp_sense_ex1.bdf** file under the text **INSERT TSD_S4 BLOCK HERE**, aligning the input and output ports with the signals present in the design file. To see a completed design schematic, refer to Figure 2.
9. On the File menu, click **Save**.

Figure 2. Completed Design Schematic



Running Full Compilation

To run a full compilation, perform the following steps:

1. On the Processing menu, click **Start Compilation**.
2. When the **Full Compilation was successful** message box appears, click **OK**.

Locating the TSD Block in the Netlist Viewers

To locate the TSD block in the Netlist Viewers, perform the following steps:

1. After a full compilation, open the **alttemp_sense_ex1.bdf** file.
2. Right-click on the **tsd_s4** instance, select **Locate**, and click **Locate in RTL Viewer** or **Locate in Technology Map Viewer**.
3. The RTL Viewer or the Technology Map Viewer window displays the location of the TSD block in the schematic of the design netlist. The RTL Viewer allows you to view a schematic of the design netlist after the Analysis & Elaboration stage and before the Quartus II synthesis and fitting optimization stage. The Technology Map Viewer allows you to view a low-level, technology-specific schematic of the design netlist after the fitting operation or after the Analysis & Synthesis stage.

Ports and Parameters

This section describes the ports and parameters for the ALTTEMP_SENSE megafunction. These ports and parameters are available to customize the ALTTEMP_SENSE megafunction to meet your requirements.

The parameter details in this section are only relevant if you bypass the MegaWizard Plug-In Manager interface and use the megafunction as a directly parameterized instantiation in your design. The details of these parameters are hidden from the ALTTEMP_SENSE MegaWizard interface.

Table 3 describes the input ports of the ALTTEMP_SENSE megafunction block.

Table 3. ALTTEMP_SENSE Megafunction Ports

Port Name	Type	Condition	Description
clk	Input	Required	Input clock signal with frequency of 1 MHz or 40 MHz. The clock divider reduces the frequency of the clk signal to 1 MHz or less before clocking the ADC.
ce	Input	Optional	The clock enable signal for the clk signal. This signal acts as an ON/OFF switch for the TSD block. This is an active-high signal. By defualt, this signal is connected to VCC.
clr	Input	Optional	The asynchronous clear signal. When the clr signal is asserted, the tsdcalo[7:0] signal is set to 11010101, and the tsdcaldone signal is set to 0. This is an active-high signal. By default, this signal is connected to GND.
tsdcalo[7:0]	Output	Required	8-bit output signal that contains the analog-to-digital-conversion temperature value. The 8-bit value maps to a unique temperature value. Refer to Table 4 for the value mapping. During device power-up or when the clr signal is asserted, the tsdcaldone[7:0] is set to 11010101.
tsdcaldone	Output	Required	Signal to indicate the completion of the temperature sensing process. This signal is asserted when the process is complete. To start a temperature sensing operation, set this signal to 0 by asserting the clr signal.

Table 4 shows the value of tsdcalo[7:0] that corresponds to the Stratix IV device temperature range. The Stratix IV temperature specification ranges from -40°C to 100°C.

Table 4. The Mapping of tsdcalo [7..0] Value to Stratix IV Device Temperature

Value of tsdcalo[7:0] in Hexadecimal	Temperature in Degree Celsius (°C)
58	-40°C
...	...
6C	-20°C
...	...
7F	-1°C
80	0°C
81	1°C
...	...
99	25°C
...	...
B2	50°C
...	...
E4	100°C

Table 5 describes the parameters of the ALTTEMP_SENSE megafunction block.

Table 5. ALTTEMP_SENSE Megafunction Parameters

Parameter	Type	Default	Description
CLK_FREQUENCY	Integer	1	This parameter specifies the frequency of the input clock signal in MHz. The valid values are 1 and 40.
CLOCK_DIVIDER_VALUE	Integer	40	This parameter specifies the value of the clock divider. The valid values are 40 and 80. This parameter can only be used when the CLK_FREQUENCY parameter is set to 40.
DEVICE_FAMILY	String	Stratix IV	This parameter specifies the targeted device family. The valid values are Stratix IV and HardCopy IV.

Document Revision History

Table 6 displays the revision history for this user guide.

Table 6. Document Revision History

Date	Document Version	Changes Made
February 2010	2.0	Updated the Temperature Sensing Operation section
November 2009	1.0	Initial release

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