Nios® II

Nios II Evaluation Kit User Guide

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Contents

About this User Guide

This user guide provides information about how to use the Nios® II Evaluation Kit.

Table 1. User Guide Revision History

Date	Description
October 2005	Updates for the Nios II version 5.1 release.
January 2005	Initial publication.

How to Contact Altera

For the most up-to-date information about Altera products, go to the Altera world-wide web site at **www.altera.com**. For technical support on this product, go to **www.altera.com/mysupport**. For additional information about Altera products, consult the sources shown below.

Information Type	USA & Canada	All Other Locations
Technical support	www.altera.com/mysupport/	www.altera.com/mysupport/
	(800) 800-EPLD (3753) (7:00 a.m. to 5:00 p.m. Pacific Time)	+1 408-544-8767 7:00 a.m. to 5:00 p.m. (GMT -8:00) Pacific Time
Product literature	www.altera.com	www.altera.com
Altera literature services	literature@altera.com	literature@altera.com
Non-technical customer service	(800) 767-3753	+ 1 408-544-7000 7:00 a.m. to 5:00 p.m. (GMT -8:00) Pacific Time
FTP site	ftp.altera.com	ftp.altera.com

Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\QuartusII** directory, **d:** drive, **chiptrip.gdf** file.
Bold italic type	Book titles are shown in bold italic type with initial capital letters. Example: ***1999 Device Data Book***.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75 (High-Speed Board Design)*.
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: <*file name*>, <*project name*>**.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of Quartus II Help topics are shown in quotation marks. Example: "Configuring a FLEX 10K or FLEX 8000 Device with the BitBlaster™ Download Cable."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input`. Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\quartusII\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c.,...	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
	The hand points to information that requires special attention.
	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
	The warning indicates information that should be read prior to starting or continuing the procedure or processes
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

Using the Nios II Evaluation Kit

Introduction

Welcome to the Nios II Evaluation Kit! This kit is a low-cost platform for evaluating the Nios II family of embedded processors. In addition to the Nios II evaluation board, the kit includes all the hardware and software development tools, documentation, and accessories you need to begin developing with the Nios II embedded processor.

This user guide will familiarize you with the contents of the Nios II evaluation kit and walk you through setting up your Nios II development environment. In this guide, you will:

- Install the development tools
- Set up and verify correct operation of the Nios II evaluation board
- Establish communication between the Nios II evaluation board and the host PC
- Compile C code and download the code to the Nios II evaluation board

When you finish this guide, you will be ready to begin designing with the Nios II embedded processor. At your aid are additional tutorials, user guides, and other documentation that go into greater detail regarding the creation and programming of the Nios II processor.

Before You Begin

Before proceeding, check the contents of the kit and verify that you received the following items:

- Nios II evaluation board
- USB cable
- Ethernet cable
- Ethernet-crossover connector
- Altera Design Software Suite
- *Nios II Evaluation Kit User Guide* (this document)

Development Tools

The kit includes the Altera Design Software Suite from Altera. This suite contains the following development tools:

- Nios II Embedded Processor Evaluation Edition
- Quartus II Web Edition Software

See **www.altera.com fo**r the latest releases of the Nios II Evaluation Edition and the Quartus II Web Edition software, both available free for download.

Your PC system must meet the minimum system requirements as described below:

- Pentium II PC running at 400 MHz or faster
- Microsoft Windows 2000, or Windows XP Professional
- Powered USB port for use with the Nios II evaluation board

The Altera Design Software Suite

The Altera Design Software Suite consists of the following CD-ROMs:

- Altera Design Software Suite CD-ROM
- Nios II Embedded Processor Evaluation Edition

The Altera Design Software Suite CD-ROM contains the Q**uartus II Web Edition Software.** The Quartus II software is a comprehensive environment for system-on-a-programmable-chip (SOPC) hardware design. Using the Quartus II software, designers can develop hardware design files, synthesize a netlist for the design, and output a configuration file for the target FPGA. Designers use the Quartus II software to assign I/O pin locations, apply compilation constraints (e.g. timing requirements), and perform timing analysis on the FPGA design. Quartus II software installation also includes the SOPC Builder system-integration tool. Nios II hardware designers use SOPC Builder to define and integrate Nios II processor-based hardware systems.

The Nios II Embedded Processor Evaluation Edition CD-ROM contains the tools listed below along with other components:

- **Nios II IDE** - Provides an integrated environment for editing, compiling, and debugging embedded software.
- **The GNU toolchain** – The GNU toolchain contains the basic tools for source-code compilation such as an assembler, C/C++ compiler, and linker.
- **The Nios II CPU Component for SOPC Builder** – The CPU component provides three processor cores, Nios II/e, Nios II/s, and Nios II/f, for the SOPC Builder hardware component library.

Installing the Development Tools

It is important to install the Altera Design Software Suite development tools in the order listed below. To install the required software, perform the following steps:

1. Insert the Altera Design Software Suite CD.
2. Install the Quartus II Web Edition software. During the installation, you can customize the installation by selecting a destination folder as well as choosing components to install. Altera recommends that you perform a complete installation.

If you choose to install a custom setup, at a minimum, you must install the Quartus II component, the SOPC Builder component, and Cyclone device family support.

3. After successfully completing the installation of the Quartus II Web Edition software, insert the Nios II Embedded Processor Evaluation Edition CD.
4. Install the Nios II Embedded Processor Evaluation Edition software. During the installation, you have the option of installing all or some of the available components. Altera recommends that you perform a complete installation.

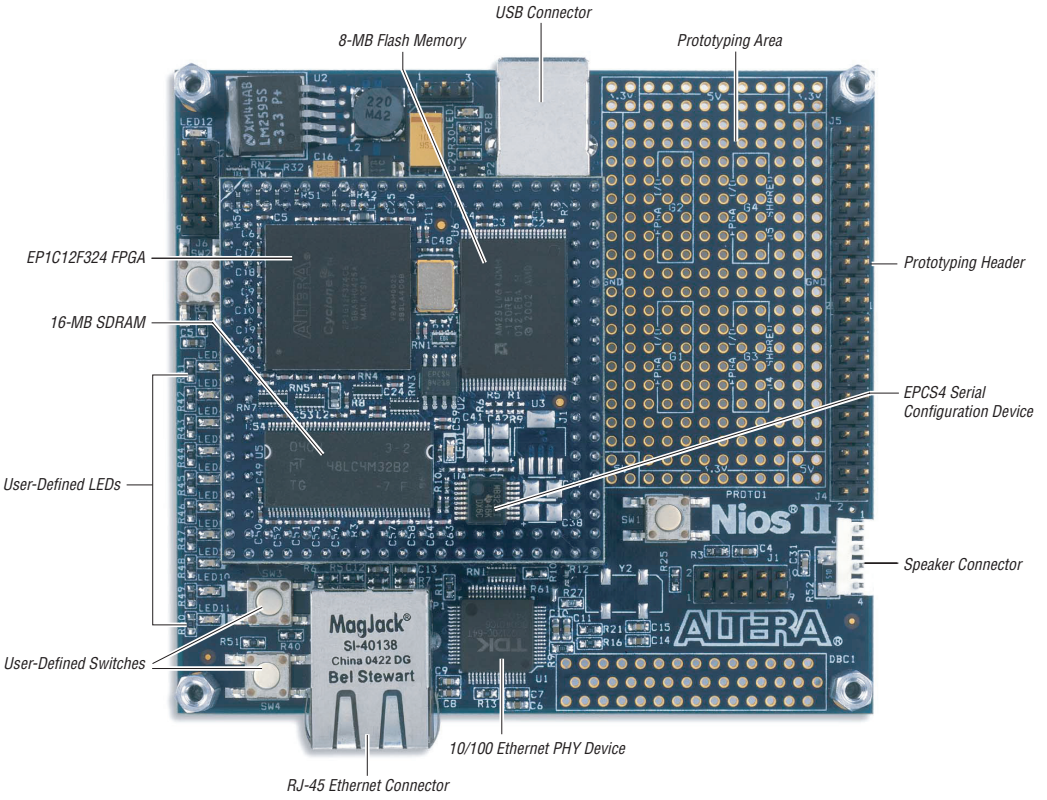
If you need to re-install the Nios II Processor Evaluation Edition, Altera recommends that you first uninstall the previous installation.

The Nios II Evaluation Board

Hardware designers can use the Nios II evaluation board as a platform to prototype complex embedded systems. Software developers can use the Nios II reference design pre-programmed on the evaluation board to begin prototyping software immediately. See "Writing Software for the Nios II Processor" on page 21 for more information.

The evaluation board consists of a base carrier board with a mounted embedded processor module. The evaluation board comes pre-configured with a Nios II processor hardware reference design and a software reference design stored in flash memory. See Figure 1 on page 10 for board component details.

Figure 1. Detailed View of the Nios II Evaluation Board



Setting Up the Nios II Evaluation Board

To set up the Nios II evaluation board, follow these steps:

1. Remove the Nios II evaluation board from its anti-static shipping bag. Take care not to expose the board to electrostatic discharge (ESD) during setup or use.
2. Place the board legs-down on a flat surface.
3. Connect the USB cable between the board and your PC. Your PC will detect new hardware.

4. Follow the on-screen instructions to install the driver for the Nios II evaluation board. You must install the Altera USB-Blaster™ driver to use the board. The driver is located at *<quartus_install_dir>*\drivers\usb-blaster.

For details on installing the USB-Blaster software driver on the host PC, see the *USB Blaster Download Cable User Guide* at **www.altera.com**.

5. Disconnect any other Altera USB download cables, such as the USB-Blaster download cable.

If another Altera USB download cable is connected to your PC while using the evaluation board, you might not be able to download or debug on one or both cables.

Further details on the board, including full schematic and pinout information is available in the directory *<Nios II kit path>*\documents\nios_cyclone_1c12_eval.

Verifying Correct Operation of the Nios II Evaluation Board

Verify the following indicators of a properly functioning Nios II evaluation board:

- The LED labeled "LED1" at the top of the board is lit.
- The LED labeled "LED1" on the embedded processor module is lit.

As soon as you apply power to the Nios II evaluation board, the embedded processor module will be configured with a Nios II processor hardware reference design, stored in the EPCS serial configuration device. Once the embedded processor module configuration is complete, the Nios II processor wakes up and initializes itself with boot code from flash memory.

After the FPGA is configured and the Nios II CPU begins to run, the Linux boot code is copied from flash and starts executing.

If you are not the first user of your Nios II evaluation board, the board may no longer contain the original factory image programmed in flash memory. If you want to restore your board to its factory default condition, see “Instructions for Restoring the Factory Configuration” on page 12.

If this is the first time you are applying power to the Nios II evaluation board and you do not see the indicators above, check all the connections. For further assistance, visit Altera's online technical support web site at **mysupport.altera.com**.

See "Using Nios II Linux" on page 13 for more information about the pre-loaded version of Nios II Linux on your Nios II evaluation board.

You now have successfully set up your evaluation board. You now have the choice to continue to "Using Nios II Linux" on page 13 to learn about the example Linux kernel that is programmed into the flash on your board, or you may skip ahead to "Starting the Nios II Development Tools" on page 16 to begin learning how to develop your own software for the Nios II processor.

Instructions for Restoring the Factory Configuration

The Nios II evaluation board can always be restored to its factory-programmed configuration. To restore the factory configuration, you must reprogram both the Cyclone FPGA on the embedded processor module and the flash memory on the embedded processor module.

To reprogram the embedded processor module, perform the following steps:

1. On the Windows Start menu, click Programs, Altera, Nios II Evaluation Kit <installed version>, **Nios II SDK Shell** to open a Nios II SDK Shell**.**

2. From the **examples** directory, change to the **factory_recovery** directory for your development kit by typing the following at the shell prompt:

   ```
   cd factory_recovery/niosII_cyclone_1c12_eval ↵
   ```

3. Run the flash-restoration script:

   ```
   ./restore_my_flash ↵
   ```

4. Follow the script's instructions.

Using Nios II Linux

This section describes the procedures for establishing a serial connection and logging into Nios II Linux to access sample network applications.

Opening a Terminal Connection to Linux

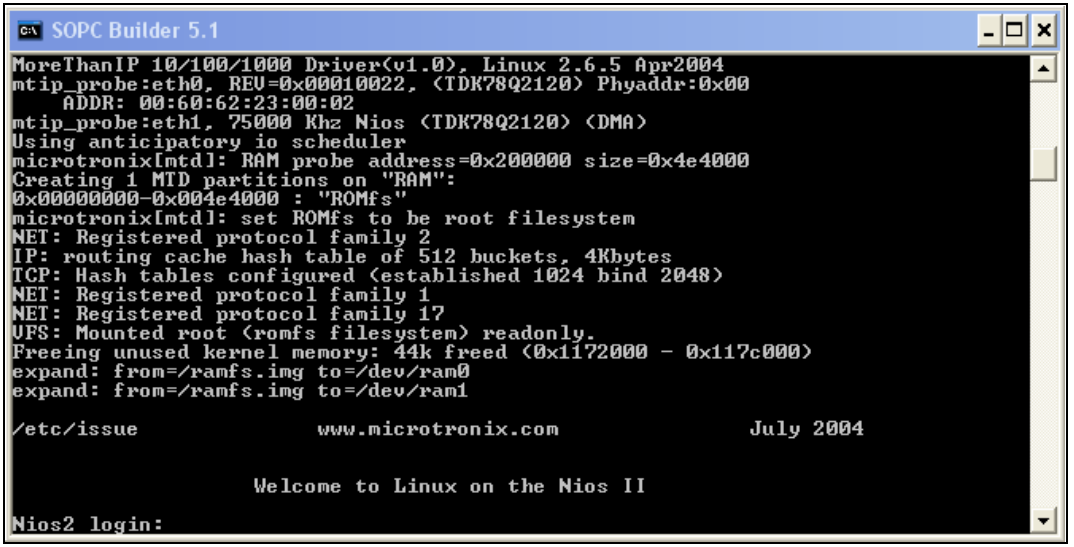
The boot code in flash memory is the µClinux 2.6 kernel. The startup procedure for the kernel will pause until a terminal connection is established between your PC and the board via the USB cable. To watch the kernel complete its startup procedure, perform the following steps:

1. On the Windows Start menu, click Programs, Altera, Nios II Evaluation Kit <*installed version*>, **Nios II SDK Shell** to start the Nios II SDK Shell.

2. At the shell prompt, type `nios2-terminal` ↵

The kernel startup messages will start scrolling, ending with a Nios II Linux login prompt. See Figure 2.

Figure 2. Nios II Linux Login Prompt



Logging into Nios II Linux

At the login prompt, use the following username and password:

Username: `nios`

Password: `uClinux`

After logging in, the Nios II Linux shell prompt (#) appears.

Enabling Network Support

If you wish to enable network support, you can do so manually or using DHCP.

Configuring Network Support Manually

✓ At the Nios II Linux shell prompt, run the following command replacing <*ip address*> and <*netmask*> with valid parameters for your local network.

```
# ifconfig eth0 <ip address> netmask <netmask> ↵
```

Configuring Network Support with DHCP

To configure your IP address with DHCP, perform the following steps:

1. Run the following command:

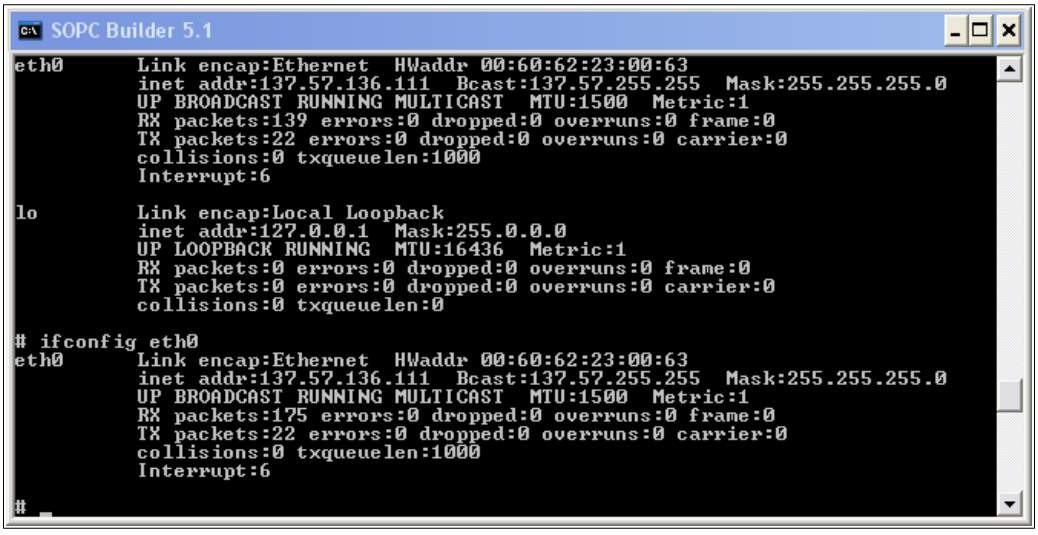
```
# dhcpcd -NRY & ↵
```

2. Wait a few moments, and then run:

```
# ifconfig eth0 ↵
```

The output will be similar to that in Figure 3 on page 15.

Figure 3. Configuring Network Support



If you don't see an `inet addr` entry when running `ifconfig`, wait a few moments and try again. It can take time to retrieve an IP address from a DHCP server.

For more information regarding Nios II Linux, visit **www.niosforum.com** where you will be able to download the latest Nios II Linux distribution for your Nios II evaluation kit.

Using Sample Network Applications

The Nios II evaluation board ships with a web server, telnet server, and an FTP server. Once network support is enabled, all these network services can be accessed through the board's IP address. For example, typing **http://<*IP address*>** into a web browser on your PC will access the web pages served from the Linux web server running on the evaluation board.

Starting the Nios II Development Tools

Once you have connected your Nios II evaluation board to your computer, you can start the Nios II integrated development environment (IDE) from the Quartus II software.

Starting the Quartus II Software

To start the Quartus II software and open a Nios II project, perform the following steps:

1. On the Windows Start menu, click Programs, Altera, **Quartus II** *<version>* **Web Edition Full**.
2. When the Altera Quartus II window displays, on the File menu, click **Open Project...**.
3. Browse to *<Nios II kit path>***\examples\verilog\niosII_cyclone_1c12_eval\standard.**
4. Select the **standard_eval_board.qpf** file and click **Open**.

   The **standard_eval_board.qpf** file contains project definitions for the standard reference design used as the example in this guide.

You can use the VHDL directory in place of the Verilog directory, if you prefer.

Downloading a Hardware Image to the FPGA

You will now configure the Cyclone device on the Nios II evaluation board by downloading a SRAM Object File (**.sof**) image. To download the Nios II **.sof** image to the Nios II evaluation board, perform the following steps:

1. On the Tools menu, click **Programmer**.
2. Click **Hardware Setup**.
3. Double-click **Nios II Evaluation Board** in the **Available hardware items** list.
4. Click **Close.**
5. Turn on the **Program/Configure** check box found on the same line as **standard_eval_board.sof**.
6. Close the Nios II SDK shell if it is still open and connected to Linux.

7. Click **Start**.

You've now reconfigured the Cyclone FPGA on your evaluation board with a new Nios II processor hardware design. Next, you will find out how to run software on this processor.

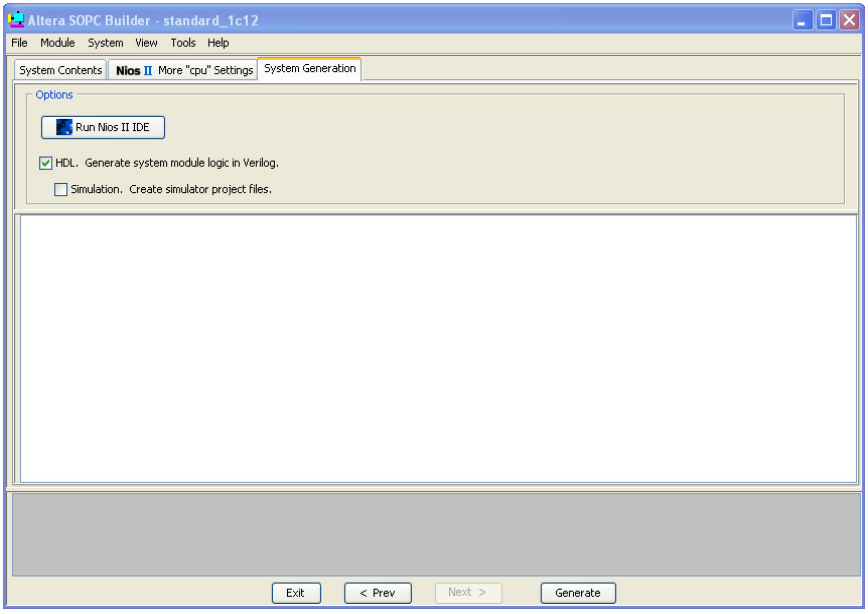
Starting the Nios II IDE from SOPC Builder

Now that you have configured the FPGA with a Nios II system **.sof** file, you can proceed to the Nios II IDE to download software to the processor.

To start the Nios II IDE, perform the following steps:

1. On the Tools menu, click **SOPC Builder**.
2. When SOPC Builder opens, click the **System Generation** tab.
3. Click **Run Nios II IDE** to start the Nios II IDE. See Figure 4.

Figure 4. Starting the Nios II IDE

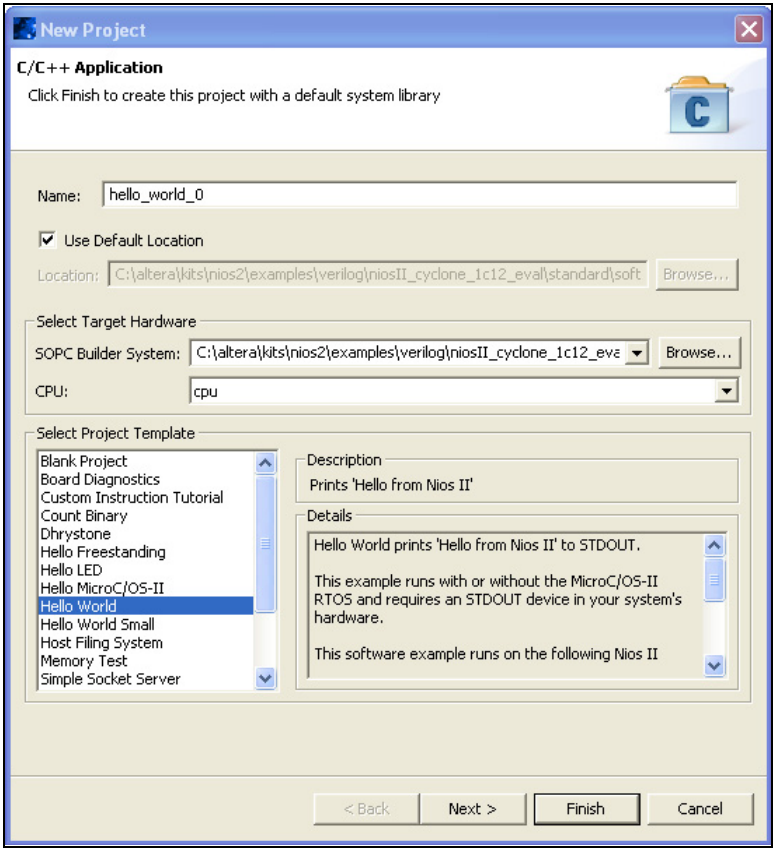


Building Your First Software Project

To create the **Hello World** project, perform the following steps:

1. On the File menu, click New, **C/C++ Application**. The New Project wizard opens. See Figure 5.

Figure 5. Nios II New Project



2. Select **Hello World** from the **Select Project Template** list.

3. Click **Finish** to create the **hello_world_0** project and associated system library project.

4. In the C/C++ Projects view on the left, right-click **hello_world_0** and select **Build Project**.

   When the build is done, the message "Build completed" displays in the Console view at the bottom of the Nios II IDE window.

If the Console view is not visible, click on the **Console** tab to display the view.

Downloading Executable Code to the Nios II Evaluation Board

From the Nios II IDE, perform the following:

1. On the Run menu, click **Run...** . The Run dialog box opens.

1. Select **Nios II Hardware** in the Configurations pane and click **New.**

2. Click the **Target Connection** tab.

3. Select **Nios II Evaluation Board** from the **JTAG cable** list.

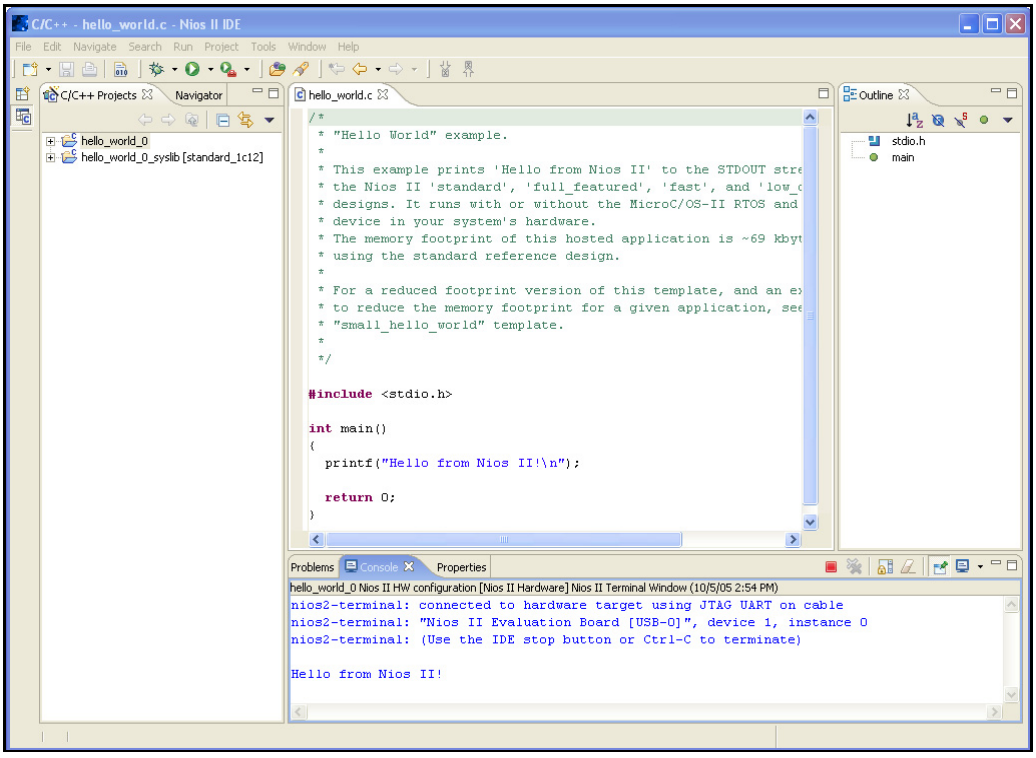
   Wait while the Nios II IDE sets up the run configuration. The Run button becomes active when this process is complete.

4. Click **Run** at the bottom of the dialog box. The **hello_world** image downloads to the Nios II evaluation board and executes.

   The results appear in the Console view of the Nios II IDE. See Figure 6 on page 20.

If the Console view is not visible, click on the **Console** tab to display the view.

Figure 6. Console View



Taking the Next Step

Congratulations! You have completed the first steps to familiarize yourself with the Nios II Evaluation Kit. If you completed all of the steps in this user guide, then you have installed your Nios II processor development environment, and verified that the Nios II evaluation board and tools function correctly.

Writing Software for the Nios II Processor

The *Nios II Software Development Tutorial*, available within the Nios II IDE, is a good place to begin learning more about writing software for the Nios II processor. This document will introduce you to the software development process for the Nios II processor, presented in a step-by-step format.

The Nios II evaluation kit includes a set of example hardware designs. The Nios II IDE includes several templates for software example designs. Table 2 shows which software example are compatible with the hardware designs in the Nios II evaluation kit.

Table 2. Compatibility of Example Software and Hardware Designs

Software Template	Hardware Design		
	Small	Standard	Full Featured
Blank Project	O	O	O
Board Diagnostics			
Custom Instruction Tutorial			
Count Binary			
Dhrystone		O	O
Hello Freestanding		O	O
Hello LED	O	O	O
Hello MicroC/OS-II			
Hello World		O	O
Hello World Small		O	O
Host Filing System		O	O
Memory Test		O	O
Simple Socket Server			
Tightly Coupled Memory			
MicroC/OS-II Message Box			
MicroC/OS-II Tutorial			
Web Server			
Zip Filing System		O	O

Creating Customized Processor Systems

Hardware and system designers can create their own customized systems using SOPC Builder and the Quartus II software. The best place to learn more about this powerful capability is by purchasing one of the following full-featured Nios II development kits:

- Nios II Development Kit, Stratix II Edition
- Nios II Development Kit, Stratix Edition
- Nios II Development Kit, Stratix Professional Edition
- Nios II Development Kit, Cyclone II Edition
- Nios II Development Kit, Cyclone Edition

These kits contain extensive reference designs, documentation, and step-by-step tutorials that will aid you in creating embedded processor subsystems just the way you require.

A 10/100 Ethernet MAC from MoreThanIP GmbH is included in the factory programmed design on the embedded processor module. If you want to generate hardware systems using this MAC, contact MoreThanIP at **www.morethanip.com**.

Learning More about the Nios II Processor

The Altera website (**www.altera.com/nios2**) provides you with the latest information on the Nios II family of embedded processors.

The Nios Forum (**www.niosforum.com**) is a user driven, web-enabled forum dedicated to designing with the Nios II processor. Users exchange information, designs, and development techniques for maximizing their experience with the Nios II processor.

Both the µClinux and eCos operating systems are available free for download from the Nios Forum.