PowerPlay Early Power Estimator User Guide

For Stratix II, Stratix II GX, & HardCopy II

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
www.altera.com

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Altera Corporation

PowerPlay Early Power Estimator For Stratix II, Stratix II GX & HardCopy II

Contents

About this User Guide

Revision History

The table below displays the revision history for the chapters in this User Guide.

Date & Document Version	Changes Made	Summary of Changes
January 2007 v1.2	Updated to match PowerPlay Early Power Estimator v6.1 including: • Cover title changed • Table 1–1 updated • Chapter 2 "System Requirements" section updated • Minor edits to page 2–2 through page 2–7, page 3–33, page 3–39, page 3–43. • Table 2–1 updated • Table 2–2 updated • Table 3–1 updated • Table 3–14 updated • Figure 3–1 updated • Figure 3–24 updated	—
May 2006 v1.1	Updated cross references to match the new chapter titles for the Quartus II 6.0 Handbook.	—
December 2005 v1.0	First publication to include Stratix II, Stratix II GX, and HardCopy II support.	—

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Typographic Conventions

This document uses the typographic conventions shown below.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: **Save As** dialog box.
bold type	External timing parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: $\mathbf{f_{MAX}}$, **\qdesigns** directory, **d:** drive, **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Document titles are shown in italic type with initial capital letters. Example: *AN 75: High-Speed Board Design.*
Italic type	Internal timing parameters and variables are shown in italic type. Examples: t_{PIA}, $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: *<file name>*, *<project name>***.pof** file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
`Courier type`	Signal and port names are shown in lowercase Courier type. Examples: `data1`, `tdi`, `input.` Active-low signals are denoted by suffix `n`, e.g., `resetn`. Anything that must be typed exactly as it appears is shown in Courier type. For example: `c:\qdesigns\tutorial\chiptrip.gdf`. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword `SUBDESIGN`), as well as logic function names (e.g., `TRI`) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ● •	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
☞	The hand points to information that requires special attention.

Visual Cue	Meaning
	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
	The warning indicates information that should be read prior to starting or continuing the procedure or processes
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.

Chapter 1. About the PowerPlay Early Power Estimator

Release Information

Table 1–1 provides information on the version of the PowerPlay Early Power Estimator spreadsheet documented in this user guide.

Table 1–1. PowerPlay Early Power Estimator Spreadsheet Versions

Device Family	PowerPlay Early Power Estimator Spreadsheet Version
Stratix® II	6.1 and later
Stratix II GX	6.1 and later
HardCopy® II	6.1 and later

Device Family Support

The PowerPlay Early Power Estimator spreadsheet provides full support for the target Altera device families listed in Table 1–2.

Table 1–2. Device Family Support

Device Family	Support
Stratix II	Full
Stratix II GX	Full
HardCopy II	Partial

General Description

Printed circuit board (PCB) designers need an accurate estimate of the amount of power the device consumes to develop an appropriate power budget, design the power supplies, voltage regulators, heat sink and cooling system. You can calculate a device's power using the Microsoft Excel-based PowerPlay Early Power Estimator spreadsheet available from the Altera web site or the PowerPlay power analyzer in the Quartus® II software. You need to enter the device resources, operating frequency, toggle rates, and other parameters in the PowerPlay early power estimator.

This user guide explains how to use the PowerPlay Early Power Estimator spreadsheet to estimate device power consumption.

These calculations should only be used as an estimation of power, not as a specification. Be sure to verify the actual power during device operation, as the information is sensitive to the actual device design and the environmental operating conditions.

For more information about available device resources, I/O standard support, and other device features, refer to the appropriate device family handbook.

Features

The features of the PowerPlay Early Power Estimator spreadsheet include:

- Estimate your design's power usage before creating the design, during the design process, or after the design is complete
- Import device resource information from the Quartus II software into the PowerPlay Early Power Estimator spreadsheet with the use of the Quartus II-generated PowerPlay Early Power Estimator file
- Perform preliminary thermal analysis of your design

Chapter 2. Setting Up PowerPlay Early Power Estimator

System Requirements

The PowerPlay Early Power Estimator spreadsheet requires:

- A PC running the Windows NT/2000/XP operating system
- Microsoft Excel 2002 or higher
- Quartus II software version 6.1 or higher if generating a file for import

Download & Install the PowerPlay Early Power Estimator

The PowerPlay Early Power Estimator spreadsheet for Altera devices is available from the Altera website (**www.altera.com**). After reading the terms and conditions and clicking **I Agree**, you can download the Microsoft Excel file to your hard drive.

By default, the Microsoft Excel 2002 macro security level is set to **High**. When the macro security level is set to **High**, macros are automatically disabled. To change the macro security level in Microsoft Excel 2002, click **Options** on the Tools menu. On the **Security** tab of the **Options** window, click **Macro Security**. On the **Security Level** tab of the **Security** dialog box, chose **Medium**. When the macro security level is set to **Medium**, a pop-up window asks you whether to enable macros or disable macros each time you open a spreadsheet that contains macros. After changing the macro security level, you have to close the spreadsheet and re-open it in order to use the macros.

Estimating Power

You can estimate power at any point in your design cycle. You can use the PowerPlay Early Power Estimator spreadsheet to estimate the power consumption if you have not begun your design, or if your design is not complete. While the PowerPlay Early Power Estimator spreadsheet can provide you with an estimate for your complete design, it is highly recommended to use the PowerPlay Power Analyzer in the Quartus II software to obtain this estimate. In general, using the PowerPlay Power Analyzer in the Quartus II software should be your preferred method of generating power estimates due to the fact that it knows your exact routing and various modes of operation.

For more information on the power estimation feature in Quartus II software, refer to the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

To use the PowerPlay Early Power Estimator, enter the device resources, operating frequency, toggle rates and other parameters in the PowerPlay Early Power Estimator. If you do not have an existing design, then you need to estimate the number of device resources your design uses in order to enter the information into the PowerPlay Early Power Estimator.

Estimating Power Before Starting the FPGA Design

FPGAs provide the convenience of a shorter design cycle and faster time-to-market than ASICs or ASSPs. This means that the board design often takes places during the FPGA design cycle, and the power planning for the device can happen before any of the FPGA design is complete.

Table 2–1 shows the advantages and disadvantages of using the PowerPlay Early Power Estimator spreadsheet before you begin the FPGA design.

Table 2–1. Power Estimation Before Designing FPGA

Advantages	Disadvantages
• Power estimation can be performed before starting your FPGA design	• Accuracy depends on your inputs and your estimation of the device resources; where this information may change (during or after your design is complete), your power estimation results may be less accurate • Process can be time consuming

To estimate power usage with the PowerPlay Early Power Estimator spreadsheet if you have not started your FPGA design, perform the following steps:

1. Download the PowerPlay Early Power Estimator spreadsheet from the Altera website (**www.altera.com**).
2. Select the target family, device, and package from the PowerPlay Early Power Estimator's **Family**, **Device**, and **Package** sections.
3. Enter values for each section in the PowerPlay Early Power Estimator. Different worksheets in the file display different power sections, such as clocks and PLLs. Power is calculated automatically, and subtotals are given for each section.
4. The calculator displays the estimated power usage in the **Total** section.

Estimating Power While Creating the FPGA Design

When the FPGA design is partially complete, you can use the PowerPlay Early Power Estimator file (<*revision name*>**_early_pwr.csv**) generated by the Quartus II software to supply information to the PowerPlay early power estimator. After importing the power estimation file information into the PowerPlay early power estimator, you can edit the PowerPlay Early Power Estimator spreadsheet to reflect the device resource estimates for the final design.

For more information on generating the power estimation file in the Quartus II software, refer to the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Table 2–2 shows the advantages and disadvantages when using the PowerPlay Early Power Estimator spreadsheet for an FPGA design that is partially complete.

Table 2–2. Power Estimation When FPGA Design Is Partially Complete

Advantages	Disadvantages
• Power estimation can be done early in the FPGA design cycle • Provides the flexibility to automatically fill in the PowerPlay Early Power Estimator spreadsheet based on Quartus II software compilation results	• Accuracy depends on your inputs and your estimation of the device resources; where this information may change (during or after your design is complete), your power estimation results may be less accurate.

Use the following steps to estimate power usage with the PowerPlay Early Power Estimator spreadsheet if your FPGA design is partially complete.

1. Compile the partial FPGA design in the Quartus II software.
2. Generate the PowerPlay Early Power Estimator file (<*revision name*>**_early_pwr.csv**) in the Quartus II software by clicking **Generate PowerPlay Early Power Estimator File** on the Project menu.
3. Download the PowerPlay Early Power Estimator spreadsheet from the Altera website (**www.altera.com**).
4. Import the PowerPlay Early Power Estimator file into the PowerPlay Early Power Estimator spreadsheet to automatically populate the PowerPlay Early Power Estimator spreadsheet entries.

5. After importing the file to populate the PowerPlay early power estimator, you can manually edit the cells to reflect final device resource estimates.

Estimating Power After Completing the FPGA Design

When you complete your FPGA design, the PowerPlay Power Analyzer in the Quartus II software provides the most accurate estimate of device power consumption. The PowerPlay Power Analyzer uses simulation, user mode and default toggle rate assignments, in addition to place-and-route information to determine power consumption. Altera strongly recommends that you use the PowerPlay Power Analyzer when your FPGA design is complete.

For more information about how to use the PowerPlay Power Analyzer in the Quartus II software, refer to the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Entering Information into the PowerPlay Early Power Estimator

You can either manually enter power information into the PowerPlay Early Power Estimator spreadsheet or load a PowerPlay Early Power Estimator file generated by the Quartus II software version 6.1. You can also clear all the values currently in the PowerPlay Early Power Estimator.

Clearing All Values

All user entered values can be reset in the PowerPlay Early Power Estimator spreadsheet by clicking **Reset**.

In order to use the Reset feature, you must enable macros for the spreadsheet. If you have not enabled macros for the spreadsheet, you need to reset all user-entered values manually.

Manually Entering Information

You can manually enter values into the PowerPlay Early Power Estimator spreadsheet in the appropriate section. White, unshaded cells are input cells and may be modified. Each section contains a column that allows you to specify a module name based on your design.

Importing a File

If you already have an existing design or a partially completed design, the power estimation report file generated by the Quartus II software contains the device resource information. You can import this device resource information from the Quartus II software PowerPlay Early

Power Estimator file into the PowerPlay Early Power Estimator. Importing a file saves you time and effort otherwise spent manually entering information into the PowerPlay Early Power Estimator. You can also manually change any of the values after importing a file.

To generate the PowerPlay Early Power Estimator file, you must first compile your design in the Quartus II software. After compiling the design, click **Generate PowerPlay Early Power Estimator File** on the Project menu. The Quartus II software creates a PowerPlay Early Power Estimator file with the name <*revision name*>**_early_pwr.csv**.

The Quartus II software cannot generate a PowerPlay Early Power Estimator file directly from a HardCopy II design. Instead, generate the PowerPlay Early Power Estimator file for the Stratix II companion revision for the project. The PowerPlay Early Power Estimator spreadsheet generates both Stratix II and HardCopy II power estimates from the Stratix II PowerPlay Early Power Estimator file.

For more information on generating the PowerPlay Early Power Estimator file in the Quartus II software, refer to the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

To import data into the PowerPlay Early Power Estimator, perform the following steps:

1. Click **Import Quartus II File** in the PowerPlay Early Power Estimator.
2. Browse to a power estimation file generated from the Quartus II software and click **Open**. The file has a name <*revision name*>**_early_pwr.csv**.
3. Click **OK** in the confirmation window to proceed.
4. When the file is imported, click **OK**. Clicking OK acknowledges the import is complete. If there are any errors during the import, an **.err** file is generated with details.

After importing a file, you must verify all your information.

Importing a file from the Quartus II software populates all input parameters on the main page that were specified in the Quartus II software. These parameters include:

- Family
- Device
- Package
- Temperature grade
- Power characteristics
- Ambient or junction temperature
- Airflow
- Heat sink
- Custom θ_{SA} or custom θ_{JA}
- Board thermal model
- Custom θ_{JB}
- Board temp T_B

The ambient or junction temperature, airflow, heat sink, custom θ_{SA} or custom θ_{JA}, board thermal model, custom θ_{JB}, and board temperature T_B parameters are optional. See "Main Input Parameters" on page 3–1 for more information on these parameters.

The f_{MAX} values imported into the PowerPlay Early Power Estimator spreadsheet are the same as the f_{MAX} values specified by the designer in the Quartus II software. You can manually edit the f_{MAX} and the toggle percentage in the PowerPlay Early Power Estimator spreadsheet to suit your system requirements.

Importing Information from PowerPlay Early Power Estimator v6.0

If you already have an existing version 6.0 PowerPlay Early Power Estimator file, you can import the data directly into version 6.1 of the PowerPlay Early Power Estimator spreadsheet using the Import Legacy feature. This can save time and effort otherwise spent manually entering information into the PowerPlay Early Power Estimator.

To import data from legacy versions of the PowerPlay Early Power Estimator, perform the following steps:

1. Click the **Import EPE v6.0** button.
2. Browse to the EPE and click Open.
3. Click **OK**. Clicking **OK** acknowledges that the import is complete.

Clicking **OK** clears any user-entered values and populates the PowerPlay Early Power Estimator spreadsheet with device resource information from the specified PowerPlay Early Power Estimator spreadsheet legacy version file.

After importing PowerPlay Early Power Estimator spreadsheets, you must manually ensure that all the information is correct.

Chapter 3. Using the PowerPlay Early Power Estimator

Introduction

The PowerPlay Early Power Estimator spreadsheet provides the ability to enter information into sections based on architectural features. The PowerPlay Early Power Estimator spreadsheet also provides a subtotal of power consumed by each architectural feature and is reported in each section in watts (W).

PowerPlay Early Power Estimator Inputs

The following sections of the user guide explain what values you need to enter for each section of the PowerPlay Early Power Estimator. The different Excel worksheets of the PowerPlay Early Power Estimator spreadsheet are referred to as sections. Sections in the PowerPlay Early Power Estimator spreadsheet calculate power representing architectural features of the device, such as clocks, RAM blocks, or DSP blocks.

Main Input Parameters

Different devices consume different amounts of power for the same design. The larger the device, the more power it consumes because of the larger die and longer interconnects in the device.

In the **Main** section, you may enter the following parameters for the device and design:

- Family
- Device
- Package
- Temperature grade
- Power characteristics
- Ambient or junction temperature
- Airflow
- Heat sink used
- Custom heat sink information
- Board thermal model
- Custom board thermal model information
- Board temperature

Parameters required depend on whether junction temperature is entered manually or auto-computed.

Table 3–1 describes the values that need to be specified in the **Main** section of the PowerPlay Early Power Estimator.

Table 3–1. Main Section Information (Part 1 of 3)

Input Parameter	Description
Family	Select the device family. The families supported are Stratix II, Stratix II GX, and HardCopy II.
Device	Select your device. Larger devices consume more static power and have higher clock dynamic power. All other power components are unaffected by device.
Package	Select the package that is used. Larger packages provide a larger cooling surface and more contact points to the circuit board, leading to lower thermal resistance. Package selection does not affect dynamic power.
Temperature Grade	Commercial devices have a maximum operating temperature of 85 °C. Industrial devices offer 100 °C operation. Military devices offer 125 °C operation. This field only affects maximum junction temperature. Currently, only Stratix II supports the military temperature range.
Power Characteristics	Select typical or theoretical worst-case silicon process. There is process variation from die-to-die. This primarily impacts the static power consumption. **Maximum** is used for thermal design, while **Typical** provides results that line up with average device measurements. Currently, only **Typical** power characteristics are available for the HardCopy II family.
Junction Temp, T_J (ºC)	Enter the junction temperature of the device. This value can range from –55 °C to 125 °C. This field is only available when **User Entered T_J** is selected. In this case, junction temperature is not calculated based on the thermal information provided.
Ambient Temp, T_A (°C)	Enter the air temperature near the device. This value can range from –55 °C to 125 °C. This field is only available when **Auto Computed T_J** is selected. If **Estimated** θ_{JA} is selected, this field is used to compute junction temperature based on power dissipation and thermal resistances through the top-side cooling solution (heat sink or none) and board (if applicable). If **Custom** θ_{JA} is selected, this field is used to compute junction temperature based on power dissipation and the custom θ_{JA} entered.

Table 3–1. Main Section Information (Part 2 of 3)

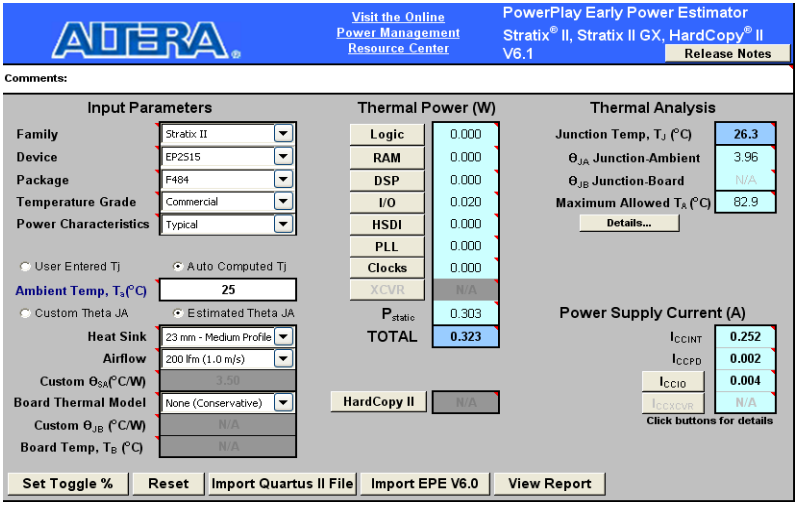
Input Parameter	Description
Heat Sink	Select the heat sink being used. You can specify no heat sink, a custom solution, or specify a heat sink with set parameters. This field is only available when you select **Auto Compute T_J** and **Estimated θ_{JA}**. Representative examples of heat sinks are provided: larger heat sinks provide lower thermal resistance, and thus lower junction temperature. If the heat sink is known, consult the datasheet and enter a Custom heatsink-to-ambient value according to the airflow in your system. The heat sink selection updates θ_{SA} and the value is seen in the Custom θ_{SA} (°C/W) parameter. If a custom solution is selected, the value is what is entered for Custom θ_{SA} (°C/W).
Airflow	Select an available ambient airflow in linear-feet per minute (lfm) or meters per second (m/s). The options are 100 lfm (0.5 m/s), 200 lfm (1.0 m/s), 400 lfm (2.0 m/s), or still air. This field is only available when you select **Auto Computed T_J** and **Estimated θ_{JA}**. Increased airflow results in a lower case-to-air thermal resistance, and thus lower junction temperature.
Custom θ_{JA} (°C/W)	Enter the junction-to-ambient thermal resistance between the device and ambient air (in °C/W). This field is only available when you select **Auto Computed T_J** and **Custom θ_{JA}** This field represents the increase between ambient temperature and junction temperature for every Watt of additional power dissipation.
Custom θ_{SA} (°C/W)	Enter the heatsink-to-ambient thermal resistance from the heat sink data sheet if you select a custom heat sink. The quoted values depend on system airflow and may also depend on thermal power dissipation. This field is only available when you select **Auto Computed T_J**, **Estimated θ_{JA}**, and if you set the Heat Sink parameter to **Custom Solution**. The Custom θ_{SA} parameter is combined with a representative case-to-heatsink resistance and an Altera-provided junction-to-case resistance to compute overall junction-to-ambient resistance through the top of the device.

Table 3–1. Main Section Information (Part 3 of 3)

Input Parameter	Description
Board Thermal Model	Select the type of board to be used in thermal analysis. If no heat sink has been selected, the Altera-provided θ_{JA} value includes the board thermal pathway. If a board thermal model is selected, you must enter a board temperature in the **Board Temp** field. This field is only available when you select **Auto Computed T_J** and **Estimated θ_{JA}**. Board thermal resistance is a function of device package, number of signal and power layers, % metallization at each layer, inter-layer thickness, and many other parameters. θ_{JB} values for a typical customer board stack (based on selected device and package) are provided for estimation purposes. Users should perform a detailed thermal simulation of their system to determine final junction temperature. This two-resistor thermal model is for early estimation only.
Custom θ_{JB} (°C/W)	Enter the junction-to-board thermal resistance obtained from thermal simulation if **Custom** is selected under Board Thermal Model. This field is only available when you select **Auto Computed T_J** and **Estimated θ_{JA}**.
Board Temp, T_B (°C)	Enter the temperature on the PCB at the back-side of the device. This temperature is combined with the θ_{JB} value of the board to compute the junction temperature for the FPGA. This field is only available when you select **Auto Computed T_J** and **Estimated θ_{JA}**. If the entered board temperature is less than ambient, the tool assumes ambient temperature in its thermal analysis since it is not possible for the board to be below ambient. Similarly, board temperatures in excess of the computed junction temperature are capped to the junction temperature.

Figure 3–1 shows the **Main** section of the PowerPlay Early Power Estimator.

Figure 3–1. PowerPlay Early Power Estimator Spreadsheet Main Section



Logic

A design is a combination of several design modules operating at different frequencies and toggle rates. Each design module can have a different amount of logic. For the most accurate power estimation, partition the design into different design modules. You can partition your design by grouping modules by clock frequency, location, hierarchy, or entities.

Each row in the **Logic** section represents a separate design module. You must enter the following parameters for each design module

- Clock frequency (f_{MAX}) in MHz
- Number of combinational adaptive look-up tables (ALUTs)
- Number of registers
- Toggle percentage

Table 3–2 describes the values that need to be entered in the **Logic** section of the PowerPlay Early Power Estimator.

Table 3–2. Logic Section Information (Part 1 of 2)

Column Heading	Description
Module	Enter a name for each module of the design.
Clock Freq (MHz)	Enter a clock frequency (in MHz). This value must be in the range of 0 to 550 MHz. 100 MHz with a 12.5% toggle means that each LUT or flip flop output toggles 12.5 million times per second (100 × 12.5%).
Combinational ALUTs (#)	Enter the number of combinational ALUTs. For Stratix II and Stratix II GX this is the sum of “combinational with no register”, “combinational with register”, and “unavailable” ALUTs from the Quartus II Compilation Report Resource Usage Summary section. For the number of Adaptive LUTs used, add the values from the following rows in the Fitter Resource Usage Summary: ● -- 7 input functions ● -- 6 input functions ● -- 5 input functions ● -- 4 input functions ● -- 3 input functions ● -- Combinational cells for routing Each Stratix II and Stratix II GX Adaptive Logic Module (ALM) contains up to two combinational ALUTs. Smaller ALUTs consume less power than larger ALUTs, but the device can fit more of them. The total number of ALUTs in the design should not exceed (number of ALMs) × 2. For HardCopy II, the number of ALUTs is estimated based on the number of HCELLs and HCELL Macros used in the design. Generally, the number of ALUTs of the HardCopy II should be comparable to the number of ALUTs for the equivalent Stratix II design.
# FFs	Enter the number of flip flops in the module. For all devices this is the sum of “register only” and “combinational with a register” ALUTs from the Quartus II Compilation Report Resource Usage Summary. For HardCopy II, the number of flip flops is determined from the Stratix II fit report. Clock routing power is calculated separately on the Clocks sheet

Table 3–2. Logic Section Information (Part 2 of 2)

Column Heading	Description
Toggle %	Enter the average percentage of logic toggling on each clock cycle. The toggle percentage ranges from 0 to 100%. Typically, the toggle percentage is 12.5%, which is the toggle percentage of a 16-bit counter. To ensure you do not underestimate the toggle percentage, you can use a higher toggle percentage. Most logic only toggles infrequently, and hence toggle rates of less than 50% are more realistic. For example, a TFF with its input tied to V_{CC} has a toggle rate of 100% because its output is changing logic states on every clock cycle (Figure 3–2). Figure 3–3 shows an example of a 4-bit counter. The first TFF with least significant bit (LSB) output `cout0` has a toggle rate of 100% because the signal toggles on every clock cycle. The toggle rate for the second TFF with output `cout1` is 50% since the signal only toggles on every two clock cycles. Consequently, the toggle rate for the third TFF with output `cout2` and fourth TFF with output `cout3` are 25% and 12.5%, respectively. Therefore, the average toggle percentage for this 4-bit counter is (100 + 50 + 25 + 12.5)/4 = 46.875%.
Routing	This shows the power dissipation due to estimated routing (in W). Routing power is highly dependent on placement and routing, which is itself a function of design complexity. The values shown are representative of routing power based on experimentation on over 100 designs. Use the Quartus II PowerPlay Power Analyzer for detailed analysis based on the routing used in your design.
Block	This shows the power dissipation due to internal toggling of the ALMs (in W). Logic block power is a function of the function implemented and relative toggle rates of the various inputs. The PowerPlay Early Power Estimator spreadsheet uses an estimate based on observed behavior across over 100 real-world designs. Use the Quartus II PowerPlay Power Analyzer for accurate analysis based on the exact synthesis of your design.
Total	This shows the total power dissipation (in W). The total power dissipation is the sum of the routing and block power.
User Comments	Enter any comments. This is an optional entry.

Figure 3–2 shows a TFF example.

Figure 3–2. TFF Example

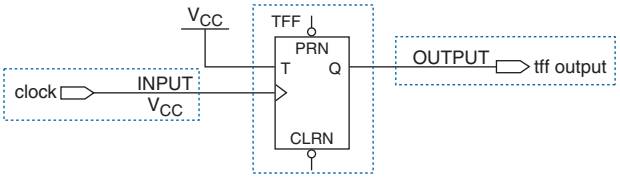


Figure 3–3 shows a 4-Bit Counter example.

Figure 3–3. 4-Bit Counter Example

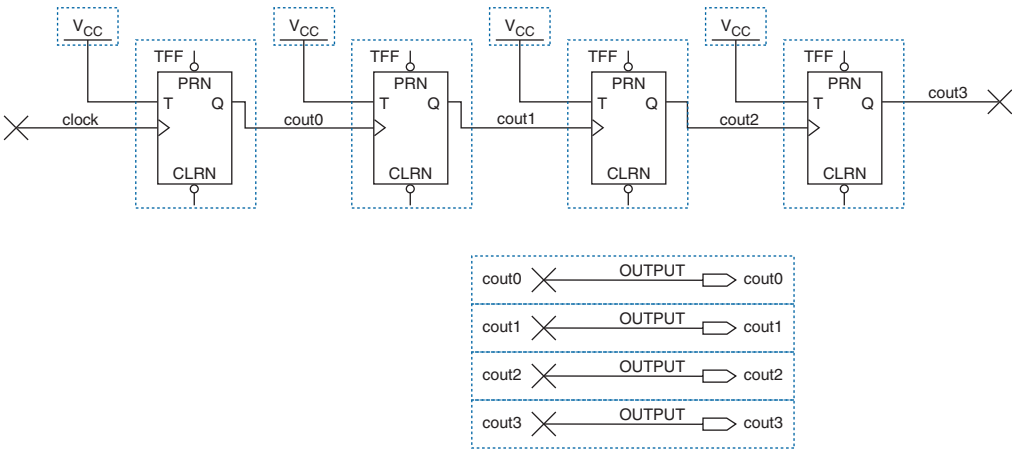


Figure 3–4 shows the Resource Usage Summary in the Quartus II software Compilation Report for a design targeting the Stratix II device family. The Compilation Report provides the total number of ALUTs and registers used by the design.

Figure 3–4. ALUT Usage in Resource Usage Summary

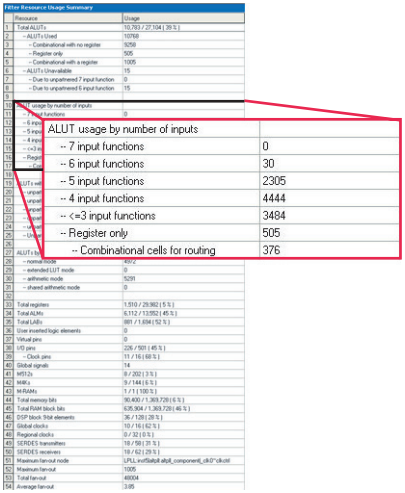
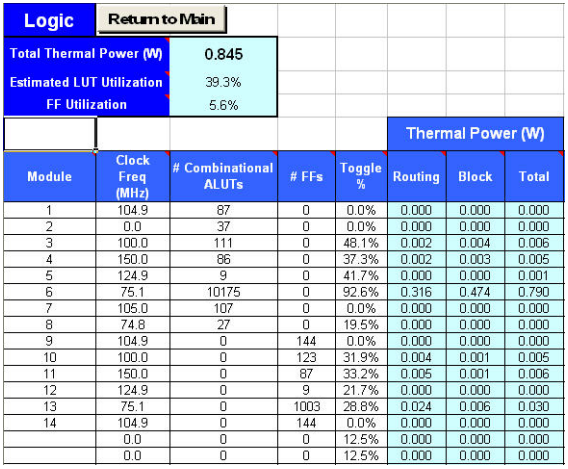


Figure 3–5 shows the device PowerPlay Early Power Estimator spreadsheet and the estimated power consumed by the logic in this design.

Figure 3–5. Logic Section in the PowerPlay Early Power Estimator



Logic | Return to Main

Total Thermal Power (W)	0.845
Estimated LUT Utilization	39.3%
FF Utilization	5.6%

					Thermal Power (W)		
Module	Clock Freq (MHz)	# Combinational ALUTs	# FFs	Toggle %	Routing	Block	Total
1	104.9	87	0	0.0%	0.000	0.000	0.000
2	0.0	37	0	0.0%	0.000	0.000	0.000
3	100.0	111	0	48.1%	0.002	0.004	0.006
4	150.0	86	0	37.3%	0.002	0.003	0.005
5	124.9	9	0	41.7%	0.000	0.000	0.001
6	75.1	10175	0	92.6%	0.316	0.474	0.790
7	105.0	107	0	0.0%	0.000	0.000	0.000
8	74.8	27	0	19.5%	0.000	0.000	0.000
9	104.9	0	144	0.0%	0.000	0.000	0.000
10	100.0	0	123	31.9%	0.004	0.001	0.005
11	150.0	0	87	33.2%	0.005	0.001	0.006
12	124.9	0	9	21.7%	0.000	0.000	0.000
13	75.1	0	1003	28.8%	0.024	0.006	0.030
14	104.9	0	144	0.0%	0.000	0.000	0.000
	0.0	0	0	12.5%	0.000	0.000	0.000
	0.0	0	0	12.5%	0.000	0.000	0.000

RAM Blocks

Stratix II and Stratix II GX device TriMatrix™ memory consists of three types of RAM blocks: M512, M4K, and M-RAM blocks. The power consumption for each type of RAM block is different and must be specified in the **RAM** section of the PowerPlay Early Power Estimator.

HardCopy II devices contain two types of RAM blocks: M4K and M-RAM.

Each row in the **RAM** section represents a design module where the RAM block(s) are the same type, have the same data width, RAM mode, and the same port parameters. If some or all of the RAM blocks in your design have different configurations, enter the information in different rows. For each design module, you need to enter the type of RAM being implemented, the number of RAM blocks, and the RAM block mode. You must also enter the following parameters for each port:

- Clock frequency (in MHz)
- The percentage of time the RAM clock is enabled
- The percentage of time the port is writing compared to reading

When selecting the RAM block mode, you must know how your RAM is implemented by the Quartus II Compiler. For example, if a ROM is implemented with two ports, it is considered a true dual-port memory and not a ROM. Single-port and ROM implementations only use port A. Simple dual-port and true dual-port implementations use port A and port B.

Table 3–3 describes the parameters in the **RAM** section of the PowerPlay Early Power Estimator.

Table 3–3. RAM Section Information (Part 1 of 3)

Column Heading	Description
Module	Enter a name for the RAM module in this column. This is an optional value.
RAM Type	Select whether the RAM is implemented as an M512, M4K or M-RAM block. The RAM type can be found in the Type column of the Quartus II Compilation Report. In the **Compilation Report**, select **Fitter**, and click **Resource Section**. Click **RAM Summary**.
# RAM Blocks	Enter the number of RAM blocks in the module that use the same type and mode and have the same parameters for each port. The parameters for each port are: clock frequency in MHz, the percentage of time the RAM is enabled, and the percentage of time the port is writing as opposed to reading. The number of RAM blocks reported can be found in the M512s, M4Ks and M-RAMs rows of the Quartus II Compilation Report Resource Usage Summary.
Data Width	Enter the width of the data for the RAM block. This value is limited based on the RAM type. The width of the RAM block can be found in the Port A Width or the Port B Width column of the Quartus II Compilation Report. In the **Compilation Report**, select **Fitter**, and click **Resource Section**. Click **RAM Summary**. For RAM blocks that have different widths for port A and port B, use the larger of the two widths. This number must be an integer. The valid range for each RAM type is: • 1-18 for M512 • 1-36 (1-18 for True Dual-Port) for M4K • 1-144 (1-72 for True Dual-Port) for MRAM

Table 3–3. RAM Section Information (Part 2 of 3)

Column Heading	Description
RAM Mode	Select from the following modes: • **Single-Port** • **Simple Dual-Port** • **True Dual-Port** • **ROM** The mode is based on how the Quartus II Compiler implements the RAM. If you are unsure how your memory module is implemented, Altera recommends compiling a test case in the required configuration in the Quartus II software. The RAM mode can be found in the Mode column of the Quartus II Compilation Report. In the **Compilation Report**, select **Fitter**, and click **Resource Section**. Click **RAM Summary**. A single-port RAM has one port with a R/W control signal. A simple dual-port RAM has one read port and one write port. A true dual-port RAM has two ports, each with a R/W control signal. ROMs are read-only single-port RAMs.
Port A – Clock Freq	Enter the clock frequency for port A of the RAM block(s) in MHz. This value is limited by the maximum frequency specification for the RAM type and device family.
Port A – Enable %	Enter the average percentage of time the input clock enable for port A is active, regardless of activity on RAM data and address inputs. The enable percentage ranges from 0 to 100%. The default is set to 25%. RAM power is primarily consumed when a clock event occurs. Using a clock enable signal to disable a port when no read or write operation is occurring can result in significant power savings.
Port A – Write %	Enter the average percentage of time port A of the RAM block is in write mode versus read mode. For simple dual-port (1R/1W) RAMs, the write port (A) is inactive when not executing a write. For single-port and true dual-port RAMs, port A reads when not written to. This field is ignored for RAMs in ROM mode. This value must be a percentage number between 0% and 100%. The default is 50%.
Port B – Clock Freq	Enter the clock frequency for port B of the RAM block(s) in MHz. This value is limited by the maximum frequency specification for the RAM type and device family. Port B is ignored for RAM blocks in ROM or single-port mode.
Port B – Enable %	Enter the average percentage of time the input clock enable for port B is active, regardless of activity on RAM data and address inputs. The enable percentage ranges from 0 to 100%. The default is set to 25%. Port B is ignored for RAM blocks in ROM or single-port mode. RAM power is primarily consumed when a clock event occurs. Using a clock enable signal to disable a port when no read or write operation is occurring can result in significant power savings.

Table 3–3. RAM Section Information (Part 3 of 3)

Column Heading	Description
Port B – R/W %	For RAM blocks in true dual-port mode, enter the average percentage of time port B of the RAM block is in write mode versus read mode. For RAM blocks in simple dual-port mode, enter the percentage of time port B of the RAM block is reading. You cannot write to port B in simple dual-port mode. Port B is ignored for RAM blocks in ROM or single-port mode. This value must be a percentage number between 0% and 100%. The default is 50%.
Toggle%	The average percentage of clock cycles that each block output signal changes value. Multiplied by clock frequency to determine the number of transitions per second. This value only affects routing power. 50% corresponds to a randomly changing signal. A random signal changes states only half the time.
Valid Width/Mode	This check fails if the entered data width or RAM mode is not compatible with the selected RAM type. M512s do not support true dual-port mode and M-RAMs do not support ROM mode. See the description of the data width column for the range of available widths for each RAM type.
Routing	This shows the power dissipation due to estimated routing (in W). Routing power is highly dependent on placement and routing, which is itself a function of design complexity. The values shown are representative of routing power based on experimentation on over 100 customer designs. Use the Quartus II PowerPlay Power Analyzer for detailed analysis based on the routing used in your design. This value is calculated automatically.
Block	This shows the power dissipation due to internal toggling of the RAM (in W). Use the Quartus II PowerPlay Power Analyzer for accurate analysis based on the exact RAM modes in your design. This value is calculated automatically.
Total	This shows the estimated power in W, based on the inputs you entered. It is the total power consumed by RAM blocks and is equal to the routing power and the block power. This value is calculated automatically.
User Comments	Enter any comments. This is an optional entry.

Figure 3–6 shows the Resource Usage Summary section in the Quartus II software Compilation Report for a design targeting the device family. The Compilation Report provides the number of RAM resources being used.

Figure 3–6. Resource Usage Summary

Fitter Resource Usage Summary

	Resource	Usage
1	Total ALUTs	10,783 / 27,104 (39 %)
2	-- ALUTs Used	10768
3	-- Combinational with no register	9258
4	-- Register only	505
5	-- Combinational with a register	1005
6	-- ALUTs Unavailable	15
7	-- Due to unpartnered 7 input function	0
8	-- Due to unpartnered 6 input function	15
9		
10	ALUT usage by number of inputs	
11	-- 7 input functions	0
12	-- 6 input functions	30
13	-- 5 input functions	2305
14	-- 4 input functions	4444
15	-- <=3 input functions	3484
16	-- Register only	505
17	-- Combinational cells for routing	376
18		
19	ALUTs without a partner	1456
20	-- unpartnered 7 input functions	0 / 0 (0 %)
21	-- unpartnered 6 input functions	30 / 30 (100 %)
22	-- unpartnered 5 input functions	559 / 2,305 (24 %)
23	-- unpartnered 4 input functions	80 / 4,444 (1 %)
24	-- unpartnered <=3 input functions	523 / 3,484 (15 %)
25	-- Unpartnered registers only	264 / 1,510 (17 %)
26		
27	ALUTs by mode	
28	-- normal mode	4972
29	-- extended LUT mode	0
30	-- arithmetic mode	5291
31	-- shared arithmetic mode	0
32		
33	Total registers	1,510 / 29,982 (5 %)
34	Total ALMs	6,112 / 13,552 (45 %)
35	Total LABs	881 / 1,694 (52 %)
36	User inserted logic elements	0
37	Virtual pins	0
38	I/O pins	226 / 501 (45 %)
39	-- Clock pins	11 / 16 (68 %)
40	Global signals	14
41	M512s	8 / 202 (3 %)
42	M4Ks	9 / 144 (6 %)
43	M-RAMs	1 / 1 (100 %)
44	Total memory bits	90,400 / 1,369,728 (6 %)
45	Total RAM block bits	635,904 / 1,369,728 (46 %)
46	DSP block 9-bit elements	36 / 128 (28 %)
47	Global clocks	10 / 16 (62 %)
48	Regional clocks	0 / 32 (0 %)
49	SERDES transmitters	18 / 58 (31 %)
50	SERDES receivers	18 / 62 (29 %)
51	Maximum fan-out node	LPLL:inst5|altpll:altpll_comp...
52	Maximum fan-out	1005
53	Total fan-out	48004
54	Average fan-out	3.85

Figure 3–7 shows the RAM Summary in the Quartus II software Compilation Report for a design targeting the device family. The Compilation Report provides the RAM type, the RAM mode, and the data width.

Figure 3–7. RAM Summary in Compilation Report

Fitter RAM Summary

	Name	Type	Mode	Port A Depth	Port A Width	Port B Depth	Port B Width	Port A Input Registers	Port A Output Registers	Port B Input Registers	Port B Output Registers	Size	Implementation Bits	M512s	M4Ks	M-RAMs
1	Case2:inst4|altsyncram:altsyncram_component|altsyncram_chu:auto_generated|ALTSYNCRAM	M-RAM	Single Port	512	36	--	--	yes	yes	--	--	49152	49152	0	0	1
2	Case3:inst2|altsyncram:altsyncram_component|altsyncram_1qe1:auto_generated|ALTSYNCRAM	M4K	Simple Dual Port	256	36	256	36	yes	no	yes	yes	9216	9216	0	2	0
3	Case3:inst5|altsyncram:altsyncram_component|altsyncram_1qe1:auto_generated|ALTSYNCRAM	M4K	Simple Dual Port	256	36	256	36	yes	no	yes	yes	9216	9216	0	2	0
4	Case4:inst20|altsyncram:altsyncram_component|altsyncram_paq1:auto_generated|ALTSYNCRAM	M4K	True Dual Port	512	36	512	36	yes	yes	yes	yes	18432	18432	0	4	0
5	Case7:inst13|altsyncram:altsyncram_component|altsyncram_18u:auto_generated|ALTSYNCRAM	M4K	ROM	512	8	--	--	yes	yes	--	--	4096	4096	0	1	0
6	myRateMatch:inst15|altsyncram:altsyncram_component|altsyncram_36d1:auto_generated|ALTSYNCRAM	M512	Simple Dual Port	128	144	128	144	yes	no	yes	yes	18432	288	8	0	0

Figure 3–8 shows the PowerPlay Early Power Estimator spreadsheet and the estimated power consumed by RAM blocks in this design.

Figure 3–8. RAM Section in the PowerPlay Early Power Estimator

RAM Return to Main

Total Thermal Power (W)	0.107
M512 Utilization	4.0%
M4K Utilization	6.9%
MRAM Utilization	100.0%

					Port A			Port B				Thermal Power (W)		
Module	RAM Type	# RAM Blocks	Data Width	RAM Mode	Clock Freq (MHz)	Enable %	Write %	Clock Freq (MHz)	Enable %	R/W %	Valid Width/ Mode	Routing	Block	Total
1	M512	8	18	Simple Dual-Port	104.9	100%	100%	104.9	100%	100%	Yes	0.007	0.015	0.022
2	M4K	4	9	True Dual-Port	100.0	100%	50%	150.0	100%	50%	Yes	0.004	0.014	0.018
3	M4K	2	18	Simple Dual-Port	100.0	100%	50%	100.0	100%	100%	Yes	0.002	0.005	0.007
4	M4K	1	8	ROM	124.9	100%	0%	0.0	0%	0%	Yes	0.000	0.002	0.002
5	M4K	2	18	Simple Dual-Port	150.0	100%	50%	150.0	100%	100%	Yes	0.003	0.008	0.011
6	M4K	1	24	Single-Port	75.1	100%	50%	0.0	0%	0%	Yes	0.001	0.002	0.003
7	MRAM	1	72	Single-Port	150.0	87%	50%	0.0	0%	0%	Yes	0.005	0.038	0.043
	M4K	0	1	Simple Dual-Port	0.0	25%	50%	0.0	25%	50%	Yes	0.000	0.000	0.000
	M4K	0	1	Simple Dual-Port	0.0	25%	50%	0.0	25%	50%	Yes	0.000	0.000	0.000

Digital Signal Processing (DSP)

Stratix II and Stratix II GX devices have dedicated DSP blocks that can implement high-speed parallel processing optimized for DSP applications. DSP blocks are ideal for implementing DSP applications that need high data throughput. The **Digital Signal Processing (DSP)** section in the PowerPlay Early Power Estimator spreadsheet provides power information for Stratix II DSP blocks.

HardCopy II devices use HCell macros which implement the supported modes of operation for the Stratix II DSP block.

Each row in the **DSP** section represents a DSP design module where all instances of the module have the same configuration, clock frequency, toggle percentage and register usage. If some (or all) DSP or multiplier instances have different configurations, you need to enter the information in different rows. You must enter the following information for each DSP or multiplier module:

- Configuration
- Clock frequency (f_{MAX}) in MHz
- Number of instances
- Toggle percentage of the data outputs
- Whether or not the inputs and outputs are registered
- Whether or not the module is pipelined

For more information on Stratix II DSP block configurations, refer to the *DSP Blocks in Stratix II Devices* chapter in volume 2 of the *Stratix II Device Handbook*. For more information on Stratix II GX and HardCopy II DSP block configurations, refer to the DSP section in the respective device handbook.

Table 3–4 describes the values that need to be entered in the **DSP** section of the PowerPlay Early Power Estimator.

Table 3–4. DSP & Multiplier Section Information (Part 1 of 2)

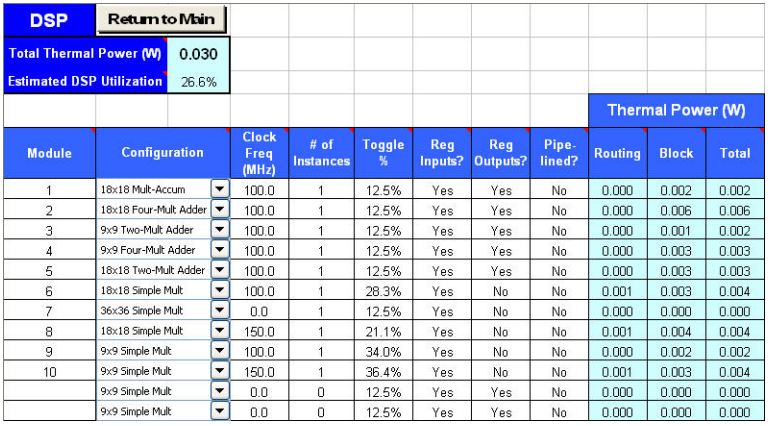
Column Heading	Description
Module	Enter a name for the DSP module in this column. This is an optional value.
Configuration	Select the DSP block configuration. The following configurations are offered: • 9 × 9 simple multiplier • 18 × 18 simple multiplier • 36 × 36 simple multiplier • 18 × 18 multiplier-accumulator • 9 × 9 two-multiplier-adder • 18 × 18 two-multiplier-adder • 9 × 9 four-multiplier-adder • 18 × 18 four-multiplier-adder
Clock Freq	Enter the clock frequency for the module in MHz. This value is limited by the maximum frequency specification for the device family.
# of Instances	Enter the number of instances that have the same configuration, clock frequency, toggle percentage and register usage. This value is independent of the number of dedicated DSP blocks being used. For example, it is possible to use four 9 × 9 simple multipliers that would all be implemented in the same DSP block in a Stratix II device. In this case, the number of instances would be four.

Table 3–4. DSP & Multiplier Section Information (Part 2 of 2)

Column Heading	Description
Toggle %	Enter the average percentage of DSP data outputs toggling on each clock cycle. The toggle percentage ranges from 0 to 50%. Typically the toggle percentage is 12.5%. For a more conservative power estimate, you can use a higher toggle percentage. In addition, 50% corresponds to a randomly changing signal (since half the time the signal changes from a 0–>0 or 1 –>1). This is considered the highest meaningful toggle rate for a DSP block.
Reg Inputs?	Select whether the input to the dedicated DSP block or multiplier block is registered using the dedicated input registers. If the dedicated input registers in the DSP or multiplier block are being used, select **Yes**. If the inputs are registered using registers in ALMs then the value is **No**.
Reg Outputs?	Select whether the outputs of the dedicated DSP block or multiplier block is registered using the dedicated output registers. If the dedicated output registers in the DSP or multiplier block are being used, select **Yes**. If the outputs are registered using registers in ALMs, then the value is **No**.
Pipe-lined?	Select whether the dedicated DSP block is pipelined.
Routing	This shows the power dissipation due to estimated routing (in W). Routing power is highly dependent on placement and routing, which is itself a function of design complexity. The values shown are representative of routing power based on experimentation on over 100 customer designs. Use the Quartus II PowerPlay Power Analyzer for detailed analysis based on the routing used in your design. This value is calculated automatically.
Block	This shows the estimated power consumed by the DSP blocks in W. This value is calculated automatically.
Total	This shows the estimated power in W, based on the inputs you entered. It is the total power consumed by DSP blocks and is equal to the routing power and the block power. This value is calculated automatically.
User Comments	Enter any comments. This is an optional entry.

Figure 3–9 shows the PowerPlay Early Power Estimator spreadsheet and the estimated power consumed by the DSP blocks in this design.

Figure 3–9. DSP Section in the PowerPlay Early Power Estimator



DSP | Return to Main

Total Thermal Power (W)	0.030
Estimated DSP Utilization	26.6%

								Thermal Power (W)		
Module	Configuration	Clock Freq (MHz)	# of Instances	Toggle %	Reg Inputs?	Reg Outputs?	Pipe-lined?	Routing	Block	Total
1	18x18 Mult-Accum	100.0	1	12.5%	Yes	Yes	No	0.000	0.002	0.002
2	18x18 Four-Mult Adder	100.0	1	12.5%	Yes	Yes	No	0.000	0.006	0.006
3	9x9 Two-Mult Adder	100.0	1	12.5%	Yes	Yes	No	0.000	0.001	0.002
4	9x9 Four-Mult Adder	100.0	1	12.5%	Yes	Yes	No	0.000	0.003	0.003
5	18x18 Two-Mult Adder	100.0	1	12.5%	Yes	Yes	No	0.000	0.003	0.003
6	18x18 Simple Mult	100.0	1	28.3%	Yes	No	No	0.001	0.003	0.004
7	36x36 Simple Mult	0.0	1	12.5%	Yes	No	No	0.000	0.000	0.000
8	18x18 Simple Mult	150.0	1	21.1%	Yes	No	No	0.001	0.004	0.004
9	9x9 Simple Mult	100.0	1	34.0%	Yes	No	No	0.000	0.002	0.002
10	9x9 Simple Mult	150.0	1	36.4%	Yes	No	No	0.001	0.003	0.004
	9x9 Simple Mult	0.0	0	12.5%	Yes	Yes	No	0.000	0.000	0.000
	9x9 Simple Mult	0.0	0	12.5%	Yes	Yes	No	0.000	0.000	0.000

General I/O Pins

Stratix II, Stratix II GX, and HardCopy II devices feature programmable I/O pins that support a wide range of industry I/O standards for increased design flexibility. The **I/O** section in the PowerPlay Early Power Estimator spreadsheet allows you to estimate the I/O pin power consumption based on the pin's I/O standards.

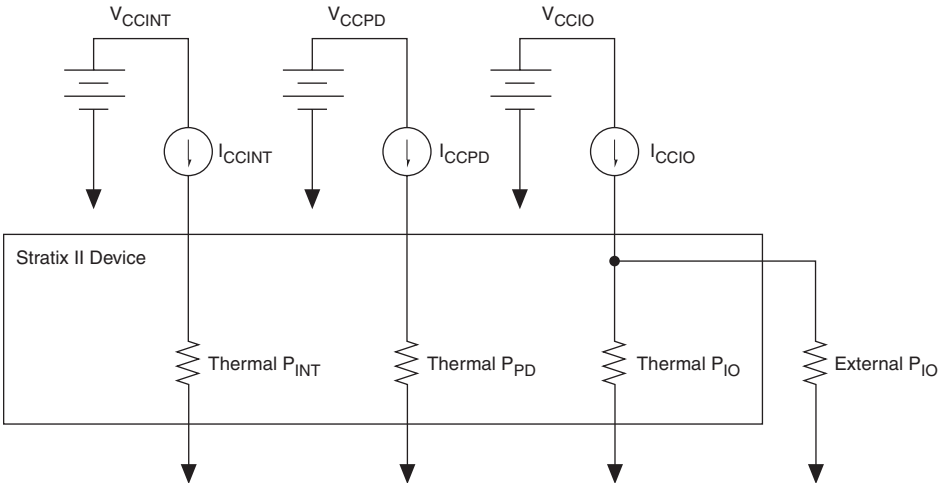
The PowerPlay Early Power Estimator spreadsheet assumes you are using external termination resistors when you design with I/O standards that recommend termination resistors (SSTL and HSTL). If your design does not use external termination resistors, you should choose the LVTTL I/O standard with the same V_{CCIO} and similar drive strength as the terminated I/O standard. For example, if you are using the SSTL-2 class II I/O standard without termination resistors (using a point-to-point connection), you should select **LVTTL/LVCMOS 2.5-V** as your I/O standard and **16mA** as the Drive Strength in the PowerPlay Early Power Estimator.

The power reported for I/O signals includes thermal and external I/O power. The total thermal power is the sum of the thermal power consumed by the device based on each power rail.

thermal power = thermal P_{INT} + thermal P_{PD} + thermal P_{IO}

Figure 3–10 shows a graphical representation of the I/O power consumption. The I_{CCIO} rail power includes both the thermal P_{IO} and the external P_{IO}.

Figure 3–10. I/O Power Representation



The V_{REF} pins consume minimal current (less than 10 µA) and is negligible when compared to the power consumed by the general purpose I/O pins. Therefore, the PowerPlay Early Power Estimator spreadsheet does not include the current for V_{REF} pins in the calculations.

Each row in the **I/O** section represents a design module where the I/O pins have the same frequency, toggle percentage, average capacitive load, I/O standard, drive strength, on-chip termination, data rate, and I/O bank. You must enter the following parameters for each design module:

- I/O standard
- Drive strength/On-chip termination
- Clock frequency (f_{MAX}) in MHz
- Number of output, input, and bidirectional pins
- I/O bank
- Pin toggle percentage
- Output enable percentage
- Average capacitance of the load
- I/O data rate

Table 3–5 describes the I/O bank parameters in the **I/O** section of the PowerPlay Early Power Estimator.

Table 3–5. I/O Bank Information in the I/O Section

Column Heading	Description
V_{CCIO}	Select the V_{CCIO} voltage for each bank. Used to cross-check selected I/O standards in table below for warning purposes.
I_{CCIO} (A)	This shows the total supply current due to the I/O pins in each I/O bank. This may be higher than the thermal power due to current supplied to off-chip termination resistors.
Unassigned	This represents the I_{CCIO} of all I/O modules not assigned to an I/O bank.

Figure 3–11 shows how the V_{CCIO} level is listed for each I/O bank. The PowerPlay Early Power Estimator spreadsheet shows the I_{CCIO} listed for each bank. Select the V_{CCIO} voltage in the V_{CCIO} column.

Figure 3–11. V_{CCIO} Listed for Each I/O Bank

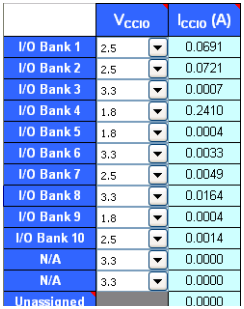


Table 3–6 describes the I/O module parameters in the **I/O** section of the PowerPlay Early Power Estimator.

Table 3–6. I/O Module Information in the I/O Section (Part 1 of 3)

Column Heading	Description
Module	Enter a name for the module in this column. This is an optional value.
I/O Standard	Select the I/O standard used for the input, output or bidirectional pins in this module from the list. The calculated I/O power varies based on the I/O standard.
Drive Strength/ On-chip Termination	Select the drive strength or on-chip termination implemented for the I/O pin(s) in this module. Drive strength and on-chip termination are mutually exclusive.

Table 3–6. I/O Module Information in the I/O Section (Part 2 of 3)

Column Heading	Description
Clock Freq (MHz)	Enter the clock frequency (in MHz). This value must be in the range of 0 to 1040 MHz. 100 MHz with a 12.5% toggle means that each I/O pin toggles 12.5 million times per second (100 × 12.5%).
# Output Pins	Enter the number of output pins used in this module. A differential pair of pins should be considered as one pin.
# Input Pins	Enter the number of input pins used in this module. A differential pair of pins should be considered as one pin.
# Bidir Pins	Enter the number of bidirectional pins used in this module. The I/O pin is treated as an output when its output enable signal is active and an input when the output enable is disabled. An I/O configured as bidirectional but used only as an output consumes more power than one configured as an output-only, due to the toggling of the input buffer every time the output buffer toggles (they share a common pin).
I/O Bank	Select the I/O bank that the module is located in. If you do not know which I/O bank the pins are assigned to, leave the value as "?." Assigning the I/O module to a bank checks whether or not your I/O voltage assignments are compatible. This allows per-bank I_{CCIO} reporting. The PowerPlay Early Power Estimator spreadsheet does not take any I/O placement constraints into consideration except if the I/O bank, I/O standard, I/O voltage are compatible.
Toggle %	Enter the average percentage of output and bidirectional pins toggling on each clock cycle. The toggle percentage ranges from 0 to 200%. If the pin uses a double data rate (DDR), you can set the data rate to single data rate (SDR) and double the toggle percentage. The Quartus II software often uses this method to output information. Typically the toggle percentage is 12.5%. To be more conservative, you can use a higher toggle percentage.
OE %	Enter the average percentage of time that: • The output I/O pins are enabled. • Bidirectional I/O pins are outputs and enabled. During the remaining time: • Output I/O pins are tristated. • Bidirectional I/O pins are inputs. This number must be a percentage between 0% and 100%.
Load (pF)	Enter the pin loading external to the chip (in pF). Only applies to outputs and bidirectional pins. Pin and package capacitance is already included in I/O model. Therefore, you only need to include off-chip capacitance in the Load parameter.

Table 3–6. I/O Module Information in the I/O Section (Part 3 of 3)

Column Heading	Description
Data Rate	Select either **SDR** or **DDR** as the I/O data rate. This indicates whether the I/O value is updated once (SDR) or twice (DDR) a cycle. If the data rate of the pin is DDR, it is possible to set the data rate to SDR and double the toggle percentage. The Quartus II software often uses this method to output information.
Bank I/O Std Check	This indicates whether the selected I/O standard is available on the selected I/O bank. Not all I/O banks can implement every I/O standard.
Bank Voltage Check	This indicates whether or not the selected I/O bank has a voltage compatible with the selected I/O standard.
Thermal Power (W), Routing	This shows the power dissipation due to estimated routing (in W). Routing power is highly dependent on placement and routing, which is itself a function of design complexity. The values shown are representative of routing power based on experimentation on over 100 real-world designs. Use the Quartus II PowerPlay Power Analyzer for detailed analysis based on the routing used in your design. This value is calculated automatically.
Thermal Power (W), Block	This shows the power dissipation due to internal and load toggling of the I/O (in W). Use the Quartus II PowerPlay Power Analyzer for accurate analysis based on the exact I/O configuration of your design. This value is calculated automatically.
Thermal Power (W), Total	This shows the total power dissipation (in W). The total power dissipation is the sum of the routing and block power. This value is calculated automatically.
Supply Current (A), I_{CCINT}	This shows the current drawn from the I_{CCINT} rail. Powers internal digital circuitry and routing.This value is calculated automatically.
Supply Current (A), I_{CCPD}	This shows the current drawn from the V_{CCPD} rail. This rail powers the pre-drive circuitry and operates at 3.3 V. This value is calculated automatically.
Supply Current (A), I_{CCIO}	This shows the current drawn from this bank's V_{CCIO} rail. Some of this current may be drawn into off-chip termination resistors. This value is calculated automatically.
User Comments	Enter any comments. This is an optional entry.

Figure 3–12 shows the I/O module parameters in the PowerPlay Early Power Estimator spreadsheet **I/O** section.

Figure 3–12. PowerPlay Early Power Estimator Spreadsheet I/O Section

														Thermal Power (W)			Supply Current (A)		
Module	I/O Standard	Drive Strength / On-Chip Termination	Clock Freq (MHz)	# Output Pins	# Input Pins	# Bidir Pins	I/O Bank	Toggle %	OE %	Load (pF)	Data Rate	Bank I/O Std Check	Bank Voltage Check	Routing	Block	Total	$I_{CC}INT$	$I_{CC}PD$	$I_{CC}IO$
1	LVTTL/LVCMOS 1.8-V	8 mA	0.0	22	0	0	5	0.0%	100.0%	0	SDR	PASS	PASS	0.000	0.001	0.001	0.000	0.000	0.000
2	LVTTL/LVCMOS 2.5-V	16 mA	100.0	0	0	6	10	35.8%	50.0%	0	SDR	PASS	PASS	0.000	0.005	0.005	0.001	0.001	0.001
3	LVDS	Default	840.1	9	0	0	2	0.0%	100.0%	0	SDR	PASS	PASS	0.000	0.140	0.140	0.003	0.000	0.060
4	LVTTL 3.3-V	24 mA	0.0	0	1	0	7	0.0%	100.0%	0	SDR	PASS	PASS	0.000	0.000	0.000	0.000	0.000	0.000
5	HSTL Class II 1.8-V	20 mA	100.0	20	0	0	4	0.0%	100.0%	0	SDR	PASS	PASS	0.000	0.148	0.148	0.000	0.000	0.241
6	LVTTL 3.3-V	24 mA	99.8	0	1	0	3	200.0%	100.0%	0	SDR	PASS	PASS	0.000	0.001	0.002	0.001	0.000	0.000
7	LVTTL 3.3-V	12 mA	75.0	0	1	0	6	200.0%	100.0%	0	SDR	PASS	PASS	0.000	0.001	0.001	0.000	0.000	0.000
8	LVTTL 3.3-V	12 mA	74.8	1	0	0	6	69.4%	100.0%	0	SDR	PASS	PASS	0.000	0.002	0.002	0.000	0.000	0.000
9	LVTTL 3.3-V	24 mA	0.0	0	1	0	3	0.0%	100.0%	0	SDR	PASS	PASS	0.000	0.000	0.000	0.000	0.000	0.000
10	LVTTL/LVCMOS 2.5-V	16 mA	100.0	0	0	30	7	33.4%	50.0%	0	SDR	PASS	PASS	0.002	0.023	0.025	0.006	0.003	0.005
11	LVTTL 3.3-V	24 mA	150.0	36	0	0	8	36.3%	100.0%	0	SDR	PASS	PASS	0.000	0.088	0.088	0.004	0.010	0.015
12	LVDS	Default	840.1	0	10	0	2	0.0%	100.0%	0	SDR	PASS	PASS	0.000	0.063	0.063	0.029	0.000	0.011
13	LVTTL/LVCMOS 2.5-V	16 mA	0.0	0	1	0	7	0.0%	100.0%	0	SDR	PASS	PASS	0.000	0.000	0.000	0.000	0.000	0.000
14	LVTTL 3.3-V	24 mA	175.0	8	0	0	3	0.0%	100.0%	0	SDR	PASS	PASS	0.000	0.000	0.000	0.000	0.000	0.000
15	LVTTL/LVCMOS 1.8-V	12 mA	0.0	6	0	0	9	0.0%	100.0%	0	SDR	PASS	PASS	0.000	0.000	0.000	0.000	0.000	0.000
16	LVTTL 3.3-V	12 mA	75.1	0	1	0	6	65.9%	100.0%	0	SDR	PASS	PASS	0.000	0.000	0.000	0.000	0.000	0.000
17	LVDS	Default	105.0	0	1	0	2	200.0%	100.0%	0	SDR	PASS	PASS	0.000	0.006	0.007	0.004	0.000	0.001
18	LVTTL 3.3-V	12 mA	175.0	0	1	0	6	200.0%	100.0%	0	SDR	PASS	PASS	0.001	0.002	0.003	0.001	0.000	0.001
19	LVTTL 3.3-V	24 mA	100.0	0	2	0	8	49.5%	100.0%	0	SDR	PASS	PASS	0.000	0.001	0.001	0.001	0.000	0.000
20	LVTTL 3.3-V	24 mA	99.8	0	1	0	8	200.0%	100.0%	0	SDR	PASS	PASS	0.000	0.001	0.002	0.001	0.000	0.000
21	LVTTL 3.3-V	12 mA	100.0	1	0	0	6	154.5%	100.0%	0	SDR	PASS	PASS	0.000	0.008	0.008	0.000	0.001	0.002
22	LVDS	Default	840.1	0	8	0	1	0.0%	100.0%	0	SDR	PASS	PASS	0.000	0.051	0.051	0.023	0.000	0.009
23	LVDS	Default	840.1	9	0	0	1	0.0%	100.0%	0	SDR	PASS	PASS	0.000	0.140	0.140	0.003	0.000	0.060
24	LVTTL/LVCMOS 1.8-V	12 mA	0.0	8	0	0	4	0.0%	100.0%	0	SDR	PASS	PASS	0.000	0.000	0.000	0.000	0.000	0.000
25	LVTTL 3.3-V	24 mA	150.0	0	2	0	8	22.8%	100.0%	0	SDR	PASS	PASS	0.000	0.000	0.001	0.000	0.000	0.000
26	LVTTL 3.3-V	12 mA	105.0	0	1	0	1	200.0%	100.0%	0	SDR	PASS	PASS	0.000	0.001	0.002	0.001	0.000	0.000
27	LVTTL 3.3-V	24 mA	0.0	0	2	0	8	0.0%	100.0%	0	SDR	PASS	PASS	0.000	0.000	0.000	0.000	0.000	0.000
	LVTTL 3.3-V	24 mA	0.0	0	0	0	7	12.5%	100.0%	0	SDR	N/A	N/A	0.000	0.000	0.000	0.000	0.000	0.000

The PowerPlay Early Power Estimator spreadsheet verifies whether or not the I/O standard selected is available in the selected I/O bank. If there is a discrepancy, it is displayed in the **Bank I/O Std Check** column, as shown in Figure 3–13.

Figure 3–13. I/O Standard Verification

Bank I/O Std Check
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS
PASS

The PowerPlay Early Power Estimator spreadsheet also verifies that the V_{CCIO} levels match the I/O standards for each I/O bank. If there is a discrepancy, it is displayed in the **Bank Voltage Check** column, as shown in Figure 3–14.

Figure 3–14. PowerPlay Early Power Estimator Spreadsheet Checks for V_{CCIO} Inconsistencies

Bank Voltage Check
PASS
PASS
FAIL?
PASS
PASS
PASS
PASS
PASS
PASS
FAIL?
PASS
PASS

Importing the Quartus II estimation file automatically populates the V_{CCIO} voltages. However, certain designs may have discrepancies. This occurs most often if I/O standards that are listed as different voltages in the PowerPlay Early Power Estimator spreadsheet can actually be in the same I/O bank on the device.

For more information on I/O standard guidelines, see the *Selectable I/O Standards in Stratix II Devices* chapter in volume 2 of the *Stratix II Device Handbook*.

If there are discrepancies between the V_{CCIO} voltages in banks, the PowerPlay Early Power Estimator spreadsheet displays the following message:

Bank and I/O voltage selection inconsistent with I/O Bank Voltage. See the Bank Voltage column.

Ensure that the correct V_{CCIO} is selected for the bank.

Figure 3–15 shows an example of the **Output Pins** report in the Quartus II software Compilation Report. The Compilation Report lists the I/O standard used on each pin.

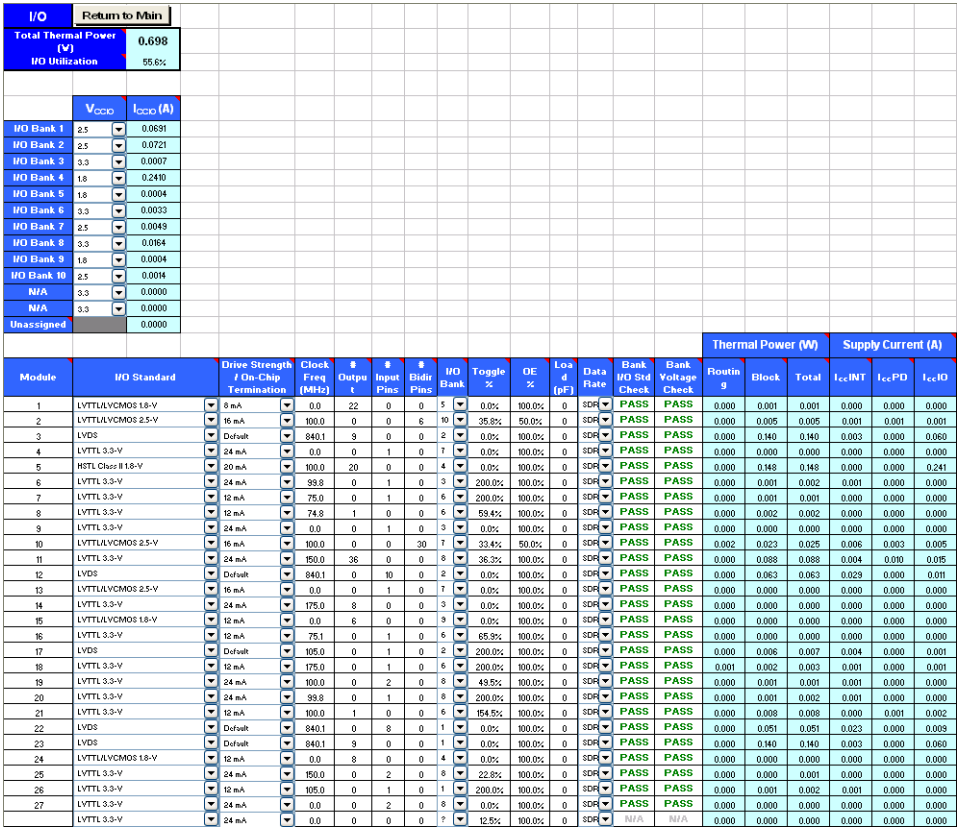
Figure 3–15. Output Pins Report in Compilation Report

Output Pins

	Name	Pin #	I/O Bank	X coordinate	Y coordinate	Cell number	Output Register	Output Enable Register	Power Up High	PCI I/O Enabled	Open Drain	TRI Primitive	Bus Hold	Weak Pull Up	I/O Standard	Current Strength
1	LogicOut	V12	7	45	0	2	no	no	no	no	no	no	no	Off	LVTTL	24mA
2	c3out[0]	N7	5	62	21	2	no	no	no	no	no	no	no	Off	1.8 V	8mA
3	c3out[10]	K2	5	62	23	3	no	no	no	no	no	no	no	Off	1.8 V	8mA
4	c3out[11]	C13	4	35	37	0	no	no	no	no	no	no	no	Off	1.8 V	12mA
5	c3out[12]	AD13	10	36	0	1	no	no	no	no	no	no	no	Off	1.8 V	12mA
6	c3out[13]	L3	5	62	22	3	no	no	no	no	no	no	no	Off	1.8 V	8mA
7	c3out[14]	AD12	10	39	0	2	no	no	no	no	no	no	no	Off	1.8 V	12mA
8	c3out[15]	L2	5	62	22	0	no	no	no	no	no	no	no	Off	1.8 V	8mA
9	c3out[16]	P3	5	62	20	0	no	no	no	no	no	no	no	Off	1.8 V	8mA
10	c3out[17]	M5	5	62	24	1	no	no	no	no	no	no	no	Off	1.8 V	8mA
11	c3out[18]	P2	5	62	20	3	no	no	no	no	no	no	no	Off	1.8 V	8mA
12	c3out[19]	N4	5	62	23	1	no	no	no	no	no	no	no	Off	1.8 V	8mA
13	c3out[1]	G10	4	49	37	2	no	no	no	no	no	no	no	Off	1.8 V	12mA
14	c3out[20]	F13	4	39	37	0	no	no	no	no	no	no	no	Off	1.8 V	12mA
15	c3out[21]	H11	4	45	37	0	no	no	no	no	no	no	no	Off	1.8 V	12mA
16	c3out[22]	AE12	10	36	0	0	no	no	no	no	no	no	no	Off	1.8 V	12mA
17	c3out[23]	K11	4	48	37	1	no	no	no	no	no	no	no	Off	1.8 V	12mA
18	c3out[24]	AC12	10	39	0	1	no	no	no	no	no	no	no	Off	1.8 V	12mA
19	c3out[25]	F12	4	42	37	2	no	no	no	no	no	no	no	Off	1.8 V	12mA
20	c3out[26]	AE13	10	36	0	2	no	no	no	no	no	no	no	Off	1.8 V	12mA
21	c3out[27]	E11	4	48	37	2	no	no	no	no	no	no	no	Off	1.8 V	12mA

Figure 3–16 shows the PowerPlay Early Power Estimator spreadsheet and the estimated power consumed by the I/O pins.

Figure 3–16. I/O Section in the PowerPlay Early Power Estimator



I/O | Return to Main

Total Thermal Power (V) I/O Utilization: 0.698 | 55.6%

	V_{CCIO}	I_{CCIO} (A)
I/O Bank 1	2.5	0.0691
I/O Bank 2	2.5	0.0721
I/O Bank 3	3.3	0.0007
I/O Bank 4	1.8	0.2410
I/O Bank 5	1.8	0.0004
I/O Bank 6	3.3	0.0033
I/O Bank 7	2.5	0.0049
I/O Bank 8	3.3	0.0164
I/O Bank 9	1.8	0.0004
I/O Bank 10	2.5	0.0014
N/A	3.3	0.0000
N/A	3.3	0.0000
Unassigned		0.0000

														Thermal Power (W)			Supply Current (A)		
Module	I/O Standard	Drive Strength / On-Chip Termination	Clock Freq (MHz)	# Output	# Input Pins	# Bidir Pins	I/O Bank	Toggle %	OE %	Load (pF)	Data Rate	Bank I/O Std Check	Bank Voltage Check	Routing	Block	Total	$I_{CC}INT$	$I_{CC}PD$	$I_{CC}IO$
1	LVTTL/LVCMOS 1.8-V	8 mA	0.0	22	0	0	5	0.0%	100.0%	0	SDR	PASS	PASS	0.000	0.001	0.001	0.000	0.000	0.000
2	LVTTL/LVCMOS 2.5-V	16 mA	100.0	0	0	6	10	35.8%	50.0%	0	SDR	PASS	PASS	0.000	0.005	0.005	0.001	0.001	0.001
3	LVDS	Default	840.1	9	0	0	2	0.0%	100.0%	0	SDR	PASS	PASS	0.000	0.140	0.140	0.003	0.000	0.060
4	LVTTL 3.3-V	24 mA	0.0	0	1	0	7	0.0%	100.0%	0	SDR	PASS	PASS	0.000	0.000	0.000	0.000	0.000	0.000
5	HSTL Class II 1.8-V	20 mA	100.0	20	0	0	4	0.0%	100.0%	0	SDR	PASS	PASS	0.000	0.148	0.148	0.000	0.000	0.241
6	LVTTL 3.3-V	24 mA	99.8	0	1	0	3	200.0%	100.0%	0	SDR	PASS	PASS	0.000	0.001	0.002	0.001	0.000	0.000
7	LVTTL 3.3-V	12 mA	75.0	0	1	0	6	200.0%	100.0%	0	SDR	PASS	PASS	0.000	0.001	0.001	0.000	0.000	0.000
8	LVTTL 3.3-V	12 mA	74.8	1	0	0	6	59.4%	100.0%	0	SDR	PASS	PASS	0.000	0.002	0.002	0.000	0.000	0.000
9	LVTTL 3.3-V	24 mA	0.0	0	1	0	3	0.0%	100.0%	0	SDR	PASS	PASS	0.000	0.000	0.000	0.000	0.000	0.000
10	LVTTL/LVCMOS 2.5-V	16 mA	100.0	0	0	30	7	33.4%	50.0%	0	SDR	PASS	PASS	0.002	0.023	0.025	0.006	0.003	0.005
11	LVTTL 3.3-V	24 mA	150.0	36	0	0	8	36.3%	100.0%	0	SDR	PASS	PASS	0.000	0.088	0.088	0.004	0.010	0.015
12	LVDS	Default	840.1	0	10	0	2	0.0%	100.0%	0	SDR	PASS	PASS	0.000	0.063	0.063	0.029	0.000	0.011
13	LVTTL/LVCMOS 2.5-V	16 mA	0.0	0	1	0	7	0.0%	100.0%	0	SDR	PASS	PASS	0.000	0.000	0.000	0.000	0.000	0.000
14	LVTTL 3.3-V	24 mA	175.0	8	0	0	3	0.0%	100.0%	0	SDR	PASS	PASS	0.000	0.000	0.000	0.000	0.000	0.000
15	LVTTL/LVCMOS 1.8-V	12 mA	0.0	6	0	0	3	0.0%	100.0%	0	SDR	PASS	PASS	0.000	0.000	0.000	0.000	0.000	0.000
16	LVTTL 3.3-V	12 mA	75.1	0	1	0	6	65.9%	100.0%	0	SDR	PASS	PASS	0.000	0.000	0.000	0.000	0.000	0.000
17	LVDS	Default	105.0	0	1	0	2	200.0%	100.0%	0	SDR	PASS	PASS	0.000	0.006	0.007	0.004	0.000	0.001
18	LVTTL 3.3-V	12 mA	175.0	0	1	0	6	200.0%	100.0%	0	SDR	PASS	PASS	0.001	0.002	0.003	0.001	0.000	0.001
19	LVTTL 3.3-V	24 mA	100.0	0	2	0	8	49.5%	100.0%	0	SDR	PASS	PASS	0.000	0.001	0.001	0.001	0.000	0.000
20	LVTTL 3.3-V	24 mA	99.8	0	1	0	8	200.0%	100.0%	0	SDR	PASS	PASS	0.000	0.001	0.002	0.001	0.000	0.000
21	LVTTL 3.3-V	12 mA	100.0	1	0	0	6	154.5%	100.0%	0	SDR	PASS	PASS	0.000	0.008	0.008	0.000	0.001	0.002
22	LVDS	Default	840.1	0	8	0	1	0.0%	100.0%	0	SDR	PASS	PASS	0.000	0.051	0.051	0.023	0.000	0.009
23	LVDS	Default	840.1	9	0	0	1	0.0%	100.0%	0	SDR	PASS	PASS	0.000	0.140	0.140	0.003	0.000	0.060
24	LVTTL/LVCMOS 1.8-V	12 mA	0.0	8	0	0	4	0.0%	100.0%	0	SDR	PASS	PASS	0.000	0.000	0.000	0.000	0.000	0.000
25	LVTTL 3.3-V	24 mA	150.0	0	2	0	8	22.8%	100.0%	0	SDR	PASS	PASS	0.000	0.000	0.001	0.000	0.000	0.000
26	LVTTL 3.3-V	12 mA	105.0	0	1	0	1	200.0%	100.0%	0	SDR	PASS	PASS	0.000	0.001	0.002	0.001	0.000	0.000
27	LVTTL 3.3-V	24 mA	0.0	0	2	0	8	0.0%	100.0%	0	SDR	PASS	PASS	0.000	0.000	0.000	0.000	0.000	0.000
	LVTTL 3.3-V	24 mA	0.0	0	0	0	?	12.5%	100.0%	0	SDR	N/A	N/A	0.000	0.000	0.000	0.000	0.000	0.000

High Speed Differential Interface (HSDI)

Stratix II, Stratix II GX, and HardCopy II devices feature dedicated circuitry that interface with high-speed differential I/O standards. These are dedicated transmitters and receivers that contain serializer and deserializer blocks respectively. The **HSDI** section in the PowerPlay Early Power Estimator spreadsheet is divided into to receiver and transmitter parts.

The power calculated in the **HSDI** section only applies to the transmitter serializer block or the receiver deserializer block. The transmitter and receiver are implemented using the `altlvds` megafunction. The I/O buffer power is calculated in the **I/O** section and the PLL power is calculated in the **PLL** section.

Each row in the **HSDI** section represents a separate receiver or transmitter domain. You must enter the following parameters for transmitter and receiver domains:

- Data rate (in Mbps)
- Number of channels in that transmitter domain.
- Toggle percentage

The receiver power is the same whether or not the DPA circuitry is used.

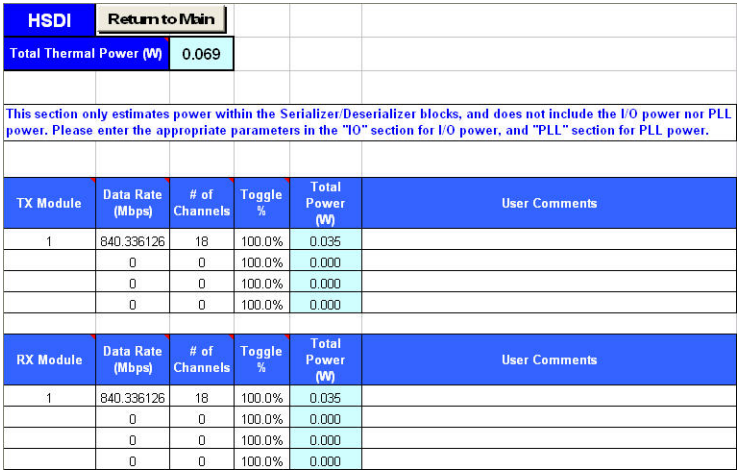
Table 3–7 describes the parameters in the **HSDI** section of the PowerPlay Early Power Estimator.

Table 3–7. HSDI Section Information

Column Heading	Description
TX/RX Module	Enter a name for the module in this column. This is an optional value.
Data Rate (Mbps)	Enter the maximum data rate in Mbps of the receiver or transmitter module. The SERDES circuitry can transmit and receive data up to 1,000 Mbps per channel. Therefore, the data rate must be a decimal number from 0 to 1,000 Mbps.
# of Channels	Enter the number of receiver and transmitter channels running at the above data rate. This number must be an integer value from 0 to 156.
Toggle %	Enter the average percentage of toggling on each clock cycle. The toggle % ranges from 0 to 100%. The default toggle percentage is 50%.
Total Power	This shows the estimated power in W, based on the data rate and number of channels entered. This value is calculated automatically.
User Comments	Enter any comments. This is an optional entry.

Figure 3–17 shows the PowerPlay Early Power Estimator spreadsheet and the estimated power consumed by HSDI blocks for this design.

Figure 3–17. HSDI Section in the PowerPlay Early Power Estimator



HSDI | Return to Main

Total Thermal Power (W)	0.069

This section only estimates power within the Serializer/Deserializer blocks, and does not include the I/O power nor PLL power. Please enter the appropriate parameters in the "IO" section for I/O power, and "PLL" section for PLL power.

TX Module	Data Rate (Mbps)	# of Channels	Toggle %	Total Power (W)	User Comments
1	840.336126	18	100.0%	0.035	
	0	0	100.0%	0.000	
	0	0	100.0%	0.000	
	0	0	100.0%	0.000	

RX Module	Data Rate (Mbps)	# of Channels	Toggle %	Total Power (W)	User Comments
1	840.336126	18	100.0%	0.035	
	0	0	100.0%	0.000	
	0	0	100.0%	0.000	
	0	0	100.0%	0.000	

Phase-Locked Loops (PLLs)

Stratix II, Stratix II GX, and HardCopy II devices feature enhanced and fast PLLs for general usage. If you are using dedicated transmitters or receivers and are using an LVDS PLL to implement serialization or deserialization, specify an LVDS PLL and enter power information in the **PLL** section.

When a fast PLL drives LVDS hardware, it is referred to as an LVDS PLL. LVDS PLLs drive LVDS clock trees and DPA buses at the VCO frequency (0 to 1040 MHz). If an LVDS PLL drives LVDS hardware only, enter the appropriate VCO frequency and specify an output frequency of 0 MHz. If the LVDS PLL also drives a clock to a pin or to the core, specify that clock frequency as the output frequency (0 to 550 MHz).

Each row in the **PLL** section represents one or more PLLs in the device. You need to enter the maximum output frequency and the VCO frequency for each PLL. You must also specify whether each PLL is an LVDS, fast or enhanced PLL. Table 3–8 describes the values that need to be entered in the **PLL** section of the PowerPlay Early Power Estimator.

Table 3–8. PLL Section Information

Column Heading	Description
Module	Enter a name for the PLL in this column. This is an optional value.
PLL Type	Select whether the PLL is an LVDS, fast or enhanced PLL.
# PLL Blocks	Enter the number of PLL blocks with the same specific output frequency and VCO frequency combination.
# DPA Buses	Enter the number of dynamic phase alignment (DPA) buses in use. DPA is only available for LVDS PLLs.
Output Freq	Enter the maximum output frequency (f_{MAX}) of the PLL in MHz. The maximum output frequency is reported in the PLL Usage column of the Quartus II Compilation Report. In the **Compilation Report**, select **Fitter**, and click **Resource Section**. Select **PLL Usage**, and click **Output Frequency**. If there are multiple clock outputs from the PLL, choose the maximum output frequency listed. The output frequency is the same as the VCO frequency for LVDS PLLs used as part of a SERDES.
VCO Freq	Enter the frequency of the voltage controlled oscillator in MHz. The VCO frequency is reported in the Nominal VCO frequency row of the Quartus II Compilation Report. In the **Compilation Report**, select **Fitter**, and click **Resource Section**. Select **PLL Summary**, and click **Nominal VCO frequency**.
Total Power	This shows the estimated power in W, based on the maximum output frequency and the VCO frequency you entered. This value is calculated automatically.
User Comments	Enter any comments. This is an optional entry.

Figure 3–18 shows the PLL Usage section in the Quartus II software Compilation Report for a design. The Compilation Report provides the maximum frequency a PLL outputs.

Figure 3–18. PLL Usage in Compilation Report

PLL Usage

	Name	Output Clock	Mult	Div	Output Frequency
1	pll1:inst1|altpll:altpll_component|_clk0	clock0	1	1	100.0 MHz
2	pll1:inst1|altpll:altpll_component|_clk1	clock1	3	2	150.0 MHz
3	LPLL:inst5|altpll:altpll_component|_clk0	clock0	1	1	75.0 MHz
4	LPLL:inst5|altpll:altpll_component|_clk1	clock1	1	1	75.0 MHz
5	pll1:inst2|altpll:altpll_component|_clk0	clock0	1	1	100.0 MHz
6	pll1:inst2|altpll:altpll_component|_clk1	clock1	3	2	150.0 MHz
7	ROMPLL:inst7|altpll:altpll_component|_clk0	clock0	5	7	125.01 MHz
8	ROMPLL:inst7|altpll:altpll_component|_clk1	clock1	1	1	175.01 MHz
9	myLVDSTX:inst6|altlvds_tx:altlvds_tx_component|lvds_tx_7s01:auto_generated|pll	clock0	1	1	105.01 MHz
10	myLVDSTX:inst6|altlvds_tx:altlvds_tx_component|lvds_tx_7s01:auto_generated|pll~ENAOUT0	enable0	1	1	105.01 MHz
11	myLVDSTX:inst6|altlvds_tx:altlvds_tx_component|lvds_tx_7s01:auto_generated|pll~SCLKOUT0	sclkout0	8	1	840.08 MHz
12	myLVDSRX:inst9|altlvds_rx:altlvds_rx_component|lvds_rx_bkv:auto_generated|pll	clock0	1	1	105.01 MHz
13	myLVDSRX:inst9|altlvds_rx:altlvds_rx_component|lvds_rx_bkv:auto_generated|pll~ENAOUT0	enable0	1	1	105.01 MHz
14	myLVDSRX:inst9|altlvds_rx:altlvds_rx_component|lvds_rx_bkv:auto_generated|pll~SCLKOUT0	sclkout0	8	1	840.08 MHz

Figure 3–19 shows the PLL Summary in the Quartus II software Compilation Report for a design targeting a Stratix II device. The Compilation Report provides the VCO frequency of a PLL.

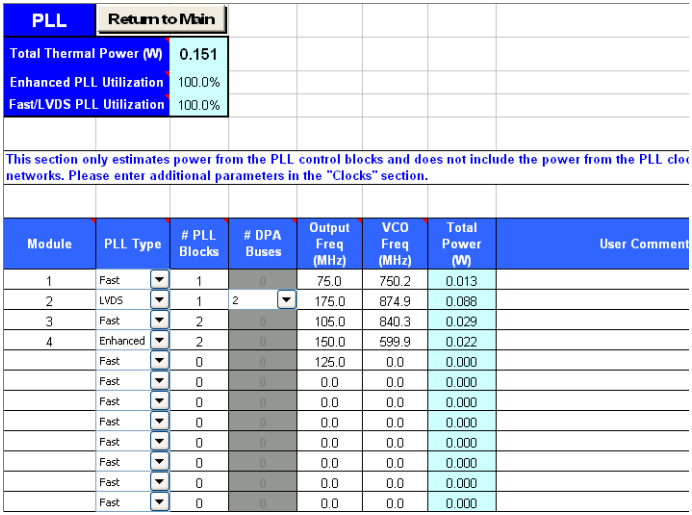
Figure 3–19. PLL Summary in Compilation Report

PLL Summary

	Name	pll1:inst1|altpll:altpll_component|pll	LPLL:inst5|altpll:altpll_component|pll	pll1:inst2|altpll:altpll_component|pll	ROMPLL:inst7|altpll:altpll_component|pll	myLVDSTX:inst6|altlvds_tx:altlvds_tx...	myLVDSRX:inst9|altlvds_rx:altlvd...
1	PLL type	Enhanced	Fast	Enhanced	Fast	Fast	Fast
2	PLL mode	Normal	Normal	Normal	Normal	Normal	Normal
3	Feedback source	--	--	--	--	--	--
4	Compensate clock	clock0	clock0	clock0	clock0	DIFFIOCLK	DIFFIOCLK
5	Switchover type	--	--	--	--	--	--
6	Switchover on loss of clock	--	--	--	--	--	--
7	Switchover counter	--	--	--	--	--	--
8	Gate lock counter	--	--	--	--	--	--
9	Input frequency 0	100.0 MHz	75.0 MHz	100.0 MHz	175.01 MHz	105.01 MHz	105.01 MHz
10	Input frequency 1	--	--	--	--	--	--
11	Nominal PFD frequency	100.0 MHz	75.0 MHz	100.0 MHz	175.0 MHz	105.0 MHz	105.0 MHz
12	Nominal VCO frequency	599.9 MHz	750.2 MHz	599.9 MHz	874.9 MHz	840.3 MHz	840.3 MHz
13	VCO post scale	--	--	--	--	--	--
14	VCO multiply	--	--	--	--	8	8
15	VCO divide	--	--	--	--	1	1
16	Freq min lock	95.92 MHz	71.92 MHz	95.92 MHz	95.68 MHz	87.52 MHz	87.52 MHz
17	Freq max lock	173.43 MHz	104.28 MHz	173.43 MHz	208.55 MHz	130.34 MHz	130.34 MHz
18	M VCO Tap	0	0	0	0	4	4
19	M Initial	1	1	1	1	1	1
20	M value	6	10	6	5	8	8
21	N value	1	1	1	1	1	1
22	M2 value	--	--	--	--	--	--
23	N2 value	--	--	--	--	--	--
24	SS counter	--	--	--	--	--	--
25	Downspread	--	--	--	--	--	--
26	Spread frequency	--	--	--	--	--	--
27	Charge pump current	114 uA	148 uA	114 uA	92 uA	131 uA	131 uA
28	Loop filter resistance	1.000000 KOhm	1.000000 KOhm	1.000000 KOhm	1.000000 KOhm	1.000000 KOhm	1.000000 KOhm
29	Loop filter capacitance	5 pF	8 pF	5 pF	2 pF	2 pF	2 pF
30	Bandwidth	6.93 MHz (5.51 MHz to 11.99 MHz)	5.22 MHz (3.95 MHz to 8.99 MHz)	6.93 MHz (5.51 MHz to 11.99 MHz)	6.74 MHz (5.41 MHz to 11.96 MHz)	6.08 MHz (4.75 MHz to 10.94 MHz)	6.08 MHz (4.75 MHz to 10.94 MHz)
31	Real time reconfigurable	Off	Off	Off	Off	Off	Off
32	Scan chain MIF file	--	--	--	--	--	--
33	Preserve counter order	Off	Off	Off	Off	Off	Off
34	PLL location	PLL_6	PLL_3	PLL_5	PLL_4	PLL_2	PLL_1
35	Inclk0 signal	clk:ab	lclk	clkfreq	romclk	tx_refclk	rx_refclk
36	Inclk1 signal	--	--	--	--	--	--

Figure 3–20 shows the PowerPlay Early Power Estimator spreadsheet and the estimated power consumed by PLLs in this design.

Figure 3–20. PLL Section in the PowerPlay Early Power Estimator



PLL | Return to Main

Total Thermal Power (W)	0.151
Enhanced PLL Utilization	100.0%
Fast/LVDS PLL Utilization	100.0%

This section only estimates power from the PLL control blocks and does not include the power from the PLL clo networks. Please enter additional parameters in the "Clocks" section.

Module	PLL Type	# PLL Blocks	# DPA Buses	Output Freq (MHz)	VCO Freq (MHz)	Total Power (W)	User Comment
1	Fast	1	0	75.0	750.2	0.013	
2	LVDS	1	2	175.0	874.9	0.088	
3	Fast	2	0	105.0	840.3	0.029	
4	Enhanced	2	0	150.0	599.9	0.022	
	Fast	0	0	125.0	0.0	0.000	
	Fast	0	0	0.0	0.0	0.000	
	Fast	0	0	0.0	0.0	0.000	
	Fast	0	0	0.0	0.0	0.000	
	Fast	0	0	0.0	0.0	0.000	
	Fast	0	0	0.0	0.0	0.000	
	Fast	0	0	0.0	0.0	0.000	
	Fast	0	0	0.0	0.0	0.000	

Clocks

Stratix II, Stratix II GX, and HardCopy II devices have a total of 48 clock domains available that can be on either a global or regional clock network. There are 16 global clocks and 8 regional clocks per quadrant for a total of 32 regional clocks. For HardCopy II devices, there is no distinction between global and regional clocks. The PowerPlay Early Power Estimator spreadsheet does not distinguish between global and regional clocks because the difference in power is not significant.

Each row in the **Clocks** section represents a clock network or a separate clock domain. You must enter the clock frequency (f_{MAX}) in MHz, the total fanout for each clock network used, the global clock enable percentage, and the local clock enable percentage. Table 3–9 describes the parameters in the **Clock** section of the PowerPlay Early Power Estimator.

Table 3–9. Clock Section Information (Part 1 of 2)

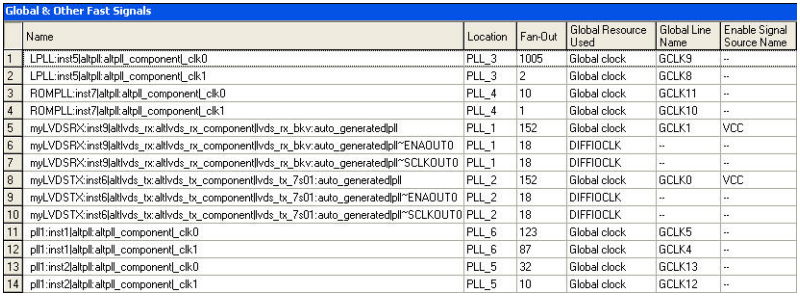
Column Heading	Description
Domain	Enter a name for the clock network in this column. This is an optional value.
Clock Freq (MHz)	Enter the frequency of the clock domain. The value must be between 0 and 550 Mhz.

Table 3–9. Clock Section Information (Part 2 of 2)

Column Heading	Description
Total Fanout	Enter the total number of flip flops and RAM, DSP, and I/O blocks fed by this clock. The number of resources driven by every global clock and regional clock signal is reported in the Fan-out column of the Quartus II Compilation Report. In the **Compilation Report**, select **Fitter** and click **Resource Section**. Select **Global & Other Fast Signals** and click **Fan-out**.
Global Enable %	Enter the average % of time that the entire clock tree is enabled. Each global clock buffer has an enable signal that can be used to dynamically shut down the entire clock tree.
Local Enable %	Enter the average % of time that clock enable is high for destination flip flops. Local clock enables for flip flops in ALMs are promoted to LAB-wide signals. When a given flip flop is disabled, the LAB-wide clock is also disabled, cutting clock power in addition to power for down-stream logic. This sheet models only the impact on clock tree power. This column is not applicable for HardCopy II devices.
Total Power (W)	This is the total power dissipation due to clock distribution (in W). This value is calculated automatically.
User Comments	Enter any comments. This is an optional entry.

Figure 3–21 shows the **Global & Other Fast Signals** report from the Quartus II software Compilation Report for an example design. The report shows the fanout for each signal that uses a global clock. The **Timing Analysis** section of the Compilation Report lists the clock signal frequencies. Enter the appropriate information from the Compilation Report into the PowerPlay Early Power Estimator.

Figure 3–21. Global & Other Fast Signals Resource Section in Compilation Report



Global & Other Fast Signals

	Name	Location	Fan-Out	Global Resource Used	Global Line Name	Enable Signal Source Name
1	LPLL:inst5|altpll:altpll_component|_clk0	PLL_3	1005	Global clock	GCLK9	--
2	LPLL:inst5|altpll:altpll_component|_clk1	PLL_3	2	Global clock	GCLK8	--
3	ROMPLL:inst7|altpll:altpll_component|_clk0	PLL_4	10	Global clock	GCLK11	--
4	ROMPLL:inst7|altpll:altpll_component|_clk1	PLL_4	1	Global clock	GCLK10	--
5	myLVDSRX:inst9|altlvds_rx:altlvds_rx_component|lvds_rx_bk:v:auto_generated|pll	PLL_1	152	Global clock	GCLK1	VCC
6	myLVDSRX:inst9|altlvds_rx:altlvds_rx_component|lvds_rx_bk:v:auto_generated|pll~ENAOUT0	PLL_1	18	DIFFIOCLK	--	--
7	myLVDSRX:inst9|altlvds_rx:altlvds_rx_component|lvds_rx_bk:v:auto_generated|pll~SCLKOUT0	PLL_1	18	DIFFIOCLK	--	--
8	myLVDSTX:inst6|altlvds_tx:altlvds_tx_component|lvds_tx_7s01:auto_generated|pll	PLL_2	152	Global clock	GCLK0	VCC
9	myLVDSTX:inst6|altlvds_tx:altlvds_tx_component|lvds_tx_7s01:auto_generated|pll~ENAOUT0	PLL_2	18	DIFFIOCLK	--	--
10	myLVDSTX:inst6|altlvds_tx:altlvds_tx_component|lvds_tx_7s01:auto_generated|pll~SCLKOUT0	PLL_2	18	DIFFIOCLK	--	--
11	pll1:inst1|altpll:altpll_component|_clk0	PLL_6	123	Global clock	GCLK5	--
12	pll1:inst1|altpll:altpll_component|_clk1	PLL_6	87	Global clock	GCLK4	--
13	pll1:inst2|altpll:altpll_component|_clk0	PLL_5	32	Global clock	GCLK13	--
14	pll1:inst2|altpll:altpll_component|_clk1	PLL_5	10	Global clock	GCLK12	--

Figure 3–22 shows the PowerPlay Early Power Estimator spreadsheet and the estimated power consumed by clocks for this design.

Figure 3–22. Clocks Section in the PowerPlay Early Power Estimator

Clocks	Return to Main					
Total Thermal Power (W)	0.110					
Domain	Clock Freq (MHz)	Total Fanout	Global Enable %	Local Enable %	Total Power (W)	User Comments
1	124.9	10	100%	50%	0.010	
2	74.8	2	100%	50%	0.006	
3	150.0	87	100%	50%	0.014	
4	150.0	10	100%	50%	0.013	
5	100.0	123	100%	50%	0.010	
6	75.1	1005	100%	50%	0.014	
7	100.0	32	100%	50%	0.009	
8	104.9	152	100%	50%	0.010	
9	175.0	1	100%	50%	0.014	
10	104.9	152	100%	50%	0.010	
	0.0	0	100%	50%	0.000	
	0.0	0	100%	50%	0.000	
	0.0	0	100%	50%	0.000	
	0.0	0	100%	50%	0.000	
	0.0	0	100%	50%	0.000	
	0.0	0	100%	50%	0.000	
	0.0	0	100%	50%	0.000	
	0.0	0	100%	50%	0.000	
	0.0	0	100%	50%	0.000	
	0.0	0	100%	50%	0.000	

Transceiver (XCVR)

Stratix II GX devices feature dedicated embedded circuitry on the right side of the device that contain up to 20 high-speed 6.375 Gbps serial transceiver channels. Stratix II GX devices have dedicated transmitters and receivers that contain serializer and deserializer blocks, respectively. This section, therefore, is only applicable for designs targeting Stratix II GX devices.

Importing a file from the Quartus II software does not populate the V_{CCH} setting field. You must enter this information manually.

The power calculated in this section applies to the transceiver blocks, including the channels used and all circuitry used in the Clock Control Unit (CCU). The transceivers are implemented using the `ALT2GXB` megafunction. The I/O buffer power and the PLL power for the transceivers are included in this section. Transmitters and receivers assume 100 Ω termination.

There are six transceiver power rails: V_{CCT}, V_{CCH}, V_{CCR}, V_{CCA}, V_{CCP}, and V_{CCL}. Table 3–10 describes the information reported for each rail.

Table 3–10. Transceiver Power Supply Information in the I/O Section

Column Heading	Description
Power Rails	Power supply rails for the transceiver blocks.
Voltage (V)	The voltage applied to the specified power rail in Volts (V).
Current (A)	The current drawn from the specified power rail in Amps (A). This includes power drawn by transceivers in user modes and unused transceivers in power-down mode.

Each row in the **XCVR** section represents a separate transceiver domain. For each transceiver domain used, you need to enter the number of channels, the mode of the transceiver, the data rate (in Mbps), the width of the parallel data bus, the Pre-Emphasis setting, and the VOD setting. For certain modes, you must specify whether the byte serializer, rate match FIFO setting, and 8B10B encoder are used.

Table 3–11 describes the values that need to be entered in the **XCVR** section of the PowerPlay Early Power Estimator.

Table 3–11. XCVR Section Information (Part 1 of 2)

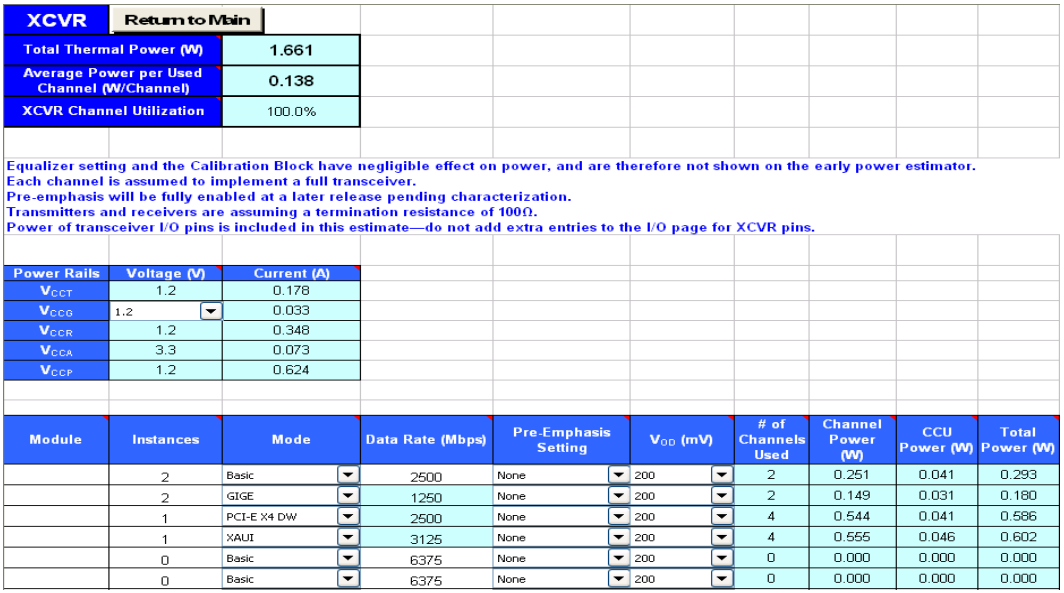
Column Heading	Description
Module	Enter a name for the module in this column. This is an optional value.
# of Channels Used	Enter the number of channels used in this transceiver domain. The channels are grouped together in one QUAD or two adjacent QUADs and clocked by a common PLL. The number of channels allowed in each domain depends on mode: PCI-Express: One to three channels for PIPEx1, four channels for PIPEx4 or eight channels for PIPEx8 XAUI: Four channels only Other modes: One to four channels.
Mode	Enter the communication protocol or standard these transceivers implement. Options include Basic 3G, Basic 6G, (OIF) CEI PHY Interface, GIGE, PCI Express (PIPE), Scrambled 5G, SONET Backplane OC12, SONET Backplane OC48, SONET Backplane OC96 and XAUI.
Data Rate (Mbps)	Enter the data rate the transceivers will operate at (in Mbps). In Basic mode this number must be specified: • Basic 3G is 622 to 3125 Mbps • Basic 6G is 3126 to 6375 Mbps For other modes the data rate is fixed.

Table 3–11. XCVR Section Information (Part 2 of 2)

Column Heading	Description
Parallel Data Width	Enter the width of the parallel data bus of each channel. The allowed range depends on the mode, data rate, byte serializer setting and 8B10B setting.
Byte Serializer Used	Enter whether or not the byte serializer/deserializer is used. If the byte serializer is used, the transceiver is in double-width mode. If it is not used, the transceiver is in single-width mode.
Rate Match FIFO Used	Enter whether or not the rate matching FIFO is used.
8B10B Encoder Used	Enter whether or not the 8B10B encoder/decoder is used.
Pre-Emphasis Setting, Pre-Tap	Enter the pre-emphasis pre-tap setting used by the transmitter. This value cannot currently be imported from Quartus II and must be entered manually
Pre-Emphasis Setting, First Post-Tap	Enter the pre-emphasis first post-tap setting used by the transmitter. This value cannot currently be imported from Quartus II and must be entered manually
Pre-Emphasis Setting, Second Post-Tap	Enter the pre-emphasis second post-tap setting used by the transmitter. This value cannot currently be imported from Quartus II and must be entered manually.
V_{OD} (mV)	Enter the output differential voltage (VOD) of the transmitter (in mV). It is assumed that the transmitter is using a termination resistance of 100 Ohms. This value cannot currently be imported from Quartus II and must be entered manually.
Channel Power (W)	This shows the total power of the Rx and Tx hardware for all channels (in W). This value is calculated automatically.
CCU Power (W)	This shows the total power of the PLLs and control circuitry used by all channels (in W). This value is calculated automatically.
Total Power (W)	This shows the total power dissipation (in W). Sum of channel + CCU power. This value is calculated automatically.
User Comments	Enter any comments. This is an optional entry.

Figure 3–23 shows the Stratix II GX device PowerPlay Early Power Estimator spreadsheet and the estimated power consumed by XCVR blocks for an example design.

Figure 3–23. XCVR Section in the Early Power Estimator



XCVR | Return to Main

Total Thermal Power (W)	1.661
Average Power per Used Channel (W/Channel)	0.138
XCVR Channel Utilization	100.0%

Equalizer setting and the Calibration Block have negligible effect on power, and are therefore not shown on the early power estimator.
Each channel is assumed to implement a full transceiver.
Pre-emphasis will be fully enabled at a later release pending characterization.
Transmitters and receivers are assuming a termination resistance of 100Ω.
Power of transceiver I/O pins is included in this estimate—do not add extra entries to the I/O page for XCVR pins.

Power Rails	Voltage (V)	Current (A)
V_{CCT}	1.2	0.178
V_{CCG}	1.2	0.033
V_{CCR}	1.2	0.348
V_{CCA}	3.3	0.073
V_{CCP}	1.2	0.624

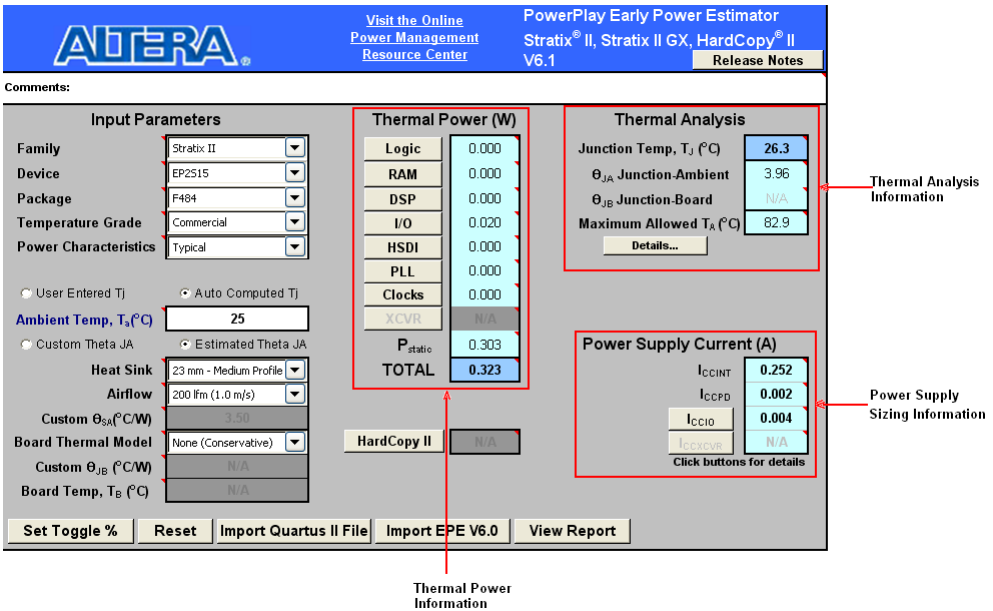
Module	Instances	Mode	Data Rate (Mbps)	Pre-Emphasis Setting	V_{OD} (mV)	# of Channels Used	Channel Power (W)	CCU Power (W)	Total Power (W)
	2	Basic	2500	None	200	2	0.251	0.041	0.293
	2	GIGE	1250	None	200	2	0.149	0.031	0.180
	1	PCI-E X4 DW	2500	None	200	4	0.544	0.041	0.586
	1	XAUI	3125	None	200	4	0.555	0.046	0.602
	0	Basic	6375	None	200	0	0.000	0.000	0.000
	0	Basic	6375	None	200	0	0.000	0.000	0.000

Power Analysis

The **Main** section of the PowerPlay Early Power Estimator spreadsheet summarizes the power and current estimates for the design. The **Main** section displays the total thermal power, thermal analysis, and power supply sizing information. The accuracy of the information depends on the information entered. The power consumed can also vary greatly depending on the toggle rates entered. The following sections provide a description of the results of the PowerPlay Early Power Estimator.

Figure 3–24 shows the Thermal Power, Thermal Analysis, and Power Supply Sizing areas in the **Main** section.

Figure 3–24. Power Areas in Main Section



Thermal Power

Thermal power is the power dissipated in the device. The total thermal power is shown in W and is a sum of the thermal power of all the resources being used in the device. The total thermal power includes the maximum power from standby and dynamic power.

The total thermal power only includes the thermal component for the **I/O** section and does not include the external power dissipation, such as from voltage referenced termination resistors.

Figure 3–25 shows the total thermal power in Watts and the static power (P_{static}) consumed by the device. The thermal power for each section is also displayed. To see how the thermal power for a section was calculated, click on the section to view the inputs entered for that section.

Figure 3–25. Thermal Power in the PowerPlay Early Power Estimator

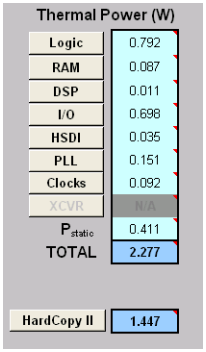


Table 3–12 describes the thermal power parameters in the PowerPlay Early Power Estimator.

Table 3–12. Thermal Power Section Information

Column Heading	Description
Logic	This shows the dynamic power consumed by ALMs and associated routing. Click **Logic** to see details.
RAM	This shows the dynamic power consumed by RAMs blocks and associated routing. Click **RAM** to see details.
DSP	This shows the dynamic power consumed by DSP blocks and associated routing. Click **DSP** to see details.
I/O	This shows the thermal power consumed by I/O pins and associated routing. This includes static power dissipated in terminated I/O standards on chip and stand-by power dissipated in I/O banks. Click **I/O** to see details.
HSDI	This shows the dynamic power consumed by SERDES hardware for high-speed differential I/O. Click **HSDI** to see details.
PLL	This shows the dynamic power consumed by PLLs. Click **PLL** to see details.
Clocks	This shows the dynamic power consumed by clock networks. Click **Clocks** to see details.
XCVR	This shows the thermal power consumed by transceiver hardware. This includes the standby power consumed by unused transceivers. Click **XCVR** to see details. If value equals N/A, then the transceivers are not available for the chosen device.

Table 3–12. Thermal Power Section Information	
Column Heading	**Description**
P_{static}	This shows the static power consumed irrespective of clock frequency. Does not include static I/O current due to termination resistors, which is included in the I/O power above. P_{static} is affected by junction temperature, selected device, and power characteristics.
TOTAL	This shows the total power dissipated as heat from the FPGA. Does not include power dissipated in off-chip termination resistors. See Power Supply Current for current draw from the FPGA supply rails. This may differ due to currents supplied to off-chip components and thus not dissipated as heat in the FPGA.
HardCopy II	This shows the approximate total power for the equivalent HardCopy II device. This field is only available when a Stratix II device is being used. For more information on the HardCopy II device suggested and further power details, click the **HardCopy II** button.

Thermal Analysis

You can choose to enter T_J directly or compute T_J based on information provided. If you choose to enter T_J, select **User Entered T_j** in the Input Parameters section. If you choose to automatically compute T_J, select **Auto Computed T_j** in the Input Parameters section.

When automatically computing T_J, the device's ambient temperature, the airflow, the heat sink solution and the board thermal model are considered to determine the junction temperature (T_J) in degrees Celsius. T_J is the estimated operating junction temperature based on your device and thermal conditions.

The device can be considered a heat source and the junction temperature is the temperature at the device. For simplicity, we can assume that the temperature of the device is constant regardless of where it is being measured. In reality, the temperature varies across the device.

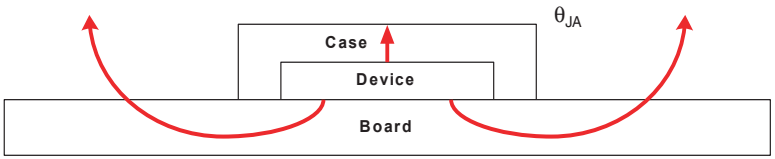
Power can be dissipated from the device through many paths. Different paths become significant depending on the thermal properties of the system. In particular, the significance of power dissipation paths vary depending on whether or not a heat sink is being used for the device.

Not Using a Heat Sink

When a heat sink is not used the major paths of power dissipation are from the device to the air. This can be referred to as a junction-to-ambient thermal resistance (θ_{JA}). In this case there are two significant junction-to-

ambient thermal resistance paths. The first is from the device through the case to the air and the second is from the device through the board to the air. Figure 3–26 shows the thermal representation without a heat sink.

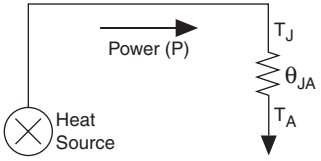
Figure 3–26. Thermal Representation without Heat Sink



Thermal Representation without Heat Sink

In the model used in the PowerPlay Early Power Estimator, power is dissipated through the case and board. Values of θ_{JA} have been calculated for differing air flow options accounting for the paths through the case and through the board. Figure 3–27 shows the thermal model for the PowerPlay Early Power Estimator without a heat sink.

Figure 3–27. Thermal Model in the PowerPlay Early Power Estimator without a Heat Sink



The ambient temperature does not change, but the junction temperature changes depending on the thermal properties. Since a change in junction temperature affects the thermal device properties used to calculate junction temperature, calculating junction temperature is an iterative process.

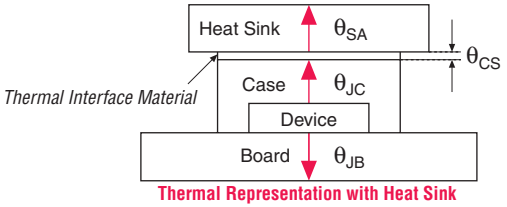
The total power is calculated based on the device resource usage which provide θ_{JA} and the ambient, board and junction temperatures using the following equation:

$$P = (T_J - T_A) / \theta_{JA}$$

Using a Heat Sink

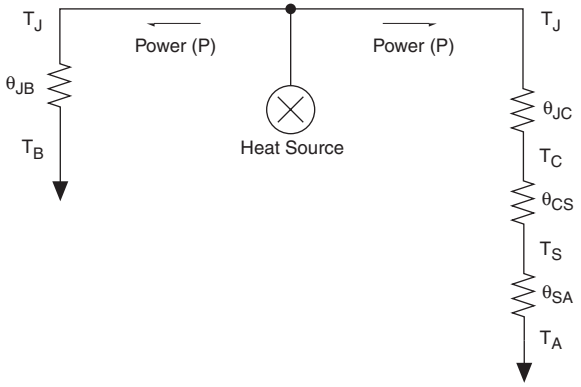
When a heat sink is used the major paths of power dissipation are from the device through the case, thermal interface material, and heat sink. There is also a path of power dissipation through the board. The path through the board has much less impact than the path to air. Figure 3–28 shows the thermal representation with a heat sink.

Figure 3–28. Thermal Representation with Heat Sink



In the model used in the PowerPlay Early Power Estimator, power can be dissipated through the board or through the case and heat sink. The thermal resistance of the path through the board is referred to as the junction-to-board thermal resistance (θ_{JA}). The thermal resistance of the path through the case, thermal interface material and heat sink is referred to as the junction-to-ambient thermal resistance (θ_{JA}). Figure 3–29 shows the thermal model for the PowerPlay Early Power Estimator.

Figure 3–29. Thermal Model for the PowerPlay Early Power Estimator with a Heat Sink



If you want the PowerPlay Early Power Estimator spreadsheet thermal model to take the junction-to-board thermal resistance (θ_{JB}) into consideration, set the Board Thermal Model to either "Typical" or "Custom." A Typical board thermal model sets θ_{JB} to a value based on the package and device selected. If you choose a Custom board thermal model, you must specify a value for θ_{JB}. If you do not want the PowerPlay Early Power Estimator spreadsheet thermal model to take the θ_{JB} resistance into consideration, set the Board Thermal Model to "None (conservative)." In this case, the path through the board is not considered for power dissipation and a more conservative thermal power estimate is obtained.

The junction-to-ambient thermal resistance (θ_{JA}) is determined by the addition of the junction-to-case thermal resistance (θ_{JC}), the case-to-heat sink thermal resistance (θ_{CS}) and the heat sink-to ambient thermal resistance (θ_{SA}).

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

Based on the device, package, airflow, and the heat sink solution selected in the main input parameters, the PowerPlay Early Power Estimator spreadsheet determines the junction-to-ambient thermal resistance (θ_{JA}).

If you are using a low, medium, or high profile heat sink, select the airflow from the options of still air and air flow rates of 100 lfm (0.5 m/s), 200 lfm (1.0 m/s), and 400 lfm (2.0 m/s). If you are using a custom heat sink, enter the heat sink-to-ambient thermal resistance (θ_{SA}). The airflow should also be incorporated into θ_{SA}. Therefore, the Airflow parameter is not applicable in this case. Obtain these values from the heat sink manufacturer.

The ambient temperature does not change, but the junction temperature changes depending on the thermal properties. Since a change in junction temperature affects the thermal device properties used to calculate junction temperature, calculating junction temperature is an iterative process.

The total power is calculated based on the device resource usage which provide θ_{JA}, θ_{JB}, and the ambient, board and junction temperature using the following equation:

$$P = \frac{(T_J - T_A)}{\theta_{JA}} + \frac{(T_J - T_B)}{\theta_{JB}}$$

Figure 3–30 shows the thermal analysis, including the junction temperature (T_J), total θ_{JA}, θ_{JB}, and the maximum allowed T_A values. For details on the values of the thermal parameters not listed, click the **Details…** button.

Figure 3–30. Thermal Analysis in the PowerPlay Early Power Estimator

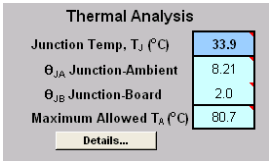


Table 3–13 describes the thermal analysis parameters in the PowerPlay Early Power Estimator.

Table 3–13. Thermal Analysis Section Information

Column Heading	Description
Junction Temp, T_J (°C)	This shows the device junction temperature estimated based on supplied thermal parameters. The junction temperature is determined by dissipating the total thermal power through the top of the chip and through the board (if selected). See **Details…** for detailed calculations used.
θ_{JA} Junction-Ambient	This shows the junction-to-ambient thermal resistance between the device and ambient air, in °C/W. This represents the increase in temperature between ambient and junction for every Watt of additional power dissipation.
θ_{JB} Junction-Board	This shows the junction-to-board thermal resistance, in °C/W. This is used in conjunction with the board temperature, as well as the top-of-chip θ_{JA} and ambient temperatures, to compute junction temperature.
Maximum Allowed T_A (°C)	This shows a guideline for the maximum ambient temperature (in °C) that the device can be subjected to without violating maximum junction temperature, based on the supplied cooling solution and device temperature grade.

Power Supply Current (A)

The power supply current provides the estimated current consumption for power supplies. The I_{CCINT} current is the supply current required from V_{CCINT}. The I_{CCPD} current is the supply current required from V_{CCPD}. The total I_{CCIO} current is the supply current required from V_{CCIO} for all I/O banks. For estimates of I_{CCIO} based on I/O banks, refer to the **I/O** section

of the PowerPlay Early Power Estimator. The total I_{CCXCVR} current is the supply current required from all the transceiver-specific power rails: V_{CCT}, V_{CCH}, V_{CCR}, V_{CCA}, V_{CCP}, and V_{CCL}. For estimates of I_{CCXCVR} based on power rails, refer to "Transceiver (XCVR)" on page 3–33.

Figure 3–31 shows the power supply current estimation. I_{CCINT}, I_{CCPD}, I_{CCIO} and I_{CCXCVR} are displayed.

Figure 3–31. Power Supply Current in the PowerPlay Early Power Estimator

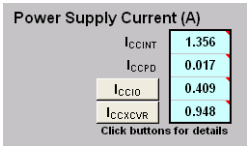


Table 3–14 describes the parameters in the Power Supply Current parameters of the PowerPlay Early Power Estimator.

Table 3–14. Power Supply Current Information

Column Heading	Description
I_{CCINT}	This shows the total current drawn from the I_{CCINT} supply (in A).
I_{CCPD}	This shows the total current drawn from the pre-drive (I_{CCPD}) supply (in A).
I_{CCIO}	This shows the total current drawn from the I_{CCIO} power rail(s). See the **I/O** sheet for details on the current drawn from each I/O rail. I_{CCIO} includes any current drawn through the I/O into off-chip termination resistors. This can result in I_{CC}IO values that are higher than the reported I/O thermal power, since this off-chip current is dissipated as heat elsewhere and does not factor into the calculation of device temperature.
I_{CCXCVR}	This shows the total current drawn from the I_{CCXCVR} rail(s). See the *XCVR* sheet for details on the current drawn from each XCVR rail.

Factors Affecting PowerPlay Early Power Estimator Spreadsheet Accuracy

There are many factors that greatly affect the estimated values displayed in the PowerPlay Early Power Estimator. In particular, it is imperative to determine whether or not the input parameters entered are accurate to ensure that the system is modeled correctly in the PowerPlay Early Power Estimator spreadsheet. In particular, information entered concerning toggle rates, airflow, temperature and heat sinks are extremely important.

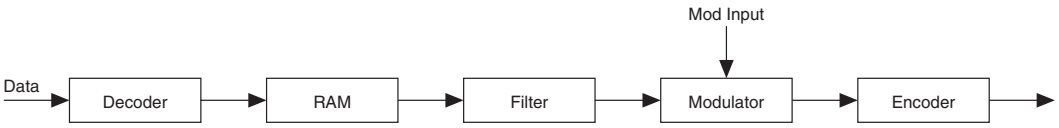
Toggle Rate

The toggle rates specified in the PowerPlay Early Power Estimator spreadsheet can have a very large impact on the dynamic power consumption displayed. In order to obtain an accurate estimate it is imperative to input toggle rates that are realistic. Determining realistic toggle rates is a non-trivial problem that requires the designer to know what kind of input the FPGA is receiving and how often it toggles.

If the design is not yet complete, it is very difficult to get an accurate estimate. The best way to approach the problem is to isolate the separate modules in the design by functionality and estimate resource usage along with toggle rates of the resources. The easiest way to accomplish this is to leverage previous designs to estimate toggle rates for modules with similar functionality.

As an example, let us assume that there is a simple design that has an input data bus that has been encoded for data transmission and has a roughly 50% toggle rate. It then goes through a decoder and is stored in RAM. The data is then filtered before being modulated with another input data bus and the result is encoded for transmission. A simple block diagram is shown in Figure 3–32.

Figure 3–32. Decoder & Encoder Block Diagram



In this case the designer would have to estimate the following:

- Data toggle rate
- Mod input toggle rate
- Resource estimate for Decoder module
- Resource estimate for RAM
- Resource estimate for Filter
- Resource estimate for Modulator
- Resource estimate for Encoder

- Toggle rate for Decoder module
- Toggle rate for RAM
- Toggle rate for Filter
- Toggle rate for Modulator
- Toggle rate for Encoder

These estimates can be done in many ways. If similar modules were used in the past with data inputs of roughly the same toggle rate, that information can be leveraged. If there are MATLAB simulations available for some blocks toggle rate information can be obtained. If the HDL is available for some of the modules they can be simulated.

If the HDL is complete, the best way to determine toggle rate is to simulate the design. The accuracy of toggle rate estimates depends heavily on the accuracy of the input vectors. Therefore, determining whether or not the simulation coverage is high gives you a good estimate of how accurate the toggle rate information is.

The Quartus II software can determine toggle rates of each resource used in the design if information from simulation tools is provided. Designs can be simulated in many different tools and information provided for the Quartus II software through a Signal Activity File (SAF). The Quartus II PowerPlay Power Analyzer provides the most accurate power estimate. The CSV output file from Quartus II can be used with the PowerPlay Early Power Estimator spreadsheet for estimating power after the design.

Airflow

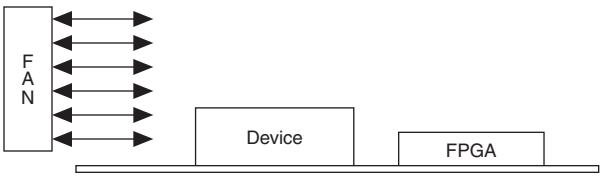
The PowerPlay Early Power Estimator spreadsheet allows the designer to specify the airflow present at the device. This value affects thermal analysis and bears directly on the power consumed by the device. To obtain an accurate estimate it is imperative to correctly determine the airflow at the FPGA, not the output of the fan providing the airflow.

Often it is difficult to place the device adjacent to the fan providing the airflow. As such, the path of the airflow is likely to traverse a length on the board before reaching the device, thus diminishing the actual airflow the device sees. In the example shown in Figure 3–33, a fan is placed at the end of the board. The airflow at the FPGA is weaker than what it is at the fan.

Figure 3–33. Airflow & FPGA Position

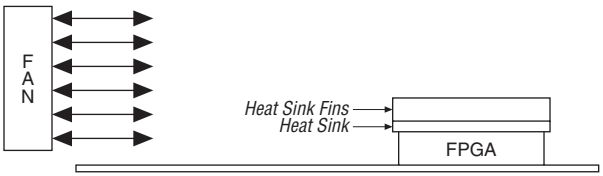
In many cases, it is also necessary to take into consideration blocked airflow. In the example below, there is a device blocking the airflow from the FPGA significantly reducing the airflow seen at the FPGA. Also, the airflow from the fan often cools board components and other devices before reaching the FPGA (Figure 3–34).

Figure 3–34. Airflow with Component & FPGA Positions



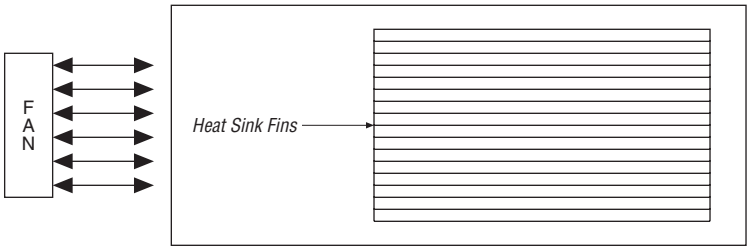
If a custom heat sink is being used, there is no need to enter the airflow directly into the PowerPlay Early Power Estimator spreadsheet but it is required to compute the θ_{SA} for the heat sink with the knowledge of what the airflow is at the device. Most heat sinks have fins located above the heat sink to facilitate airflow. Figure 3–35 shows the case of an FPGA with a heat sink.

Figure 3–35. AirFlow & Heat Sinks



When placing the heat sink on the FPGA, it is imperative that the direction of the fins correspond with the direction of the airflow. A top view shows the correct orientation of the fins (Figure 3–36).

Figure 3–36. Heat Sink (Top View)



The considerations above can heavily influence the airflow seen at the device. When entering information into the PowerPlay Early Power Estimator spreadsheet, it is necessary to consider these implications in order to get an accurate airflow value. It is the designer's responsibility to determine the actual airflow at the FPGA and correctly input this value into the PowerPlay Early Power Estimator spreadsheet.

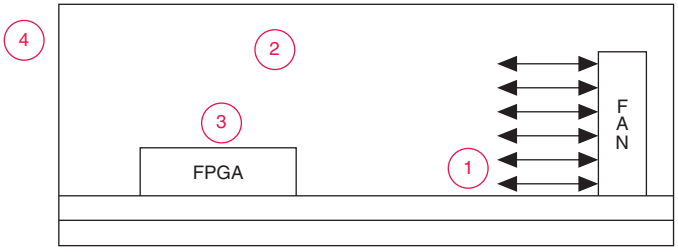
Temperature

The PowerPlay Early Power Estimator spreadsheet requires you to enter the ambient air temperature for the device in order to calculate the device thermal information correctly. Ambient temperature refers to the temperature of the air around the device. This is almost always much higher than the ambient temperature outside of the system. To get an accurate representation of ambient temperature for the device, the temperature must be measured as close to the device as possible. This can be done with a thermocouple.

Entering the incorrect ambient air temperature could drastically alter the power estimates in the PowerPlay Early Power Estimator spreadsheet. The figure below illustrates a simple system with the FPGA housed in a box.

In this case, the temperature is very different at each of the numbered locations illustrated in Figure 3–37.

Figure 3–37. Temperature Variances



For example, location 3 is where the ambient temperature pertaining to the device should be obtained for input into the PowerPlay Early Power Estimator spreadsheet. Points 1 and 2 are cooler than location 3; location 4 is likely close to 25 degrees C. Temperatures close to devices in a system are often around 50-60 degrees but the values can vary significantly. In order to obtain accurate power estimates from the PowerPlay Early Power Estimator spreadsheet, it is very important to get a realistic estimate of the ambient temperature near the FPGA device.

Heat Sink

When using a heat sink, the power is determined by the following equations.

$$(T_J - T_A) / \theta_{JA} = P$$

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

The value θ_{JC} is specific to the FPGA and can be obtained from the data sheet. The value θ_{CS} refers to the material that binds the heat sink to the FPGA and is approximated to be 0.1 C/W. The value θ_{SA} is obtained from the manufacturer of the heat sink. It is important to ensure that when this value is obtained that it is for the right conditions for the FPGA which include analyzing the correct heat sink information at the appropriate airflow at the device.

For more information on how to determine heat sink information refer to *AN 358: Thermal Management for 90-nm FPGAs* and www.altera.com.