Altera Phase-Locked Loop (ALTERA_PLL) Megafunction User Guide

UG-01087-1.1 User Guide

This user guide describes the features and behavior of the ALTERA_PLL megafunction that you can configure through the parameter editor in the Quartus® II software.

This user guide assumes that you are familiar with megafunctions and how to create them. If you are unfamiliar with Altera megafunctions or the MegaWizard Plug-In Manager, refer to the *Megafunction Overview User Guide*.

The Quartus II software provides the ALTERA_PLL parameter editor to specify the phase-locked loop (PLL) circuitry in the supported devices. When configured, the ALTERA_PLL instantiates the generic PLL, which creates a simple migration path from previous PLL architectures to future architectures and allows placement flexibility between different PLL types.

Features

This section describes the features available for configuration in the ALTERA_PLL megafunction.

- Supports five different clock feedback modes: direct, external feedback, normal, source synchronous, and zero delay buffer mode. For more information, refer to "Operation Modes" on page 5.
- Generates as many as 18 clock output signals. For more information, refer to "Output Clocks" on page 6.

Device Family Support

The ALTERA_PLL megafunction supports the Stratix® V device family.

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Parameter Settings

The ALTERA_PLL parameter editor appears in the I/O category of the MegaWizard Plug-In Manager. This section describes the parameters available to configure the ALTERA_PLL megafunction for your application.

Table 1 describes the parameters of the ALTERA_PLL megafunction.

Table 1. ALTERA_PLL Megafunction Parameters (Part 1 of 2)

Parameter	Legal Values	Description
Device Speed Grade	2, 3, or 4	Specifies the speed grade for a device. The lower the number, the faster the speed grade.
PLL Mode	Integer-N PLL or Fractional-N PLL	Specifies the mode used for the ALTERA_PLL megafunction. If the selection is omitted, the default is **Integer-N PLL**.
Reference Clock Frequency	—	Specifies the input frequency for the input clock, `refclk`, in MHz. The default value is 100.0 MHz. The minimum and maximum value is dependent on the device used. The PLL reads only the numerals in the first six decimal places.
Channel Spacing	—	Specifies the fractional frequencies, in kHz, to the phase frequency detector. The default value is 0.0 kHz. This parameter is available only if you set the PLL mode to **Fractional-N PLL**.
Operation Mode	direct, external feedback, normal, source synchronous, or zero delay buffer	Specifies the operation of the PLL. If the selection is omitted, the default is **direct**. ■ In **direct** mode, the PLL minimizes the length of the feedback path to produce the smallest possible jitter at the PLL output. The internal-clock and external-clock outputs of the PLL are phase-shifted with respect to the PLL clock input. In this mode, the PLL does not compensate for any clock networks. ■ In **external feedback** mode, you must connect the `fbclk` input port to an input pin, and a board-level connection must connect both the input pin and external clock output port, `fboutclk`. The `fbclk` port is aligned with the input clock. ■ In **normal** mode, the PLL compensates for the delay of the internal clock network used by the clock output. If the PLL is also used to drive an external clock output pin, a corresponding phase shift of the signal on the output pin results. ■ In **source-synchronous** mode, the clock delay from pin to I/O input register matches the data delay from pin to I/O input register. ■ In **zero-delay buffer** mode, the PLL must feed an external clock output pin and compensate for the delay introduced by that pin. The signal observed on the pin is synchronized to the input clock. The PLL clock output connects to the `altbidir` port and drives `zdbfbclk` as an output port. If the PLL also drives the internal clock network, a corresponding phase shift of that network results. Note that for direct, normal, and source-synchronous modes, the ALTERA_PLL megafunction makes the assignments in the Quartus II IP File (**.qip**) file based on the compensation mode that you have selected.
Enable Locked Output Port	On or Off	Turn on this parameter to enable the `locked` port. The default setting is on.

Table 1. ALTERA_PLL Megafunction Parameters (Part 2 of 2)

Parameter	Legal Values	Description
Check Actual Value	On or Off	Turn on this parameter to enable actual value checking of the reference clock frequency and each of the output clock frequencies. Turn on this parameter after you have completed specifying all the requested settings.
Number of Clocks	1 to 18	Specifies the number of output clocks required in the ALTERA_PLL design. The requested settings for output frequency, phase shift, and duty cycle are shown based on the number of clocks selected.
Frequency	—	Specifies the output frequency of the corresponding output clock port, `outclk[]` in MHz. The default value is 100.0 MHz. The minimum and maximum values depend on the device used. The PLL only reads the numerals in the first six decimal places. When you turn on the **Check Actual Value** option, the parameter editor produces a warning message if the requested settings for one of the output clocks cannot be approximated.
Phase Shift	—	Specifies the phase shift for the corresponding output clock port, `outclk[]`, in picoseconds (ps). If omitted, the default value is 0 ps.
Duty Cycle	1 to 99	Specifies the duty cycle in percentage for the corresponding output clock port, `outclk[]`. If omitted, the default value is 50.

Functional Description

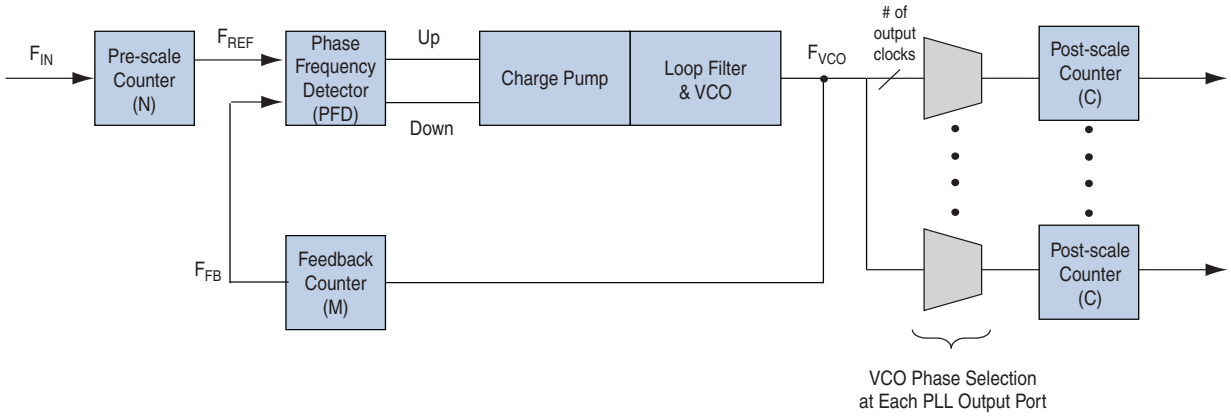
A PLL is a frequency-control system that generates an output clock by synchronizing itself to an input clock. The PLL compares the phase difference between the input signal and the output signal of a voltage-controlled oscillator (VCO) and then performs phase synchronization to maintain a constant phase angle (lock) on the frequency of the input or reference signal. The synchronization or negative feedback loop of the system forces the PLL to be phase-locked.

You can configure PLLs as frequency multipliers, dividers, demodulators, tracking generators, or clock recovery circuits. You can use PLLs to generate stable frequencies, recover signals from a noisy communication channel, or distribute clock signals throughout your design.

Building Blocks of a PLL

This section describes the basic building blocks of a PLL and common terms to describe PLL behaviors. The main blocks of the PLL are the phase frequency detector (PFD), charge pump, loop filter, voltage controlled oscillator (VCO), and counters, such as a feedback counter (M), a pre-scale counter (N), and post-scale counters(C). The PLL architecture depends on the device you use in your design. The block diagram in Figure 1 shows and describes a typical PLL architecture.

Figure 1. Typical PLL Block Diagram



The following terms are commonly used to describe the behavior of a PLL:

- **PLL lock time**—also known as the PLL acquisition time, PLL lock time is the amount of time required by the PLL to attain the target frequency and phase relationship after power-up, after a programmed output frequency change, or after a reset of the PLL.

  Simulation software does not model a realistic PLL lock time. Simulation shows an unrealistically fast lock time. For the actual lock time specification, refer to the device datasheet.

- **PLL resolution**—the minimum frequency increment value of a PLL VCO. The value is based on the number of bits in the M and N counter.
- **PLL sample rate**—the F_{REF} sampling frequency required to perform the phase and frequency correction in the PLL. The PLL sample rate is f_{REF} /N.

The following sections describe the PLL lock, operation modes, and features available for configuration in the ALTERA_PLL megafunction.

For more information about the PLL building blocks, refer to the Phase-Locked Loop Basics, PLL page of the Altera website.

PLL Lock

The PLL lock is dependent on the two inputs signals in the phase frequency detector. The lock signal is an asynchronous output of the PLLs.

The number of cycles required to gate the lock signal depends on the PLL input clock which clocks the gated-lock circuitry. Divide the maximum lock time of the PLL by the period of the PLL input clock to calculate the number of clock cycles required to gate the lock signal.

For more information about the maximum lock time for the PLL, refer to the *DC and Switching Characteristics for Stratix V Devices* chapter in volume 3 of the *Stratix V Device Handbook*.

Operation Modes

The ALTERA_PLL megafunction supports five different clock feedback modes. Each mode allows clock multiplication and division, phase shifting, and duty-cycle programming.

The following list describes the operation modes for the ALTERA_PLL megafunction:

- **Direct mode**—the PLL minimizes the length of the feedback path to produce the smallest possible jitter at the PLL output. In this mode, the PLL does not compensate for any clock networks.
- **External Feedback mode**—the PLL compensates for the `fbclk` feedback input to the PLL, thus minimizing the delay between the input clock pin and the feedback clock pin.
- **Normal mode**—the PLL feedback path source is a global or regional clock network, minimizing clock delay to registers for that clock type and specific PLL output. You can specify PLL output that is compensated.
- **Source-Synchronous mode**—the data and clock signals arrive at the same time at the input pins. In this mode, the signals are guaranteed to have the same phase relationship at the clock and data ports of any Input Output Enable (IOE) register.
- **Zero-Delay Buffer mode**—the PLL feedback path is confined to the dedicated PLL external output pin. The clock port driven off-chip is phase aligned with the clock input for a minimal delay between the clock input and the external clock output.

For detailed information about the PLL operation modes, refer to the *Clock Networks and PLLs in Stratix V Devices* chapter in volume 1 of the *Stratix V Device Handbook*.

Output Clocks

The ALTERA_PLL megafunction can generate as many as 18 clock output signals. The generated clock output signals clock the core or external blocks outside the core.

You can use the `reset` signal to reset the output clock value to 0 and disable the PLL output clocks.

For more information about clock networks in Stratix V devices, refer to the *Clock Networks and PLLs in Stratix V Devices* chapter in volume 1 of the *Stratix V Device Handbook*.

Each output clock has a set of requested settings where you can specify the value of output frequency, phase shift, and duty cycle. The requested settings are the settings that you want to implement in your design.

To check whether the requested settings comply with the actual values to be implemented in the PLL circuit, in the **General** tab, turn on **Check Actual Value**. The actual frequency is the closest frequency setting (best approximate of the requested settings) that can be implemented in the PLL circuit. Use the values shown in the **Info Message** column as a guide for you to adjust the requested settings.

You have to specify all the requested settings before turning on **Check Actual Value**.

Ports

This section describes the ports available in the ALTERA_PLL megafunction.

Figure 2 shows the top-level ports of the ALTERA_PLL megafunction.

Figure 2. ALTERA_PLL Ports

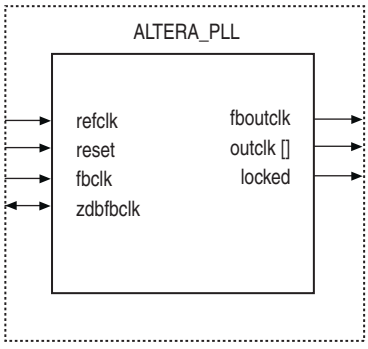


Table 2 describes the input and output ports of the ALTERA_PLL megafunction block.

Table 2. ALTERA_PLL Megafunction Ports

Port Name	Type	Condition	Description
fbclk	Input	Optional	The external feedback input port for the PLL. The megafunction creates this port when the PLL is operating in external feedback mode or zero-delay buffer mode. To complete the feedback loop, a board-level connection must connect the fbclk port and the external clock output port of the PLL.
fboutclk	Output	Optional	The port that feeds the fbclk port through the mimic circuitry. The fboutclk port is available only if the PLL is in external feedback mode.
locked	Output	Optional	The megafunction drives this port high when the PLL acquires lock. The port remains high as long as the PLL is locked. The PLL asserts the locked port when the phases and frequencies of the reference clock and feedback clock are the same or within the lock circuit tolerance. When the difference between the two clock signals exceeds the lock circuit tolerance, the PLL loses lock.
outclk[]	Output	Required	The clock output of the PLL. The frequency of the output clock depends on the parameter settings.
refclk	Input	Required	The reference clock that drives the clock network.
reset	Input	Required	The synchronized reset port for the output clocks. Drive this port high to reset all output clocks to the initial value of 0.
zdbfbclk	Bidirectional	Optional	The bidirectional port that connects to the mimic circuitry. This port must connect to a bidirectional pin that is placed on the positive feedback dedicated output pin of the PLL. The zdbfbclk port is available only if the PLL is in zero-delay buffer mode.

Document Revision History

Table 3 shows the revision history for this document.

Table 3. Document Revision History

Date	Version	Changes
January 2011	1.1	■ Added two new parameters in Table 1. ■ Updated Figure 2.
July 2010	1.0	Initial release.