ALTDQ_DQS2 Megafunction

User Guide

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UG-01089-1.0

Document last updated for Altera Complete Design Suite version: 10.0
Document publication date: September 2010

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1. About This Megafunction

This user guide describes the features of the ALTDQ_DQS2 megafunction that you can configure through the MegaWizard™ interface in the Quartus® II software.

The ALTDQ_DQS2 megafunction controls the double data rate (DDR) I/O elements (IOEs) for the data (DQ) and data strobe (DQS) signals in Stratix® V devices. A DQ group consists of six I/Os that share a common interface circuitry. Typically, one I/O is assigned to the DQS, one I/O is assigned to the complementary DQS, and four I/Os are assigned to the DQs.

This user guide assumes that you are familiar with megafunction and how to create them. If you are unfamiliar with Altera megafunctions or the MegaWizard interface, refer to the *Megafunction Overview User Guide*.

Features

The ALTDQ_DQS2 megafunction provides the following features:

- Access to dynamic on-chip termination (OCT) controls to switch between parallel termination during reads to series termination during writes.
- High-performance support for DDR interface standards
- 4- to 36-bit programmable DQ group widths
- Half-rate registers to enable successful data transfers between the I/O registers and the core logic
- Access to I/O delay chains to fine-tune delays on the data or strobe signals

Device Support

The ALTDQ_DQS2 megafunction supports Stratix V devices only.

Resource Utilization and Performance

For details about the resource usage and performance of your design, refer to the compilation reports in the Quartus II software.

To view the compilation reports in the Quartus II software, follow these steps:

1. On the Processing menu, click **Start Compilation** to run a full compilation.
2. After compiling the design, on the Processing menu, click **Compilation Report**.
3. In the Table of Contents browser, expand the **Fitter** folder by clicking the "+" icon.
4. Under **Fitter**, expand **Resource section**, and select **Resource Usage Summary** to view the resource usage information.
5. Under **Fitter**, expand **Resource section**, and select **Resource Utilization by Entity** to view the resource utilization information.

2. Parameter Settings

This section describes the parameter settings for the ALTDQ_DQS2 megafunction.

You can parameterize the megafunction using the MegaWizard Plug-In Manager or the command-line interface (CLI). Altera recommends that you configure the megafunction using the MegaWizard Plug-In Manager.

Expert users may choose to instantiate and parameterize the megafunction using the `ip-generate` command through the CLI. This method requires command-line scripting knowledge.

For more information about using the `ip-generate` command, refer to "IP-Generate Command" on page A–1.

Table 2–1 lists the MegaWizard and CLI parameter settings for the ALTDQ_DQS2 megafunction.

All CLI parameter values listed in Table 2–1 are type string, therefore you must enclose the values in double quotes.

Table 2–1. ALTDQ_DQS2 Parameter Settings (Part 1 of 3)

MegaWizard Parameter		CLI Parameter		Description
Name	Legal Values	Name	Legal Values	
General Settings Section				
Pin Width	**1** to **36**	`pin_width`	`1` to `36`	Specifies the number of DQ pins. The default value is **9** (`9`).
Pin Type	**input, output, bidirectional**	`pin_type`	`input,output, bidir`	Specifies the type of DQ pins. The default value is **bidirectional** (`bidir`).
Extra output-only pins	**0** to **36**	`extra_output_ width`	`0` to `36`	Specifies the number of additional output-only DQ pins. The default value is **0** (`0`).
Memory frequency	**200–600**	`input_freq`	`200–600`	Specifies the full-rate frequency of the incoming DQS signal from the external device in MHz. The default value is **300** MHz (`300`).
Use dynamic configuration scan chains	—	`use_dynamic_config`	`true ,false`	Specifies whether to allow run-time configuration of multiple delay chains, phase shifts, and transfer registers. This option is disabled by default.

Table 2–1. ALTDQ_DQS2 Parameter Settings (Part 2 of 3)

MegaWizard Parameter		CLI Parameter		Description
Name	**Legal Values**	**Name**	**Legal Values**	
Output Path Section				
Use half-rate output path	—	`half_rate_output`	`true ,false`	Specifies whether to double the width of the data bus on the FPGA side, and clock the FPGA side interface using the half-rate clock. If this option is enabled, you must drive the `hr_clock_in` port with the half-rate clock signal. This option is enabled by default.
Use output phase alignment blocks	—	`use_output_phase_alignment`	`true ,false`	Specifies whether to allow phase shift on the output path based on the delay settings from the DLL. This option is disabled by default.
Capture Strobe Section				
Capture strobe type	**Single**, **Differential**, **Complimentary**	`capture_strobe_type`	`single`, `differential`, `complimentary`	Specifies the type of capture strobe (DQS signal from the external device). The default value is **Single** (`single`).
Use inverted capture strobe	—	`invert_capture_strobe`	`true, false`	Specifies whether to capture data with an inverted capture strobe. This option is disabled by default.
DQS phase shift	**0**, **45**, **90**, **135**,**180** degrees	`dqs_phase_setting`	`0, 1, 2, 3, 4`	Specifies the phase shift value for the DQS delay chain to shift the incoming strobe within the data valid window during read and write operations. The default value is **90** degrees (`2`).
Use capture strobe enable block	—	`use_dqs_enable`	`true, false`	Specifies whether to use the capture strobe enable block, which allows control over the preamble state of the capture strobe. This option is disabled by default.
DQS enable phase setting	**0**, **45**, **90**, **135** degrees	`dqs_enable_phase_setting`	`0, 1, 2, 3`	Specifies the value of phase shift to shift the full-rate clock signal that drives the capture strobe enable block. The default value is **0** degrees (`0`).

Table 2–1. ALTDQ_DQS2 Parameter Settings (Part 3 of 3)

MegaWizard Parameter		CLI Parameter		Description
Name	Legal Values	Name	Legal Values	
Generate output strobe	—	use_output_strobe	true, false	Specifies whether to generate an output strobe signal based on the OE signal and the full-rate clock. This option is enabled by default.
Bidirectional capture strobe	—	use_bidir_strobe	true, false	Specifies whether to turn on a bidirectional capture strobe (capture strobe and output strobe is on the same port). This option is disabled by default.
Differential/ complimentary output strobe	—	differential_ output_strobe	true, false	Specifies whether to turn on a differential or complimentary output strobe. This option is disabled by default.

ALTDQ_DQS2 Datapaths

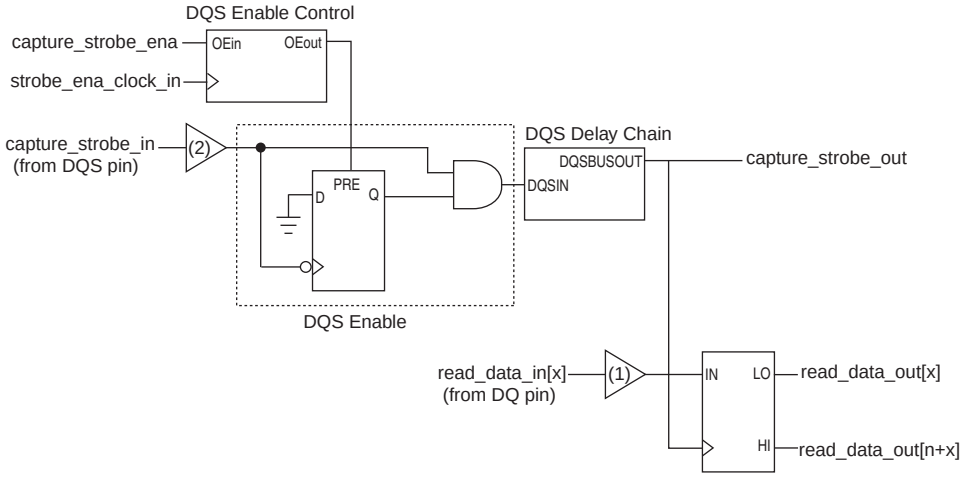
This section describes the read and write datapaths and how other megafunctions are used with the ALTDQ_DQS2 megafunction.

DQ and DQS Input Path

The DQ and DQS input path receives the DQ and DQS signal from the external device during read operations.

Figure 3–1 shows the input path where n = the number of DQ pins and x = 0 to (n-1).

Figure 3–1. DQ and DQS Input Path



Notes to Figure 3–1:

(1) For bidirectional DQ, the input of the buffer connects to the `read_write_data_io[x]` port.

(2) For bidirectional DQS, the input of the buffer connects to the `strobe_io` port.

Table 3–1 lists the blocks in the DQ and DQS input path.

Table 3–1. DQ and DQS input Path (Part 1 of 2)

Block name	Description
DQS enable	Represents the AND-gate control on the DQS input that grounds the DQS input strobe when the strobe goes to Z after a DDR read postamble. The DQS enable block enables the registers to allow enough time for the DQS delay settings to travel from the DQS phase-shift circuitry or core logic to all the DQS logic blocks before the next change. For more information about the DQS enable block, refer to "Update Enable Circuitry" in the *External Memory Interfaces in Stratix V Devices* chapter of the *Stratix V Device Handbook*.

Table 3–1. DQ and DQS input Path (Part 2 of 2)

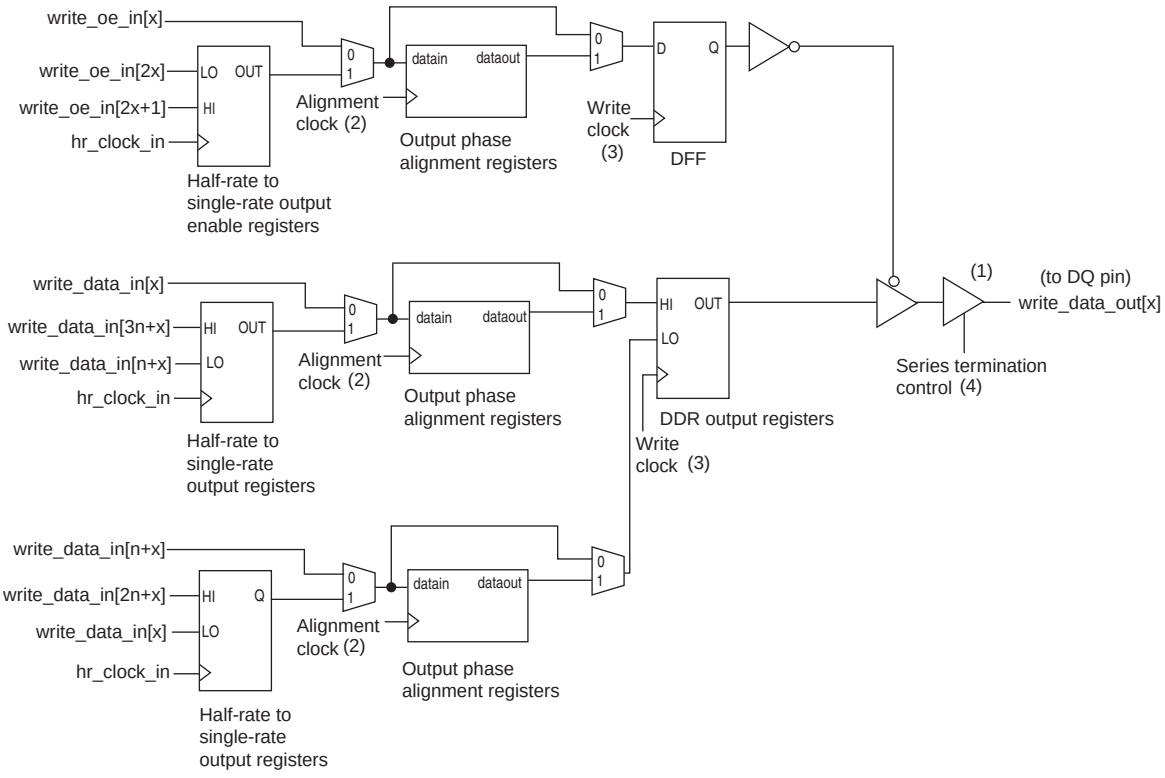
Block name	Description
DQS enable control	Represents the circuitry that controls the DQS enable block. A DQS enable control block controls each DQS enable block. For more information about the DQS enable control, refer to "DQS Postamble Circuitry" in the *External Memory Interfaces in Stratix V Devices* chapter of the *Stratix V Device Handbook*.
DQS delay chain	Represents the delay chains that delay signals. For more information about the DQS delay chain block, refer to "DQS Delay Chain" in the *External Memory Interfaces in Stratix V Devices* chapter of the *Stratix V Device Handbook*.

DQ Output Path

The DQ output path sends the DQ signal to the external device during write operations.

Figure 3–2 shows the output path where n = the number of DQ pins and x = 0 to (n-1).

Figure 3–2. DQ Output Path

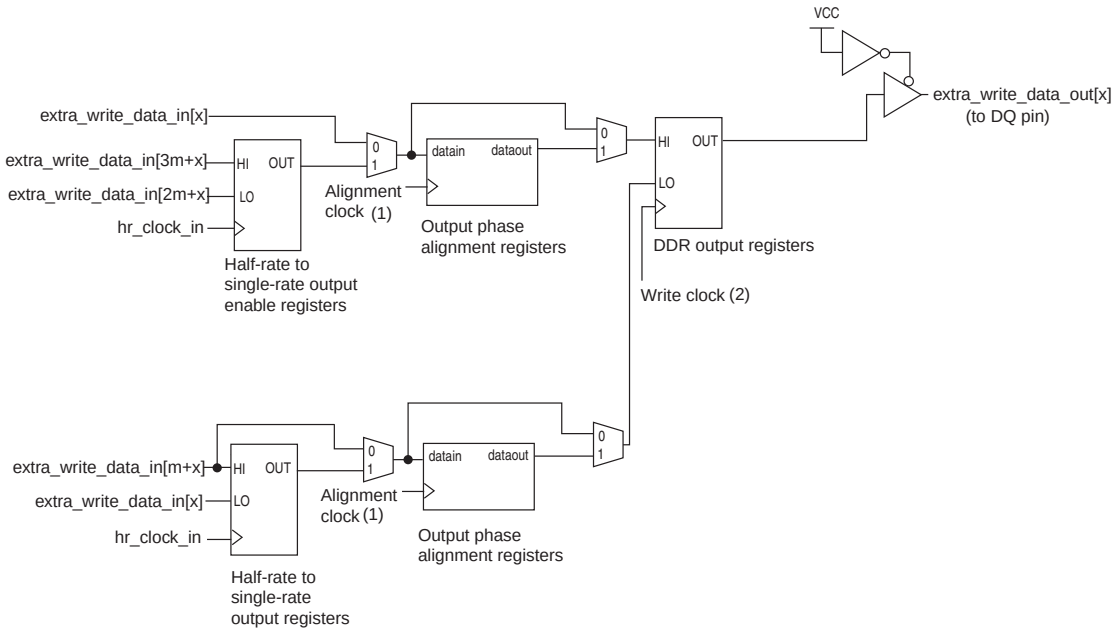


Notes to Figure 3–2:

(1) For bidirectional DQ, the output of the buffer connects to there `read_write_data_io[x]` port.
(2) The alignment clock comes from the write-leveling delay chains
(3) The write clock comes from the PLL or the write-leveling delay chains
(4) The series termination control connects to the ALTOCT megafunction.

Figure 3–3 shows the DQ output path for additional DQ pins usage, where *m*= the number of DQ pins and *y* = 0 to (*m*-1).

Figure 3–3. DQ Output Path (for Additional DQ Pins Usage)



Notes to Figure 3–3:

(1) The alignment clock comes from the write-leveling delay chains.

(2) The write clock comes from the PLL or the write-leveling delay chains.

Table 3–2 lists the blocks in the DQ output path.

Table 3–2. DQ Output Path

Block name	Description
Half-rate to single-rate output enable registers	Represents a group of registers that convert half-rate data to single-rate data.
Output phase alignment registers	Represents the circuitry required to phase shift the DQ-output signals. Use this block for write-leveling purposes in DDR3 SDRAM interfaces.
DDR output registers	Represents the DDIO registers that transfer DDR signals from the core to the DQ/DQS pins.

For more information about how the input and output paths are mapped to the device IOEs, refer to "I/O Element Registers" in the *External Memory Interfaces in Stratix V Devices* chapter of the *Stratix V Device Handbook*.

Connect the ALTDQ_DQS2 megafunction to the ALTOCT, ALTDLL, and ALTERA_PLL megafunctions to utilize their features.

The following list describes how the ALTOCT, ALTDLL, and ALTERA_PLL megafunctions are used with the ALTDQ_DQS2 megafunction:

- ALTDLL—The ALTDLL megafunction instantiates a delay-locked loop (DLL) circuit in your design. The DLL circuit represents the specialized phase-shift reference circuit for calibrating the delay settings of the DQS delay chains, allowing the delay chains to compensate for PVT variations. The DLL uses a reference clock at the same frequency as the input DQS signal to compute the amount of delay required at each DQS pin on the FPGA to perform the phase-shift.

  For more information about DLL in Stratix V devices, refer to the *DQS Phase-Shift Circuitry* section in the *External Memory Interfaces in Stratix V Devices* chapter of the *Stratix V Device Handbook*.

  For more information about the ALTDLL megafunction, refer to the *ALTDLL and ALTDQ_DQS Megafunction User Guide*.

- ALTERA_PLL—The ALTERA_PLL megafunction instantiates a phase-locked loop (PLL) circuit in your design. The PLL generates the related clock signals that are used by the IOEs.

  For more information about the Stratix V PLL, refer to the *Clock Networks and PLLs in Stratix V Devices* chapter of the *Stratix V Device Handbook*.

  For more information about the ALTERA_PLL megafunction, refer to the *Altera Phase-Locked Loop (ALTERA_PLL) Megafunction User Guide*.

- ALTOCT—The ALTOCT megafunction instantiates an on-chip termination (OCT) calibration block in your design. The block provides dynamic OCT control for I/O impedance matching and termination. The OCT maintains signal quality, saves board space, and reduces external component costs.

  For more information about dynamic OCT control, refer to the *Dynamic On-Chip Termination Control* section in the *External Memory Interfaces in Stratix V Devices* chapter of the *Stratix V Device Handbook*.

  For more information about the ALTOCT megafunction, refer to the *Dynamic Calibrated On-Chip Termination (ALTOCT) Megafunction User Guide*.

ALTDQ_DQS2 Ports

This section describes the ports of the ALTDQ_DQS2 megafunction.

Figure 3–4 shows the ports of the megafunction.

Figure 3–4. ALTDQ_DQS2 Block Diagram

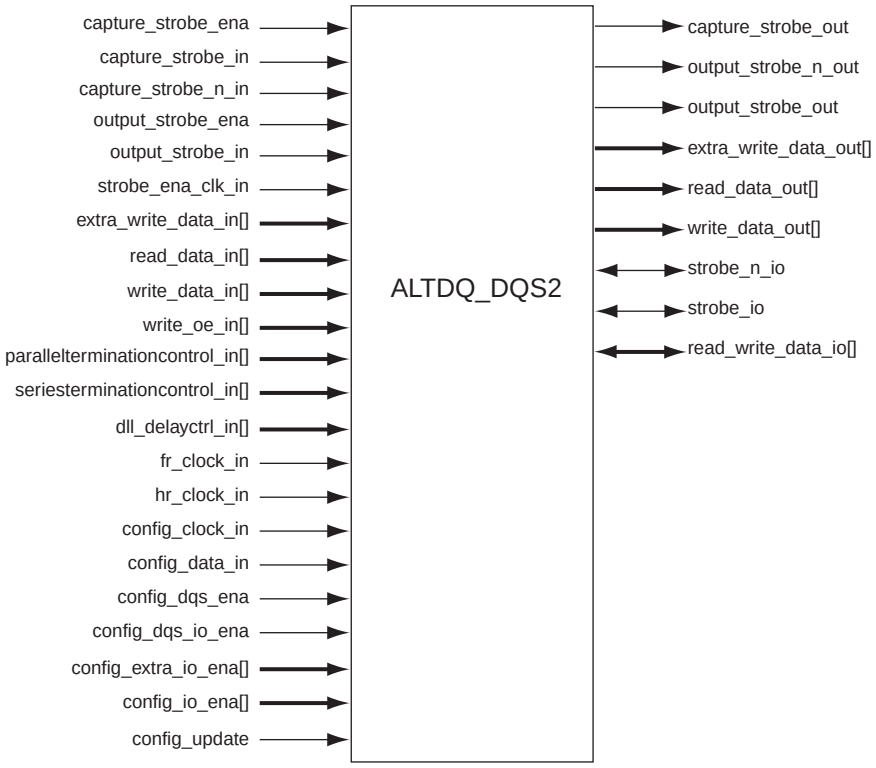


Table 3–3 lists the ALTDQ_DQS2 megafunction data strobe ports.

Table 3–3. ALTDQ_DQS2 Megafunction Data Strobe Ports (Part 1 of 2)

Port Name	Type	Width	Description
capture_strobe_ena	Input	1	Controls the DQS enable control block—Acts as the output enable signal for signals coming from the input registers (capture_strobe_in port) to reach the DQS delay chain block.
capture_strobe_in	Input	1	Receives the clock signal from the external device . For example, a DQS signal from the external memory.
capture_strobe_n_in	Input	1	Receives the negative polarity clock signal from the external device. For example, a DQSn signal from the external memory. This port is available when the capture strobe type is set to differential or complimentary.
capture_strobe_out	Output	1	Sends the delayed clock signal to the core. For example, a delayed DQS signal from the DQS delay chain.
output_strobe_ena	Input	1	The output enable signal for the output_strobe_out port.
output_strobe_in	Input	1	Receives the clock signal from the core. For example, a DQS signal from the core.

Table 3–3. ALTDQ_DQS2 Megafunction Data Strobe Ports (Part 2 of 2)

Port Name	Type	Width	Description
output_strobe_out	Output	1	Sends clock signal to the external device. For example, a DQS signal to the external memory.
output_strobe_n_out	Output	1	Sends the negative polarity clock signal to the external device (For example, DQSn signal to the external memory). This port is available when you set the output strobe type to differential or complimentary.
strobe_ena_clk_in	Input	1	Receives the clock signal from the clock pin or the PLL to clock the DQS enable control block.
strobe_io	Bidirectional	1	Sends and receives the bidirectional clock signal.
strobe_n_io	Bidirectional	1	Sends and receives the negative polarity clock signal for differential or complimentary strobe configuration.

Table 3–4 lists the ALTDQ_DQS2 megafunction data ports where *n*= number of DQ pins, *m*= number of additional output-only DQ pins, *x* = 0 to (*n*-1), and y= 0 to (m-1).

Table 3–4. ALTDQ_DQS2 Megafunction Data Ports (Part 1 of 2)

Port Name	Type	Width *(1)*	Description
extra_write_data_in[]	Input	Full-rate = 2*m* Half-rate = 4*m*	Receives data signal from the core. This port connects to the input port of the half-rate data to single-rate data output registers block (Figure 3–3 on page 3–3). In full-rate mode, only the extra_write_data_in[y] and extra_write_data_in[m+y] ports are used.
extra_write_data_out[]	Output	*m*	Sends data to the external device. This port connects to the output port of the output buffer (Figure 3–3 on page 3–3).
read_data_in[]	Input	*n*	Receives data from the external device. This port connects to the input port of the input buffer located between the DQ pin and the DDR input registers block. This is an input-only DQ port that receives data from the external device to the core. This port connects to the input port of the input buffer located between the DQ-pin and the DDR input registers block (Figure 3–1 on page 3–1).
read_data_out[]	Output	2*n*	Sends the captured data from the external device to the core. This port connects to the output port of the DDR input register block (Figure 3–1 on page 3–1). The read_data_out[x] port outputs the positive-edge triggered data, and the read_data_out[n+x] port outputs the negative-edge triggered data.
read_write_data_io[]	Bidirectional	*n*	Receives and sends data between the core and the external device. You must assign the bidirectional DQ port with the Output Termination and Input Termination assignments.

Table 3–4. ALTDQ_DQS2 Megafunction Data Ports (Part 2 of 2)

Port Name	Type	Width *(1)*	Description
write_data_in[]	Input	Full-rate = 2*n* Half-rate = 4*n*	Receives DDR data signal from the core to be sent out to the external device. For example, data to be written to the external memory during write operation. This port connects to the input port of the half-rate data to single-rate data output registers block (Figure 3–2 on page 3–2). In full-rate mode, the megafunction uses only the write_data_in[x] and write_data_in[n+x] ports.
write_data_out[]	Input	*n*	Sends the DDR data signal to the external device. For example, data to be written to the external memory during write operation. This port connects to the output port of the output buffer located between the DDR output registers block and the DQ-out pin (Figure 3–2 on page 3–2).
write_oe_in[]	Input	Full-rate = *n* Half-rate = 2*n*	Receives the output enable signal from the core to control the output buffer. For example, output enable control when writing data to the external memory during write operation. This port connects to the input port of the half-rate data to single-rate data output-enable registers block (Figure 3–2 on page 3–2). In full-rate mode, the megafunction uses only the write_oe_in[x] port.

Note to Table 3–4:
(1) The port width applies to full-rate mode, unless otherwise specified.

To understand how these ports connect to the IOEs, refer to "I/O Elements" in the *External Memory Interfaces in Stratix V Devices* chapter of the *Stratix V Device Handbook*.

Table 3–5 lists the terminal control ports.

Table 3–5. ALTDQ_DQS2 Megafunction Temination Control Ports

Port name	Type	Width	Description
parallelterminationcontrol_in[]	Input	16	Controls the calibrated parallel termination ports of the input buffers. You must connect this port to the parallelterminationcontrol[15:0] port of the ALTOCT megafunction. Ensure that the termination block located in the ALTOCT instance is assigned with the termination control block assignment.
seriesterminationcontrol_in[]	Input	16	Controls the calibrated series termination ports of the output buffers. You must connect this port to the seriesterminationcontrol[15:0] port of the ALTOCT megafunction. Ensure that the termination block located in the ALTOCT instance is assigned with the termination control block assignment.

For more information about dynamic OCT control in Stratix V devices, refer to the *DC and Switching Characteristics for Stratix V Devices* chapter in volume 3 of the *Stratix V Device Handbook*.

Table 3–6 lists the PLL and DLL ports.

Table 3–6. PLL and DLL Ports

Port name	Type	Width	Description
dll_delayctrl_in[]	Input	7	Receives the 7-bit delay settings from the dll_delayctrlout port of the ALTDLL megafunction instance. This 7-bit signal controls delay through the DQS delay chains. Compilation error occurs if this port is not connected to a DLL.
fr_clock_in	Input	1	Receives the full-rate clock signal from a clock pin, or the PLL clock output port.
hr_clock_in	Input	1	Receives the half-rate clock signal from a clock pin, or the PLL clock output port.

For more information about DLL in Stratix V device, refer to "Delay-Locked Loop" in the *External Memory Interfaces in Stratix V Devices* chapter of the *Stratix V Device Handbook*.

For more information about PLL in Stratix V devices, refer to "PLL Specifications" in *DC and Switching Characteristics for Stratix V Devices* chapter of the *Stratix V Device Handbook*.

The I/O and DQS configuration blocks represent a set of serial-to-parallel shift registers that dynamically changes the settings of various device configuration bits. The I/O and DQS configuration blocks shift a serial configuration data stream into the shift registers, and then load the data stream into the configuration registers. The shift registers power-up low. Every I/O pin contains an I/O configuration block. Every DQS group contains a DQS configuration block and an I/O configuration block.

Table 3–7 lists the dynamic configuration ports where *n*= number of DQ pins and *m*= number of additional DQ pins.

Table 3–7. ALTDQ_DQS2 Megafunction Dynamic Configuration Ports

Port name	Type	Width	Description
config_clock_in	Input	1	Receives the clock signal to clock all dynamic configuration blocks. You can connect this port to a clock pin, or the PLL clock output port.
config_data_in	Input	1	Receives the serial configuration data stream that shifts into the serial-to-parallel shift registers.
config_dqs_ena	Input	1	Receives the clock enable signal for the DQS configuration block.
config_dqs_io_ena	Input	1	Receives the clock enable signal for the DQS I/O configuration block.
config_extra_io_ena[]	Input	*m*	Receives the clock enable signal for the additional I/O configuration block.
config_io_ena[]	Input	*n*	Receives the clock enable signal for the I/O configuration block.
config_update	Input	1	Receives the signal to load the bits from the serial-to-parallel shift registers to the configuration registers.

For more information about the dynamic configuration blocks in Stratix V device, refer to "I/O Configuration Block and DQS Configuration Block" in the *External Memory Interfaces in Stratix V Devices* chapter of the *Stratix V Device Handbook*.

A. IP-Generate Command

This section describes how you can use the `ip-generate` command to create custom variations of the ALTDQ_DQS2 megafunction.

Using IP-Generate Command

You can use **ip-generate.exe**, a command-line executable, to configure parameters. The command creates or modifies custom megafunction variations, which you can then instantiate in a design file.

To run the `ip-generate` command, follow these steps:

1. The **ip-generate.exe** executable file is located in the <*quartus_install_dir*>**quartus****sopc_builder****bin**\ directory. Ensure that you include the directory path into your operating system environment.
2. To obtain the options for the `ip-generate` command, type the following command in the command prompt:

   ```
   ip-generate –help
   ```

3. To instantiate the megafunction using the executable file, type the following syntax:

   ```
   ip-generate --component-name=altdq_dqs2 --component-system-
   param=DEVICE_FAMILY="Stratix V" --file-set=QUARTUS_SYNTH --output-
   name[=<file_name>] --component-
   param[=<parameter_name>][=<parameter_value>]
   ```

   The <*file_name*> is the instance name. For example, `my_dqdqs2`. The <*parameter_name*> is the name of the parameter that you configure with the value stated in <*parameter_value*>.

You must use the `--component-param[=<parameter_name>][=<parameter_value>]` option for every parameter assignment. Parameters that are not assigned take the default values. Ensure that you type the exact case and spaces for the parameter names and values.

The following list describes two examples of how you can use this command:

- To create an ALTDQ_DQS2 instance named `my_dqdqs2` with all the default parameter values, type the following command:

  ```
  ip-generate --component-name=altdq_dqs2 --component-system-param=DEVICE_FAMILY="Stratix V" --output-name=my_dqdqs2 --file-set=QUARTUS_SYNTH
  ```

- To create an ALTDQ_DQS2 instance named `mydq_dqs2` without output strobe ports, and with a 135 degrees DQS phase shift, type the following command:

  ```
  ip-generate --component-name=altdq_dqs2 --component-system-param=DEVICE_FAMILY="Stratix V" --output-name=my_dqdqs2 --file-set=QUARTUS_SYNTH --component-param=USE_OUTPUT_STROBE="False" --component-param=DQS_PHASE_SETTING="3"
  ```

  This command generates two files—**my_dqdqs2.v** and **my_dqdqs2_altdq_dqs2.sv**. The **my_dqdqs2.v** file contains the `my_dqdqs2` top-level module, and the **my_dqdqs2_altdq_dqs2.sv** file contains the source code. Both files are in Verilog HDL format.

  The `ip-generate` command generates the ports for the instance based on the parameter values.

For more information about the ports, refer to the "ALTDQ_DQS2 Ports" on page 3–5.

For more information about the parameters, refer to the "Parameter Settings" on page 2–1.

Document Revision History

Table A–1 lists the revision history for this document.

Table A–1. Document Revision History

Date	Version	Changes
September 2010	1.0	Initial release.