



# **100G Development Kit, Stratix V GX Edition**

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## **User Guide**



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The Altera® Stratix® V GX 100G Development Kit is a complete design environment that includes both the hardware and software you need to develop Stratix V GX FPGA designs. The following list describes what you can accomplish with the kit:

- Develop and test designs to interface with a variety of different optical modules.
- Develop and test Interlaken designs.
- Develop and test memory subsystems consisting of DDR3 or QDR II memory.
- Build designs capable of migrating to Altera's HardCopy® IV ASICs.

## Kit Features

This section briefly describes the Stratix V GX 100G Development Kit contents.

### Hardware

The Stratix V GX 100G Development Kit includes the following hardware:

- Stratix V GX 100G development board—A development platform that allows you to develop and prototype hardware designs running on the Stratix V GX FPGA.



For detailed information about the board components and interfaces, refer to the *100G Development Kit, Stratix V GX Edition Reference Manual*.

- CFP loopback board
- One SFP loopback module
- QSFP loopback module
- Two Interlaken loopback boards
- Heatsink and fan
- Power supply and cables—The kit includes the following items:
  - Power supply and AC adapters for North America/Japan, Europe, and the United Kingdom
  - Ethernet and USB cables



If using the optic modules (CFP, SFP, QSFP) you must set the user switch SW4.7 to enabled (1) to turn on the laser. When done using the optic modules, set SW4.7 to disabled (0).

### Software

The software for this kit, described in the following sections, is available on the Altera website for immediate downloading. You can also request to have Altera mail the software to you on DVDs.

## Quartus II Software

Your kit includes a license for the Development Kit Edition (DKE) of the Quartus II software (Windows platform only). For one year, this license entitles you to most of the features of the Subscription Edition (excluding the IP Base Suite).



After the year, your DKE license will no longer be valid and you will not be permitted to use this version of the Quartus II software. To continue using the Quartus II software, you should download the free Quartus II Web edition or purchase a subscription to Quartus II software. For more information, refer to the [Design Software](#) page of the Altera website.

The Quartus II Development Kit Edition (DKE) software includes the following items:

- Quartus II Software—The Quartus II software, including the Qsys system integration tool, provides a comprehensive environment for network on a chip (NoC) design. The Quartus II software integrates into nearly any design environment and provides interfaces to industry-standard EDA tools.
- MegaCore® IP Library—A library that contains Altera IP MegaCore functions. You can evaluate MegaCore functions by using the OpenCore Plus feature to do the following:
  - Simulate behavior of a MegaCore function within your system.
  - Verify functionality of your design, and quickly and easily evaluate its size and speed.
  - Generate time-limited device programming files for designs that include MegaCore functions.
  - Program a device and verify your design in hardware.



The OpenCore Plus hardware evaluation feature is an evaluation tool for prototyping only. You must purchase a license to use a MegaCore function in production.



For more information about OpenCore Plus, refer to [AN 320: OpenCore Plus Evaluation of Megafunctions](#).

- Nios® II Embedded Design Suite (EDS)—A full-featured set of tools that allows you to develop embedded software for the Nios II processor which you can include in your Altera FPGA designs.

## Stratix V GX 100G Development Kit Installer

The license-free Stratix V GX 100G Development Kit installer includes all the documentation and design examples for the kit.

For information on installing the Development Kit Installer, refer to [“Software Installation” on page 3-1](#).

### Introduction

The remaining chapters in this user guide lead you through the following Stratix V GX 100G development board setup steps:

- Inspecting the contents of the kit
- Installing the design and kit software
- Setting up, powering up, and verifying correct operation of the 100G development board
- Configuring the Stratix V GX FPGA
- Running the Board Test System designs



For complete information about the 100G development board, refer to the [100G Development Kit, Stratix V GX Edition Reference Manual](#).

### Before You Begin

Before using the kit or installing the software, check the kit contents and inspect the boards to verify that you received all of the items listed in “[Kit Features](#)” on page 1–1. If any of the items are missing, contact Altera before you proceed.

### Inspect the Boards

To inspect each board, perform the following steps:

1. Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment.



Without proper anti-static handling, you can damage the board.

2. Verify that all components are on the board and appear intact.

### References

Use the following links to check the Altera website for other related information:

- For the latest board design files and reference designs, refer to the [100G Development Kit, Stratix V GX](#) page.
- For additional daughter cards available for purchase, refer to the [Development Board Daughtercards](#) page.
- For the Stratix V GX device documentation, refer to the [Literature: Stratix V Devices](#) page.
- To purchase devices from the eStore, refer to the [Devices](#) page.
- For Stratix V GX OrCAD symbols, refer to the [Capture CIS Symbols](#) page.

- For Nios II 32-bit embedded processor solutions, refer to the [Embedded Processing](#) page.

This chapter explains how to install the following software:

- Quartus II Subscription Edition Software
- Stratix V GX 100G Development Kit
- USB-Blaster™ II driver

### Installing the Quartus II Subscription Edition Software

The Quartus II Subscription Edition Software provides the necessary tools for developing hardware and software for Altera devices. Included in the Quartus II Subscription Edition Software are the Quartus II software, the Nios II EDS, and the MegaCore IP Library. The Quartus II software (including SOPC Builder) and the Nios II EDS are the primary FPGA development tools used to create the reference designs in this kit. To install the Altera development tools, perform the following steps:

1. Download the Quartus II Subscription Edition Software from the [Quartus II Subscription Edition Software](#) page of the Altera website. Alternatively, you can request a DVD from the [Altera IP and Software DVD Request Form](#) page of the Altera website.
2. Follow the on-screen instructions to complete the installation process.



If you have difficulty installing the Quartus II software, refer to [Altera Software Installation and Licensing Manual](#).

### Licensing Considerations


Purchasing this kit entitles you to a one-year license for the Development Kit Edition (DKE) of the Quartus II software.

After the year, your DKE license will no longer be valid and you will not be permitted to use this version of the Quartus II software. To continue using the Quartus II software, you should download the free Quartus II Web edition or purchase a subscription to Quartus II software.

Before using the Quartus II software, you must activate your license, identify specific users and computers, and obtain and install a license file.

If you already have a licensed version of the subscription edition, you can use that license file with this kit. If not, you need to obtain and install a license file. To begin, go to the [Self Service Licensing Center](#) page of the Altera website, log into or create your myAltera account, and take the following actions:


1. On the [Activate Products](#) page, enter the serial number provided with your development kit in the **License Activation Code** box.

 Your serial number is printed on the development kit box below the bottom bar code. The number is 10 or 11 alphanumeric characters and does not contain hyphens. [Figure 3-1](#) shows *3S150SPXXXX* as an example serial number.

**Figure 3-1. Locating Your Serial Number**



2. Consult the Activate Products table, to determine how to proceed.
  - a. If the administrator listed for your product is someone other than you, skip the remaining steps and contact your administrator to become a licensed user.
  - b. If the administrator listed for your product is you, proceed to step 3.
  - c. If the administrator listed for your product is *Stocking*, activate the product, making you the administrator, and proceed to step 3.
3. Use the [Create New License](#) page to license your product for a specific user (you) on specific computers. The [Manage Computers](#) and [Manage Users](#) pages allow you to add users and computers not already present in the licensing system.

 To license the Quartus II software, you need your computer's network interface card (NIC) ID, a number that uniquely identifies your computer. On the computer you use to run the Quartus II software, type `ipconfig /all` at a command prompt to determine the NIC ID. Your NIC ID is the 12-digit hexadecimal number on the **Physical Address** line.

4. When licensing is complete, Altera emails a **license.dat** file to you. Store the file on your computer and use the **License Setup** page of the **Options** dialog box in the Quartus\_II software to enable the software.

 For complete licensing details, refer to [Altera Software Installation and Licensing Manual](#).

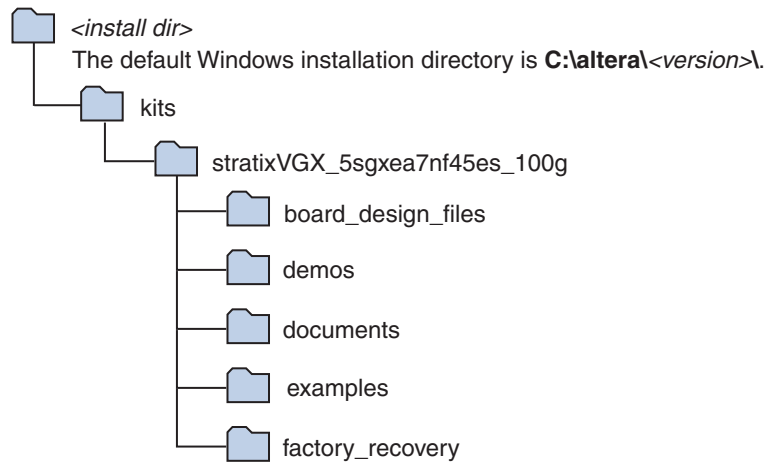
## Installing the Stratix V GX 100G Development Kit

To install the Stratix V GX 100G Development Kit, perform the following steps:

1. Download the Stratix V GX 100G Development Kit installer from the [100G Development Kit, Stratix V GX](#) page of the Altera website. Alternatively, you can request a development kit DVD from the [Altera Kit Installations DVD Request Form](#) page of the Altera website.
2. Run the Stratix V GX 100G Development Kit installer you acquired in “Software” on page 1-1.
3. Follow the on-screen instructions to complete the installation process. Be sure that the installation directory you choose is in the same relative location to the Quartus II software installation.

The installation program creates the Stratix V GX 100G Development Kit directory structure shown in [Figure 3-2](#).

**Figure 3-2. Stratix V GX 100G Development Kit Installed Directory Structure <sup>(1)</sup>**



**Note to Figure 3-2:**

(1) Early-release versions might have slightly different directory names.



[Table 3-1](#) lists the file directory names and a description of their contents.

**Table 3-1. Installed Directory Contents**

Directory Name	Description of Contents
<b>board_design_files</b>	Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design.
<b>demos</b>	Contains demonstration applications.
<b>documents</b>	Contains the kit documentation.
<b>examples</b>	Contains the sample design files for the Stratix V GX 100G Development Kit.
<b>factory_recovery</b>	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

## Installing the USB-Blaster II Driver

The Stratix V GX 100G development board includes integrated USB-Blaster II circuitry for FPGA programming. However, for the host computer and board to communicate, you must install the USB-Blaster driver II on the host computer.

-  Installation instructions for the USB-Blaster II driver for your operating system are available on the Altera website. On the [Altera Programming Cable Driver Information](#) page of the Altera website, locate the table entry for your configuration and click the link to access the instructions.
-  For USB-Blaster II configuration details, refer to the [On-Board USB-Blaster II](#) page.

This chapter explains how to set up the Stratix V GX 100G development board.

### Setting Up the Board

To prepare and apply power to the board, perform the following steps:

1. The Stratix V GX 100G development board ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be currently configured with the default settings, follow the instructions in [“Factory Default Switch Settings” on page 4-2](#) to return the board to its factory settings before proceeding.
2. The 100G development board ships with design examples stored in the flash memory device.
3. Connect the +19 V, 120 W to the DC Power Jack (J1) on the FPGA board and plug the cord into a power outlet.



Use only the supplied power supply. Power regulation circuitry on the board can be damaged by power supplies with greater voltage.

4. Set the POWER switch (SW1) to the on position. When power is supplied to the board, blue LED (D1) illuminates indicating that the board has power.

The MAX II device on the board contains (among other things) a parallel flash loader (PFL) megafunction. When the board powers up, the PFL reads a design from flash memory and configures the FPGA. Pressing the PGM\_SEL (S8) push-button loads the design into the FPGA from flash using the PFL in the MAX II device.

When configuration is complete, the MAX\_CONF\_DN LED (D25) illuminates, signaling that the Stratix V GX device configured successfully.



The kit includes a MAX II design which contains the MAX II PFL megafunction. The design resides in the `<install dir>\kits\stratixVGX_5sgxea7nf45es_100g\examples\max2` directory.

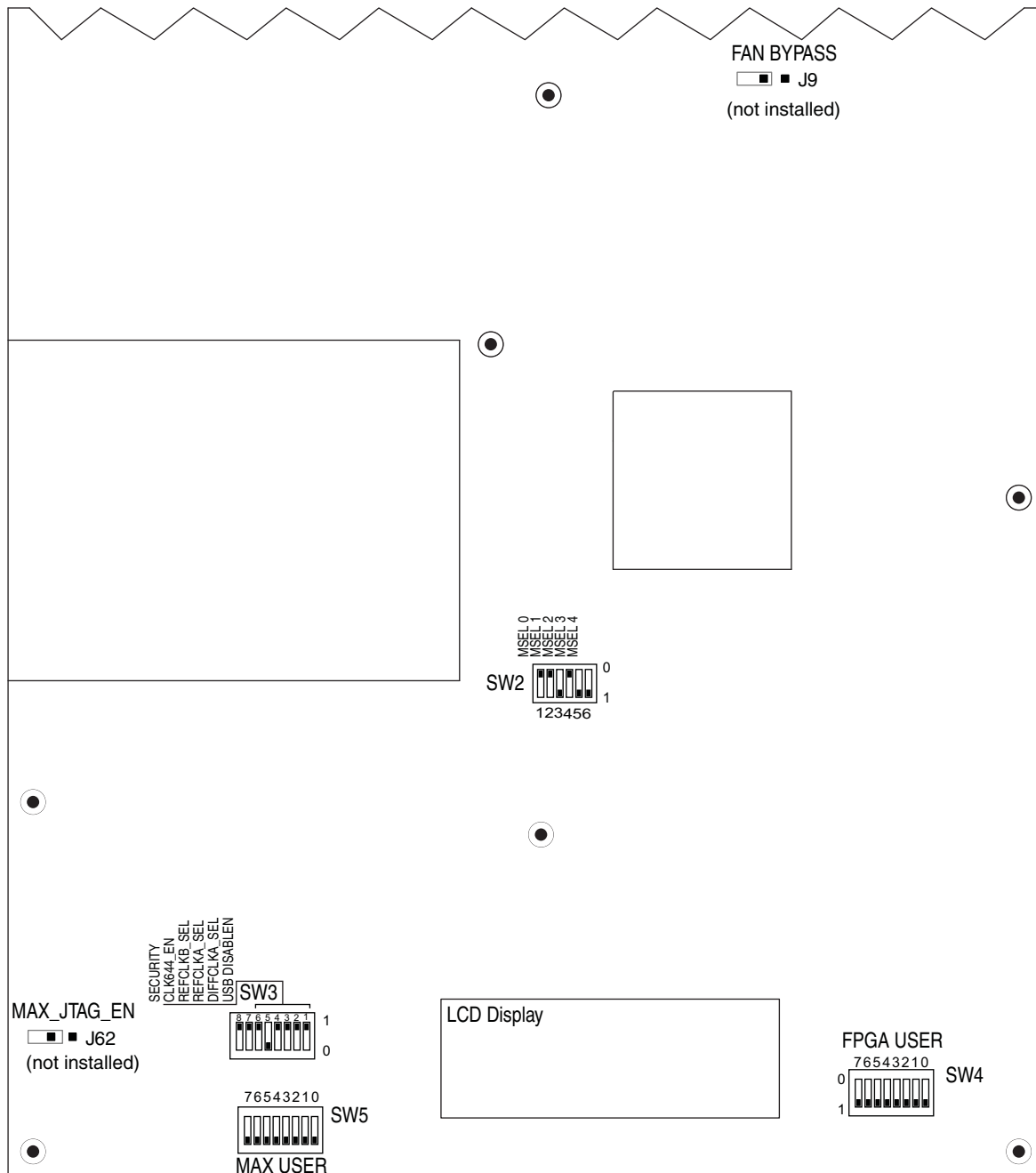


For more information about the PFL megafunction, refer to [AN 386: Parallel Flash Loader Megafunction User Guide](#).

## Factory Default Switch Settings

This section shows the factory switch settings for the Stratix V GX 100G development board. [Figure 4-1](#) shows the switch locations and the default position of each switch.

**Figure 4-1. Switch Locations and Default Settings**



To restore the switches to their factory default settings, perform the following steps:

1. Set DIP switch bank (SW2) to match [Table 4–1](#) and [Figure 4–1](#).

**Table 4–1. SW2 Dip Switch Settings**

Switch	Board Label	Function	Default Position
0	MSEL 0	Switch 0 has the following options: ■ Open = Logic 1 ■ Closed = Logic 0	Closed
1	MSEL 1	Switch 1 has the following options: ■ Open = Logic 1 ■ Closed = Logic 0	Closed
2	MSEL 2	Switch 2 has the following options: ■ Open = Logic 1 ■ Closed = Logic 0	Open
3	MSEL 3	Switch 4 has the following options: ■ Open = Logic 1 ■ Closed = Logic 0	Closed
4	MSEL 4	Switch 4 has the following options: ■ Open = Logic 1 ■ Closed = Logic 0	Open
5	—	Switch 4 has the following options: ■ Open = Logic 1 ■ Closed = Logic 0	Closed

2. Set DIP switch bank (SW3) to match [Table 4–2](#) and [Figure 4–1](#).

**Table 4–2. SW3 DIP Switch Settings (Part 1 of 2)**

Switch	Board Label	Function	Default Position
1	USB_DISABLEN	Switch 4 has the following options: ■ When off (1), USB is enabled. ■ When on (0), USB is disabled.	1
2	DIFFCLKA_SEL	Switch 4 has the following options: ■ When off (1), SMA is selected. ■ When on (0), PLL is selected.	1
3	REFCLKA_SEL	Switch 3 has the following options: ■ When off (1), SMA is selected. ■ When on (0), PLL is selected.	1
4	DIFFCLKB_SEL	Switch 4 has the following options: ■ When off (1), SMA is selected. ■ When on (0), PLL is selected.	1

**Table 4–2. SW3 DIP Switch Settings (Part 2 of 2)**

Switch	Board Label	Function	Default Position
5	REFCLKB_SEL	Switch 5 has the following options: <ul style="list-style-type: none"> <li>■ When on (1), the SMA is selected.</li> <li>■ When off (0), the PLL is selected.</li> </ul>	0
6	CLK_644_EN	Switch 6 has the following options: <ul style="list-style-type: none"> <li>■ When on (1), 644-MHz clock is enabled.</li> <li>■ When off (0), 644-MHz clock is disabled.</li> </ul>	1
7	SECURITY	Switch 7 has the following options: <ul style="list-style-type: none"> <li>■ When on (1), configuration security is enabled.</li> <li>■ When off (0), configuration security is disabled.</li> </ul> When enabled, the FPGA cannot be accessed via JTAG if the device has already been programmed by the PFL.	1
8	—	—	—

3. Set jumper blocks (J9, J62) to match [Table 4–3](#) and [Figure 4–1](#).

**Table 4–3. Jumper Settings**

Board Reference	Description	Shunt Position
J9	Fan Bypass — Shunt installed forces the fan to ON and at full speed.	Not Installed
J62	MAX_JTAG_EN (logic 1) — Shunt installed removes MAX II from JTAG chain.	Not Installed

 For more information about the FPGA board settings, refer to the *100G Development Kit, Stratix V GX Edition Reference Manual*.

The Stratix V GX 100G Development Kit ships with the Board Update Portal design example stored in the factory portion of the flash memory on the board. The design consists of a Nios II embedded processor, an Ethernet MAC, and an HTML web server.

When you power up the board, the FPGA configures with the Board Update Portal design example from flash memory. The design can obtain an IP address from any DHCP server and serve a web page from the flash on your board to any host computer on the same network. The web page allows you to upload new FPGA designs to the user hardware 1 portion of flash memory, and provides links to useful information on the Altera website, including kit-specific links and design resources.

The source code for the Board Update Portal design resides in the `<install dir>\kits\stratixVGX_5sgxea7nf45es_100g\examples` directory. If the Board Update Portal is corrupted or deleted from the flash memory, refer to [“Restoring the Flash Device to the Factory Settings” on page A-4](#) to restore the board with its original factory contents.

### Connecting to the Board Update Portal Web Page

This section provides instructions to connect to the Board Update Portal web page.



Before you proceed, ensure that you have the following:

- A PC with a connection to a working Ethernet port on a DHCP enabled network.
- A separate working Ethernet port connected to the same network for the board.
- The Ethernet and power cables that are included in the kit.

To connect to the Board Update Portal web page, perform these steps:

1. Attach the Ethernet cable from the board to your LAN.
2. Power up the board. The board connects to the LAN's gateway router, and obtains an IP address. The LCD on the board displays the IP address.
3. Launch a web browser on a PC that is connected to the same network, and enter the IP address from the LCD into the browser address bar. The Board Update Portal web page appears in the browser.



You can click **Stratix V GX 100G Development Kit** on the Board Update Portal web page to access the kit's home page for documentation updates and additional new designs.



You can also navigate directly to the [100G Development Kit, Stratix V GX](#) page of the Altera website to determine if you have the latest kit software.

## Using the Board Update Portal to Update User Designs

The Board Update Portal allows you to write new designs to the user hardware 1 portion of flash memory. Designs must be in the Nios II Flash Programmer File (.flash) format.



Design files available from the [100G Development Kit, Stratix V GX](#) page include .flash files. You can also create .flash files from your own custom design. Refer to [“Preparing Design Files for Flash Programming” on page A-2](#) for information about preparing your own design for upload.

To upload a design over the network into the user portion of flash memory on your board, perform the following steps:

1. Perform the steps in [“Connecting to the Board Update Portal Web Page”](#) to access the Board Update Portal web page.
2. In the **Hardware File Name** field specify the .flash file that you either downloaded from the Altera website or created on your own. If there is a software component to the design, specify it in the same manner using the **Software File Name** field, otherwise leave the **Software File Name** field blank.
3. Click **Upload**.
4. To configure the FPGA with the new user design after the flash memory upload process is complete, press PGM\_SEL (S8) until POF 1 LED (D34) illuminates, and then press LOAD (S5) to configure the user hardware portion of flash memory.



As long as you don't overwrite the factory image in the flash memory device, you can continue to use the Board Update Portal to write new designs to the user hardware 1 portion of flash memory. If you do overwrite the factory image, you can restore it by following the instructions in [“Restoring the Flash Device to the Factory Settings” on page A-4](#).

The kit includes a design example and an application called the Board Test System to test the functionality of the Stratix V GX 100G development board. The application provides an easy-to-use interface to alter functional settings and observe the results. You can use the application to test board components, modify functional parameters, observe performance, and measure power usage. (While using the application, you reconfigure the FPGA several times with test designs specific to the functionality you are testing.) The application is also useful as a reference for designing systems. To install the application, follow the steps in [“Installing the Stratix V GX 100G Development Kit”](#) on page 3–3.

The Board Test System GUI communicates over the JTAG bus to a test design running in the Stratix V GX device.

Several designs are provided to test the major board features. Each design provides data for one or more tabs in the application. The Configure menu identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, the appropriate tab appears and allows you to exercise the related board features. Highlights appear in the board picture around the corresponding components.

### Preparing the Board

With the power to the board off, following these steps:

1. Connect the USB cable to the board.
2. Ensure that the development board switches and jumpers are set to the default positions as shown in the [“Factory Default Switch Settings”](#) section starting on page 4–2.



For more information about the board’s DIP switch and jumper settings, refer to the [100G Development Kit, Stratix V GX Edition Reference Manual](#).

3. Turn the power to the board on. The board loads the design stored in the user hardware 1 portion of flash memory into the FPGA. If your board is still in the factory configuration or if you have downloaded a newer version of the Board Test System to flash memory through the Board Update Portal, the design loads the GPIO and flash memory tests.



To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The application cannot run correctly unless the USB cable is attached and the board is on.

### Running the Board Test System

To run the application, navigate to the `<install_dir>\kits\stratixVGX_5sgxea7nf45es_100g\examples\board_test_system` directory and run the **BoardTestSystem.exe** application.



On Windows, click **Start > All Programs > Altera > Stratix V GX 100G Development Kit <version> > Board Test System** to run the application.

A GUI appears, displaying the application tab that corresponds to the design running in the FPGA.



If using the optic modules (CFP, SFP, QSFP) you must set the user switch SW4.7 to enabled (1) to turn on the laser. When done using the optics, set SW4.7 to disabled (0).

## Using the Board Test System

This section describes each control in the Board Test System application.

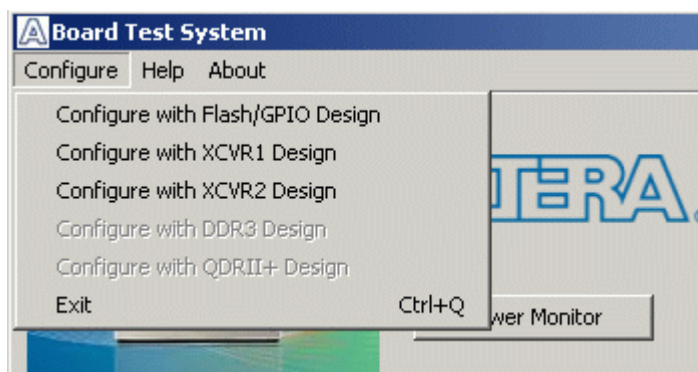


The Board Test System and Power Monitor share the JTAG bus with other applications like the Nios II debugger and the SignalTap® II Embedded Logic Analyzer. Because the Quartus II programmer uses most of the bandwidth of the JTAG bus, other applications using the JTAG bus might time out. Be sure to close the other applications before attempting to reconfigure the FPGA using the Quartus II Programmer.

## The Configure Menu

Use the Configure menu (Figure 6–1) to select the design you want to use. Each design example tests different functions that corresponds to one or more application tabs.

**Figure 6–1. The Configure Menu**



To configure the FPGA with a test system design, perform the following steps:

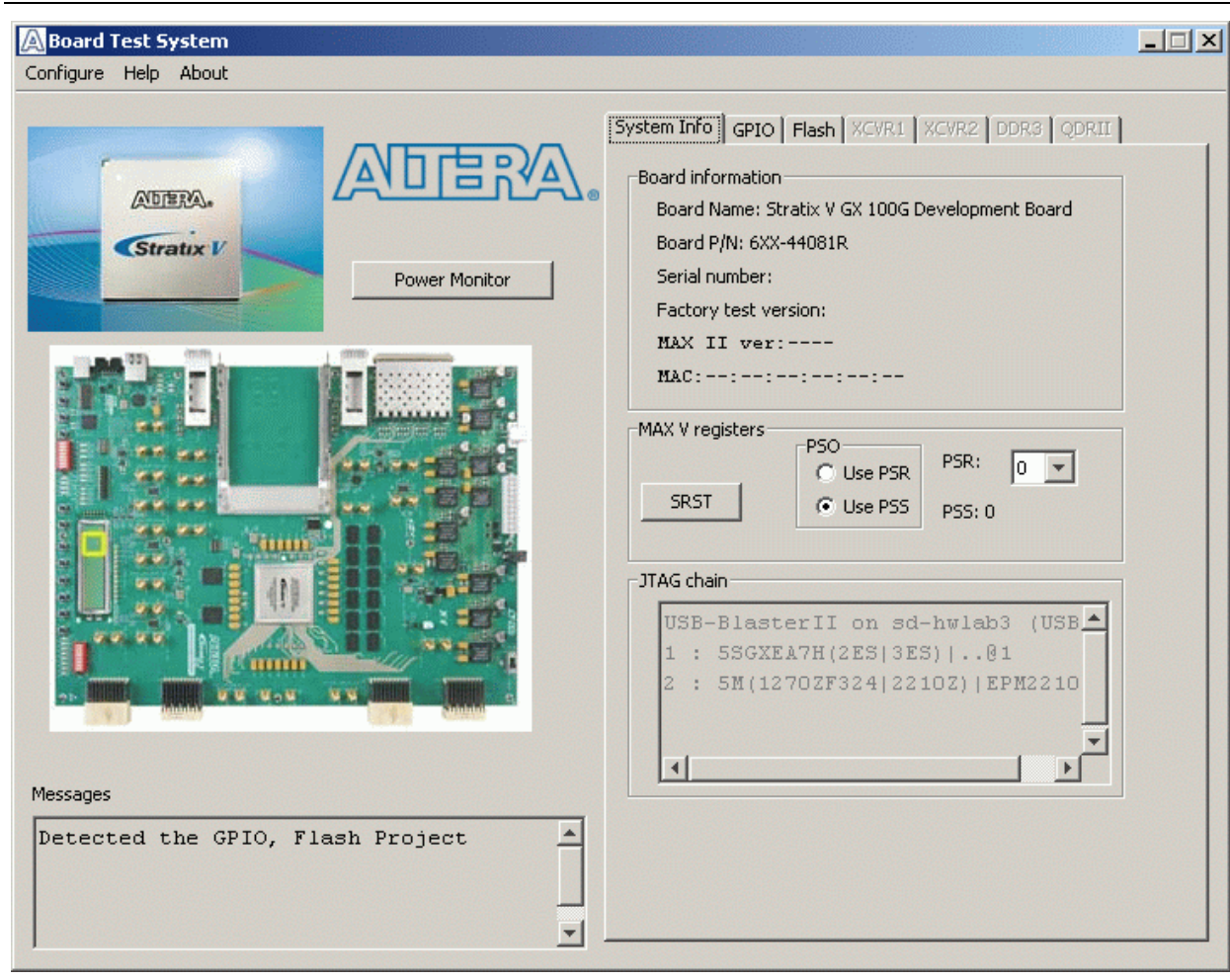
1. On the Configure menu, click the configure command that corresponds to the functionality you wish to test.
2. In the dialog box that appears, click **Configure** or **Download Start** to download the corresponding design's Raw-Binary Format (.rbf) configuration file to the FPGA. The download process usually takes about a minute.
3. When configuration finishes, close the Quartus II Programmer, if open. The design begins running in the FPGA. The corresponding GUI application tabs that interface with the design are enabled.

## The System Info Tab

The **System Info** tab shows board's current configuration. This tab displays the contents of the MAX II registers, the JTAG chain, the board's MAC address, the flash memory map, and other details stored on the board.

Figure 6-2 shows the initial GUI for a board that is in the factory configuration.

**Figure 6-2. Board Test System Graphical User Interface**



The following sections describe the controls on the **General** tab.

### Power Monitor

This button starts the Power Monitor application that measures and reports current power and temperature information for the board. Because the application communicates over the JTAG bus to the MAX II device, you can measure the power of any design in the FPGA, including your own designs. For details, refer to [“The Power Monitor” on page 6-17](#).

### Board Information


The **Board information** controls display static information about your board.

- **Name**—Indicates the official name of the board, given by the Board Test System.
- **Part number**—Indicates the part number of the board.
- **Serial number**—Indicates the serial number of the board.
- **Factory test version**—Indicates the version of the Board Test System currently running on the board.
- **Factory test date**—Indicates the release date of the Board Test System currently running on the board.
- **MAX II ver**—Indicates the version of MAX II code currently running on the board, which resides in the `<install dir>\kits\stratixVGX_5sgxea7nf45es_100g\examples` directory. Newer revisions of this code might be available on the [100G Development Kit, Stratix V GX](#) page of the Altera website.
- **MAC address**—Indicates the MAC address of the board.

## MAX II Registers

The **MAX II registers** control allow you to view and change the current MAX II register values as described in [Table 6–1](#). Changes to the register values with the GUI take effect immediately. For example, writing a 0 to SRST resets the board.

**Table 6–1. MAX II Registers**

Register Name	Read/Write Capability	Description
System Reset (SRST)	Write only	Set to 0 to initiate an FPGA reconfiguration.
Page Select Register (PSR)	Read / Write	Determines which of the flash memory to use for FPGA reconfiguration. The flash memory ships with pages 0 and 1 preconfigured.
Page Select Override (PSO)	Read / Write	When set to 0, the value in PSR determines the page of flash memory to use for FPGA reconfiguration. When set to 1, the value in PSS determines the page of flash memory to use for FPGA reconfiguration.
Page Select Switch (PSS)	Read only	<p>Holds the current value of the illuminated USER_POF LEDs (D32, D33, D34).</p> <ul style="list-style-type: none"> <li>■ 0 = USER_POF1 LED (D34)</li> <li>■ 1 = USER_POF2 LED (D33)</li> <li>■ 2 = USER_POF3 LED (D32)</li> </ul> <p> This state selects a page not supported by the default memory map. Use of this extra page may require the flash to be re-imaged if you want to return to the factory state.</p>

- **SRST**—Resets the system and reloads the FPGA with a design from flash memory based on the other MAX II register values.

- **PSO**—Sets the MAX II PSO register. The following options are available:
  - **Use PSR**—Allows the PSR to determine the page of flash memory to use for FPGA reconfiguration.
  - **Use PSS**—Allows the PSS to determine the page of flash memory to use for FPGA reconfiguration.
- **PSS**—Displays the MAX II PSS register value.
- **PSR**—Sets the MAX II PSR register. The numerical values in the list corresponds to the page of flash memory to load during FPGA reconfiguration. Refer to [Table 6-1](#) for more information.



Because the **System Info** tab requires that a specific design is running in the FPGA at a specific clock speed, writing a 0 to SRST; or changing the PSO value can cause the Board Test System to stop running.

### JTAG Chain

The **JTAG chain** control shows all the devices currently in the JTAG chain. The Stratix V GX device is always the first device in the chain.

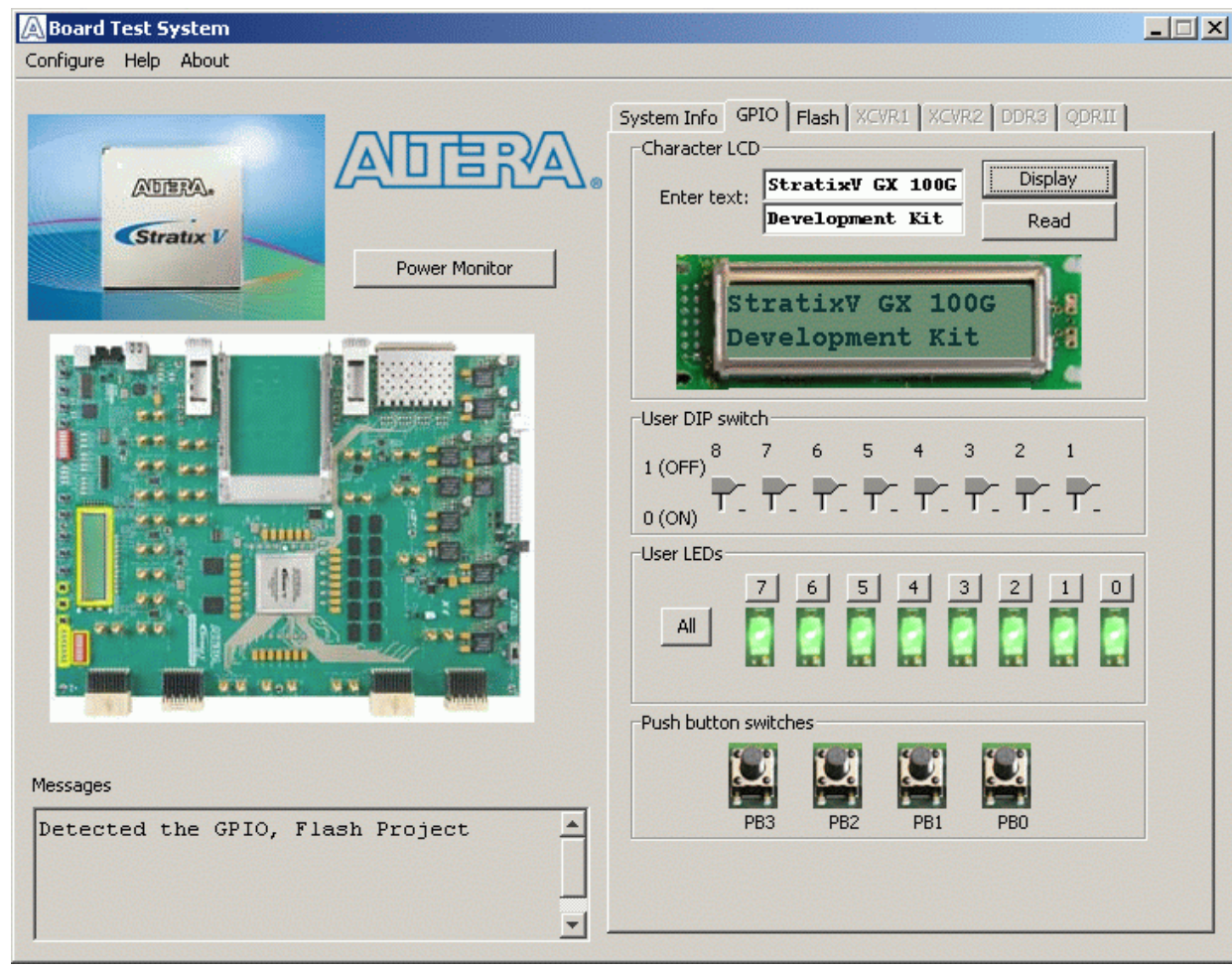


MAX\_JTAG\_EN (J62) includes the MAX II device in the JTAG chain when a jumper is not installed. To remove the MAX II device from the chain, install a jumper to J62.

## The GPIO Tab

The **GPIO** tab allows you to interact with all the general purpose user I/O components on your board. Figure 6-3 shows the **GPIO** tab.

Figure 6-3. The GPIO Tab



The following sections describe the controls on the **GPIO** tab.

### Character LCD

This controls allows you to display text strings on the character LCD on your board. Type text in the text boxes and then click **Display**.



If you exceed the 16 character display limit on either line, a warning message appears.

### User DIP Switch

The read-only User DIP switch control displays the current positions of the switches in the user DIP switch bank (SW4). Change the switches on the board to see the graphical display change accordingly.

## User LEDs

This control displays the current state of the user LEDs.

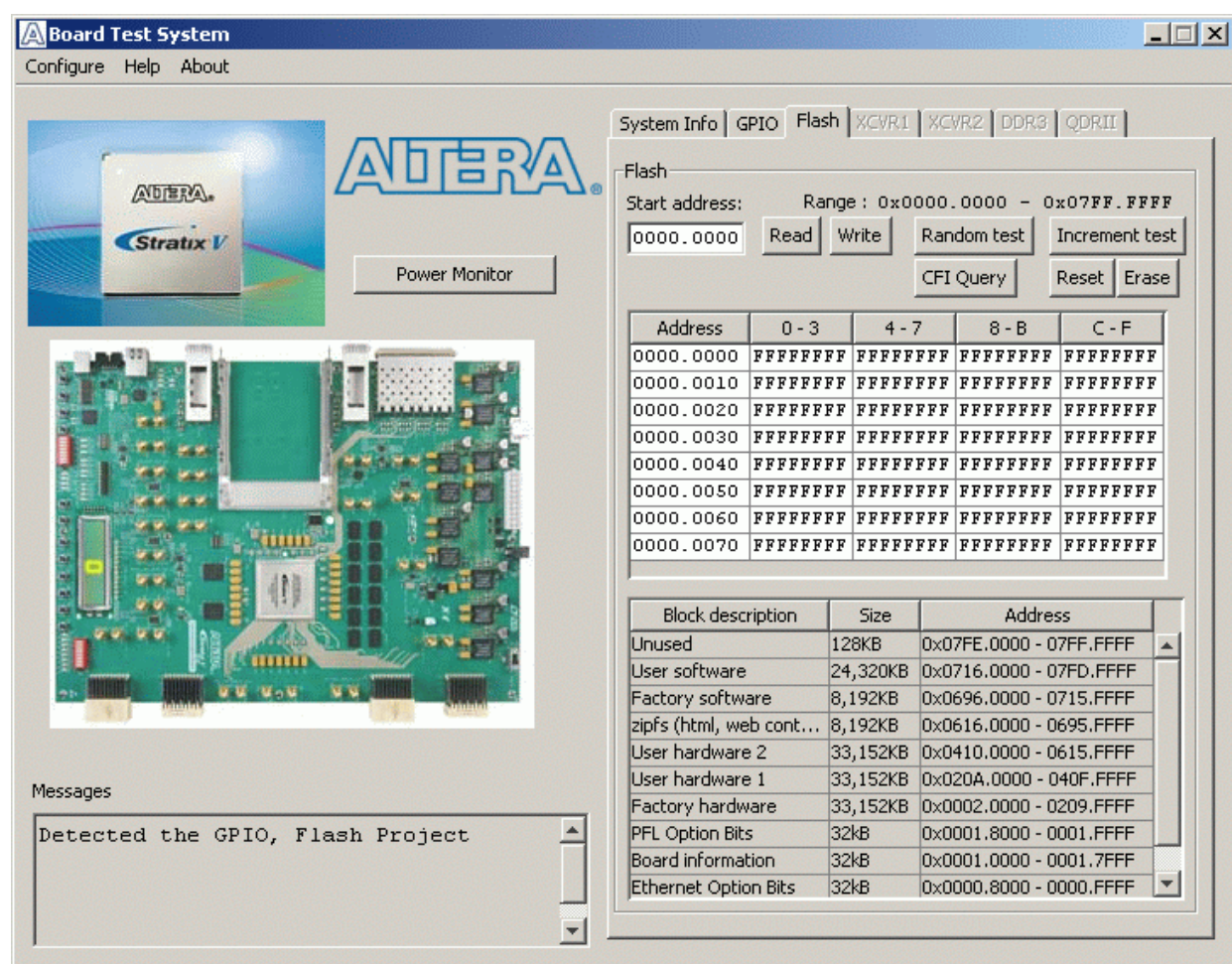
## Push Button Switches

This read-only control displays the current state of the board user push buttons. Press a push button on the board to see the graphical display change accordingly.

## The Flash Tab

The **Flash** tab allows you to read and write flash memory on your board. Figure 6-4 shows the **Flash** tab.

Figure 6-4. The Flash Tab



The following sections describe the controls on the **Flash** tab.

### Start address

This control allows you to enter an 8-hex digit (preceding with the 0x hex identifier).

## Range

Static display that shows the flash address range.

## Read

The **Read** control reads the flash memory on your board. To see the flash memory contents, type a starting address in the text box and click **Read**. Values starting at the specified address appear in the table.



If you enter an address outside of the flash memory address space, a warning message identifies the valid flash memory address range.

## Write

The **Write** control writes the flash memory on your board. To update the flash memory contents, change values in the table and click **Write**. The application writes the new values to flash memory and then reads the values back to guarantee that the graphical display accurately reflects the memory contents.

## Random Test

Starts a random data pattern test to flash memory, which is limited to a scratch page in the upper 128K block.

## CFI Query

The **CFI Query** control updates the memory table, displaying the CFI ROM table contents from the flash device.

## Increment Test

Starts an incrementing data pattern test to flash memory, which is limited to a scratch page in the upper 128K block.

## Reset

The **Reset** control executes the flash device's reset command and updates the memory table displayed on the **Flash** tab.

## Erase

Erases flash memory, which is limited to a scratch page in the upper 128K block.

## Data Display/Entry Boxes

This control, consisting of a table with an Address column and four 32-bit data columns, allows you to view and enter SRAM data.

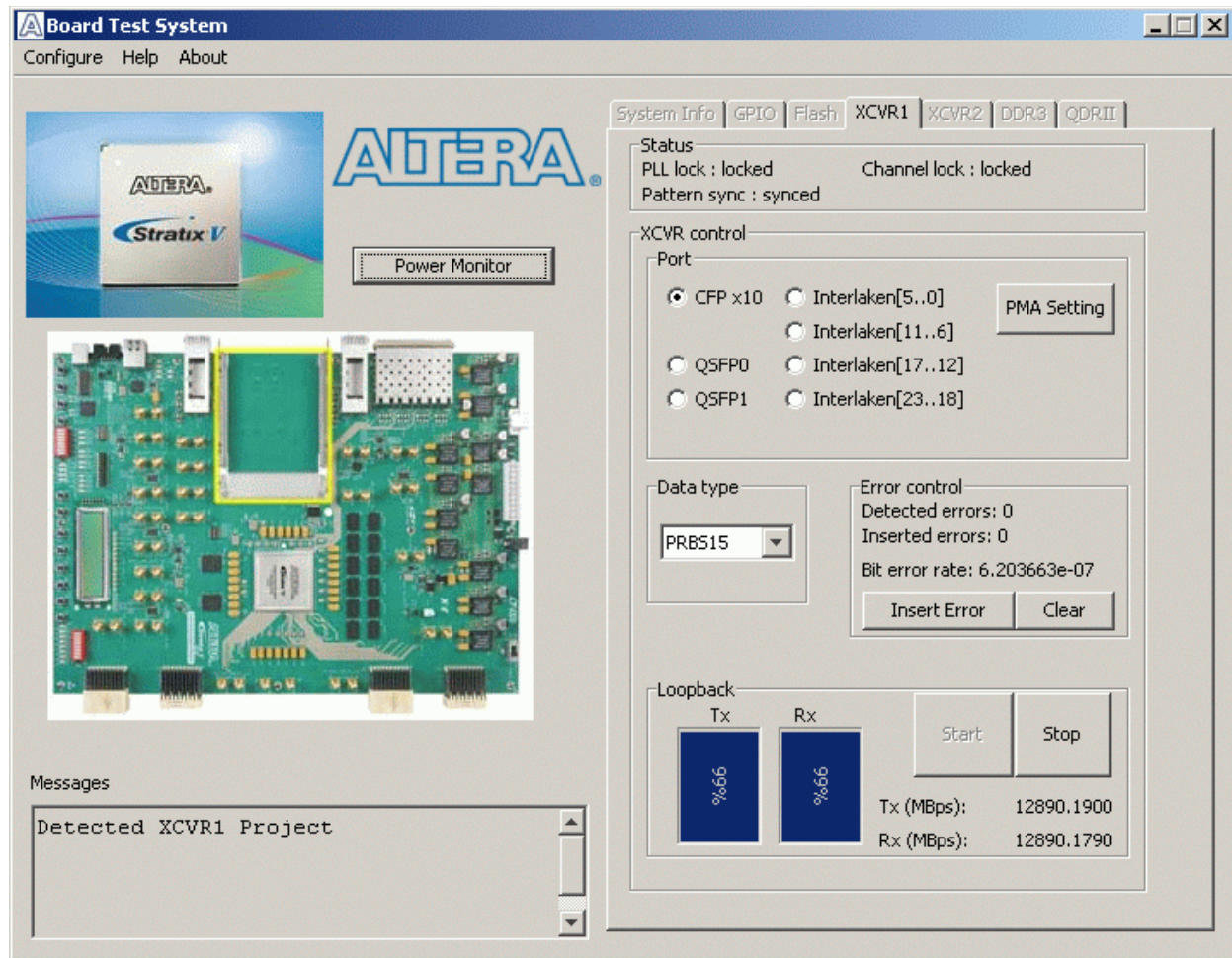
## Flash Memory Map

Displays the flash memory map for the 100G Development Kit, Stratix V GX Edition.

## The XCVR1 Tab

The **XCVR1** tab allows you to perform loopback tests on the CFP, QSFP, and Interlaken ports. Figure 6-5 shows the **XCVR1** tab.

Figure 6-5. The XCVR1 Tab



The following sections describe the controls on the **XCVR1** tab.

### Status

The **Status** control displays the following status information during the loopback test:

- **PLL lock**—Shows the PLL locked or unlocked state.
- **Channel lock**—Shows the channel locked or unlocked state. When locked, all lanes are word aligned and channel bonded, and all TX and RX PLL lanes are phase locked to data; RX lanes are word aligned and deskewed.
- **Pattern sync**—Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected after channel lock is acquired.

## Port

The **Port** control allows you to specify which interface to test. The following port tests are available:

- CFP x10
- QSFP0, QSFP1
- Interlaken[5..0], [11..6], [17..12], [23..18]

## PMA Setting

The **PMA Setting** button allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback**—Routes signals from the receiver to the transmitter. Enter the following values to enable the serial loopbacks:
  - 0 = High speed serial transceiver signals to loopback on the board
  - 1 = Serial loopback (internal loopback)
  - 2 = Reverse serial loopback pre-CDR
  - 4 = Reverse serial loopback post-CDR
- **VOD**—Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap**
  - **Pre**—Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.
  - **First post**—Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
  - **Second post**—Specifies the amount of pre-emphasis on the second post tap of the transmitter buffer.
- **Equalizer**—Specifies the setting for the receiver equalizer.
- **DC gain**—Specifies the DC portion of the receiver equalizer.

## Data Type

The **Data type** control specifies the type of data contained in the transactions. The following data types are available for analysis:

- **PRBS 7**—Selects pseudo-random 7-bit sequences
- **PRBS 15**—Selects pseudo-random 15-bit sequences
- **PRBS 23**—Selects pseudo-random 23-bit sequences
- **PRBS 31**—Selects pseudo-random 31-bit sequences
- **HF**—Selects highest frequency divide-by-2 data pattern "10101010"
- **HF1**—Selects next highest frequency divide-by-6 data pattern "111000111000"
- **HF2**—Selects second lowest frequency divide-by-22 data pattern
- **LF**—Selects lowest frequency divide by 33 data pattern

## Error Control

The **Error control** controls display data errors detected during analysis and allow you to insert errors:

- **Detected errors**—Displays the number of data errors detected in the hardware.
- **Inserted errors**—Displays the number of errors inserted into the transmit data stream.
- **Insert Error**—Inserts a one-word error into the transmit data stream each time you click the button. **Insert Error** is only enabled during transaction performance analysis.
- **Clear**—Resets the **Detected errors** and **Inserted errors** counters to zeros.

## Start

The **Start** control initiates the active port transaction performance analysis.

## Stop

The **Stop** control terminates transaction performance analysis.



Always click **Clear** before **Start**.

## Performance Indicators

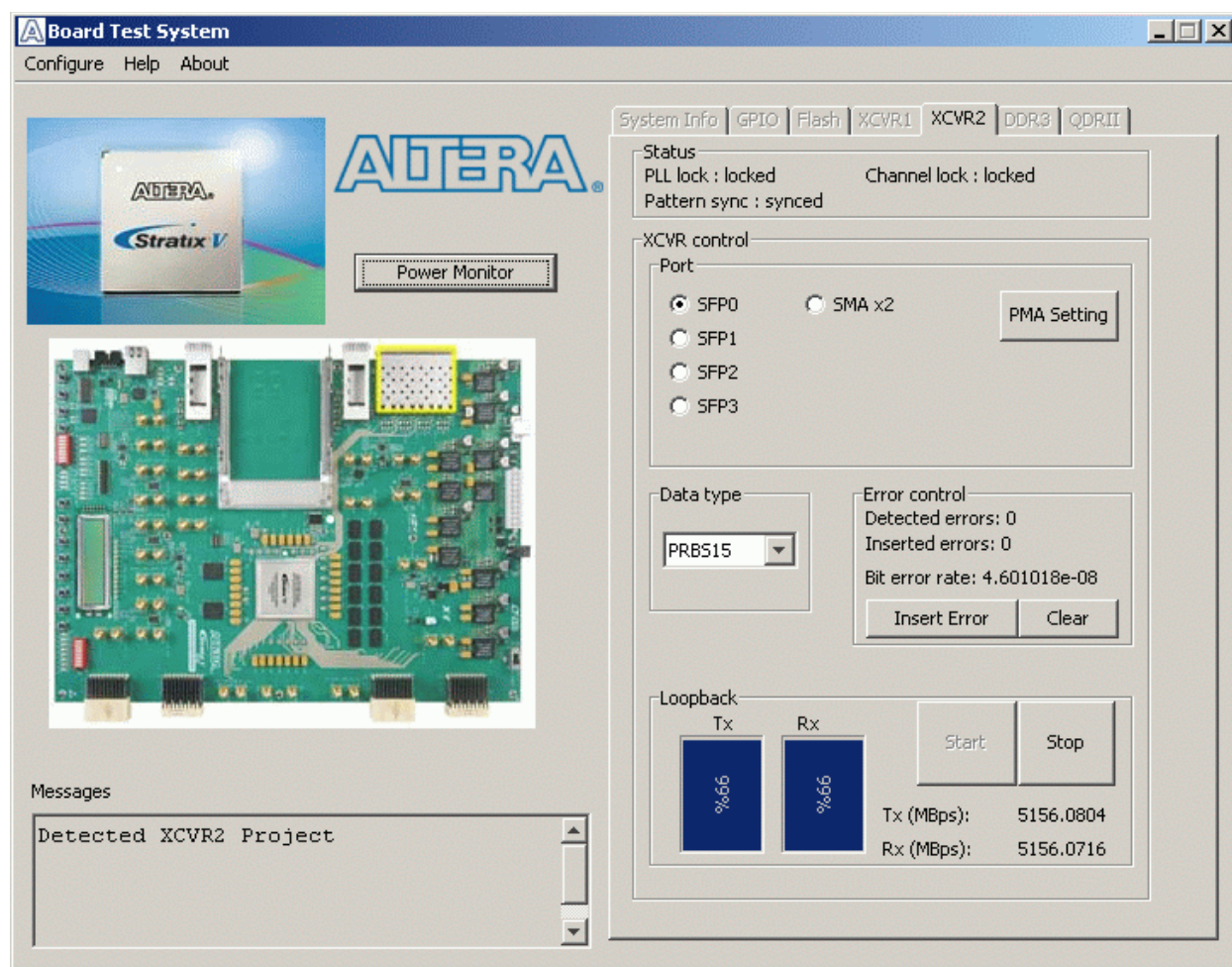
These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **TX and RX performance bars**—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **Tx (MBps) and Rx (MBps)**—Show the number of bytes of data analyzed per second.

## The XCVR2 Tab

The **XCVR2** tab allows you to perform loopback tests on the CFP, QSFP, and Interlaken ports. [Figure 6-6](#) shows the **XCVR2** tab.

**Figure 6-6. The XCVR2 Tab**



The following sections describe the controls on the **XCVR2** tab.

### Status

The **Status** control displays status information during the loopback test. For details on this control, refer to [“Status” on page 6-9](#).

### Port

The **Port** control allows you to specify which interface to test. The following port tests are available:

- SFP0, SFP1, SFP2, SFP3
- SMA x2

## PMA Setting

The **PMA Setting** button allows you to make changes to the PMA parameters that affect the active transceiver interface. For details, refer to “PMA Setting” on page 6-10.

## Data Type

The **Data type** control specifies the type of data contained in the transactions. For details, refer to “Data Type” on page 6-10.

## Error Control

This control displays data errors detected during analysis and allows you to insert errors. For details, refer to “Error Control” on page 6-11.

## Start

The **Start** control initiates the active port transaction performance analysis.

## Stop

The **Stop** control terminates transaction performance analysis.



Always click **Clear** before **Start**.

## Performance Indicators

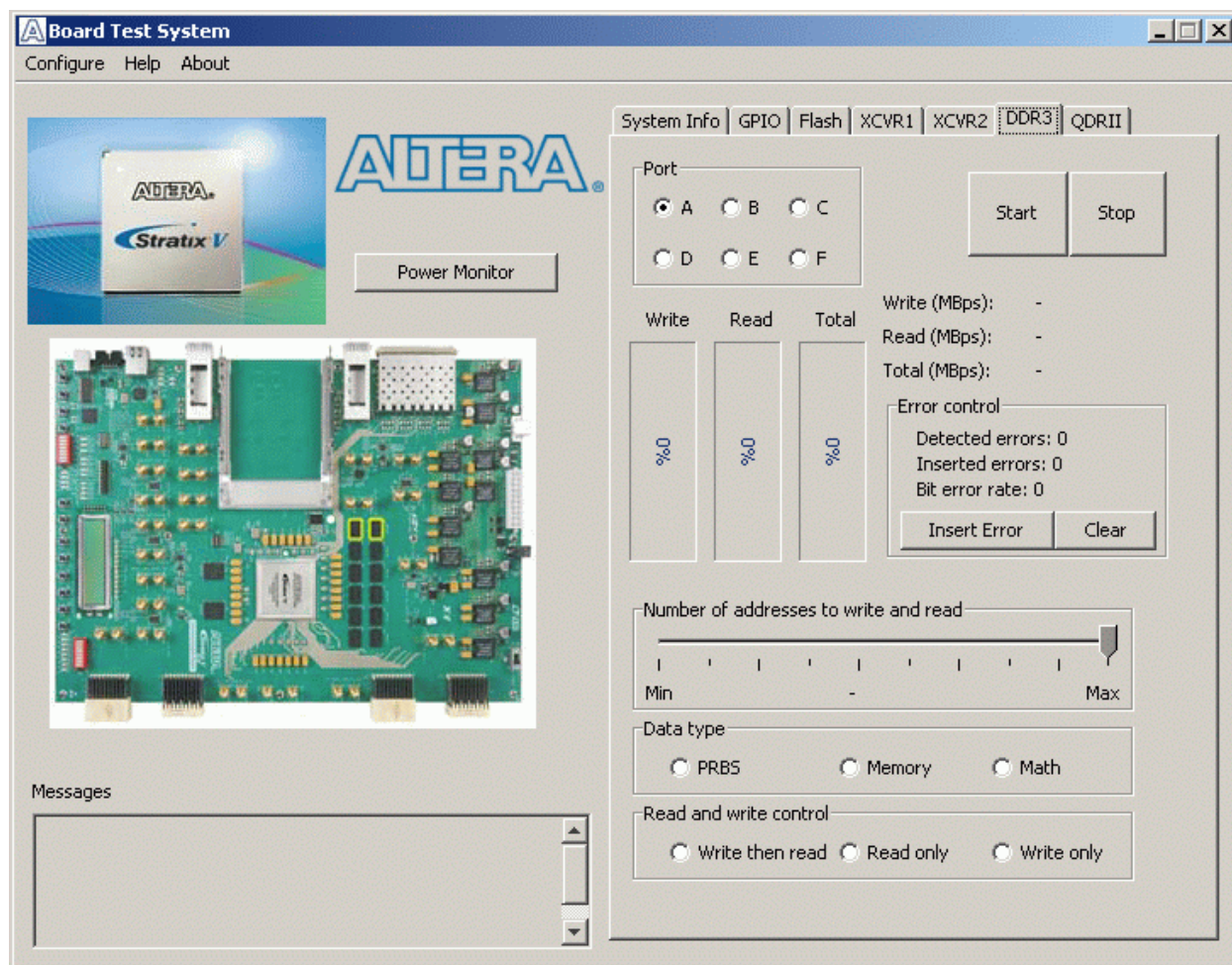
These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **TX** and **RX** performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **Tx (MBps)** and **Rx (MBps)**—Show the number of bytes of data analyzed per second.

## The DDR3 Tab

The **DDR3** tab allows you to read and write the DDR3 memory on your board. Figure 6-7 shows the **DDR3** tab.

Figure 6-7. The DDR3 Tab



The following sections describe the controls on the **DDR3** tab.

### Port

The **Port** control directs communication to one of six DDR3 memory ports connected to banks 7 and 8 of the Stratix V GX FPGA. Each port is 32 bits composed of two 16-bit devices.

### Start

The **Start** control initiates DDR3 memory transaction performance analysis.

### Stop

The **Stop** control terminates transaction performance analysis.

## Performance Indicators

These controls display current transaction performance analysis information collected since you last pressed **Start**:

- **Write** and **Read** performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve as % of 4268 MBps.
- **Total** performance bar—Shows the sum of **Write** and **Read**.
- **Write (MBps)**, **Read (MBps)**, and **Total (MBps)**—Show the number of bytes of data analyzed per second.

## Error Control

This control displays data errors detected during analysis and allows you to insert errors. For details, refer to [“Error Control” on page 6-11](#).

## Number of Addresses to Write and Read

This control determines the number of addresses to use in each iteration of reads and writes.

## Data type

The **Data type** control specifies the type of data contained in the transactions. The following data types are available for analysis:

- **PRBS**—Selects pseudo-random bit sequences.
- **Memory**—Selects a generic data pattern stored in the on chip memory of the Stratix V GX device.
- **Math**—Selects data generated from a simple math function within the FPGA fabric.

## Read and write control

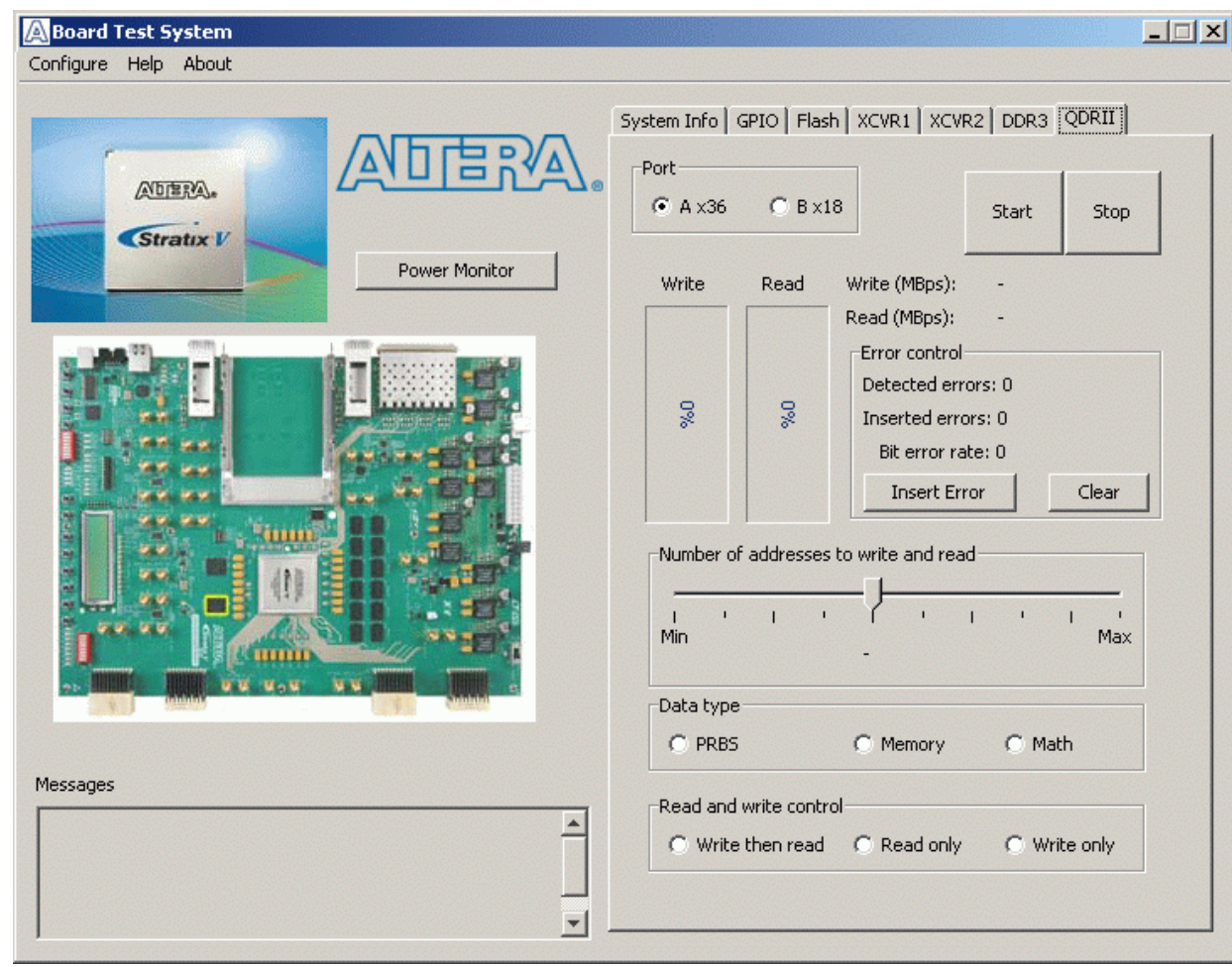
Specifies the type of transactions to analyze. The following transaction types are available for analysis:

- **Write then read**—Selects read and write transactions for analysis.
- **Read only**—Selects read transactions for analysis.
- **Write only**—Selects write transactions for analysis.

## The QDRII Tab

The **QDRII** tab allows you to read and write the QDR II memory on your board and independently test each QDR II port. Figure 6-8 shows the **QDRII** tab.

Figure 6-8. The QDRII Tab



The following sections describe the controls on the **QDRII** tab.

### Port

The **Port** control directs communication to one of two QDR II ports on your board.

### Start

The **Start** control initiates QDR II memory transaction performance analysis.

### Stop

The **Stop** control terminates transaction performance analysis.

## Performance Indicators

These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **Write** and **Read** performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **Write (MBps)** and **Read (MBps)**—Show the number of bytes of data analyzed per second.

## Error Control

This control displays data errors detected during analysis and allows you to insert errors. For details, refer to [“Error Control” on page 6-11](#).

## Number of Addresses to Write and Read

This control determines the number of addresses to use in each iteration of reads and writes.

## Data Type

The Data type control specifies the type of data contained in the transactions. The following data types are available for analysis:

- **PRBS**—Selects pseudo-random bit sequences.
- **Memory**—Selects a generic data pattern stored in the on chip memory of the Stratix V GX device.
- **Math**—Selects data generated from a simple math function within the FPGA fabric.

# The Power Monitor

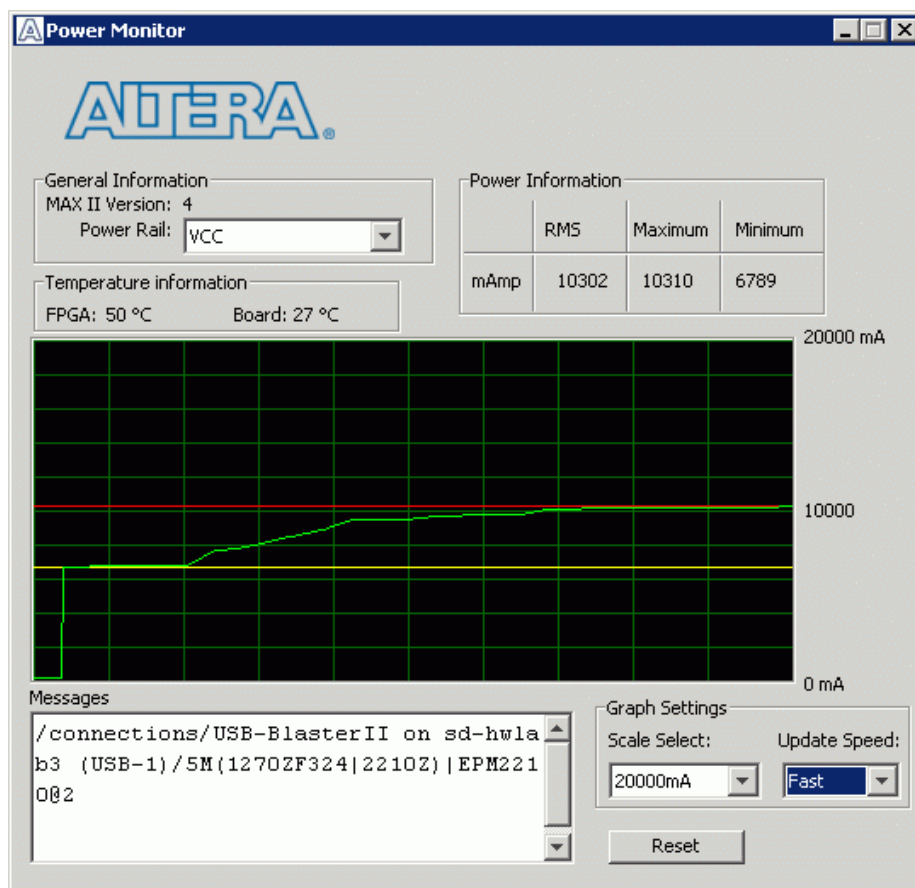
The Power Monitor measures and reports current power and temperature information for the board. To start the application, click **Power Monitor** in the Board Test System application.



You can also run the Power Monitor as a stand-alone application. **PowerMonitor.exe** resides in the `<install dir>\kits\stratixVGX_5sgxea7nf45es_100g\examples\board_test_system` directory. On Windows, click **Start** > **All Programs** > **Altera** > **Stratix V GX 100G Development Kit** <version> > **Power Monitor** to start the application.

The Power Monitor communicates with the MAX II device on the board through the JTAG bus. A power monitor circuit attached to the MAX II device allows you to measure the power that the Stratix V GX FPGA device is consuming regardless of the design currently running. Figure 6-9 shows the Power Monitor.

**Figure 6-9. The Power Monitor**



The following sections describe the Power Monitor controls.

### General Information

The **General information** controls display the following information about the MAX II device:

- **MAX II version**—Indicates the version of MAX II code currently running on the board. The MAX V code resides in the `<install dir>\kits\stratixVGX_5sgxea7nf45es_100g\factory_recovery` and `<install dir>\kits\stratixVGX_5sgxea7nf45es_100g\examples\max2` directories. Newer revisions of this code might be available on the [100G Development Kit, Stratix V GX](#) page of the Altera website.
  - **Power Rail**—Indicates the currently-selected power rail.
- For more information on the power rails, refer to the [100G Development Kit, Stratix V GX Edition Reference Manual](#).

## Temperature Information

The **Temperature information** control displays the temperature readings for the FPGA and the board.

## Power Information

The **Power information** control displays current, maximum, and minimum power readings for the following unit:

- **mAmp**

## Power Graph

The power graph displays the mWatt power consumption of your board over time. The green line indicates the current value. The red line indicates the maximum value read since the last reset. The yellow line indicates the minimum value read since the last reset.

## Graph Settings

The following **Graph settings** controls allow you to define the look and feel of the power graph:

- **Scale select**—Specifies the amount to scale the power graph. Select a smaller number to zoom in to see finer detail. Select a larger number to zoom out to see the entire range of recorded values.
- **Update speed**—Specifies how often to refresh the graph.

## Reset

This **Reset** control clears the graph, resets the minimum and maximum values, and restarts the Power Monitor.

# The Clock Control

The Clock Control application sets the Si5338 programmable oscillator to any frequency between 10 MHz and 810 MHz with eight digits of precision to the right of the decimal point. The oscillator drives a 2-to-4 buffer that drives a copy of the clock to all four edges of the FPGA.

The Clock Control application runs as a stand-alone application. **ClockControl.exe** resides in the *<install*

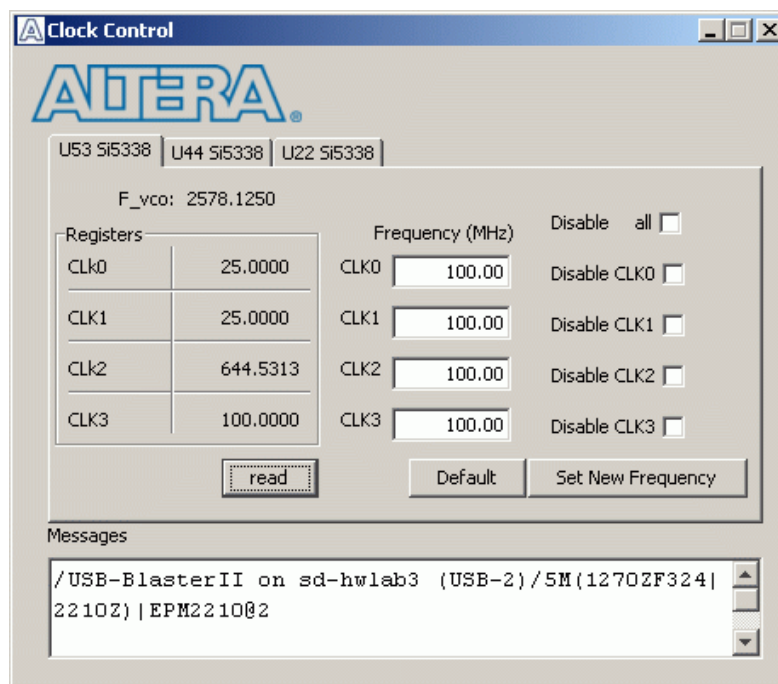
*dir>\kits\stratixVGX\_5sgxea7nf45es\_100g\examples\board\_test\_system* directory. On Windows, click **Start > All Programs > Altera > Stratix V GX 100G Development Kit <version> > Clock Control** to start the application.



For more information about the Si5338 and the Stratix V GX 100G development board's clocking circuitry and clock input pins, refer to the *100G Development Kit, Stratix V GX Edition Reference Manual*.

The Clock Control communicates with the MAX II device on the board through the JTAG bus. Figure 6-10 shows the Clock Control.

**Figure 6-10. The Clock Control**



The following sections describe the Clock Control controls.

## Clock Tabs

There are three tabs to control each clock generator device. The **U53 SiF338** tab controls the clocks to the Stratix V fabric clock input and the reference clocks for all the optical interfaces. The default is 100 MHz for the fabric and 644.53125 MHz for the reference clocks for the transceivers. The **U44 SiF338** tab controls the clocks for the DDR3 and the Interlaken interface; its default is 100MHz for the DDR3 interface and 625MHz for the Interlaken interface. The **U22 SiF338** tab controls the clocks for the QDR II interface and the transceivers for the optical interfaces. The default frequencies for these interfaces are 100MHz for the QDR II interface and 644.53125 MHz for the transceivers.

## Registers

The Registers control shows the current values from the clock driver.

## Frequency

Enter the desired frequencies for each CLK. The range of this GUI is from 5 MHz to 710 MHz. There are some limitations for what frequencies are allowed.

## Disable

The **Disable** controls enables and disables all or selected outputs of the clock generators.

## Read

Reads the register values and calculates the frequency based on these values.

## Default

This control sets the frequency for the oscillator associated with the active tab back to its default value. This can also be accomplished by power cycling the board.

## Set New Frequency

The **Set New Frequency** control sets the Si5338 programmable oscillator frequency to the value in the **Target frequency** control. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time. Altera recommends resetting the FPGA logic after changing frequencies.

# Configuring the FPGA Using the Quartus II Programmer

You can use the Quartus II Programmer to configure the FPGA with a specific **.sof**. Before configuring the FPGA, ensure that the Quartus II Programmer and the USB-Blaster driver are installed on the host computer, the USB cable is connected to the 100G development board, power to the board is on, and no other applications that use the JTAG chain are running.

To configure the Stratix V GX FPGA, perform the following steps:

1. Start the Quartus II Programmer.
2. Click **Add File** and select the path to the desired **.sof**.
3. Turn on the **Program/Configure** option for the added file.
4. Click **Start** to download the selected file to the FPGA. Configuration is complete when the progress bar reaches 100%.



Using the Quartus II programmer to configure a device on the board causes other JTAG-based applications such as the Board Test System and the Power Monitor to lose their connection to the board. Restart those applications after configuration is complete.



As you develop your own project using the Altera tools, you can program the flash memory device so that your own design loads from flash memory into the FPGA on power up. This appendix describes the preprogrammed contents of the common flash interface (CFI) flash memory device on the Stratix V GX 100G development board and the Nios II EDS tools involved with reprogramming the user portions of the flash memory device.

The Stratix V GX 100G development board ships with the CFI flash device preprogrammed with a default factory FPGA configuration for running the Board Update Portal design example and a default user configuration for running the Board Test System demonstration. There are several other factory software files written to the CFI flash device to support the Board Update Portal. These software files were created using the Nios II EDS, just as the hardware design was created using the Quartus II software.



For more information about Altera development tools, refer to the [Design Software](#) page of the Altera website.

## CFI Flash Memory Map

[Table A-1](#) shows the default memory contents of the 1-Gb CFI flash device. For the Board Update Portal to run correctly and update designs in the user memory, this memory map must not be altered.

**Table A-1. Byte Address Flash Memory Map**

Block Description	Size	Address Range
Unused	128	0x07FE.0000 - 0x07FF.FFFF
User software	24,320	0x0716.0000 - 0x07F7.FFFF
Factory software	8,192	0x0696.0000 - 0x0715.FFFF
zipfs (html, web content)	8,192	0x0616.0000 - 0x0695.FFFF
User hardware 2	33,152	0x0410.0000 - 0x0615.FFFF
User hardware 1	33,152	0x020A.0000 - 0x040F.FFFF
Factory hardware	33,152	0x0002.0000 - 0x0209.FFFF
PFL option bits	32	0x0001.8000 - 0x0001.FFFF
Board information	32	0x0001.0000 - 0x0001.7FFF
Ethernet option bits	32	0x0000.8000 - 0x0000.FFFF
User design reset vector	32	0x0000.0000 - 0x0000.7FFF



Altera recommends that you do not overwrite the factory hardware and factory software images unless you are an expert with the Altera tools. If you unintentionally overwrite the factory hardware or factory software image, refer to [“Restoring the Flash Device to the Factory Settings” on page A-4](#).

## Preparing Design Files for Flash Programming

You can obtain designs containing prepared **.flash** files from the [100G Development Kit, Stratix V GX](#) page of the Altera website or create **.flash** files from your own custom design.

The Nios II EDS **sof2flash** command line utility converts your Quartus II-compiled **.sof** into the **.flash** format necessary for the flash device. Similarly, the Nios II EDS **elf2flash** command line utility converts your compiled and linked Executable and Linking Format File (**.elf**) software design to **.flash**. After your design files are in the **.flash** format, use the Board Update Portal or the Nios II EDS **nios2-flash-programmer** utility to write the **.flash** files to the user hardware [1](#) and user software locations of the flash memory.



For more information about Nios II EDS software tools and practices, refer to the [Embedded Software Development](#) page of the Altera website.

## Creating Flash Files Using the Nios II EDS

If you have an FPGA design developed using the Quartus II software, and software developed using the Nios II EDS, follow these instructions:

1. On the Windows Start menu, click **All Programs > Altera > Nios II EDS > Nios II Command Shell**.
2. In the Nios II command shell, navigate to the directory where your design files reside and type the following Nios II EDS commands:

- For Quartus II **.sof** files:

```
sof2flash --input=<yourfile>_hw.sof --output=<yourfile>_hw.flash --offset=0x020A0000
--pfl --optionbit=0x00081000 --programmingmode=PS
```

- For Nios II **.elf** files:

```
elf2flash --base=0x0 --end=0x07FFFFFF --reset=0x07160000 --input=<yourfile>_sw.elf
--output=<yourfile>_sw.flash
--boot=$SOPC_KIT_NIOS2/components/altera_nios2/boot_loader_cfi.srec
```

The resulting **.flash** files are ready for flash device programming. If your design uses additional files such as image data or files used by the runtime program, you must first convert the files to **.flash** format and concatenate them into one **.flash** file before using the Board Update Portal to upload them.



The Board Update Portal standard **.flash** format conventionally uses either **<filename>\_hw.flash** for hardware design files or **<filename>\_sw.flash** for software design files.

## Programming Flash Memory Using the Board Update Portal

Once you have the necessary **.flash** files, you can use the Board Update Portal to reprogram the flash memory. Refer to [“Using the Board Update Portal to Update User Designs”](#) on page 5–2 for more information.



If you have generated a **.sof** that operates without a software design file, you can still use the Board Update Portal to upload your design. In this case, leave the **Software File Name** field blank.

## Programming Flash Memory Using the Nios II EDS

The Nios II EDS offers a **nios2-flash-programmer** utility to program the flash memory directly. To program the **.flash** files or any compatible S-Record File (**.srec**) to the board using **nios2-flash-programmer**, perform the following steps:

1. Attach the USB-Blaster cable and power up the board.
2. If the board has powered up and the LCD displays either "Connecting..." or a valid IP address (such as 152.198.231.75), proceed to step 8. If no output appears on the LCD or if the MAX\_CONF\_DN LED (D25) does not illuminate, continue to step 3 to load the FPGA with a flash-writing design.
3. Launch the Quartus II Programmer to configure the FPGA with a **.sof** capable of flash programming. Refer to ["Configuring the FPGA Using the Quartus II Programmer" on page 6–21](#) for more information.
4. Click **Add File** and select *<install*  
`dir>\kits\stratixVGX_5sgxea7nf45es_100g\factory_recovery\s5gx100g_fpga_b  
up.sof`.
5. Turn on the **Program/Configure** option for the added file.
6. Click **Start** to download the selected configuration file to the FPGA. Configuration is complete when the progress bar reaches 100%. The MAX\_CONF\_DN LED (D25) illuminates indicating that the flash device is ready for programming.
7. On the Windows Start menu, click **All Programs > Altera > Nios II EDS > Nios II Command Shell**.
8. In the Nios II command shell, navigate to the *<install*  
`dir>\kits\stratixVGX_5sgxea7nf45es_100g\factory_recovery` directory (or to the directory of the **.flash** files you created in ["Creating Flash Files Using the Nios II EDS" on page A–2](#)) and type the following Nios II EDS command:

```
nios2-flash-programmer --base=0x0 <yourfile>_hw.flash ↵
```

9. After programming completes, if you have a software file to program, type the following Nios II EDS command:

```
nios2-flash-programmer --base=0x0 <yourfile>_sw.flash ↵
```

10. Press the PGM\_SEL button (S8) until the POF 1 LED (D34) illuminates, and then press the LOAD (S5) to load and run the user hardware design.

Programming the board is now complete.



For more information about the **nios2-flash-programmer** utility, refer to the [Nios II Flash Programmer User Guide](#).

## Restoring the Flash Device to the Factory Settings

This section describes how to restore the original factory contents to the flash memory device on the 100G development board. Make sure you have the Nios II EDS installed, and perform the following instructions:

1. Set the board switches to the factory default settings described in “[Factory Default Switch Settings](#)” on page 4–2.
2. Launch the Quartus II Programmer to configure the FPGA with a .sof capable of flash programming. Refer to “[Configuring the FPGA Using the Quartus II Programmer](#)” on page 6–21 for more information.
3. Click **Add File** and select *<install*  
`dir>\kits\stratixVGX_5sgxea7nf45es_100g\factory_recovery\s5gx100g_fpga_bup.sof`.
4. Turn on the **Program/Configure** option for the added file.
5. Click **Start** to download the selected configuration file to the FPGA. Configuration is complete when the progress bar reaches 100%. The MAX\_CONF\_DN LED (D25) illuminates indicating that the flash device is ready for programming. The flash device is ready for programming.
6. On the Windows Start menu, click **All Programs > Altera > Nios II EDS > Nios II Command Shell**.
7. In the Nios II command shell, navigate to the *<install*  
`dir>\kits\stratixVGX_5sgxea7nf45es_100g\factory_recovery` directory and type the following command to run the restore script:  
`./restore.sh` ↵  
 Restoring the flash memory might take several minutes. Follow any instructions that appear in the Nios II command shell.
8. After all flash programming completes, cycle the POWER switch (SW1) off then on.
9. Using the Quartus II Programmer, click **Add File** and select *<install*  
`dir>\kits\stratixVGX_5sgxea7nf45es_100g\factory_recovery\s5gx100g_fpga_bup.sof`.
10. Turn on the **Program/Configure** option for the added file.
11. Click **Start** to download the selected configuration file to the FPGA. Configuration is complete when the progress bar reaches 100%. The MAX\_CONF\_DN LED (D25) illuminates indicating the flash memory device is now restored with the factory contents. The flash device is ready for programming.
12. Cycle the POWER switch (SW1) off then on to load and run the restored factory design.
13. The restore script cannot restore the board’s MAC address automatically. In the Nios II command shell, type the following Nios II EDS command:  
`nios2-terminal` ↵  
 and follow the instructions in the terminal window to generate a unique MAC address.

 To ensure that you have the most up-to-date factory restore files and information about this product, refer to the [100G Development Kit, Stratix V GX](#) page of the Altera website.

## Restoring the MAX II CPLD to the Factory Settings

This section describes how to restore the original factory contents to the MAX II CPLD on the 100G development board. Make sure you have the Nios II EDS installed, and perform the following instructions:

1. Set the board switches to the factory default settings described in “[Factory Default Switch Settings](#)” on page 4-2.

 Installing a shunt to MAX\_JTAG\_EN (J62) removes the MAX II device in the JTAG chain.

2. Launch the Quartus II Programmer.
3. Click **Auto Detect**.
4. Click **Add File** and select *<install dir>\kits\stratixVGX\_5sgxea7nf45es\_100g\factory\_recovery\max2.pof*.
5. Turn on the **Program/Configure** option for the added file.
6. Click **Start** to download the selected configuration file to the MAX II CPLD. Configuration is complete when the progress bar reaches 100%.

 To ensure that you have the most up-to-date factory restore files and information about this product, refer to the [100G Development Kit, Stratix V GX](#) page of the Altera website.



This chapter provides additional information about the document and Altera.

## Document Revision History

The following table shows the revision history for this document.

Date	Version	Changes
February 2012	1.0	Initial release.

## How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact <sup>(1)</sup>	Contact Method	Address
Technical support	Website	<a href="http://www.altera.com/support">www.altera.com/support</a>
Technical training	Website	<a href="http://www.altera.com/training">www.altera.com/training</a>
	Email	<a href="mailto:custrain@altera.com">custrain@altera.com</a>
Product literature	Website	<a href="http://www.altera.com/literature">www.altera.com/literature</a>
Nontechnical support (general) (software licensing)	Email	<a href="mailto:nacomp@altera.com">nacomp@altera.com</a>
	Email	<a href="mailto:authorization@altera.com">authorization@altera.com</a>










### Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

## Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
<b>Bold Type with Initial Capital Letters</b>	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, <b>Save As</b> dialog box. For GUI elements, capitalization matches the GUI.
<b>bold type</b>	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, <b>\qdesigns</b> directory, <b>D:</b> drive, and <b>chiptrip.gdf</b> file.
<i>Italic Type with Initial Capital Letters</i>	Indicate document titles. For example, <i>Stratix IV Design Guidelines</i> .
<i>italic type</i>	Indicates variables. For example, $n + 1$ . Variable names are enclosed in angle brackets (< >). For example, <file name> and <project name>.pdf file.
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.

Visual Cue	Meaning
"Subheading Title"	Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, "Typographic Conventions."
Courier type	<p>Indicates signal, port, register, bit, block, and primitive names. For example, <code>data1</code>, <code>tdi</code>, and <code>input</code>. The suffix <code>n</code> denotes an active-low signal. For example, <code>resetn</code>.</p> <p>Indicates command line commands and anything that must be typed exactly as it appears. For example, <code>c:\qdesigns\tutorial\chiptrip.gdf</code>.</p> <p>Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword <code>SUBDESIGN</code>), and logic function names (for example, <code>TRI</code>).</p>
	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	The question mark directs you to a software help system with related information.
	The feet direct you to another document or website with related information.
	The multimedia icon directs you to a related multimedia presentation.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the <a href="#">Email Subscription Management Center</a> page of the Altera website, where you can sign up to receive update notifications for Altera documents.