SYNCHRONOUS DRAM

MT48LC2M32B2 - 512K x 32 x 4 banks

For the latest data sheet, please refer to the Micron Web site: www.micron.com/sdramds

FEATURES

- PC100 functionality
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto Precharge, includes CONCURRENT AUTO PRECHARGE, and Auto Refresh Modes
- Self Refresh Mode
- 64ms, 4,096-cycle refresh (15.6µs/row)
- LVTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply
- Supports CAS latency of 1, 2, and 3

OPTIONS / MARKING

OPTIONS	MARKING
• Configuration	
2 Meg x 32 (512K x 32 x 4 banks)	2M32B2
• Plastic Package - OCPL[1]	
86-pin TSOP (400 mil)	TG
• Timing (Cycle Time)	
5ns (200 MHz)	-5
5.5ns (183 MHz)	-55
6ns (166 MHz)	-6
7ns (143 MHz)	-7
• Operating Temperature Range	
Commercial (0° to +70°C)	None
Extended (-40°C to +85°C)	IT[2]

NOTE: 1. Off-center parting line
2. Available on -7

Part Number Example:

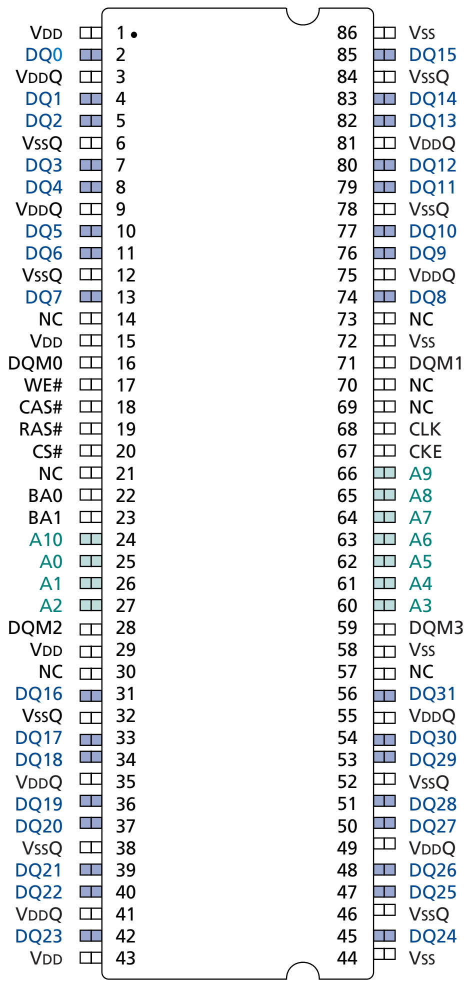
MT48LC2M32B2TG-7

KEY TIMING PARAMETERS

SPEED GRADE	CLOCK FREQUENCY	ACCESS TIME CL = 3*	SETUP TIME	HOLD TIME
-5	200 MHz	4.5ns	1.5ns	1ns
-55	183 MHz	5ns	1.5ns	1ns
-6	166 MHz	5.5ns	1.5ns	1ns
-7	143 MHz	5.5ns	2ns	1ns

*CL = CAS (READ) latency

PIN ASSIGNMENT (TOP VIEW)
86-PIN TSOP



Note: The # symbol indicates signal is active LOW.

	2 Meg x 32
Configuration	512K x 32 x 4 banks
Refresh Count	4K
Row Addressing	2K (A0-A10)
Bank Addressing	4 (BA0, BA1)
Column Addressing	256 (A0-A7)

64Mb (x32) SDRAM PART NUMBER

PART NUMBER	ARCHITECTURE
MT48LC2M32B2TG	2 Meg x 32

GENERAL DESCRIPTION

The 64Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 67,108,864-bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 16,777,216-bit banks is organized as 2,048 rows by 256 columns by 32 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank, A0-A10 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable READ or WRITE burst lengths of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The 64Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless, high-speed, random-access operation.

The 64Mb SDRAM is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access.

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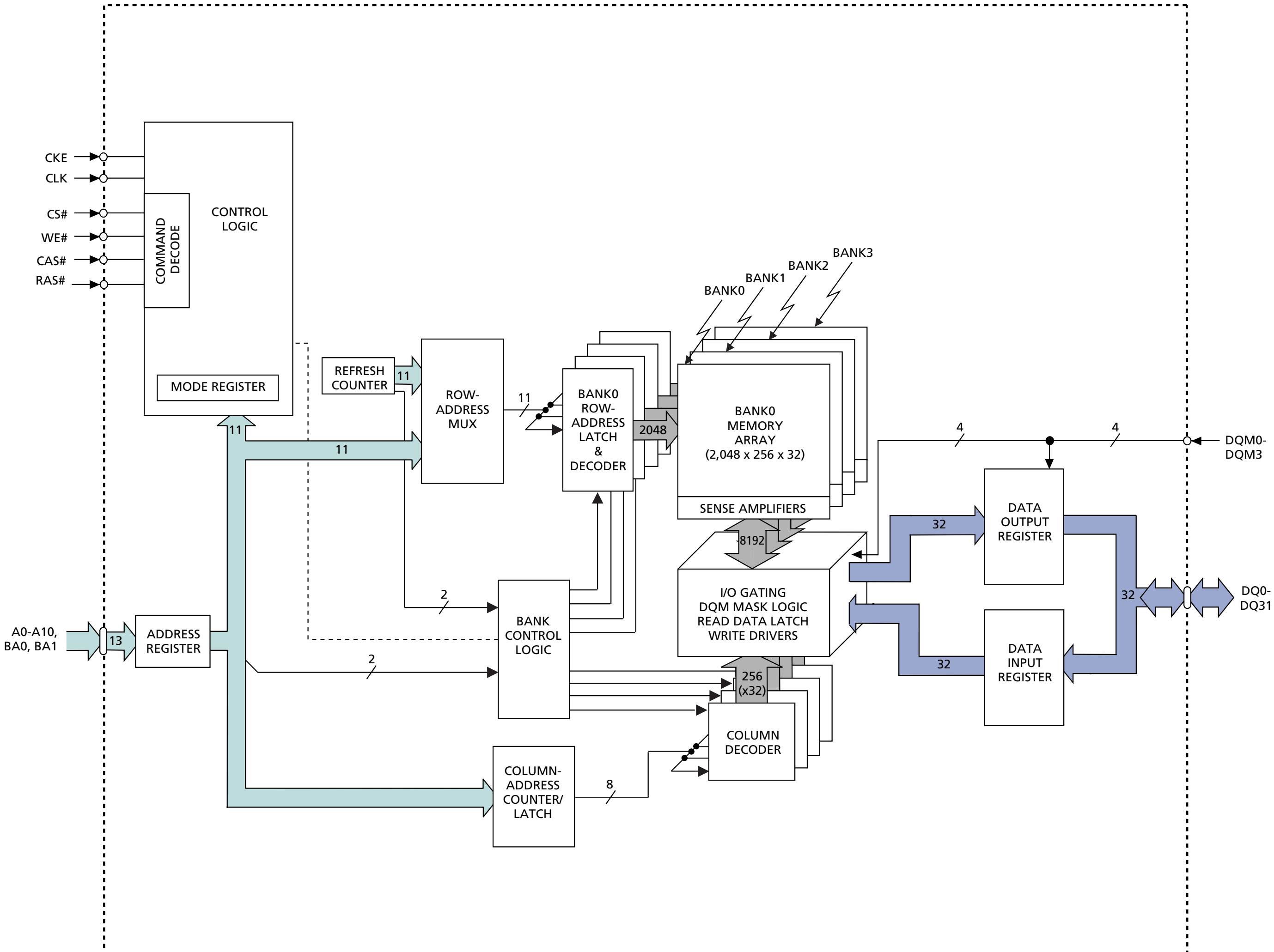
FUNCTIONAL BLOCK DIAGRAM

2 Meg x 32 SDRAM



PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
68	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
67	CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), ACTIVE POWER-DOWN (row active in any bank) or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
20	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
17, 18, 19	WE#, CAS#, RAS#	Input	Command Inputs: WE# , CAS#, and RAS# (along with CS#) define the command being entered.
16, 71, 28, 59	DQM0-DQM3	Input	Input/Output Mask: DQM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) during a READ cycle. DQM0 corresponds to DQ0-DQ7; DQM1 corresponds to DQ8-DQ15; DQM2 corresponds to DQ16-DQ23; and DQM3 corresponds to DQ24-DQ31. DQM0-DQM3 are considered same state when referenced as DQM.
22, 23	BA0, BA1	Input	Bank Address Input(s): BA0 and BA1 define to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied.
25-27, 60-66, 24	A0-A10	Input	Address Inputs: A0-A10 are sampled during the ACTIVE command (row-address A0-A10) and READ/WRITE command (column-address A0-A7 with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
2, 4, 5, 7, 8, 10, 11, 13, 74, 76, 77, 79, 80, 82, 83, 85, 31, 33, 34, 36, 37, 39, 40, 42, 45, 47, 48, 50, 51, 53, 54, 56	DQ0-DQ31	Input/ Output	Data I/Os: Data bus.
14, 21, 30, 57, 69, 70, 73	NC	–	No Connect: These pins should be left unconnected. Pin 70 is reserved for SSTL reference voltage supply.
3, 9, 35, 41, 49, 55, 75, 81	V_{DDQ}	Supply	DQ Power Supply: Isolated on the die for improved noise immunity.
6, 12, 32, 38, 46, 52, 78, 84	V_{SSQ}	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
1, 15, 29, 43	V_{DD}	Supply	Power Supply: +3.3V ±0.3V. (See note 27 on page 35.)
44, 58, 72, 86	V_{SS}	Supply	Ground.

FUNCTIONAL DESCRIPTION

In general, this 64Mb SDRAM (512K x 32 x 4 banks) is a quad-bank DRAM that operates at 3.3V and includes a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 16,777,216-bit banks is organized as 2,048 rows by 256 columns by 32-bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 and BA1 select the bank, A0-A10 select the row). The address bits (A0-A7) registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Initialization

SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Once power is applied to V_{DD} and $V_{DD}Q$ (simultaneously) and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin), the SDRAM requires a 100µs delay prior to issuing any command other than a COMMAND INHIBIT or a NOP. Starting at some point during this 100µs period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands should be applied.

Once the 100µs delay has been satisfied with at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied. All banks must then be precharged, thereby placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for Mode Register programming. Because the Mode Register will power up in an unknown state, it should be loaded prior to applying any operational command.

Register Definition

MODE REGISTER

The Mode Register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, an operating mode and a write burst mode, as shown in Figure 1. The Mode Register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode Register bits M0-M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4-M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the write burst mode, and M10 is reserved for future use.

The Mode Register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Burst Length

Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 1. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4, or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

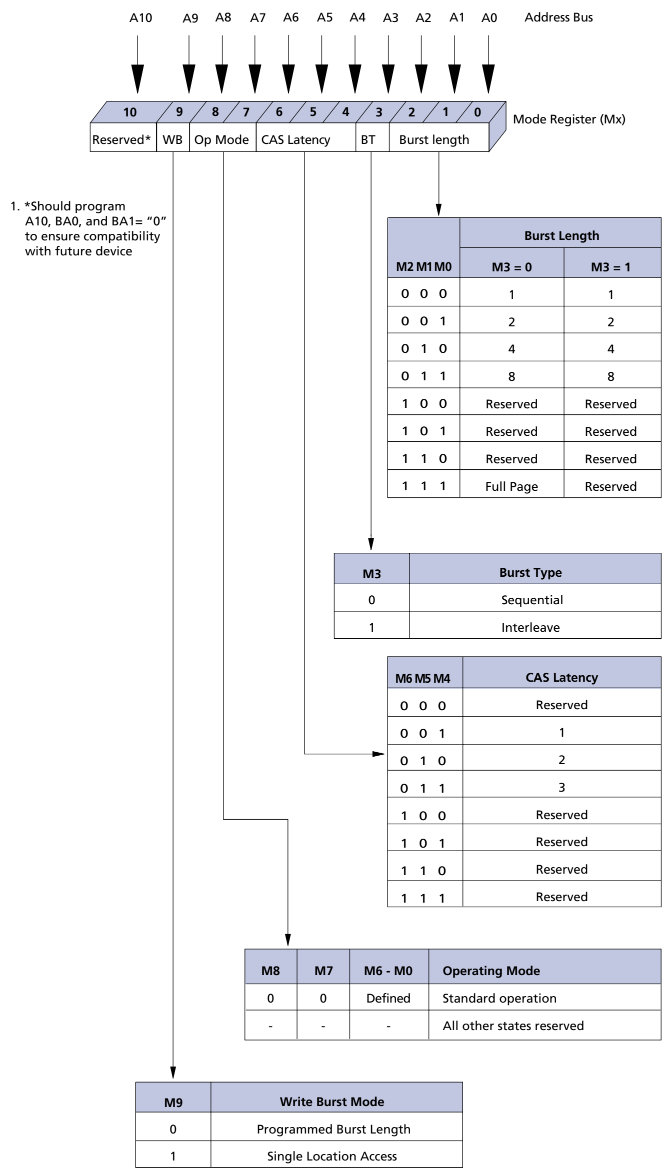
When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-A7 when the burst length is set to two; by A2-A7 when the burst length is set to four; and by A3-A7 when the burst length is set to eight. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 1.

Figure 1
Mode Register Definition



M2 M1 M0	Burst Length M3 = 0	Burst Length M3 = 1
0 0 0	1	1
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Full Page	Reserved

M3	Burst Type
0	Sequential
1	Interleave

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	1
0 1 0	2
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

M8	M7	M6 - M0	Operating Mode
0	0	Defined	Standard operation
-	-	-	All other states reserved

M9	Write Burst Mode
0	Programmed Burst Length
1	Single Location Access

Table 1
Burst Definition

Burst Length	Starting Column Address	Order of Accesses Within a Burst: Type = Sequential	Order of Accesses Within a Burst: Type = Interleaved
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (256)	n = A0-A7 (Location 0-256)	Cn, Cn + 1, Cn + 2 Cn + 3, Cn + 4... ...Cn - 1, Cn...	Not Supported

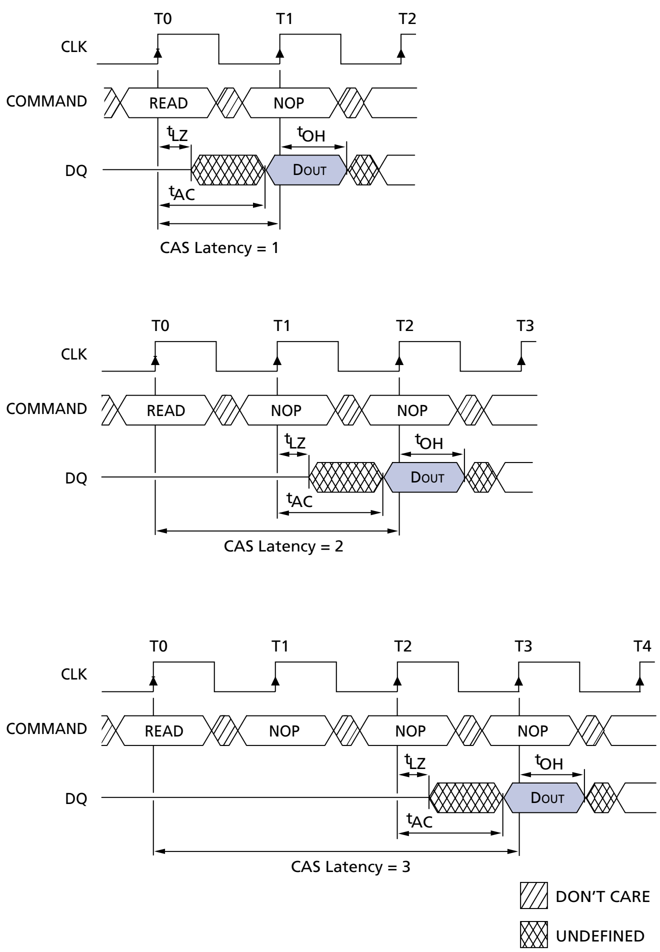
NOTE:
1. For a burst length of two, A1-A7 select the block-of-two burst; A0 selects the starting column within the block.
2. For a burst length of four, A2-A7 select the block-of-four burst; A0-A1 select the starting column within the block.
3. For a burst length of eight, A3-A7 select the block-of-eight burst; A0-A2 select the starting column within the block.
4. For a full-page burst, the full row is selected and A0-A7 select the starting column.
5. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
6. For a burst length of one, A0-A7 select the unique column to be accessed, and mode register bit M3 is ignored.

CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to one, two or three clocks.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available by clock edge *n* + *m*. The DQs will start driving as a result of the clock edge one cycle earlier (*n* + *m* - 1), and provided that the relevant access times are met, the data will be valid by clock edge *n* + *m*. For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the DQs will start driving after T1 and the data will be valid by T2, as shown in Figure 2. Table 2 below indicates the operating frequencies at which each CAS latency setting can be used.

Figure 2
CAS Latency



Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both READ and WRITE bursts.

Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Write Burst Mode

When M9 = 0, the burst length programmed via M0-M2 applies to both READ and WRITE bursts; when M9 = 1, the programmed burst length applies to READ bursts, but write accesses are single-location (nonburst) accesses.

Table 2
CAS Latency

SPEED	ALLOWABLE OPERATING FREQUENCY (MHz)		
	CAS LATENCY = 1	CAS LATENCY = 2	CAS LATENCY = 3
- 5	-	-	≤200
-55	-	-	≤183
- 6	≤50	≤100	≤166
- 7	≤50	≤100	≤143

Commands

Truth Table 1 provides a quick reference of available commands. This is followed by a written description of each command. Three additional Truth Tables appear following the Operation section; these tables provide current state/next state information.

TRUTH TABLE 1 – COMMANDS AND DQM OPERATION

(Note: 1)

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	DQM	ADDR	DQs	NOTES
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	3
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H[8]	Bank/Col	X	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H[8]	Bank/Col	Valid	4
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op-Code	X	2
Write Enable/Output Enable	–	–	–	–	L	–	Active	8
Write Inhibit/Output High-Z	–	–	–	–	H	–	High-Z	8

NOTE:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. A0-A10 define the op-code written to the Mode Register.
3. A0-A10 provide row address, BA0 and BA1 determine which bank is made active.
4. A0-A7 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0 and BA1 determine which bank is being read from or written to.
5. A10 LOW: BA0 and BA1 determine the bank being precharged. A10 HIGH: All banks precharged and BA0 and BA1 are "Don't Care."
6. This command is AUTO REFRESH if CKE is HIGH; SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
8. Activates or deactivates the DQs during WRITEs (zero-clock delay) and READs (two-clock delay). DQM0 controls DQ0-DQ7; DQM1 controls DQ8-DQ15; DQM2 controls DQ16-DQ23; and DQM3 controls DQ24-DQ31.

COMMAND INHIBIT

The COMMAND INHIBIT function prevents new commands from being executed by the SDRAM, regardless of whether the CLK signal is enabled. The SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to an SDRAM which is selected (CS# is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER

The mode register is loaded via inputs A0-A10. See mode register heading in the Register Definition section. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until ^{t}MRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0 and BA1 inputs selects the bank, and the address provided on inputs A0-A10 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0 and BA1 (B1) inputs selects the bank, and the address provided on inputs A0-A7 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Read data appears on the DQs subject to the logic level on the DQM inputs two clocks earlier. If a given DQMx signal was registered HIGH, the corresponding DQs will be High-Z two clocks later; if the DQMx signal was registered LOW, the corresponding DQs will provide valid data. DQM0 corresponds to DQ0-DQ7, DQM1 corresponds to DQ8-DQ15, DQM2 corresponds to DQ16-DQ23 and DQM3 corresponds to DQ24-DQ31.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0 and BA1 inputs selects the bank, and the address provided on inputs A0-A7 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered LOW, the corresponding data will be written to memory; if the DQM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (^{t}RP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0 and BA1 select the bank. Otherwise BA0 and BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

AUTO PRECHARGE

Auto precharge is a feature which performs the same individual-bank PRECHARGE function described above, without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A PRECHARGE of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst, except in the full-page burst mode, where auto precharge does not apply. Auto precharge is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (^{t}RP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in the Operation section of this data sheet.

BURST TERMINATE

The BURST TERMINATE command is used to truncate either fixed-length or full-page bursts. The most recently registered READ or WRITE command prior to the BURST TERMINATE command will be truncated, as shown in the Operation section of this data sheet.

AUTO REFRESH

AUTO REFRESH is used during normal operation of the SDRAM and is analagous to CAS#-BEFORE-RAS# (CBR) REFRESH in conventional DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required.

The addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an AUTO REFRESH command. The 64Mb SDRAM requires 4,096 AUTO REFRESH cycles every 64ms (^{t}REF), regardless of width option. Providing a distributed AUTO REFRESH command every 15.625µs will meet the refresh requirement and ensure that each row is refreshed. Alternatively, 4,096 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate (^{t}RC), once every 64ms.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). Once the SELF REFRESH command is registered, all the inputs to the SDRAM become "Don't Care" with the exception of CKE, which must remain LOW.

Once self refresh mode is engaged, the SDRAM provides its own internal clocking, causing it to perform its own AUTO REFRESH cycles. The SDRAM must remain in self refresh mode for a minimum period equal to ^{t}RAS and may remain in self refresh mode for an indefinite period beyond that.

The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) prior to CKE going back HIGH. Once CKE is HIGH, the SDRAM must have NOP commands issued (a minimum of two clocks) for ^{t}XSR because time is required for the completion of any internal refresh in progress.

Upon exiting SELF REFRESH mode, AUTO REFRESH commands must be issued every 15.625ms or less as both SELF REFRESH and AUTO REFRESH utililze the row refresh counter.

Operation

BANK/ROW ACTIVATION

Before any READ or WRITE commands can be issued to a bank within the SDRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated. See Figure 3.

After opening a row (issuing an ACTIVE command), a READ or WRITE command may be issued to that row, subject to the ^{t}RCD specification. ^{t}RCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be issued. For example, a ^{t}RCD specification of 20ns with a 125 MHz clock (8ns period) results in 2.5 clocks, rounded to 3. This is reflected in Figure 4, which covers any case where 2 < ^{t}RCD (MIN)/^{t}CK - 3. (The same procedure is used to convert other specification limits from time units to clock cycles.)

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by ^{t}RC.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by ^{t}RRD.

Figure 3
Activating a Specific Row in a Specific Bank

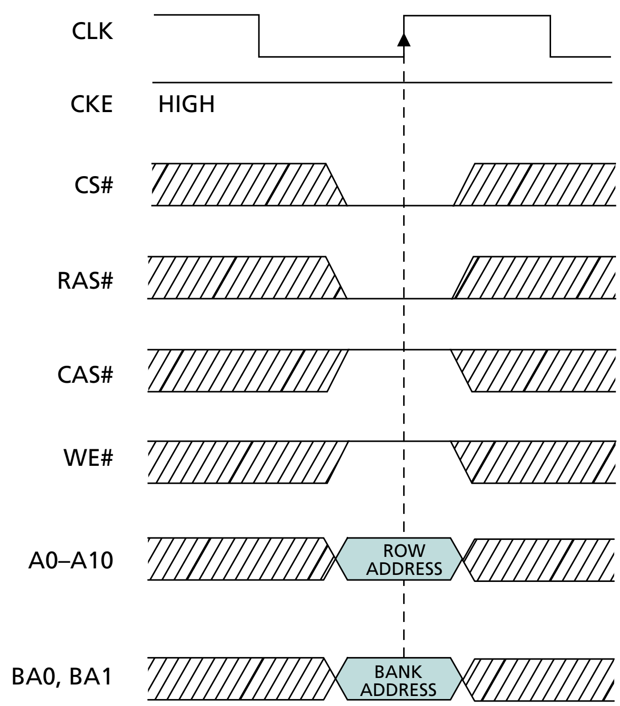
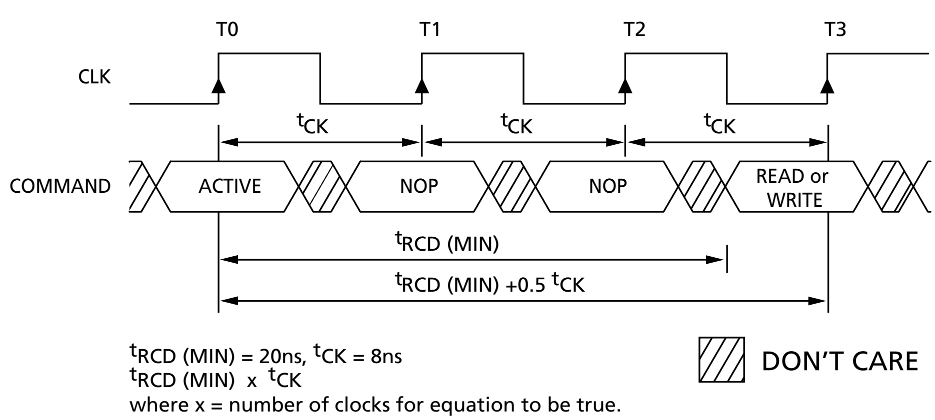


Figure 4
Example: Meeting ^{t}RCD (MIN) When 2 < ^{t}RCD (MIN)/^{t}CK - 3



READs

READ bursts are initiated with a READ command, as shown in Figure 5.

The starting column and bank addresses are provided with the READ command, and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic READ commands used in the following illustrations, auto precharge is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid by the next positive clock edge. Figure 6 shows general timing for each possible CAS latency setting.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z. A full-page burst will continue until terminated. (At the end of the page, it will wrap to column 0 and continue.)

Data from any READ burst may be truncated with a subsequent READ command, and data from a fixed-length READ burst may be immediately followed by data from a READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst that is being truncated. The new READ command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* equals the CAS latency minus one. This is shown in Figure 7 for CAS latencies of one, two and

Figure 5
READ Command

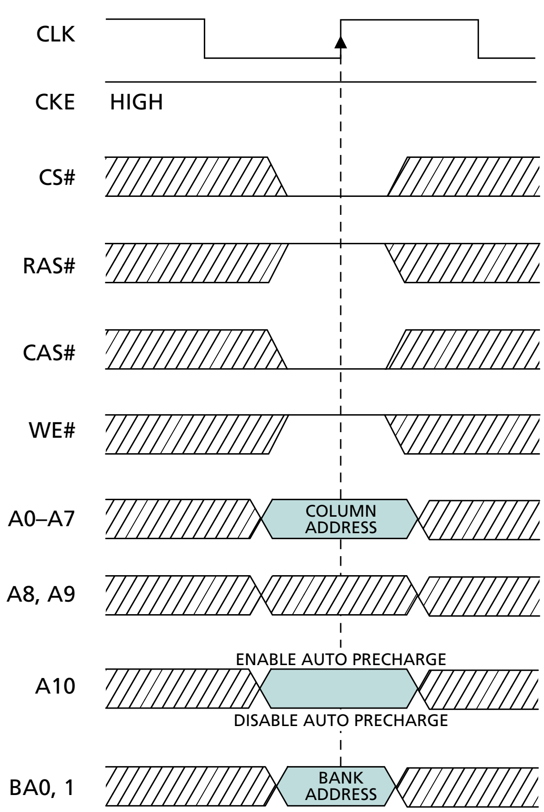
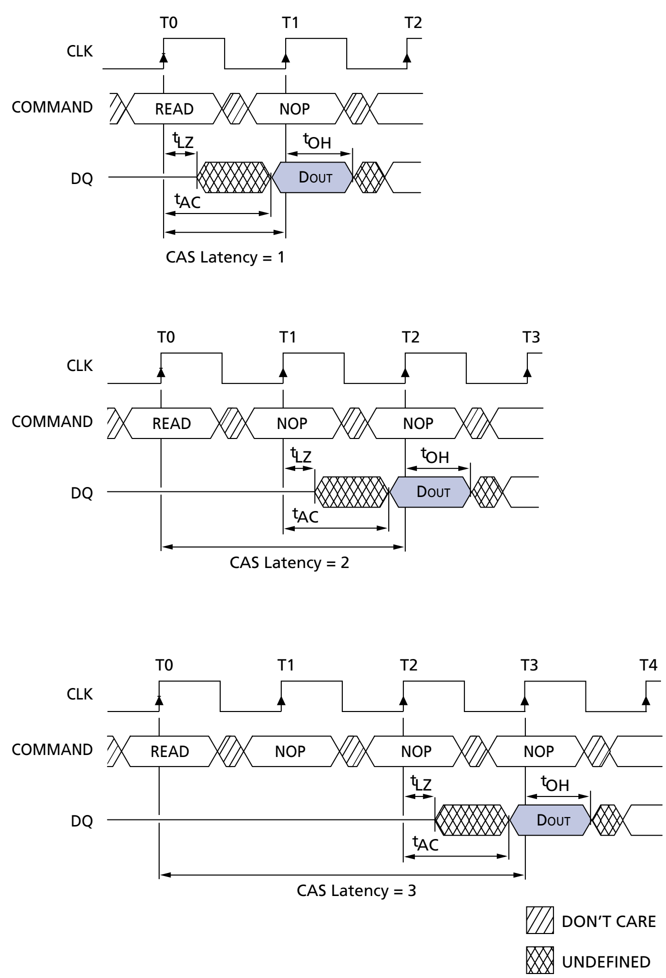
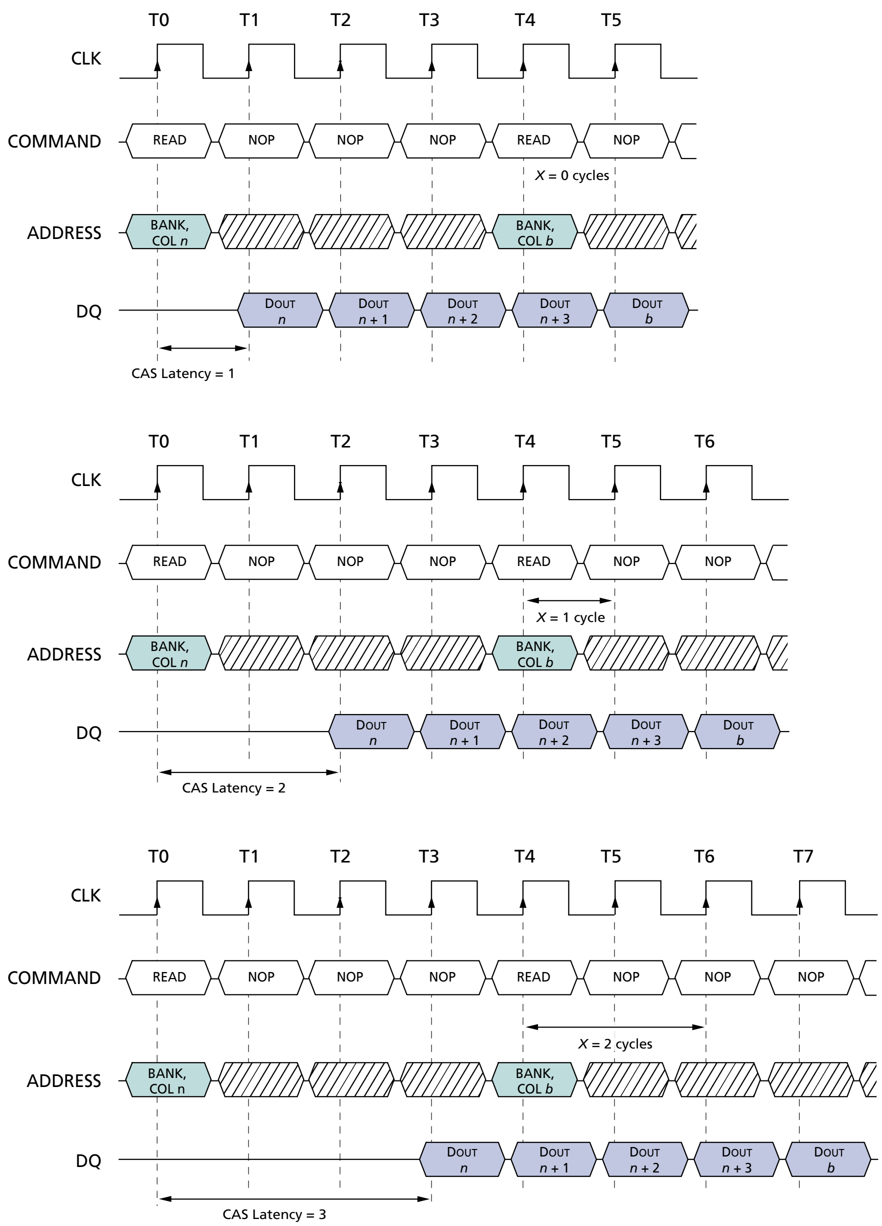


Figure 6
CAS Latency



three; data element $n + 3$ is either the last of a burst of four or the last desired of a longer burst. This 64Mb SDRAM uses a pipelined architecture and therefore does not require the $2n$ rule associated with a prefetch architecture. A READ command can be initiated on any clock cycle following a previous READ command. Full-speed random read accesses can be performed to the same bank, as shown in Figure 8, or each subsequent READ may be performed to a different bank.

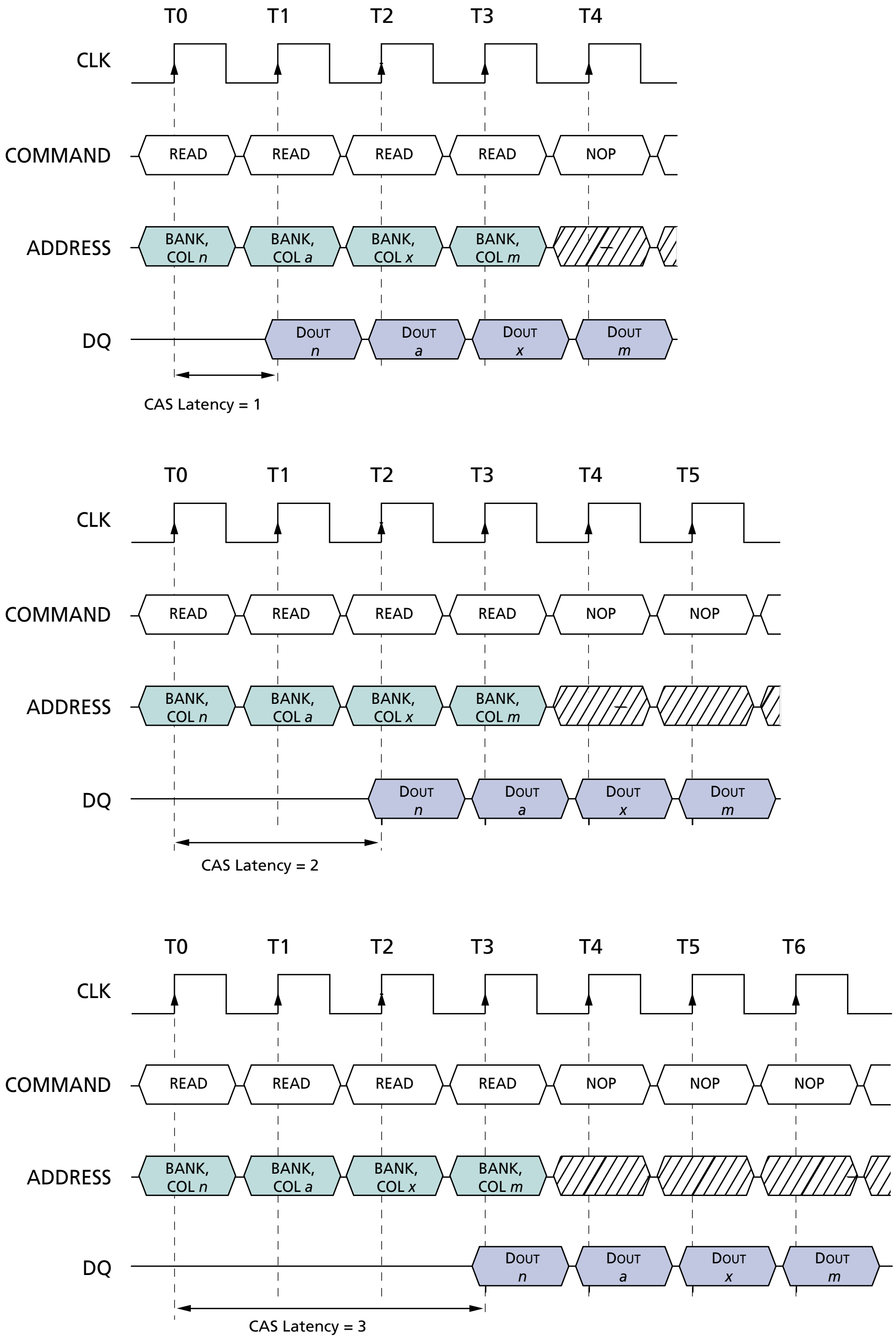
Figure 7
Consecutive READ Bursts



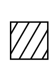
NOTE: Each READ command may be to either bank. DQM is LOW.

DON'T CARE

Figure 8
Random READ Accesses

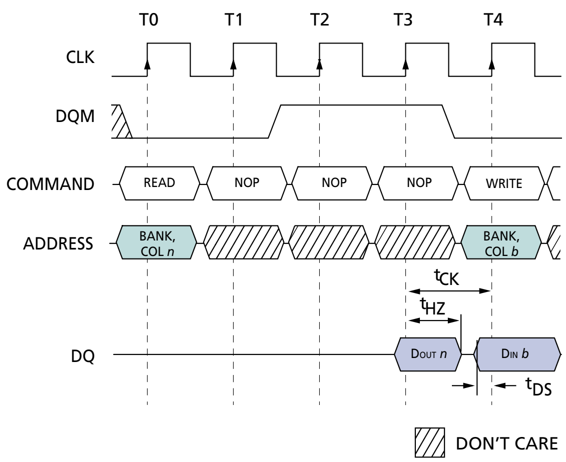


NOTE: Each READ command may be to either bank. DQM is LOW.



Data from any READ burst may be truncated with a subsequent WRITE command, and data from a fixed-length READ burst may be immediately followed by data from a WRITE command (subject to bus turn-around limitations). The WRITE burst may be initiated on the clock edge immediately following the last (or last desired) data element from the READ burst, provided that I/O contention can be avoided. In a given system design, there may be a possibility that the device driving the input data will go Low-Z before the SDRAM DQs go High-Z. In this case, at least a single-cycle delay should occur between the last read data and the WRITE command.

Figure 9
READ to WRITE

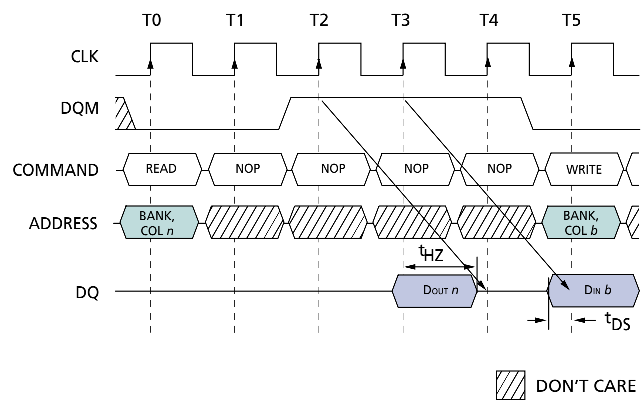


NOTE: A CAS latency of three is used for illustration. The READ command may be to any bank, and the WRITE command

The DQM input is used to avoid I/O contention, as shown in Figures 9 and 10. The DQM signal must be asserted (HIGH) at least two clocks prior to the WRITE command (DQM latency is two clocks for output buffers) to suppress data-out from the READ. Once the WRITE command is registered, the DQs will go High-Z (or remain High-Z), regardless of the state of the DQM signal; provided the DQM was active on the clock just prior to the WRITE command that truncated the READ command. If not, the second WRITE will be an invalid WRITE. For example, if DQM was low during T4 in Figure 10, then the WRITEs at T5 and T7 would be valid, while the WRITE at T6 would be invalid.

The DQM signal must be de-asserted prior to the WRITE command (DQM latency is zero clocks for input buffers) to ensure that the written data is not masked. Figure 9 shows the case where the clock frequency allows for bus contention to be avoided without adding a NOP cycle, and Figure 10 shows the case where the additional NOP is needed.

Figure 10
READ to WRITE with Extra Clock Cycle

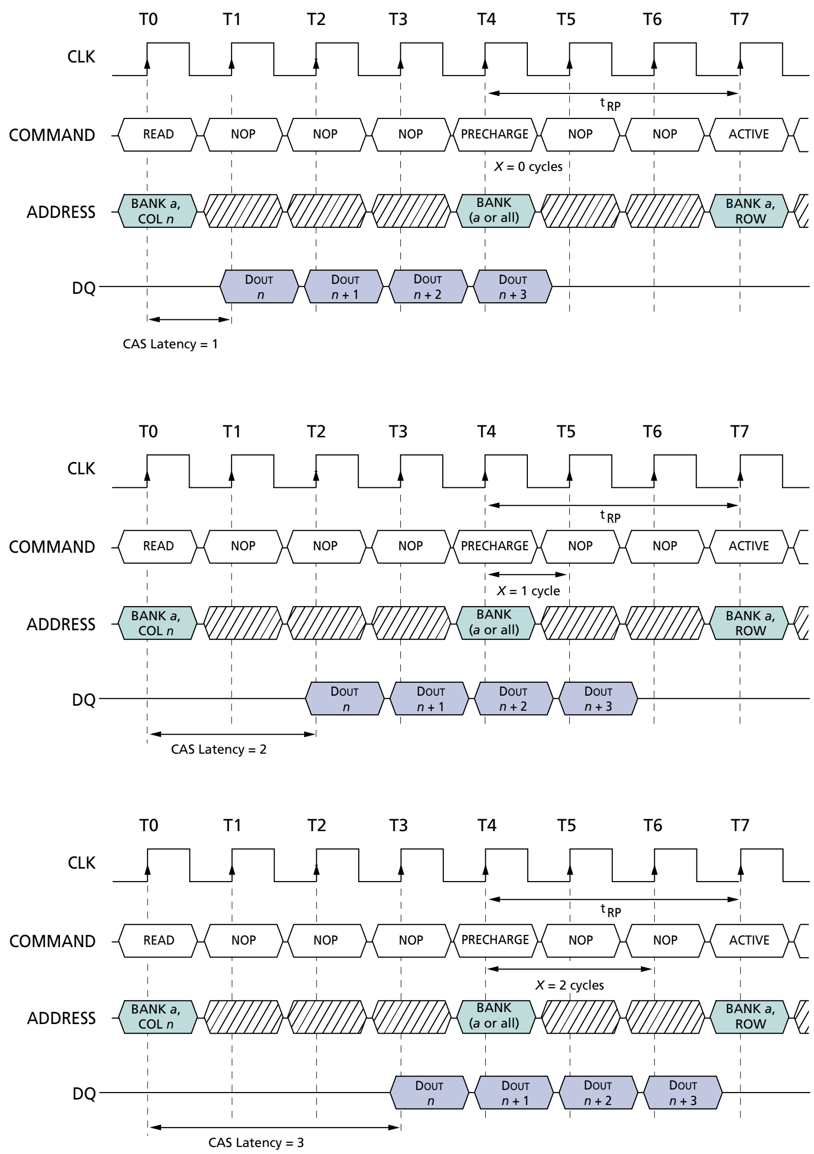


NOTE: A CAS latency of three is used for illustration. The READ command may be to any bank, and the WRITE command may be to any bank.

A fixed-length READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that auto precharge was not activated), and a full-page burst may be truncated with a PRECHARGE command to the same bank. The PRECHARGE command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* equals the CAS latency minus one. This is shown in Figure 11 for each possible CAS latency; data element *n* + 3 is either the last of a burst of four or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^tRP is met. Note that part of the row precharge time is hidden during the access of the last data element(s).

In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same

Figure 11
READ to PRECHARGE



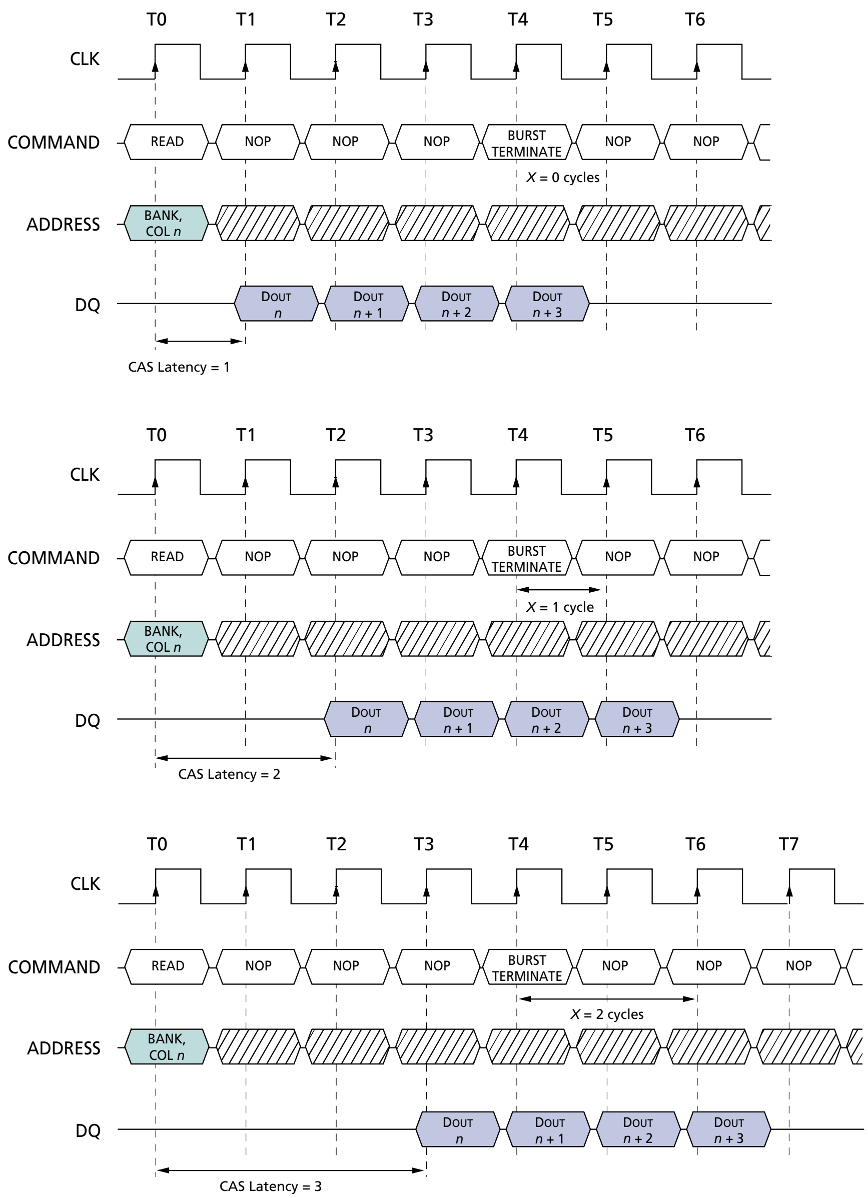
NOTE: DQM is LOW.

DON'T CARE

operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the PRECHARGE command is that it can be used to truncate fixed-length or full-page bursts.

Full-page READ bursts can be truncated with the BURST TERMINATE command, and fixed-length READ bursts may be truncated with a BURST TERMINATE command, provided that auto precharge was not activated. The BURST TERMINATE command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* equals the CAS latency minus one. This is shown in Figure 12 for each possible CAS latency; data element *n* + 3 is the last desired data element of a longer burst.

Figure 12
Terminating a READ Burst



NOTE: DQM is LOW.

WRITEs

WRITE bursts are initiated with a WRITE command, as shown in Figure 13.

The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations,auto precharge is disabled.

During WRITE bursts, the first valid data-in element will be registered coincident with the WRITE command. Subsequent data elements will be registered on each successive positive clock edge. Upon completion of a fixed-length burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data will be ignored (see Figure 14). A full-page burst will continue until terminated. (At the end of the page, it will wrap to column 0 and continue.)

Data for any WRITE burst may be truncated with a subsequent WRITE command, and data for a fixed-length WRITE burst may be immediately followed by data for a WRITE command. The new WRITE command can be issued on any clock following the previous WRITE command, and the data provided coincident with the new command applies to the new command. An example is shown in Figure 15. Data $n + 1$ is either the last of a burst of two or the last desired of a longer burst. This 64Mb SDRAM uses a pipelined architecture and therefore does not require the $2n$ rule associated with a prefetch architecture. A WRITE command can be initiated on any clock cycle following a previous WRITE command. Full-speed random write accesses within a page can be performed to the same bank, as shown in Figure 16, or each subsequent WRITE may be performed to a different bank.

Figure 13
WRITE Command

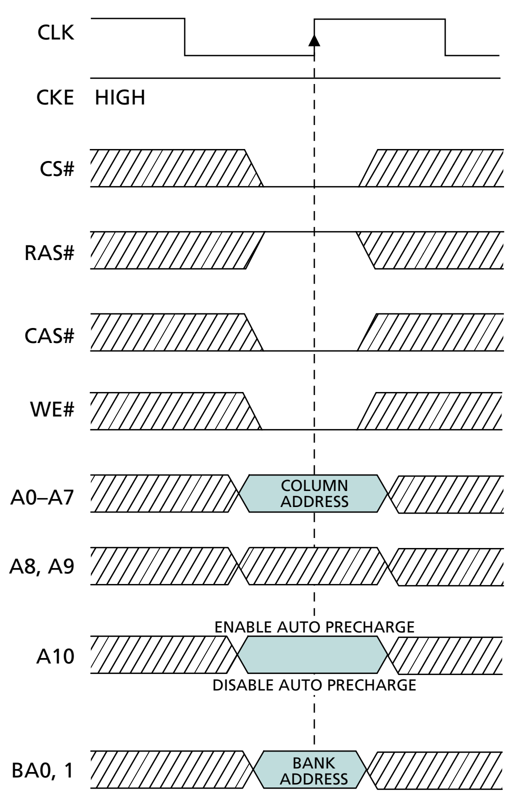


Figure 14
WRITE Burst

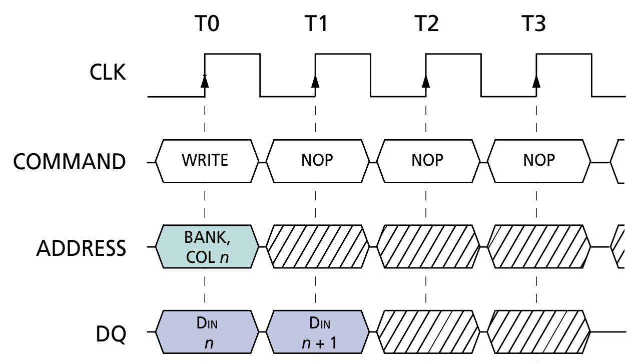
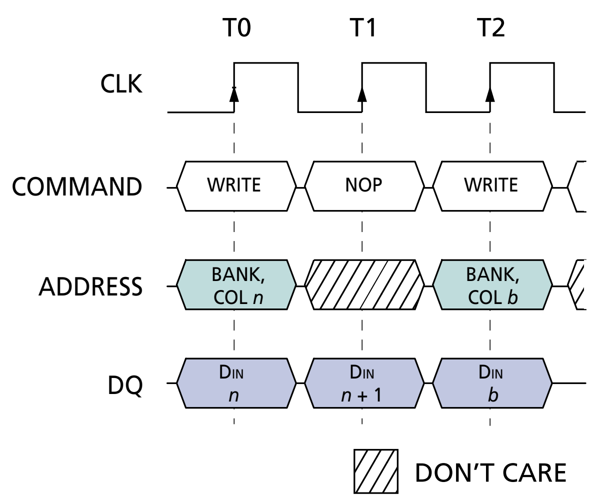


Figure 15
WRITE to WRITE



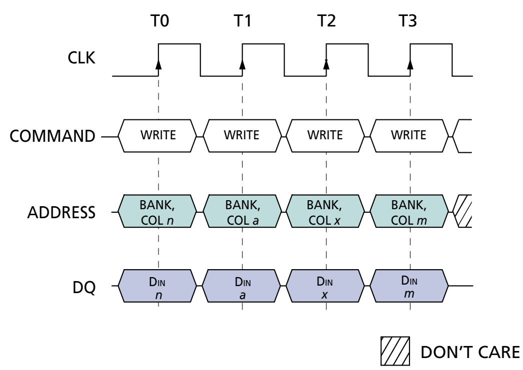
NOTE: DQM is LOW. Each WRITE command may be to any bank.

Data for any WRITE burst may be truncated with a subsequent READ command, and data for a fixed-length WRITE burst may be immediately followed by a READ command. Once the READ command is registered, the data inputs will be ignored, and WRITEs will not be executed. An example is shown in Figure 17. Data *n* + 1 is either the last of a burst of two or the last desired of a longer burst.

Data for a fixed-length WRITE burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that auto precharge was not activated), and a full-page WRITE burst may be truncated with a PRECHARGE command to the same bank. The PRECHARGE command should be issued ^tWR after the clock edge at which the last desired input data element is registered. The "two-clock" write-back requires at least one clock plus time, regardless of frequency, in auto precharge mode. In addition, when truncating a WRITE burst, the DQM signal must be used to mask input data for the clock edge prior to, and the clock edge coincident with, the PRECHARGE command. An example is shown in Figure 18. Data *n* + 1 is either the last of a burst of two or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^tRP is met. The precharge will actually begin coincident with the clock-edge (T2 in Figure 18) on a "one-clock" ^tWR and sometime between the first and second clock on a "two-clock" ^tWR (between T2 and T3 in Figure 18.)

In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the PRECHARGE command is that it can be used to truncate fixed-length or full-page bursts.

Figure 16
Random WRITE Cycles



NOTE: Each WRITE command may be to any bank. DQM is LOW.

Figure 17
WRITE to READ

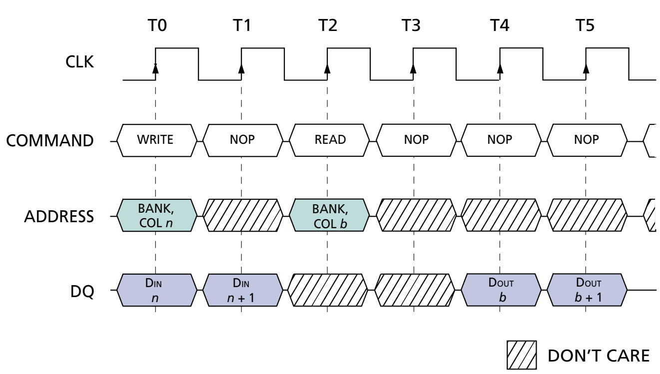
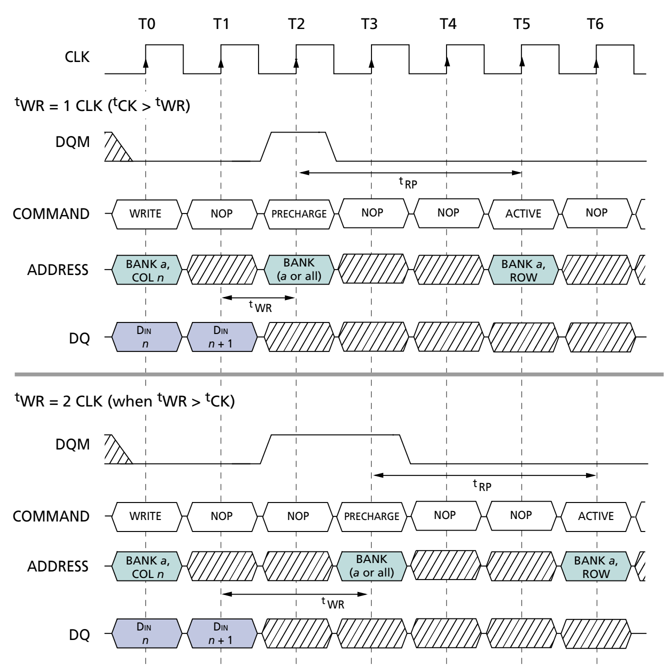


Figure 18
WRITE to PRECHARGE

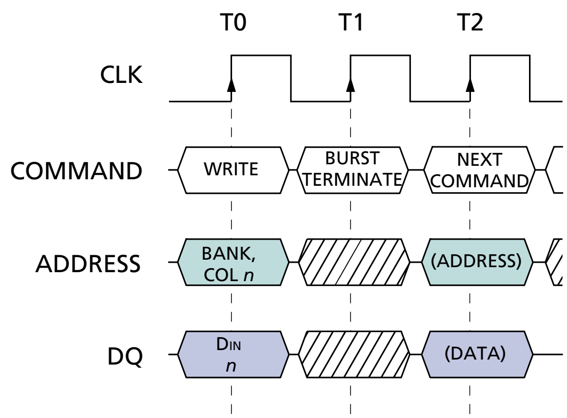


NOTE: DQM could remain LOW in this example if the WRITE burst is a fixed length of two.

DON'T CARE

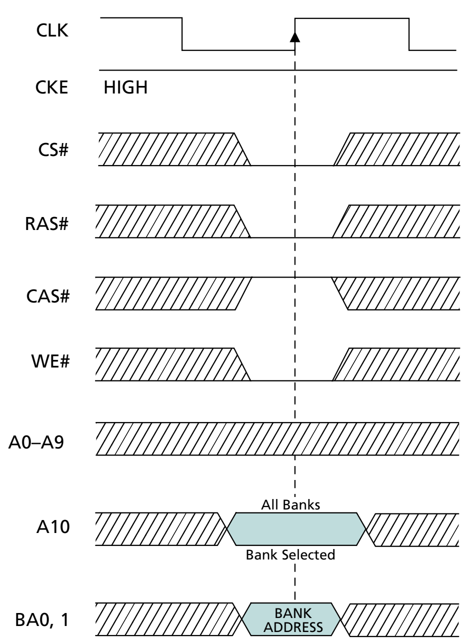
Fixed-length or full-page WRITE bursts can be truncated with the BURST TERMINATE command. When truncating a WRITE burst, the input data applied coincident with the BURST TERMINATE command will be ignored. The last data written (provided that DQM is LOW at that time) will be the input data applied one clock previous to the BURST TERMINATE command. This is shown in Figure 19, where data *n* is the last desired data element of a longer burst.

Figure 19
Terminating a WRITE Burst



NOTE: DQMs are LOW.

Figure 20
PRECHARGE Command



PRECHARGE

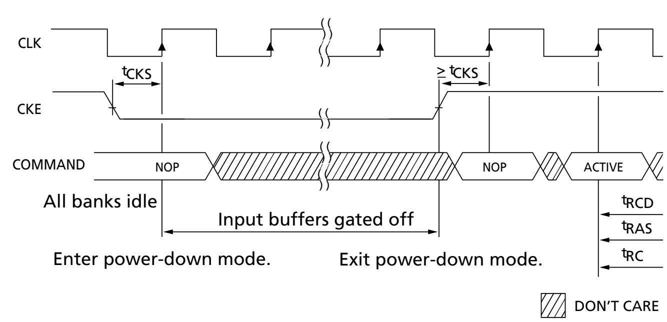
The PRECHARGE command (Figure 20) is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (^{t}RP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0 and BA1 select the bank. When all banks are to be precharged, inputs BA0 and BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

POWER-DOWN

Power-down occurs if CKE is registered LOW coincident with a NOP or COMMAND INHIBIT when no accesses are in progress (see Figure 21). If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in either bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CKE, for maximum power savings while in standby. The device may not remain in the power-down state longer than the refresh period (64ms) since no refresh operations are performed in this mode.

The power-down state is exited by registering a NOP or COMMAND INHIBIT and CKE HIGH at the desired clock edge (meeting ^{t}CKS).

Figure 21
Power-Down



CLOCK SUSPEND

The clock suspend mode occurs when a column access/burst is in progress and CKE is registered LOW. In the clock suspend mode, the internal clock is deactivated, "freezing" the synchronous logic.

For each positive clock edge on which CKE is sampled LOW, the next internal positive clock edge is suspended. Any command or data present on the input pins at the time of a suspended internal clock edge is ignored; any data present on the DQ pins remains driven; and burst counters are not incremented, as long as the clock is suspended. (See examples in Figures 22 and 23.)

Clock suspend mode is exited by registering CKE HIGH; the internal clock and related operation will resume on the subsequent positive clock edge.

BURST READ/SINGLE WRITE

The burst read/single write mode is entered by programming the write burst mode bit (M9) in the Mode Register to a logic 1. In this mode, all WRITE commands result in the access of a single column location (burst of one), regardless of the programmed burst length. READ commands access columns according to the programmed burst length and sequence, just as in the normal mode of operation (M9 = 0).

Figure 22
CLOCK SUSPEND During WRITE Burst

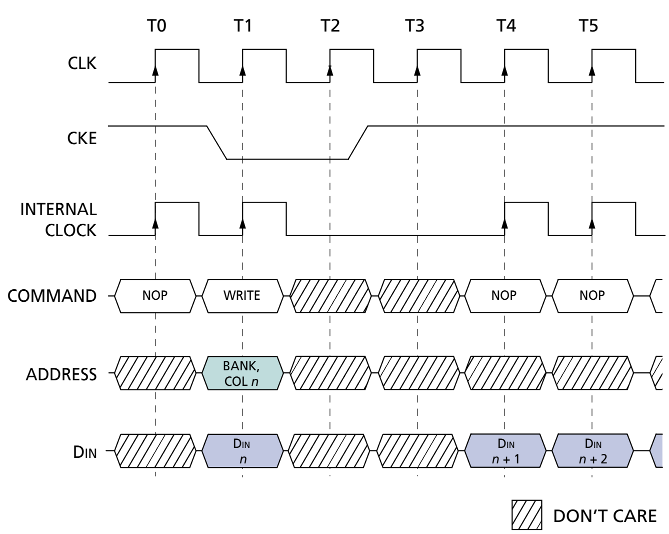
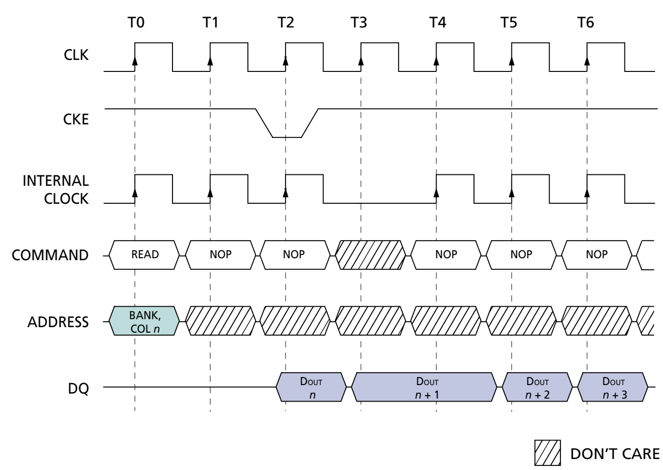


Figure 23
CLOCK SUSPEND During READ Burst



NOTE: For this example, CAS latency = 2, burst length = 4 or greater, and DQM is LOW.

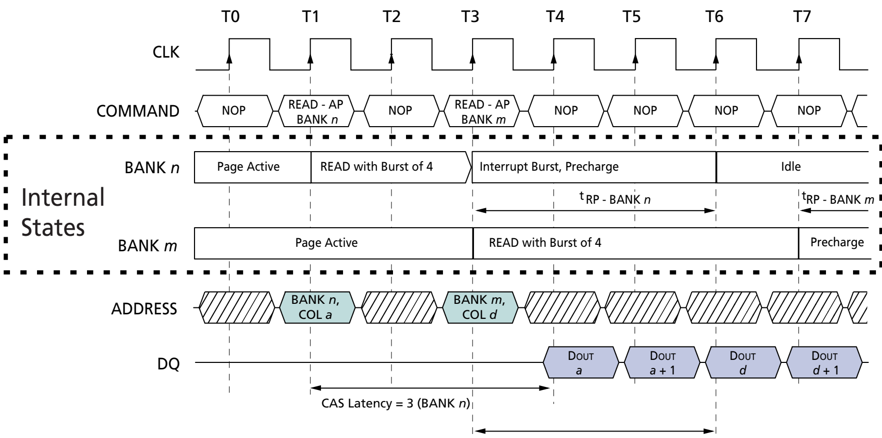
CONCURRENT AUTO PRECHARGE

An access command to (READ or WRITE) another bank while an access command with auto precharge enabled is executing is not allowed by SDRAMs, unless the SDRAM supports CONCURRENT AUTO PRECHARGE. Micron SDRAMs support CONCURRENT AUTO PRECHARGE. Four cases where CONCURRENT AUTO PRECHARGE occurs are defined below.

READ with auto precharge

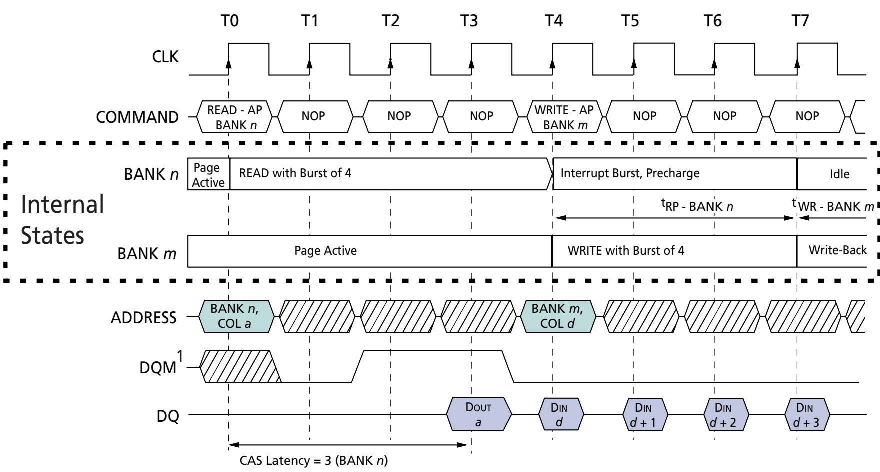
1. Interrupted by a READ (with or without auto precharge): A READ to bank *m* will interrupt a READ on bank *n*, CAS latency later. The PRECHARGE to bank *n* will begin when the READ to bank *m* is registered (Figure 24).
2. Interrupted by a WRITE (with or without auto precharge): A WRITE to bank *m* will interrupt a READ on bank *n* when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The PRECHARGE to bank n will begin when the WRITE to bank m is registered (Figure 25).

Figure 24
READ With Auto Precharge Interrupted by a READ



NOTE: DQM is LOW.

Figure 25
READ With Auto Precharge Interrupted by a WRITE



NOTE: 1. DQM is HIGH at T2 to prevent DOUT-*a*+1 from contending with DIN-*d* at T4.

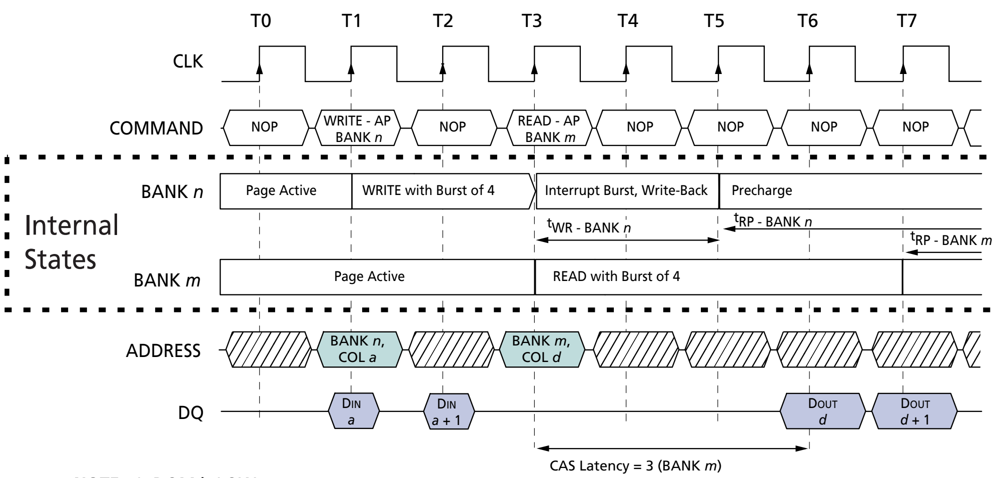
DON'T CARE

WRITE WITH AUTO PRECHARGE

3. Interrupted by a READ (with or without auto precharge): A READ to bank *m* will interrupt a WRITE on bank *n* when registered, with the data-out appearing CAS latency later. The PRECHARGE to bank *n* will begin after ^tWR is met, where ^tWR begins when the READ to bank *m* is registered. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m* (Figure 26).

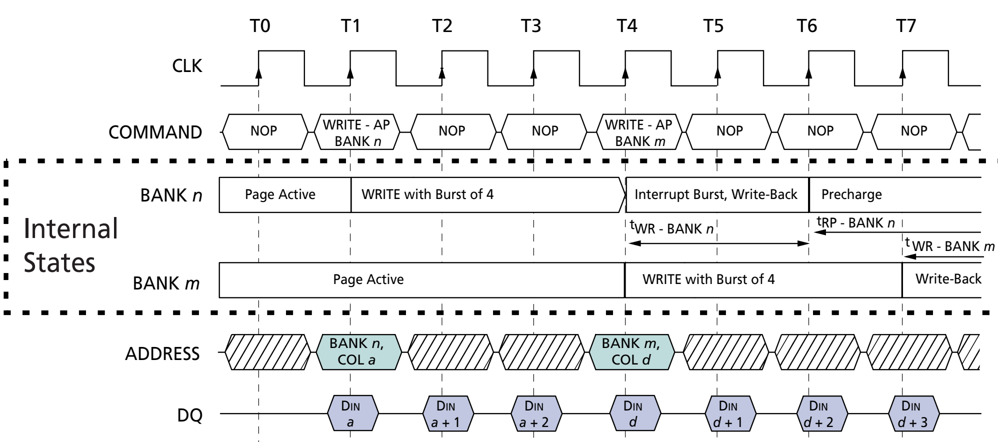
4. Interrupted by a WRITE (with or without auto precharge): A WRITE to bank *m* will interrupt a WRITE on bank *n* when registered. The PRECHARGE to bank *n* will begin after ^tWR is met, where ^tWR begins when the WRITE to bank *m* is registered. The last valid data WRITE to bank *n* will be data registered one clock prior to a WRITE to bank *m* (Figure 27).

Figure 26
WRITE With Auto Precharge Interrupted by a READ



NOTE: 1. DQM is LOW.

Figure 27
WRITE With Auto Precharge Interrupted by a WRITE



NOTE: 1. DQM is LOW.

DON'T CARE

TRUTH TABLE 2 – CKE

(Notes: 1-4)

CKE_{n-1}	CKE_n	CURRENT STATE	$COMMAND_n$	$ACTION_n$	NOTES
L	L	Power-Down	X	Maintain Power-Down	
		Self Refresh	X	Maintain Self Refresh	
		Clock Suspend	X	Maintain Clock Suspend	
L	H	Power-Down	COMMAND INHIBIT or NOP	Exit Power-Down	5
		Self Refresh	COMMAND INHIBIT or NOP	Exit Self Refresh	6
		Clock Suspend	X	Exit Clock Suspend	7
H	L	All Banks Idle	COMMAND INHIBIT or NOP	Power-Down Entry	
		All Banks Idle	AUTO REFRESH	Self Refresh Entry	
		Reading or Writing	VALID	Clock Suspend Entry	
H	H		See Truth Table 3		

NOTE:
1. CKE_n is the logic state of CKE at clock edge *n*; CKE_{n-1} was the state of CKE at the previous clock edge.
2. Current state is the state of the SDRAM immediately prior to clock edge *n*.
3. $COMMAND_n$ is the command registered at clock edge *n*, and $ACTION_n$ is a result of $COMMAND_n$.
4. All states and sequences not shown are illegal or reserved.
5. Exiting power-down at clock edge *n* will put the device in the all banks idle state in time for clock edge *n + 1* (provided that ^tCKS is met).
6. Exiting self refresh at clock edge *n* will put the device in the all banks idle state once ^tXSR is met. COMMAND INHIBIT or NOP commands should be issued on any clock edges occurring during the ^tXSR period. A minimum of two NOP commands must be provided during ^tXSR period.
7. After exiting clock suspend at clock edge *n*, the device will resume operation and recognize the next command at clock edge *n + 1*.

TRUTH TABLE 3 – CURRENT STATE BANK *n*, COMMAND TO BANK *n*

(Notes: 1-6; notes appear below and on next page)

CURRENT STATE	CS#	RAS#	CAS#	WE#	COMMAND (ACTION)	NOTES
Any	H	X	X	X	COMMAND INHIBIT (NOP/Continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/Continue previous operation)	
Idle	L	L	H	H	ACTIVE (Select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	LOAD MODE REGISTER	7
	L	L	H	L	PRECHARGE	11
Row Active	L	H	L	H	READ (Select column and start READ burst)	10
	L	H	L	L	WRITE (Select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (Deactivate row in bank or banks)	8
Read (Auto Precharge Disabled)	L	H	L	H	READ (Select column and start new READ burst)	10
	L	H	L	L	WRITE (Select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (Truncate READ burst, start PRECHARGE)	8
	L	H	H	L	BURST TERMINATE	9
Write (Auto Precharge Disabled)	L	H	L	H	READ (Select column and start READ burst)	10
	L	H	L	L	WRITE (Select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (Truncate WRITE burst, start PRECHARGE)	8
	L	H	H	L	BURST TERMINATE	9

NOTE:

1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH (see Truth Table 2) and after ^tXSR has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted, i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.
3. Current state definitions:
   - Idle: The bank has been precharged, and ^tRP has been met.
   - Row Active: A row in the bank has been activated, and ^tRCD has been met. No data bursts/accesses and no register accesses are in progress.
   - Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
   - Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Truth Table 3, and according to Truth Table 4.
   - Precharging: Starts with registration of a PRECHARGE command and ends when ^tRP is met. Once ^tRP is met, the bank will be in the idle state.
   - Row Activating: Starts with registration of an ACTIVE command and ends when ^tRCD is met. Once ^tRCD is met, the bank will be in the row active state.
   - Read w/Auto Precharge Enabled: Starts with registration of a READ command with auto precharge enabled and ends when ^tRP has been met. Once ^tRP is met, the bank will be in the idle state.

NOTE (continued):

Write w/Auto
Precharge Enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when ^{t}RP has been met. Once ^{t}RP is met, the bank will be in the idle state.

5. The following states must not be interrupted by any executable command; COMMAND INHIBIT or NOP commands must be applied on each positive clock edge during these states.

   Refreshing: Starts with registration of an AUTO REFRESH command and ends when ^{t}RC is met. Once ^{t}RC is met, the SDRAM will be in the all banks idle state.

   Accessing Mode
   Register: Starts with registration of a LOAD MODE REGISTER command and ends when ^{t}MRD has been met. Once ^{t}MRD is met, the SDRAM will be in the all banks idle state.

   Precharging All: Starts with registration of a PRECHARGE ALL command and ends when ^{t}RP is met. Once ^{t}RP is met, all banks will be in the idle state.
6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle.
8. May or may not be bank-specific; if all banks are to be precharged, all must be in a valid state for precharging.
9. Not bank-specific; BURST TERMINATE affects the most recent READ or WRITE burst, regardless of bank.
10. READs or WRITEs listed in the Command (Action) column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
11. Does not affect the state of the bank and acts as a NOP to that bank.

TRUTH TABLE 4 – CURRENT STATE BANK *n*, COMMAND TO BANK *m*

(Notes: 1-6; notes appear below and on next page)

CURRENT STATE	CS#	RAS#	CAS#	WE#	COMMAND (ACTION)	NOTES
Any	H	X	X	X	COMMAND INHIBIT (NOP/Continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/Continue previous operation)	
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank *m*	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	7
	L	H	L	L	WRITE (Select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (Auto Precharge Disabled)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start new READ burst)	7, 10
	L	H	L	L	WRITE (Select column and start WRITE burst)	7, 11
	L	L	H	L	PRECHARGE	9
Write (Auto Precharge Disabled)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	7, 12
	L	H	L	L	WRITE (Select column and start new WRITE burst)	7, 13
	L	L	H	L	PRECHARGE	9
Read (With Auto Precharge)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start new READ burst)	7, 8, 14
	L	H	L	L	WRITE (Select column and start WRITE burst)	7, 8, 15
	L	L	H	L	PRECHARGE	9
Write (With Auto Precharge)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	7, 8, 16
	L	H	L	L	WRITE (Select column and start new WRITE burst)	7, 8, 17
	L	L	H	L	PRECHARGE	9

NOTE:
1. This table applies when CKE_{n-1} was HIGH and CKE_n is HIGH (see Truth Table 2) and after ^tXSR has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted; i.e., the current state is for bank *n* and the commands shown are those allowed to be issued to bank m (assuming that bank *m* is in such a state that the given command is allowable). Exceptions are covered in the notes below.
3. Current state definitions:
   - Idle: The bank has been precharged, and ^tRP has been met.
   - Row Active: A row in the bank has been activated, and ^tRCD has been met. No data bursts/accesses and no register accesses are in progress.
   - Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
   - Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
   - Read w/Auto Precharge Enabled: Starts with registration of a READ command with auto precharge enabled, and ends when ^tRP has been met. Once ^tRP is met, the bank will be in the idle state.

NOTE (continued):

4. AUTO REFRESH, SELF REFRESH, and LOAD MODE REGISTER commands may only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs to bank *m* listed in the Command (Action) column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
8. CONCURRENT AUTO PRECHARGE: Bank *n* will initiate the auto precharge command when its burst has been interrupted by bank *m*'s burst.
9. Burst in bank *n* continues as initiated.
10. For a READ without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the READ on bank *n*, CAS latency later (Figure 7).
11. For a READ without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the READ on bank *n* when registered (Figures 9 and 10). DQM should be used one clock prior to the WRITE command to prevent bus contention.
12. For a WRITE without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the WRITE on bank *n* when registered (Figure 17), with the data-out appearing CAS latency later. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m*.
13. For a WRITE without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the WRITE on bank *n* when registered (Figure 15). The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m*.
14. For a READ with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the READ on bank *n*, CAS latency later. The PRECHARGE to bank *n* will begin when the READ to bank *m* is registered (Figure 24).
15. For a READ with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the READ on bank *n* when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The PRECHARGE to bank *n* will begin when the WRITE to bank *m* is registered (Figure 25).
16. For a WRITE with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the WRITE on bank *n* when registered, with the data-out appearing CAS latency later. The PRECHARGE to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the READ to bank *m* is registered. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m* (Figure 26).
17. For a WRITE with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the WRITE on bank *n* when registered. The PRECHARGE to bank *n* will begin after ^{t}WR is met, where ^{t}WR begins when the WRITE to bank *m* is registered. The last valid WRITE to bank *n* will be data registered one clock prior to the WRITE to bank *m* (Figure 27).

ABSOLUTE MAXIMUM RATINGS*

Voltage on VDD, VDDQ Supply
Relative to VSS .... -1V to +4.6V
Voltage on Inputs, NC or I/O Pins
Relative to VSS .... -1V to +4.6V
Operating Temperature, T_A .... 0°C to +70°C
Extended Temperature .... -40°C to +85°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 6, 27; notes appear on page 35) (VDD, VDDQ = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	VDD, VDDQ	3	3.6	V	27
INPUT HIGH VOLTAGE: Logic 1; All inputs	VIH	2	VDD + 0.3	V	22
INPUT LOW VOLTAGE: Logic 0; All inputs	VIL	-0.3	0.8	V	22
INPUT LEAKAGE CURRENT: Any input 0V ≤ VIN ≤ VDD (All other pins not under test = 0V)	II	-5	5	µA	
OUTPUT LEAKAGE CURRENT: DQs are disabled; 0V ≤ VOUT ≤ VDDQ	IOZ	-5	5	µA	
OUTPUT LEVELS: Output High Voltage (IOUT = -4mA)	VOH	2.4	–	V	
Output Low Voltage (IOUT = 4mA)	VOL	–	0.4	V	

I_{DD} SPECIFICATIONS AND CONDITIONS

(Notes: 1, 6, 11, 13, 27; notes appear on page 35) (V_{DD}, $V_{DD}Q$ = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MAX -6	MAX -7	UNITS	NOTES
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; ^{t}RC = ^{t}RC (MIN); CAS latency = 3	I_{DD1}	150	130	mA	3, 18, 19, 26
STANDBY CURRENT: Power-Down Mode; CKE = LOW; All banks idle	I_{DD2}	2	2	mA	
STANDBY CURRENT: Active Mode; CS# = HIGH; CKE = HIGH; All banks active after ^{t}RCD met; No accesses in progress	I_{DD3}	60	50	mA	3, 12, 19, 26
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All banks active, CAS latency = 3	I_{DD4}	180	160	mA	3, 18, 19, 26
AUTO REFRESH CURRENT: CAS latency = 3; CKE, CS# = HIGH — ^{t}RFC = ^{t}RFC (MIN)	I_{DD5}	225	225	mA	3, 12, 18, 19, 26, 29
SELF REFRESH CURRENT: CKE ≤ 0.2V	I_{DD6}	2	2	mA	4

I_{DD} SPECIFICATIONS AND CONDITIONS

(Notes: 1, 6, 11, 13, 27; notes appear on page 35) (V_{DD}, $V_{DD}Q$ = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MAX -5	MAX -55	UNITS	NOTES
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; ^{t}RC = ^{t}RC (MIN); CAS latency = 3	I_{DD1}	200	190	mA	3, 18, 19, 26
STANDBY CURRENT: Power-Down Mode; CKE = LOW; All banks idle	I_{DD2}	2	2	mA	
STANDBY CURRENT: Active Mode; CS# = HIGH; CKE = HIGH; All banks active after ^{t}RCD met; 19, 26 No accesses in progress	I_{DD3}	80	70	mA	3, 12,
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All banks active, CAS latency = 3	I_{DD4}	280	260	mA	3, 18, 19, 26
AUTO REFRESH CURRENT: CAS latency = 3; CKE, CS# = HIGH — ^{t}RFC = ^{t}RFC (MIN)	I_{DD5}	225	225	mA	3, 12, 18, 19, 26, 29
SELF REFRESH CURRENT: CKE ≤ 0.2V	I_{DD6}	2	2	mA	4

CAPACITANCE

(Note: 2; notes appear on page 35)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Capacitance: CLK	C_{I1}	2.5	4.0	pF
Input Capacitance: All other input-only pins	C_{I2}	2.5	4.0	pF
Input/Output Capacitance: DQs	C_{IO}	4.0	6.5	pF

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 5, 6, 8, 9, 11; notes appear on page 35)

AC CHARACTERISTICS			-5		-55			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from CLK (pos. edge)	CL = 3	$^tAC(3)$		4.5		5	ns	
	CL = 2	$^tAC(2)$		-		-	ns	
	CL = 1	$^tAC(1)$		-		-	ns	
Address hold time		^tAH	1		1		ns	
Address setup time		^tAS	1.5		1.5		ns	
CLK high-level width		^tCH	2		2		ns	
CLK low-level width		^tCL	2		2		ns	
Clock cycle time	CL = 3	$^tCK(3)$	5		5.5		ns	23
	CL = 2	$^tCK(2)$	-		-		ns	23
	CL = 1	$^tCK(1)$	-		-		ns	23
CKE hold time		^tCKH	1		1		ns	
CKE setup time		^tCKS	1.5		1.5		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		^tCMH	1		1		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		^tCMS	1.5		1.5		ns	
Data-in hold time		^tDH	1		1		ns	
Data-in setup time		^tDS	1.5		1.5		ns	
Data-out high-impedance time	CL = 3	$^tHZ(3)$	4.5		5		ns	10
	CL = 2	$^tHZ(2)$	-		-		ns	10
	CL = 1	$^tHZ(1)$	-		-		ns	10
Data-out low-impedance time		^tLZ	1		1		ns	
Data-out hold time		^tOH	1.5		2		ns	
ACTIVE to PRECHARGE command		^tRAS	38.7	120k	38.7	120k	ns	
ACTIVE to ACTIVE command period		^tRC	55		55		ns	
AUTO REFRESH period		^tRFC	60		60		ns	
ACTIVE to READ or WRITE delay		^tRCD	15		16.5		ns	
Refresh period (4,096 rows)		^tREF		64		64	ms	
PRECHARGE command period		^tRP	15		16.5		ns	
ACTIVE bank *a* to ACTIVE bank *b* command		^tRRD	10		11		ns	25
Transition time		^tT	0.3	1.2	0.3	1.2	ns	7
WRITE recovery time		^tWR	2		2		^tCK	24
Exit SELF REFRESH to ACTIVE command		^tXSR	55		55		ns	20

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 5, 6, 8, 9, 11; notes appear on page 35)

AC CHARACTERISTICS			-6		-7			
PARAMETER		**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Access time from CLK (pos. edge)	CL = 3	^{t}AC (3)		5.5		5.5	ns	
	CL = 2	^{t}AC (2)		7.5		8	ns	
	CL = 1	^{t}AC (1)		17		17	ns	
Address hold time		^{t}AH	1		1		ns	
Address setup time		^{t}AS	1.5		2		ns	
CLK high-level width		^{t}CH	2.5		2.75		ns	
CLK low-level width		^{t}CL	2.5		2.75		ns	
Clock cycle time	CL = 3	^{t}CK (3)	6		7		ns	23
	CL = 2	^{t}CK (2)	10		10		ns	23
	CL = 1	^{t}CK (1)	20		20		ns	23
CKE hold time		^{t}CKH	1		1		ns	
CKE setup time		^{t}CKS	1.5		2		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		^{t}CMH	1		1		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		^{t}CMS	1.5		2		ns	
Data-in hold time		^{t}DH	1		1		ns	
Data-in setup time		^{t}DS	1.5		2		ns	
Data-out high-impedance time	CL = 3	^{t}HZ (3)		5.5		5.5	ns	10
	CL = 2	^{t}HZ (2)		7.5		8	ns	10
	CL = 1	^{t}HZ (1)		17		17	ns	10
Data-out low-impedance time		^{t}LZ	1		1		ns	
Data-out hold time		^{t}OH	2		2.5		ns	
ACTIVE to PRECHARGE command		^{t}RAS	42	120k	42	120k	ns	
ACTIVE to ACTIVE command period		^{t}RC	60		70		ns	
AUTO REFRESH period		^{t}RFC	60		70		ns	
ACTIVE to READ or WRITE delay		^{t}RCD	18		20		ns	
Refresh period (4,096 rows)		^{t}REF		64		64	ms	
PRECHARGE command period		^{t}RP	18		20		ns	
ACTIVE bank *a* to ACTIVE bank *b* command		^{t}RRD	12		14		ns	25
Transition time		^{t}T	0.3	1.2	0.3	1.2	ns	7
WRITE recovery time		^{t}WR	1CLK+ 6ns		1CLK+ 7ns		^{t}CK	24
			12ns		14ns		ns	28
Exit SELF REFRESH to ACTIVE command		^{t}XSR	70		70		ns	20

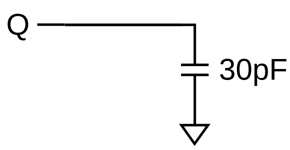
AC FUNCTIONAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 11; notes appear on page 35)

PARAMETER		SYMBOL	-5	-55	-6	-7	UNITS	NOTES
READ/WRITE command to READ/WRITE command		^tCCD	1	1	1	1	^tCK	17
CKE to clock disable or power-down entry mode		^tCKED	1	1	1	1	^tCK	14
CKE to clock enable or power-down exit setup mode		^tPED	1	1	1	1	^tCK	14
DQM to input data delay		^tDQD	0	0	0	0	^tCK	17
DQM to data mask during WRITEs		^tDQM	0	0	0	0	^tCK	17
DQM to data high-impedance during READs		^tDQZ	2	2	2	2	^tCK	17
WRITE command to input data delay		^tDWD	0	0	0	0	^tCK	17
Data-in to ACTIVE command	CL = 3	^tDAL (3)	5	5	5	5	^tCK	15, 21
	CL = 2	^tDAL (2)	-	-	4	4	^tCK	15, 21
	CL = 1	^tDAL (1)	-	-	3	3	^tCK	15, 21
Data-in to PRECHARGE command		^tDPL	2	2	2	2	^tCK	16, 21
Last data-in to burst STOP command		^tBDL	1	1	1	1	^tCK	17
Last data-in to new READ/WRITE command		^tCDL	1	1	1	1	^tCK	17
Last data-in to PRECHARGE command		^tRDL	2	2	2	2	^tCK	16, 21
LOAD MODE REGISTER command to ACTIVE or REFRESH command		^tMRD	2	2	2	2	^tCK	26
Data-out to high-impedance from PRECHARGE command	CL = 3	^tROH (3)	3	3	3	3	^tCK	17
	CL = 2	^tROH (2)	-	-	2	2	^tCK	17
	CL = 1	^tROH (1)	-	-	–	1	^tCK	17

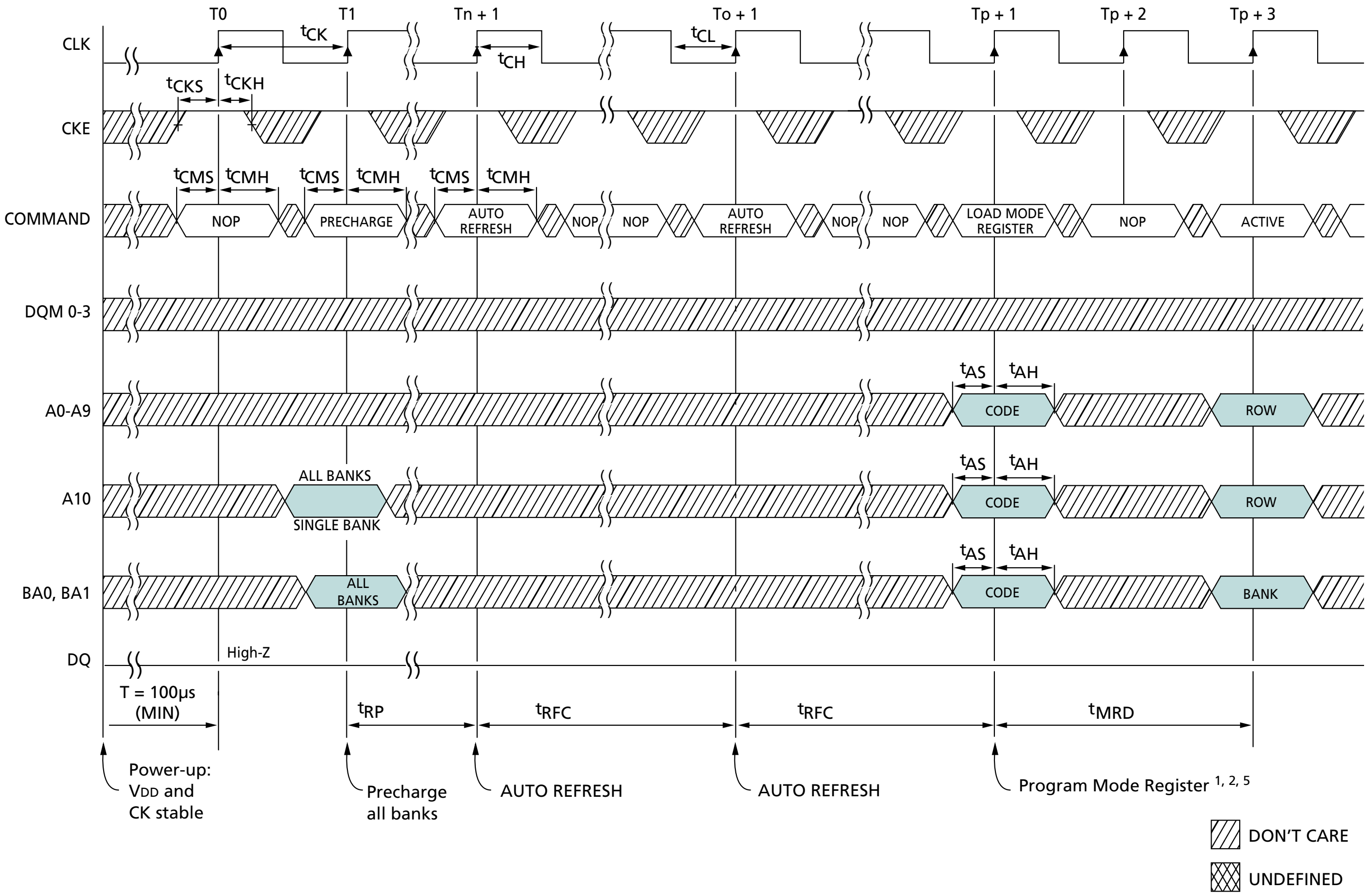
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{DD}, $V_{DD}Q$ = +3.3V; f = 1 MHz, T_A = 25°C; pin under test biased at 1.4V. AC can range from 0pF to 6pF.
3. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ +70°C and -40°C ≤ T_A ≤ +85°C for IT parts) is ensured.
6. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (V_{DD} and $V_{DD}Q$ must be powered up simultaneously. V_{SS} and $V_{SS}Q$ must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
7. AC characteristics assume ^tT = 1ns.
8. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.



9. Outputs measured at 1.5V with equivalent load:
10. ^tHZ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet ^tOH before going High-Z.
11. AC timing and I_{DD} tests have V_{IL} = .25 and V_{IH} = 2.75, with timing referenced to 1.5V crossover point.
12. Other input signals are allowed to transition no more than once in any two-clock period and are otherwise at valid V_{IH} or V_{IL} levels.
13. I_{DD} specifications are tested after the device is properly initialized.
14. Timing actually specified by ^tCKS; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by ^tWR plus ^tRP; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by ^tWR.
17. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The I_{DD} current will decrease as the CAS latency is reduced. This is due to the fact that the maximum cycle rate is slower as the CAS latency is reduced.
19. Address transitions average one transition every two clocks.
20. CLK must be toggled a minimum of two times during this period.
21. Based on ^tCK = 143 MHz for -7, 166 MHz for -6, 183 MHz for -55, and 200 MHz for -5.
22. V_{IH} overshoot: V_{IH}(MAX) = $V_{DD}Q$ + 1.2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL}(MIN) = -1.2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate.
23. The clock frequency must remain constant during access or precharge states (READ, WRITE, including ^tWR, and PRECHARGE commands). CKE may be used to reduce the data rate.
24. Auto precharge mode only.
25. JEDEC and PC100 specify three clocks.
26. ^tCK = 7ns for -7, 6ns for -6, 5.5ns for -5.5, and 5ns for -5.
27. V_{DD}(MIN) = 3.135V for -6, -55, and -5 speed grades.
28. Check factory for availability of specially screened devices having ^tWR = 10ns. ^tWR = 1 ^tCK for 100 MHz and slower (^tCK = 10ns and higher) in manual precharge.

INITIALIZE AND LOAD MODE REGISTER



TIMING PARAMETERS

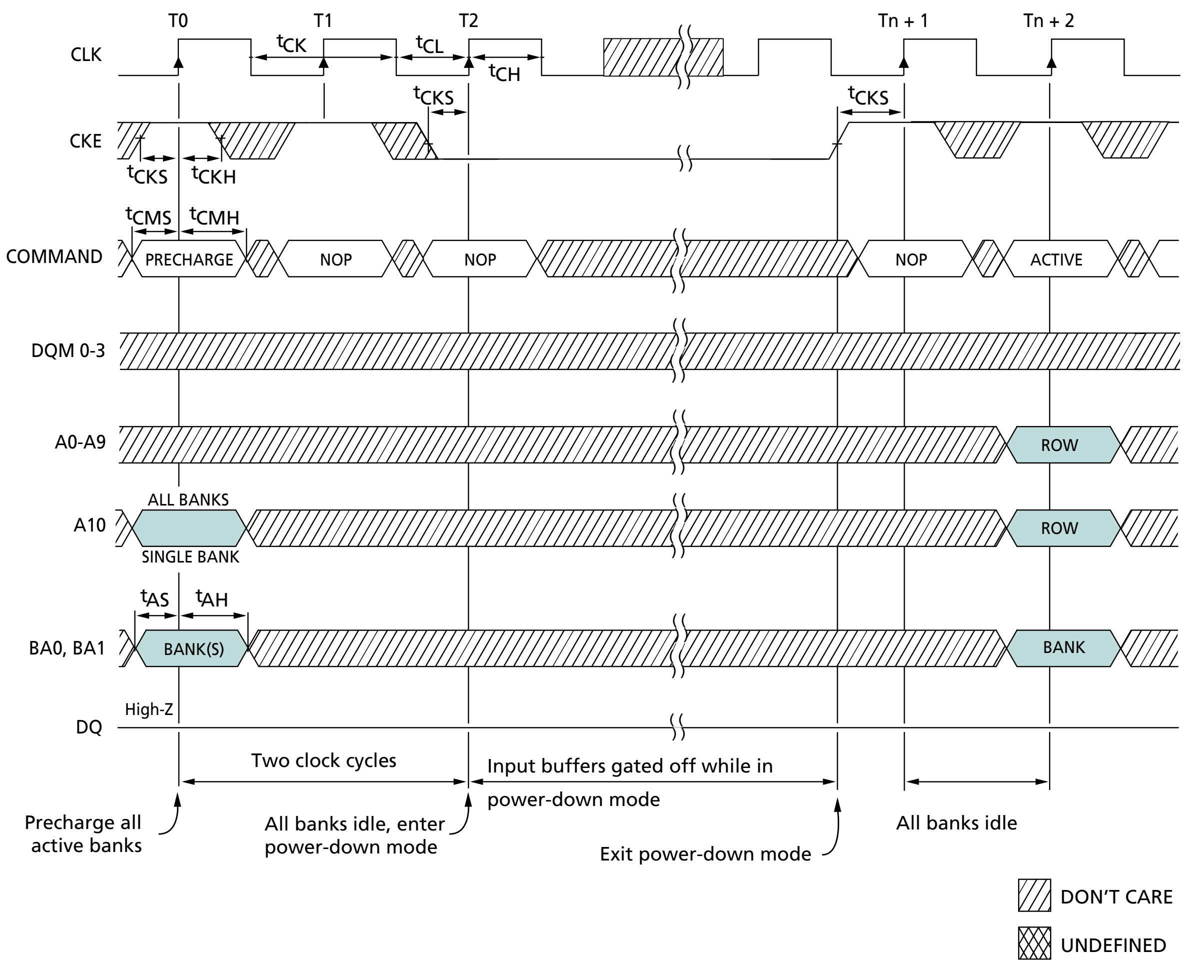
SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
^tAH	1		1		1		ns
^tAS	1.5		1.5		2		ns
^tCH	2		2.5		2.75		ns
^tCL	2		2.5		2.75		ns
^tCLK (3)	5		6		7		ns
^tCLK (2)			10		10		ns
^tCLK (1)			20		20		ns

SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
^tCKH	1		1		1		ns
^tCKS	1.5		1.5		2		ns
^tCMH	1		1		1		ns
^tCMS	1.5		1.5		2		ns
^tMRD	2		2		2		^tCK
^tRFC	60		60		70		ns
^tRP	15		18		20		ns

*CAS latency indicated in parentheses.

NOTE: 1. The Mode Register may be loaded prior to the AUTO REFRESH cycles if desired.
2. Outputs are guaranteed High-Z after command is issued.

POWER-DOWN MODE [1]



TIMING PARAMETERS

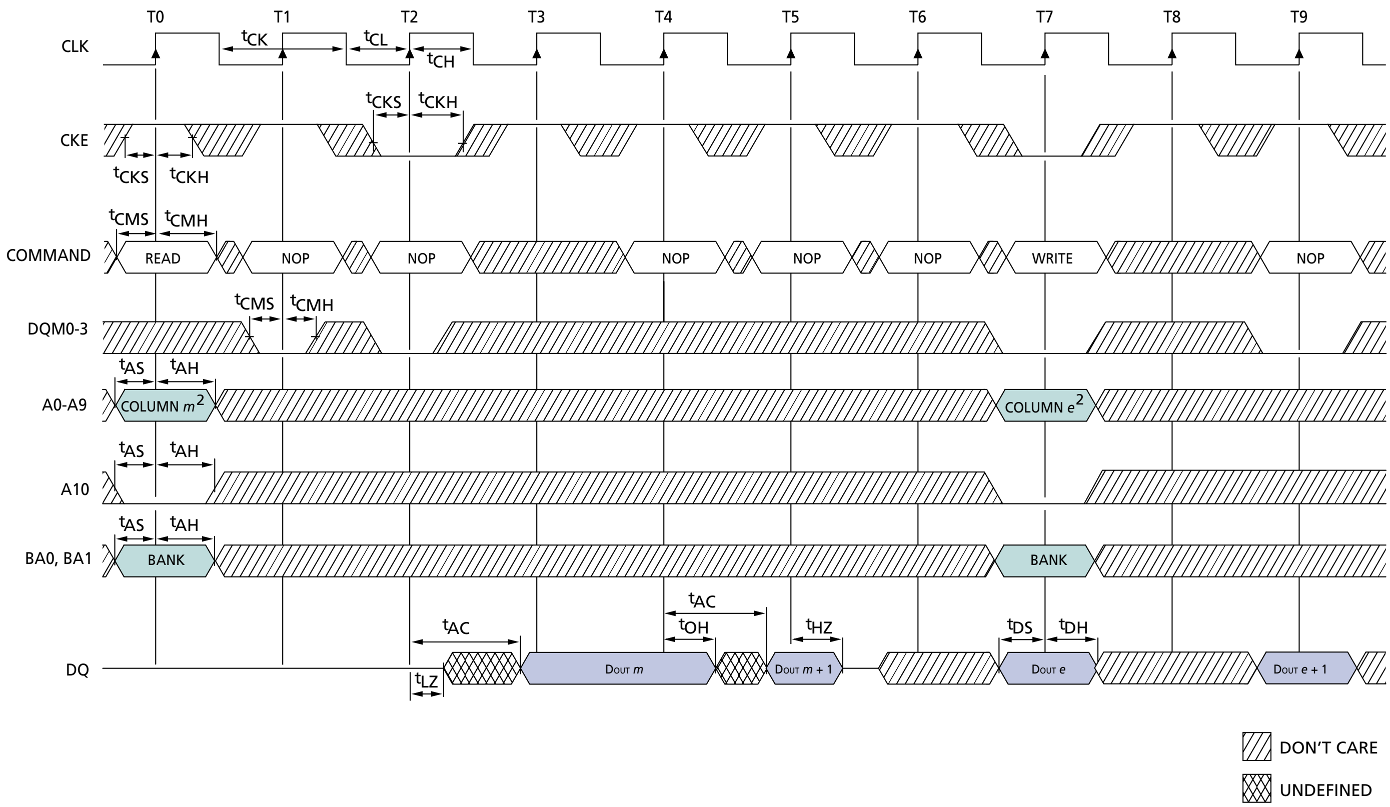
SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
tAH	1		1		1		ns
tAS	1.5		1.5		2		ns
tCH	2		2.5		2.75		ns
tCL	2		2.5		2.75		ns
tCK (3)	5		6		7		ns
tCK (2)			10		10		ns

SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
tCK (1)			20		20		ns
tCKH	1		1		1		ns
tCKS	1.5		1.5		2		ns
tCMH	1		1		1		ns
tCMS	1.5		1.5		2		ns

*CAS latency indicated in parentheses.

NOTE: 1. Violating refresh requirements during power-down may result in a loss of data.

CLOCK SUSPEND MODE [1]



TIMING PARAMETERS

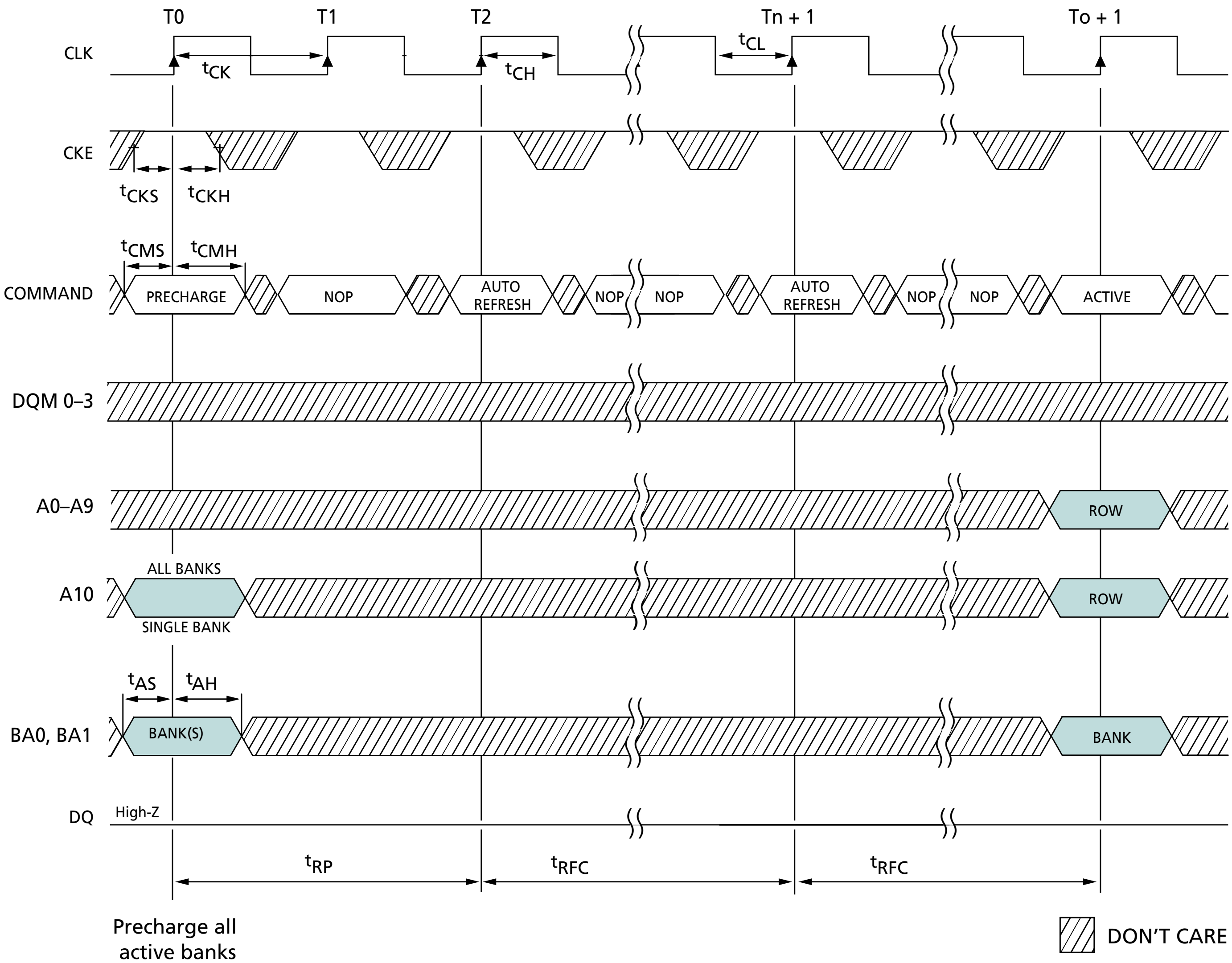
SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
^tAC (3)		4.5		5.5		5.5	ns
^tAC (2)				7.5		8	ns
^tAC (1)				17		17	ns
^tAH	1		1		1		ns
^tAS	1.5		1.5		2		ns
^tCH	2		2.5		2.75		ns
^tCL	2		2.5		2.75		ns
^tCK (3)	5		6		7		ns
^tCK (2)	–		10		10		ns
^tCK (1)	–		20		20		ns
^tCKH	1		1		1		ns

SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
^tCKS	1.5		1.5		2		ns
^tCMH	1		1		1		ns
^tCMS	1.5		1.5		2		ns
^tDH	1		1		1		ns
^tDS	1.5		1.5		2		ns
^tHZ (3)		4.5		5.5		5.5	ns
^tHZ (2)		–		7.5		8	ns
^tHZ (1)		–		17		17	ns
^tLZ	1		1		1		ns
^tOH	1.5		2		2.5		ns

*CAS latency indicated in parentheses.

NOTE: 1. For this example, the burst length = 2, the CAS latency = 3, and auto precharge is disabled.
2. A8 and A9 = "Don't Care."

AUTO REFRESH MODE



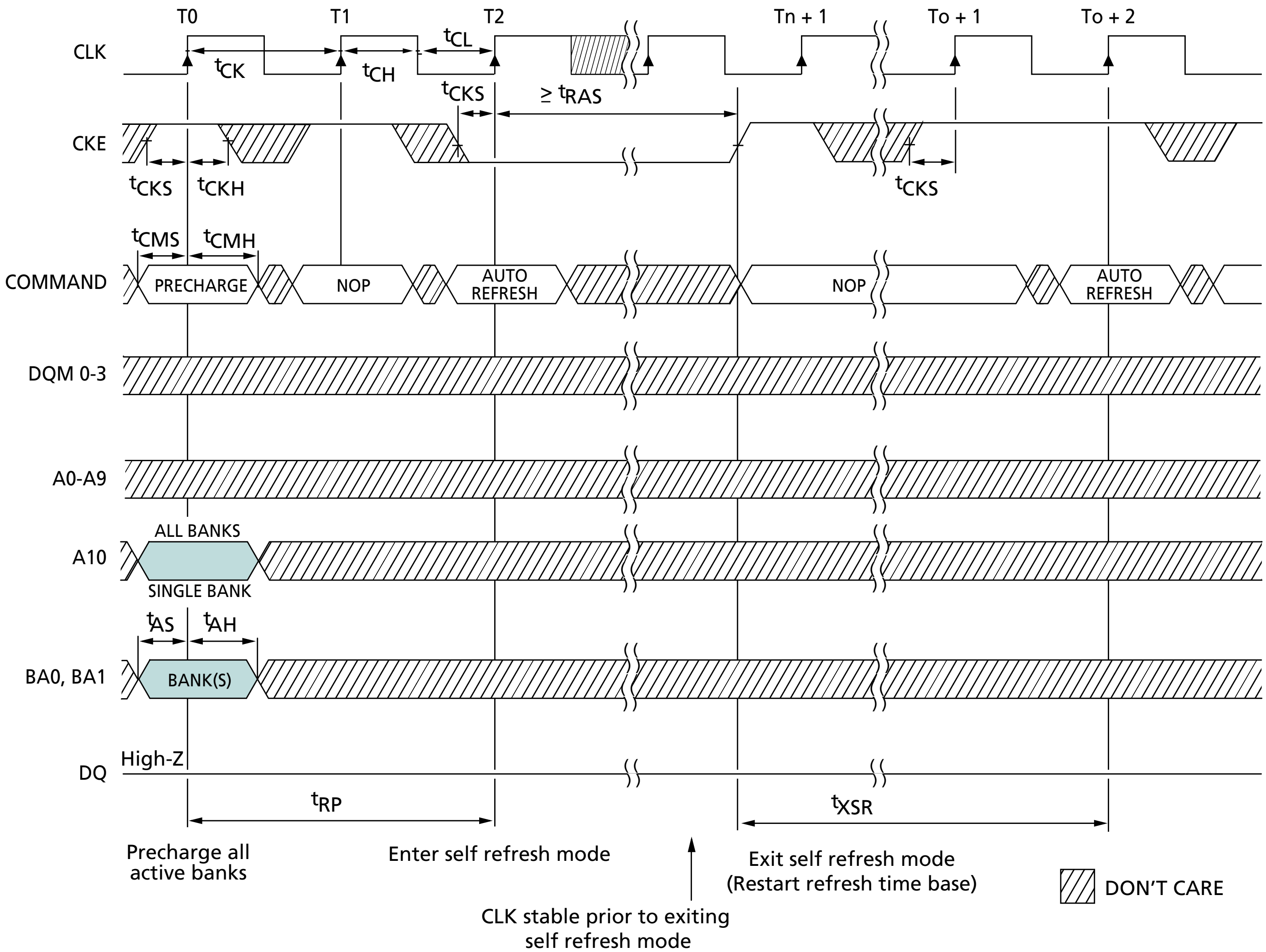
TIMING PARAMETERS

SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
^tAH	1		1		1		ns
^tAS	1.5		1.5		2		ns
^tCH	2		2.5		2.75		ns
^tCL	2		2.5		2.75		ns
^tCK (3)	5		6		7		ns
^tCK (2)			10		10		ns
^tCK (1)			20		20		ns

SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
^tCKH	1		1		1		ns
^tCKS	1.5		1.5		2		ns
^tCMH	1		1		1		ns
^tCMS	1.5		1.5		2		ns
^tRFC	60		60		70		ns
^tRP	15		18		20		ns

*CAS latency indicated in parentheses.

SELF REFRESH MODE



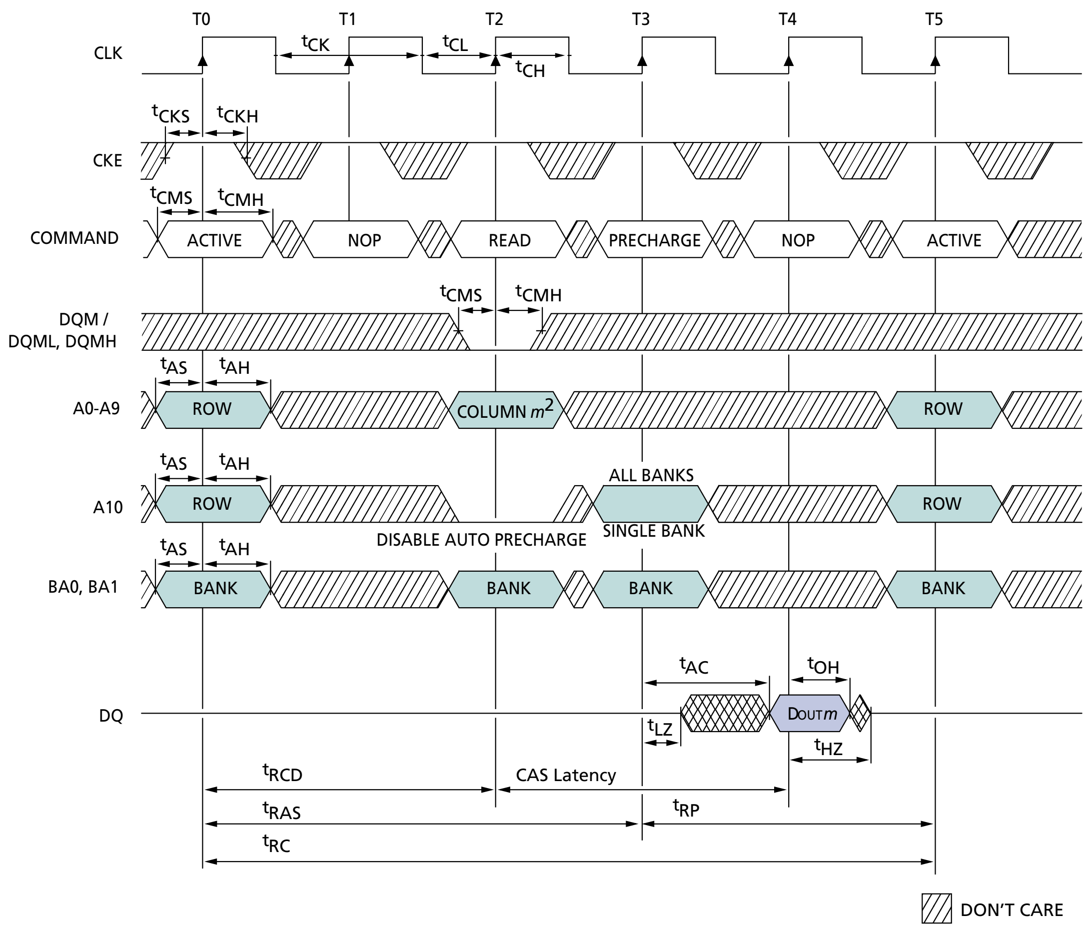
TIMING PARAMETERS

SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
^{t}AH	1		1		1		ns
^{t}AS	1.5		1.5		2		ns
^{t}CH	2		2.5		2.75		ns
^{t}CL	2		2.5		2.75		ns
^{t}CK (3)	5		6		7		ns
^{t}CK (2)			10		10		ns
^{t}CK (1)			20		20		ns

SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
^{t}CKH	1		1		1		ns
^{t}CKS	1.5		1.5		2		ns
^{t}CMH	1		1		1		ns
^{t}CMS	1.5		1.5		2		ns
^{t}RAS	38.7	120,000	42	120,000	42	120,000	ns
^{t}RP	15		18		20		ns
^{t}XSR	55		70		70		ns

*CAS latency indicated in parentheses.

SINGLE READ[1]



TIMING PARAMETERS

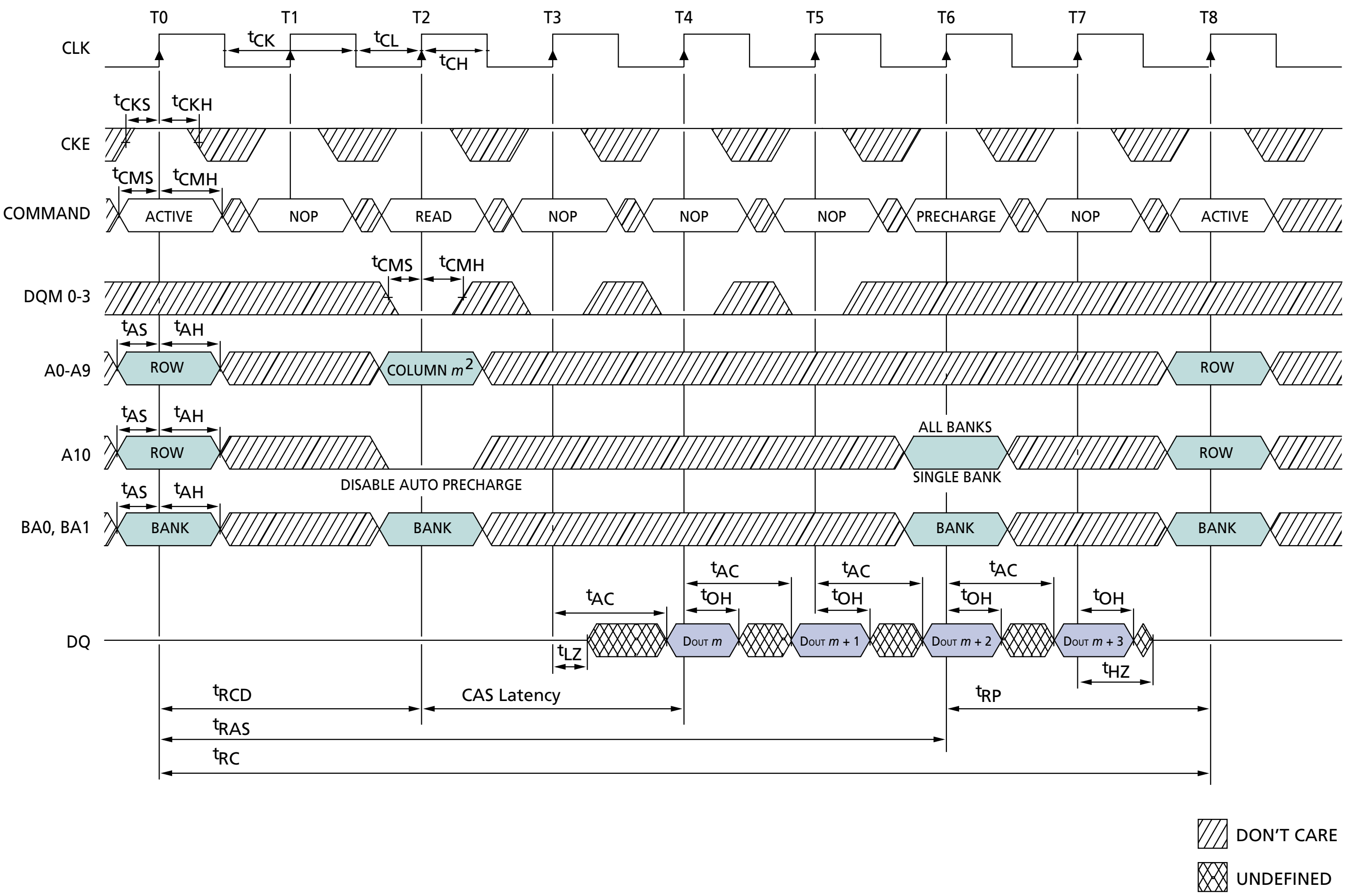
SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
^tAC (3)		4.5		5.5		5.5	ns
^tAC (2)		-		7.5		8	ns
^tAC (1)		-		17		17	ns
^tAH	1		1		1		ns
^tAS	1.5		1.5		2		ns
^tCH	2		2.5		2.75		ns
^tCL	2		2.5		2.75		ns
^tCK (3)	5		6		7		ns
^tCK (2)	-		10		10		ns
^tCK (1)	-		20		20		ns
^tCKH	1		1		1		ns
^tCKS	1.5		1.5		2		ns

SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
^tCMH	1		1		1		ns
^tCMS	1.5		1.5		2		ns
^tHZ (3)		4.5		5.5		5.5	ns
^tHZ (2)		-		7.5		8	ns
^tHZ (1)		-		17		17	ns
^tLZ	1		1		1		ns
^tOH	1.5		2		2.5		ns
^tRAS	38.7	120,000	42	120,000	42	120,000	ns
^tRC	55		60		70		ns
^tRCD	15		18		20		ns
^tRP	15		18		20		ns

*CAS latency indicated in parentheses.

NOTE: 1. For this example, the burst length = 1, the CAS latency = 2, and the READ burst is followed by a "manual" PRECHARGE.
2. A8, A9 = "Don't Care."

READE – WITHOUT AUTO PRECHARGE [1]



TIMING PARAMETERS

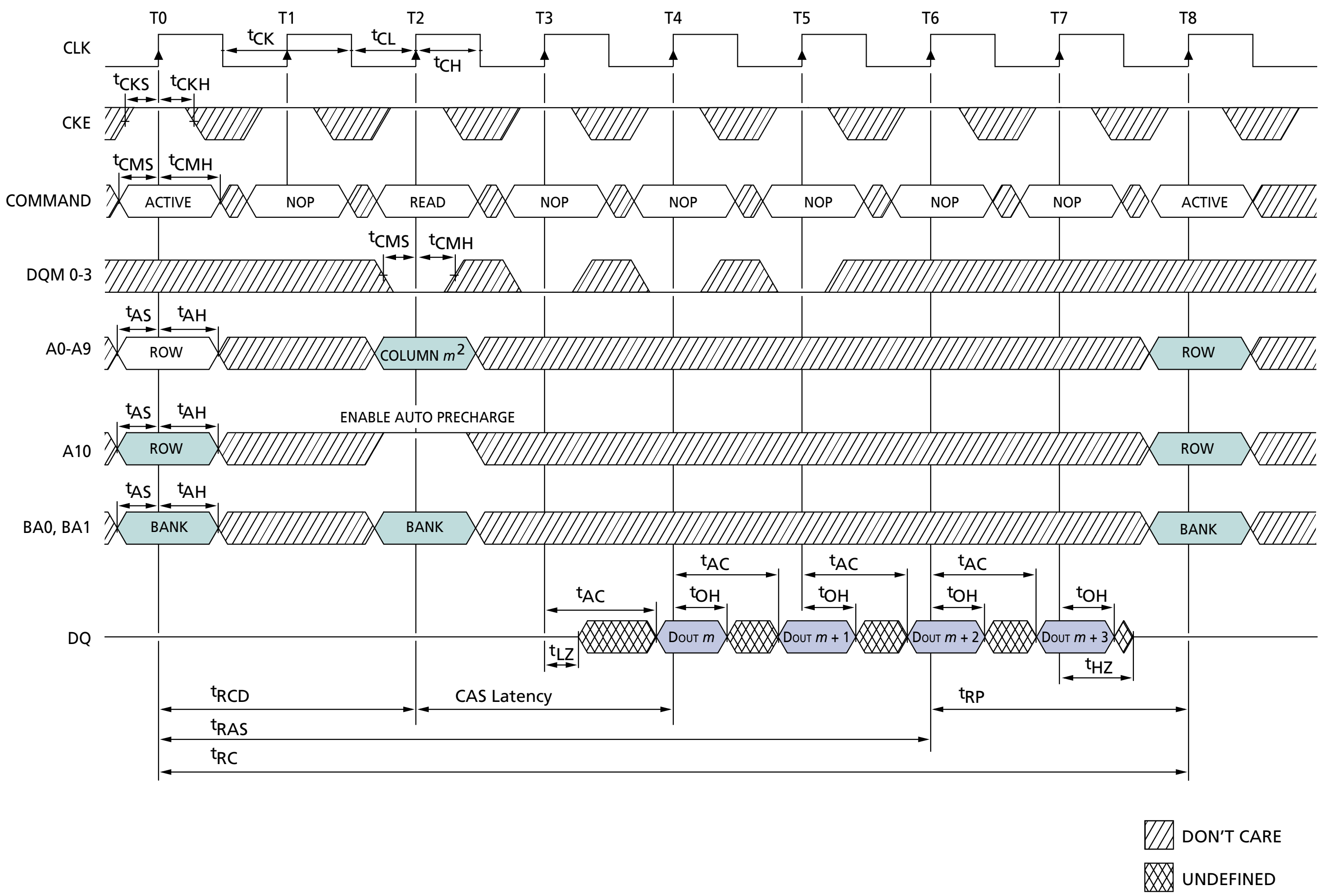
SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
tAC (3)		4.5		5.5		5.5	ns
tAC (2)		-		7.5		8	ns
tAC (1)		-		17		17	ns
tAH	1		1		1		ns
tAS	1.5		1.5		2		ns
tCH	2		2.5		2.75		ns
tCL	2		2.5		2.75		ns
tCK (3)	5		6		7		ns
tCK (2)	-		10		10		ns
tCK (1)	-		20		20		ns
tCKH	1		1		1		ns
tCKS	1.5		1.5		2		ns

SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
tCMH	1		1		1		ns
tCMS	1.5		1.5		2		ns
tHZ (3)		4.5		5.5		5.5	ns
tHZ (2)		-		7.5		8	ns
tHZ (1)		-		17		17	ns
tLZ	1		1		1		ns
tOH	1.5		2		2.5		ns
tRAS	38.7	120,000	42	120,000	42	120,000	ns
tRC	55		60		70		ns
tRCD	15		18		20		ns
tRP	15		18		20		ns

*CAS latency indicated in parentheses.

NOTE: 1. For this example, the burst length = 4, the CAS latency = 2, and the READ burst is followed by a "manual" PRECHARGE.
2. A8 and A9 = "Don't Care."

READE – WITH AUTO PRECHARGE [1]



TIMING PARAMETERS

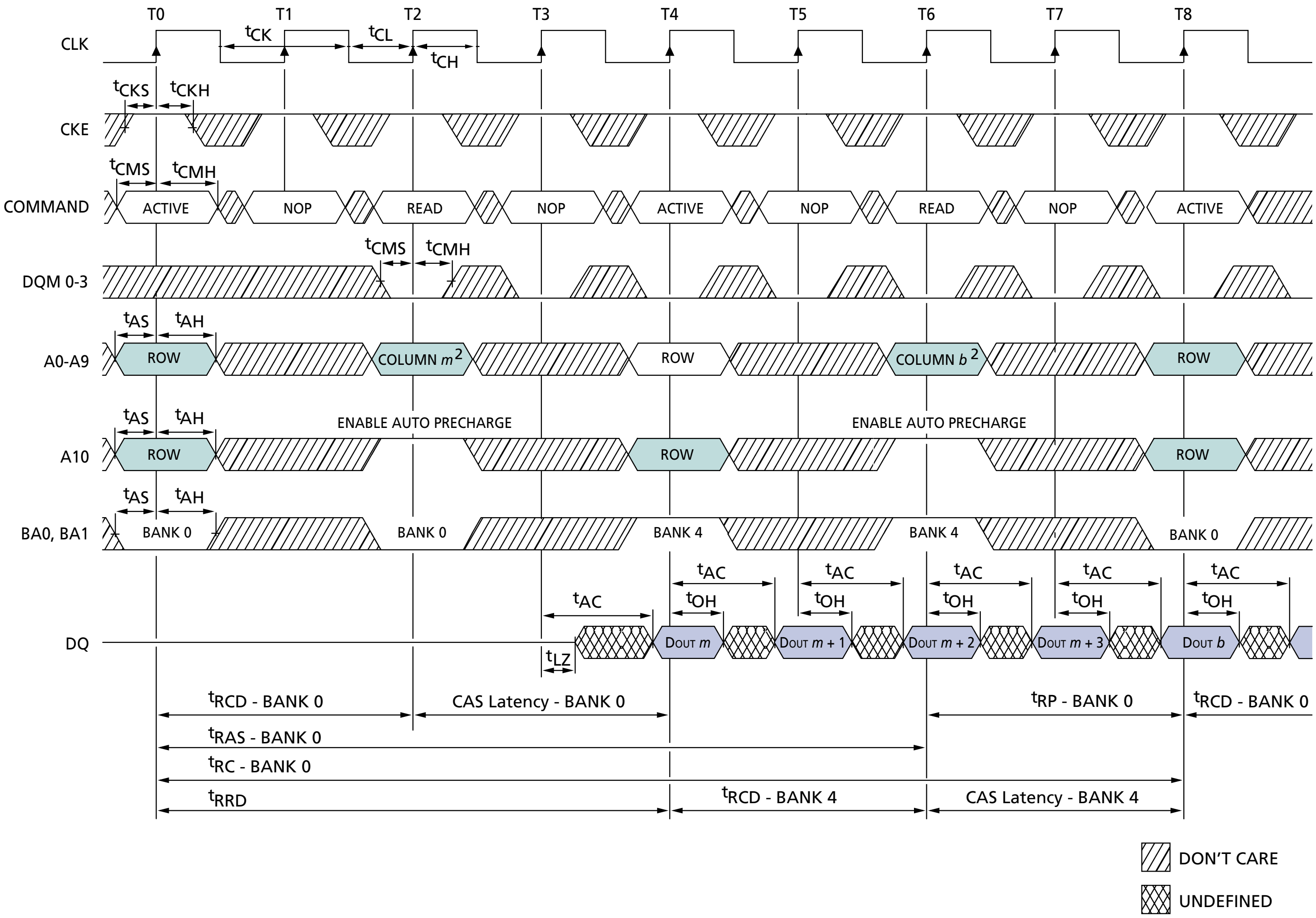
SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
^{t}AC (3)		4.5		5.5		5.5	ns
^{t}AC (2)		-		7.5		8	ns
^{t}AC (1)		-		17		17	ns
^{t}AH	1		1		1		ns
^{t}AS	1.5		1.5		2		ns
^{t}CH	2		2.5		2.75		ns
^{t}CL	2		2.5		2.75		ns
^{t}CK (3)	5		6		7		ns
^{t}CK (2)	-		10		10		ns
^{t}CK (1)	-		20		20		ns
^{t}CKH	1		1		1		ns
^{t}CKS	1.5		1.5		2		ns

SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
^{t}CMH	1		1		1		ns
^{t}CMS	1.5		1.5		2		ns
^{t}HZ (3)		4.5		5.5		5.5	ns
^{t}HZ (2)		-		7.5		8	ns
^{t}HZ (1)		-		17		17	ns
^{t}LZ	1		1		1		ns
^{t}OH	1.5		2		2.5		ns
^{t}RAS	38.7	120,000	42	120,000	42	120,000	ns
^{t}RC	55		60		70		ns
^{t}RCD	15		18		20		ns
^{t}RP	15		18		20		ns

*CAS latency indicated in parentheses.

NOTE: 1. For this example, the burst length = 4, and the CAS latency = 2.
2. A8 and A9 = "Don't Care."

ALTERNATING BANK READ ACCESSES [1]



TIMING PARAMETERS

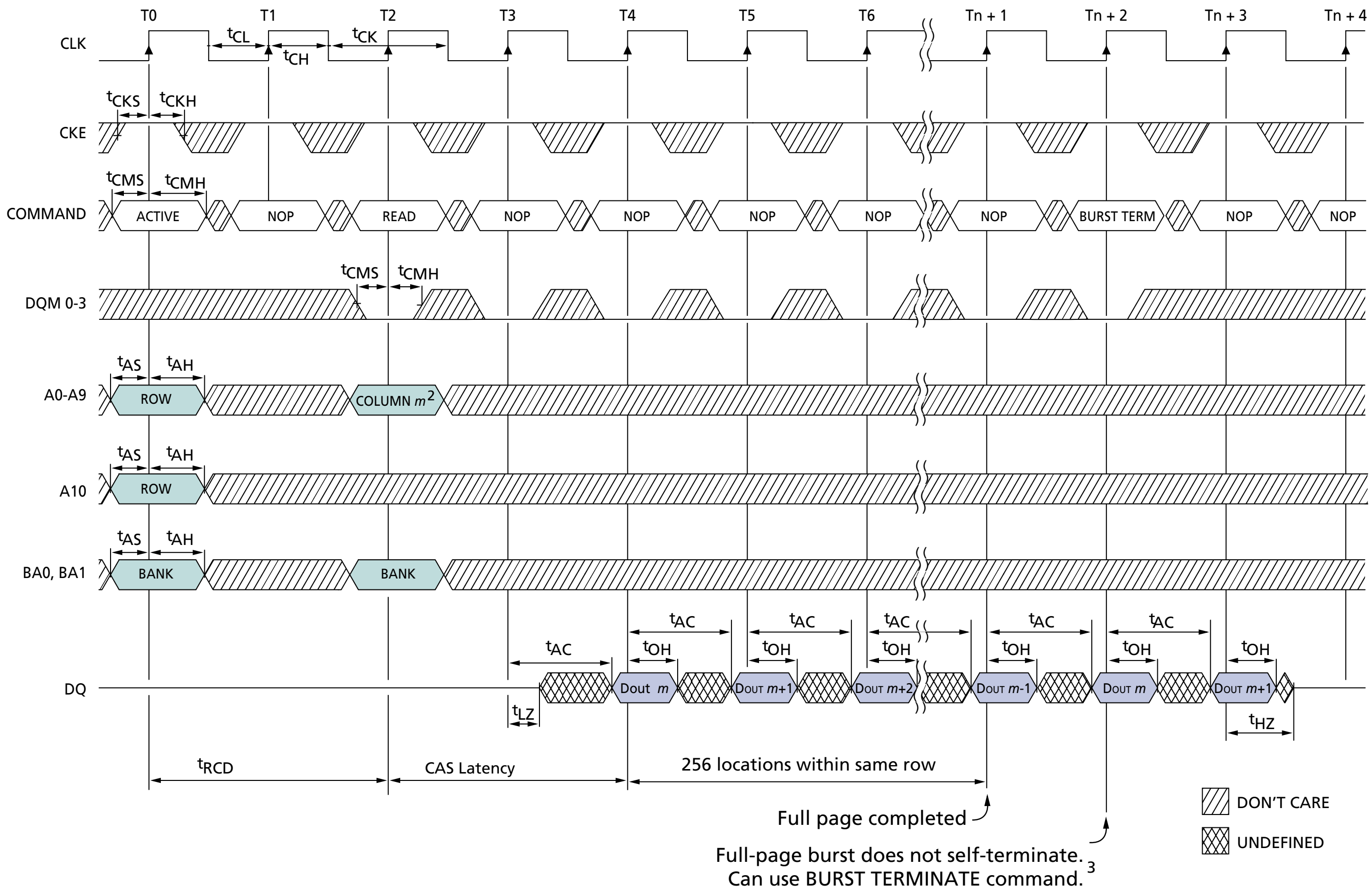
SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
^tAC (3)		4.5		5.5		5.5	ns
^tAC (2)		-		7.5		8	ns
^tAC (1)		-		17		17	ns
^tAH	1		1		1		ns
^tAS	1.5		1.5		2		ns
^tCH	2		2.5		2.75		ns
^tCL	2		2.5		2.75		ns
^tCK (3)	5		6		7		ns
^tCK (2)	-		10		10		ns
^tCK (1)	-		20		20		ns
^tCKH	1.5		1		1		ns

SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
^tCKS	1.5		1.5		2		ns
^tCMH	1		1		1		ns
^tCMS	1.5		1.5		2		ns
^tLZ	1		1		1		ns
^tOH	1.5		2		2.5		ns
^tRAS	38.7	120,000	42	120,000	42	120,000	ns
^tRC	55		60		70		ns
^tRCD	15		18		20		ns
^tRP	15		18		20		ns
^tRRD	10		12		14		ns

*CAS latency indicated in parentheses.

NOTE: 1. For this example, the burst length = 4, and the CAS latency = 2.
2. A8 and A9 = "Don't Care."

READ – FULL-PAGE BURST [1]



TIMING PARAMETERS

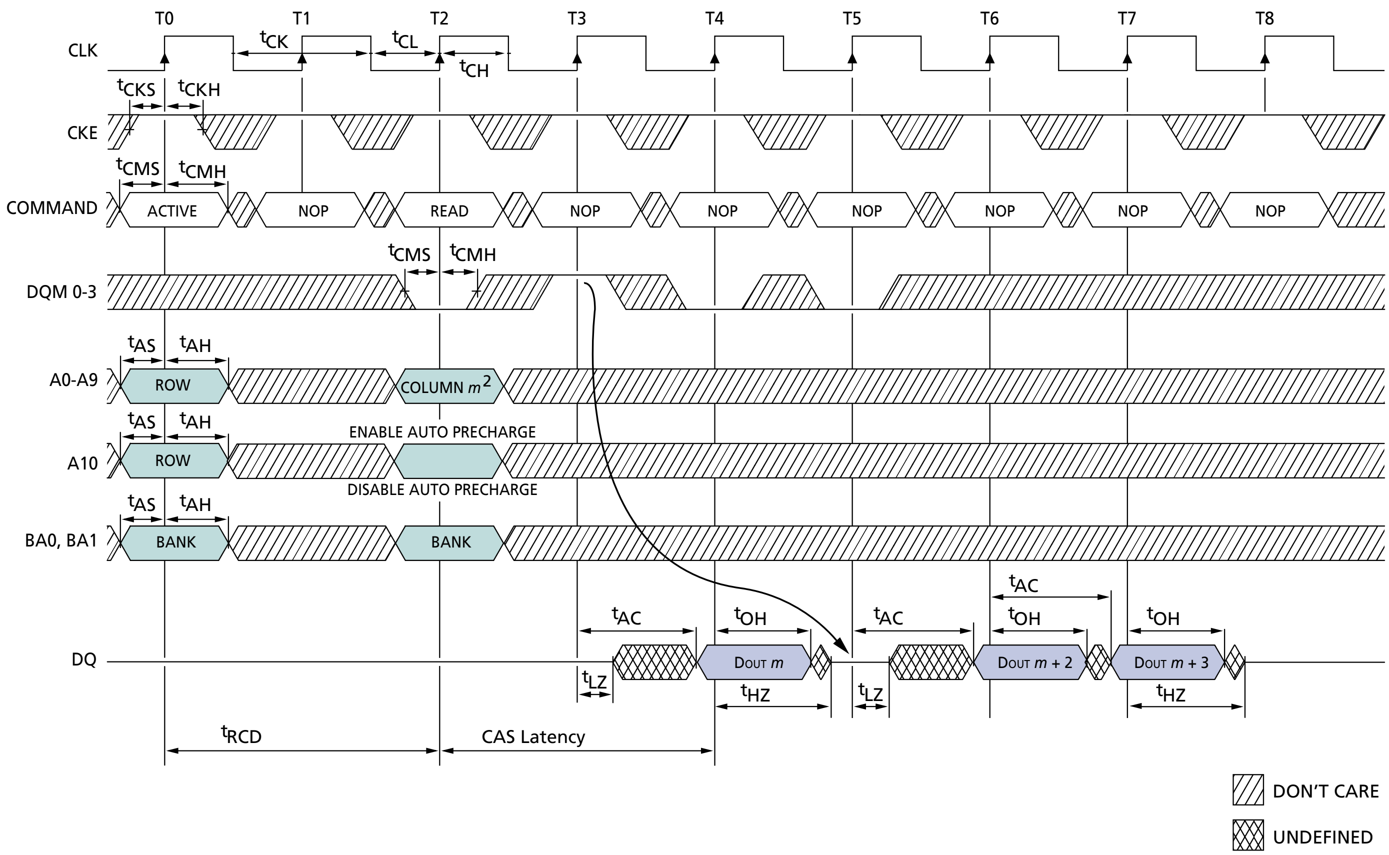
SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
^{t}AC (3)		4.5		5.5		5.5	ns
^{t}AC (2)		-		7.5		8	ns
^{t}AC (1)		-		17		17	ns
^{t}AH	1		1		1		ns
^{t}AS	1.5		1.5		2		ns
^{t}CH	2		2.5		2.75		ns
^{t}CL	2		2.5		2.75		ns
^{t}CK (3)	5		6		7		ns
^{t}CK (2)	-		10		10		ns
^{t}CK (1)	-		20		20		ns

SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
^{t}CKH	1		1		1		ns
^{t}CKS	1.5		1.5		2		ns
^{t}CMH	1		1		1		ns
^{t}CMS	1.5		1.5		2		ns
^{t}HZ (3)		4.5		5		5.5	ns
^{t}HZ (2)		-		7.5		8	ns
^{t}HZ (1)		-		17		17	ns
^{t}LZ	1		1		1		ns
^{t}OH	1.5		2		2.5		ns
^{t}RCD	15		18		20		ns

*CAS latency indicated in parentheses.

NOTE: 1. For this example, the CAS latency = 2.
2. A8 and A9 = "Don't Care."
3. Page left open; no ^{t}RP.

READ – DQM OPERATION [1]



TIMING PARAMETERS

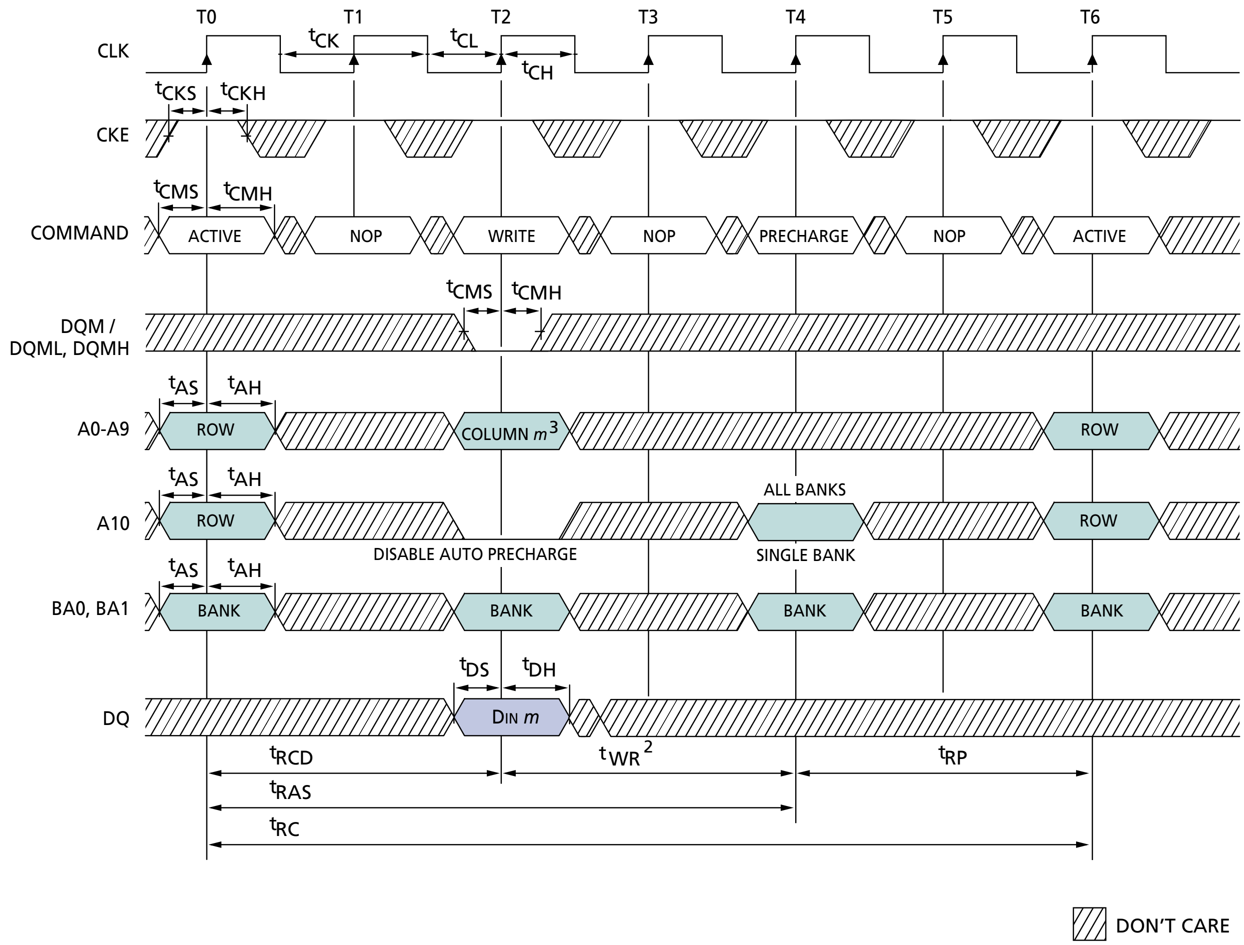
SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
^tAC (3)		4.6		5.5		5.5	ns
^tAC (2)		-		7.5		8	ns
^tAC (1)		-		17		17	ns
^tAH	1		1		1		ns
^tAS	1.5		1.5		2		ns
^tCH	2		2.5		2.75		ns
^tCL	2		2.5		2.75		ns
^tCK (3)	5		6		7		ns
^tCK (2)	-		10		10		ns
^tCK (1)	-		20		20		ns

SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
^tCKH	1		1		1		ns
^tCKS	1.5		1.5		2		ns
^tCMH	1		1		1		ns
^tCMS	1.5		1.5		2		ns
^tHZ (3)		4.5		5		5.5	ns
^tHZ (2)		-		7.5		8	ns
^tHZ (1)		-		17		17	ns
^tLZ	1		1		1		ns
^tOH	1.5		2		2.5		ns
^tRCD	15		18		20		ns

*CAS latency indicated in parentheses.

NOTE: 1. For this example, the CAS latency = 2.
2. A8 and A9 = "Don't Care."

SINGLE WRITE



TIMING PARAMETERS

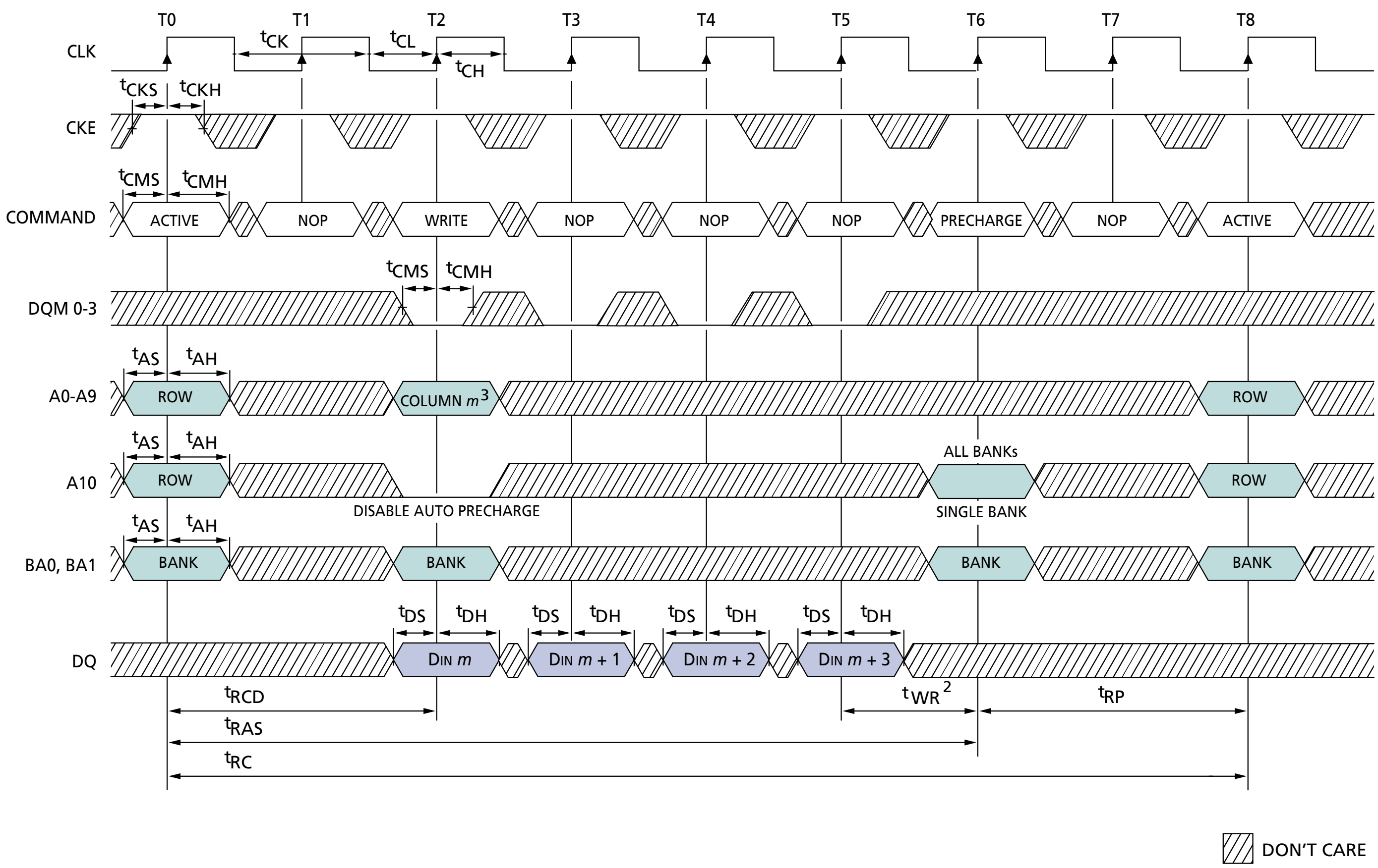
SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
^tAH	1		1		1		ns
^tAS	1.5		1.5		2		ns
^tCH	2		2.5		2.75		ns
^tCL	2		2.5		2.75		ns
^tCK (3)	5		6		7		ns
^tCK (2)			10		10		ns
^tCK (1)			20		20		ns
^tCKH	1		1		1		ns
^tCKS	1.5		1.5		2		ns

SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
^tCMH	1		1		1		ns
^tCMS	1.5		1.5		2		ns
^tDH	1		1		1		ns
^tDS	1.5		1.5		2		ns
^tRAS	38.7	120,000	42	120,000	42	120,000	ns
^tRC	55		60		70		ns
^tRCD	15		18		20		ns
^tRP	15		18		20		ns
^tWR	2 ^tCK		12		14		ns

*CAS latency indicated in parentheses.

NOTE:
1. For this example, the burst length = 4, and the WRITE burst is followed by a "manual" PRECHARGE.
2. 10ns is required between <DIN m> and the PRECHARGE command, regardless of frequency, to meet ^tWR.
3. A8, A9 = "Don't Care."

WRITE – WITHOUT AUTO PRECHARGE [1]



TIMING PARAMETERS

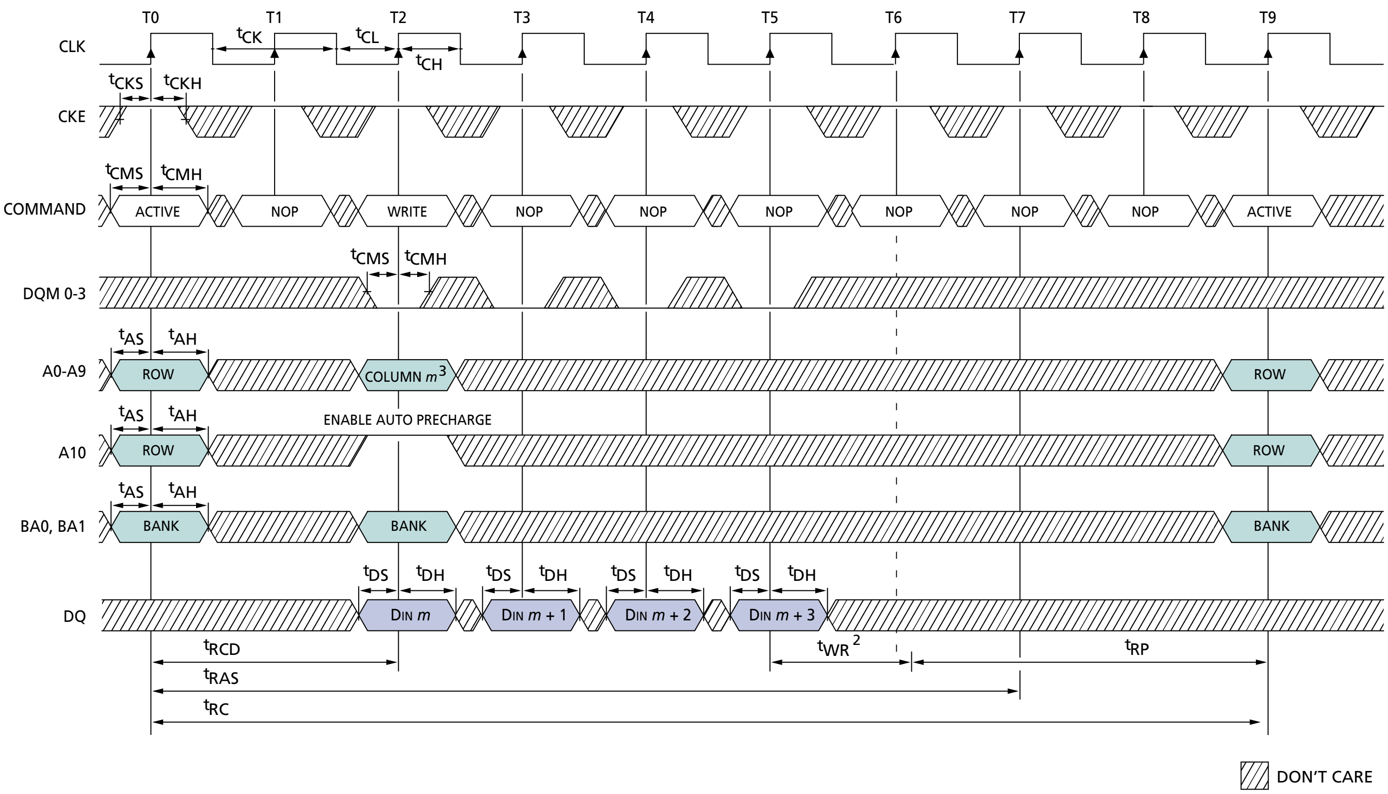
SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
^tAH	1		1		1		ns
^tAS	1.5		1.5		2		ns
^tCH	2		2.5		2.75		ns
^tCL	2		2.5		2.75		ns
^tCK (3)	5		6		7		ns
^tCK (2)			10		10		ns
^tCK (1)			20		20		ns
^tCKH	1		1		1		ns
^tCKS	1.5		2		2		ns

SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
^tCMH	1		1		1		ns
^tCMS	1.5		1.5		2		ns
^tDH	1		1		1		ns
^tDS	1.5		1.5		2		ns
^tRAS	38.7	120,000	42	120,000	42	120,000	ns
^tRC	55		60		70		ns
^tRCD	15		18		20		ns
^tRP	15		18		20		ns
^tWR[4]	2 ^tCK		12		14		ns

*CAS latency indicated in parentheses.

NOTE:
1. For this example, the burst length = 4, and the WRITE burst is followed by a "manual" PRECHARGE.
2. Faster frequencies require two clocks (when $^tWR > ^tCK$).
3. A8 and A9 = "Don't Care."
4. ^tWR of 1 CLK available if running 100 MHz or slower. Check factory for availability.

WRITE – WITH AUTO PRECHARGE [1]



TIMING PARAMETERS

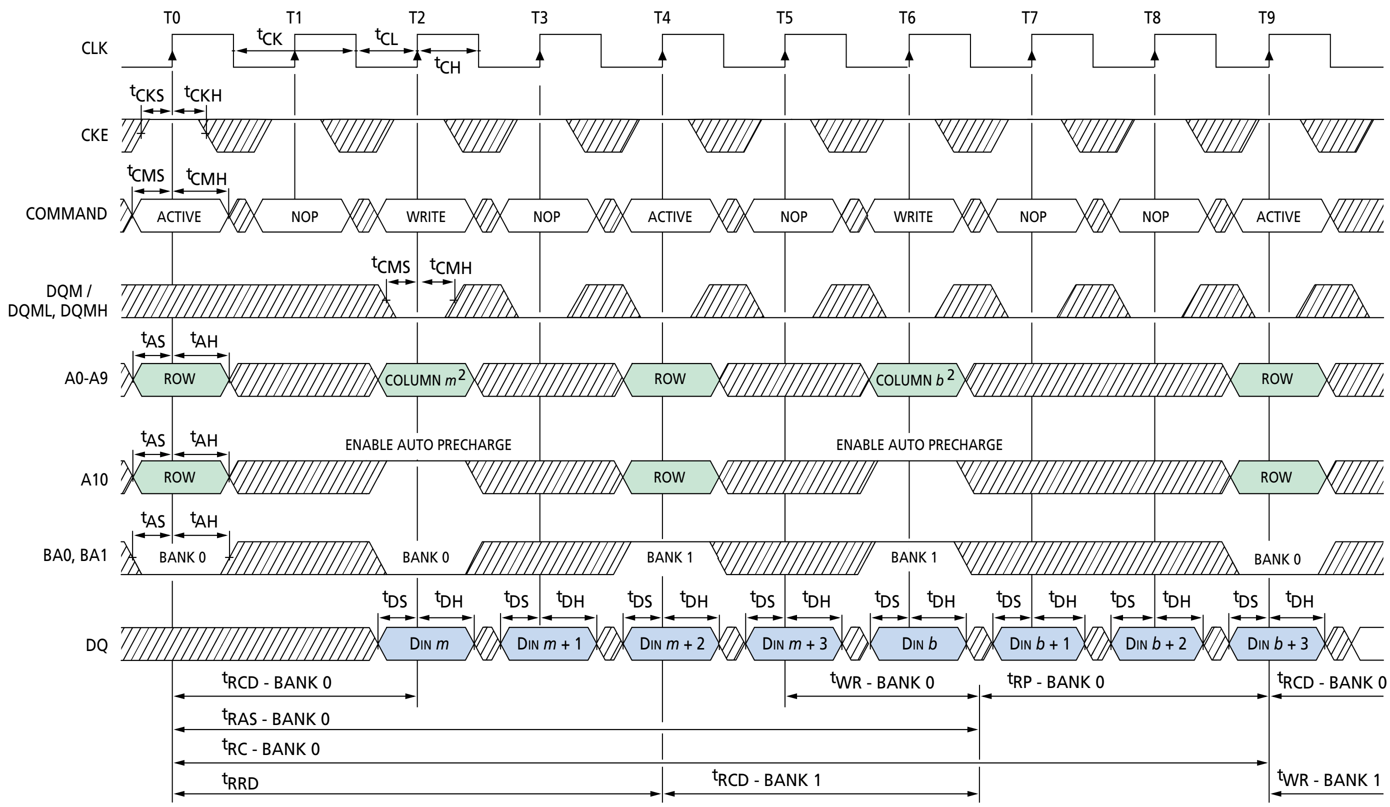
SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
^{t}AH	1		1		1		ns
^{t}AS	1.5		1.5		2		ns
^{t}CH	2		2.5		2.75		ns
^{t}CL	2		2.5		2.75		ns
^{t}CK (3)	5		6		7		ns
^{t}CK (2)			10		10		ns
^{t}CK (1)			20		20		ns
^{t}CKH	1		1		1		ns
^{t}CKS	1.5		2		2		ns
^{t}CMH	1		1		1		ns

SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
^{t}CMS	1.5		1.5		2		ns
^{t}DH	1		1		1		ns
^{t}DS	1.5		1.5		2		ns
^{t}RAS	38.7	120,000	42	120,000	42	120,000	ns
^{t}RC	55		60		70		ns
^{t}RCD	15		18		20		ns
^{t}RP	15		18		20		ns
^{t}WR	2 ^{t}CK		1 CLK+ 6		1 CLK+ 7		ns

*CAS latency indicated in parentheses.

NOTE:
1. For this example, the burst length = 4.
2. Faster frequencies require two clocks (when ^{t}WR > ^{t}CK).
3. A8 and A9 = "Don't Care."

ALTERNATING BANK WRITE ACCESSES [1]



TIMING PARAMETERS

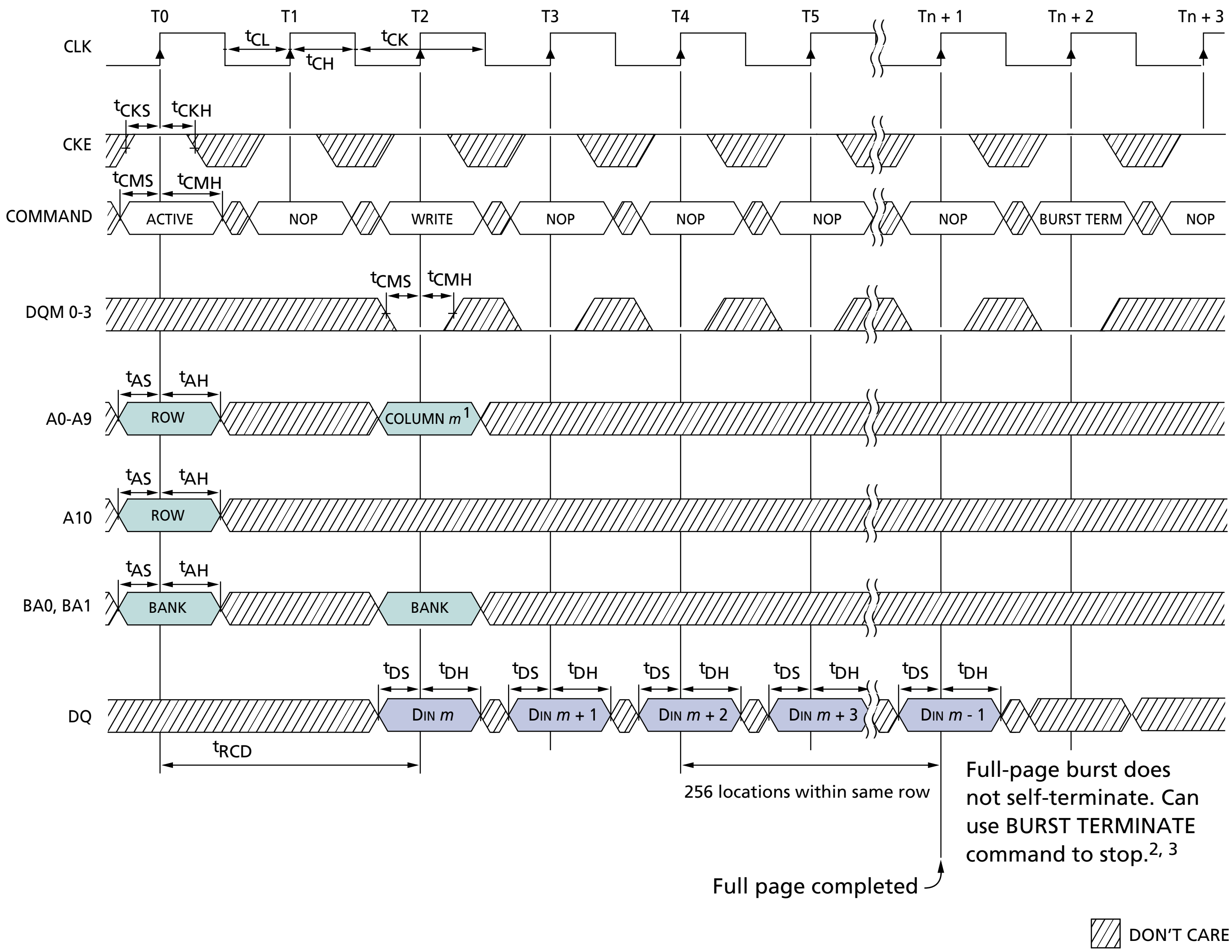
SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
tAH	1		1		1		ns
tAS	1.5		1.5		2		ns
tCH	2		2.5		2.75		ns
tCL	2		2.5		2.75		ns
tCK (3)	5		6		7		ns
tCK (2)			10		10		ns
tCK (1)			20		20		ns
tCKH	1		1		1		ns
tCKS	1.5		2		2		ns
tCMH	1		1		1		ns
tCMS	1.5		1.5		2		ns

SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
tDH	1		1		1		ns
tDS	1.5		1.5		2		ns
tRAS	38.7		42	120,000	42	120,000	ns
tRC	55		60		70		ns
tRCD	15		18		20		ns
tRP	15		18		20		ns
tRRD	10		12		14		ns
tWR	2 tCK		1 CLK+ 6		1 CLK+ 7		ns

*CAS latency indicated in parentheses.

NOTE:
1. For this example, the burst length = 4.
2. Faster frequencies require two clocks (when tWR > tCK).
3. A8 and A9 = "Don't Care."

WRITE – FULL-PAGE BURST



TIMING PARAMETERS

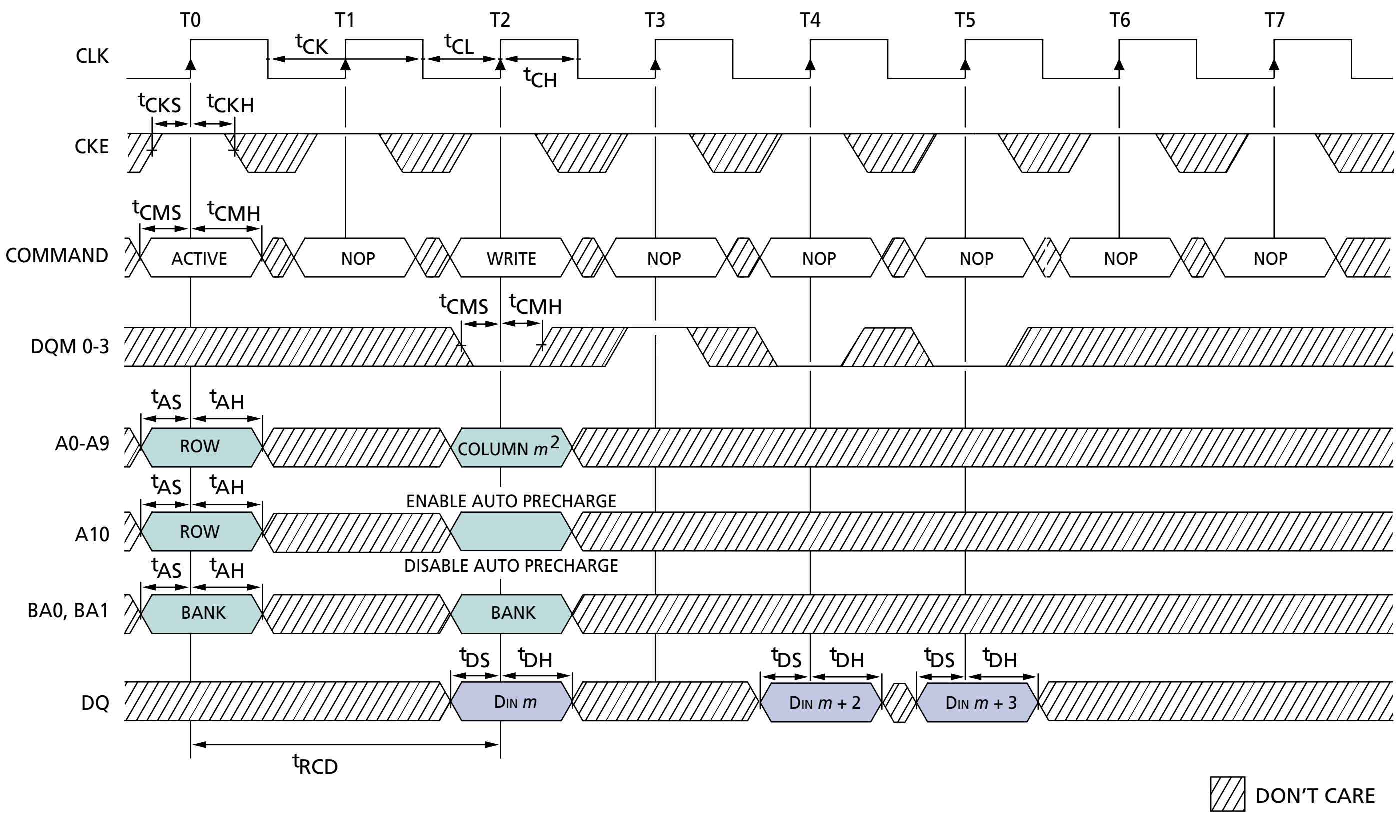
SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
^{t}AH	1		1		1		ns
^{t}AS	1.5		1.5		2		ns
^{t}CH	2		2.5		2.75		ns
^{t}CL	2		2.5		2.75		ns
^{t}CK (3)	5		6		7		ns
^{t}CK (2)			10		10		ns
^{t}CK (1)			20		20		ns

SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
^{t}CKH	1		1		1		ns
^{t}CKS	1.5		1.5		2		ns
^{t}CMH	1		1		1		ns
^{t}CMS	1.5		2		2		ns
^{t}DH	1		1		1		ns
^{t}DS	1.5		1.5		2		ns
^{t}RCD	15		18		20		ns

*CAS latency indicated in parentheses.

NOTE:
1. A8 and A9 = "Don't Care."
2. ^{t}WR must be satisfied prior to PRECHARGE command.
3. Page left open; no ^{t}RP.

WRITE – DQM OPERATION [1]



TIMING PARAMETERS

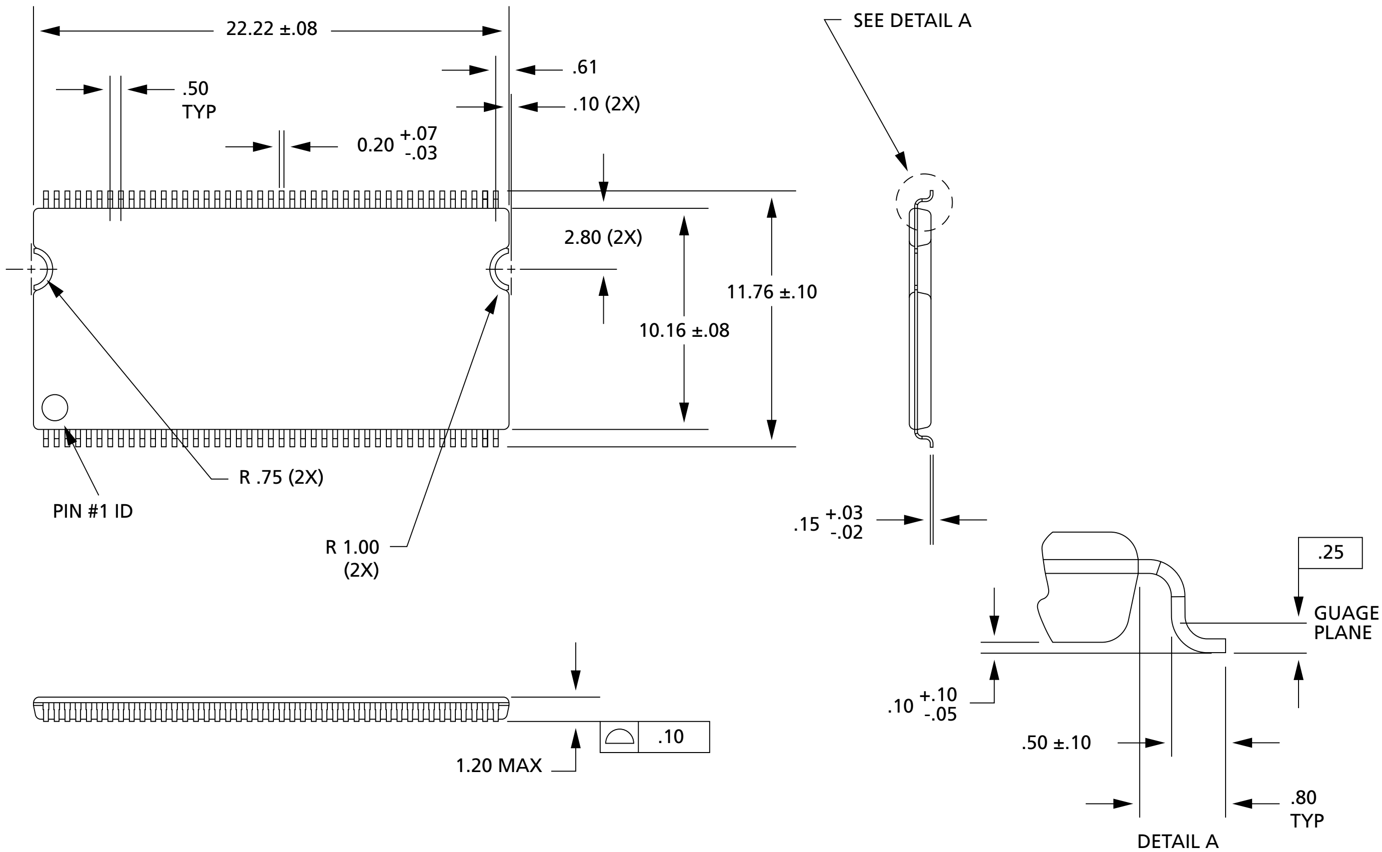
SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
^tAH	1		1		1		ns
^tAS	1.5		1.5		2		ns
^tCH	2		2.5		2.75		ns
^tCL	2		2.5		2.75		ns
^tCK (3)	5		6		7		ns
^tCK (2)			10		10		ns
^tCK (1)			20		20		ns

SYMBOL*	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
^tCKH	1		1		1		ns
^tCKS	1.5		2		2		ns
^tCMH	1		1		1		ns
^tCMS	1.5		1.5		2		ns
^tDH	1		1		1		ns
^tDS	1.5		1.5		2		ns
^tRCD	15		18		20		ns

*CAS latency indicated in parentheses.

NOTE: 1. For this example, the burst length = 4.
2. A8 and A9 = "Don't Care."

86-PIN PLASTIC TSOP (400 MIL)



NOTE: 1. All dimensions in millimeters $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.025mm per side.

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