JEDEC JESD204B

An early look at the third-generation high speed serial interface for data converters

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Document information

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1. Introduction – The evolution of a transformative high-speed data converter interface

The JEDEC standards organization has published two versions of the JESD204 high-speed serial digital interface specification for data converters and logic devices. The first revision, the JESD204 2006 specification, brought the advantages of SerDes-based high-speed serial (3.125 Gbps maximum) interfaces to data converters. The second revision, the JESD204A 2008 specification, added critically important enhancements: the support for multiple data lanes and the support for lane synchronization. Lane synchronization enables JESD204A to be used in quadrature (I/Q) sampling systems, the technology which underpins modern 3G, 3G+ and 4G broadband wireless communications; see Figure 1.

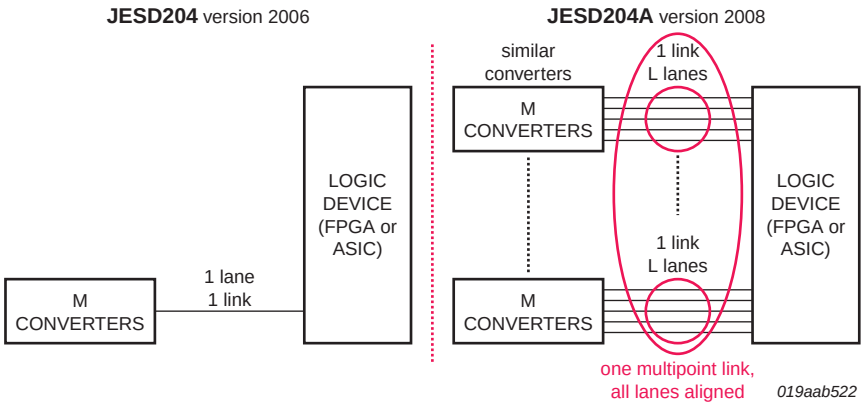

Fig 1. JESD204 (2006) versus JESD204A (2008)

A third revision of the specification, JESD204B, has been recently completed by an international JEDEC JC-16 task group (Project 150.01), comprising about 65 members from 25 companies (systems OEMs and semiconductor companies). The published JESD204B specification from JEDEC is expected in the second half of 2011. JESD204B is expected to introduce three new enhancements that promise to drive this new interface into ubiquitous adoption by data acquisition system engineers worldwide. These enhancements are: a higher maximum lane rate (higher bandwidth); support for deterministic latency through the interface; and support for harmonic frame clocking (or single clock architecture data converters); see Table 1.

Table 1. Evolution of the JESD204 specification

Function	JESD204	JESD204A	JESD204B
JEDEC specification release	2006	2008	2011
Maximum lane rate (Gbps)	3.125	3.125	12.5
Support for multiple lanes?	no	yes	yes
Support for lane synchronization?	no	yes	yes
Support for multi-device synchronization?	no	yes	yes
Support for deterministic latency?	no	no	yes
Support for harmonic clocking?	no	no	yes

There are numerous system design benefits associated with JESD204A/B compared to legacy parallel interfaces. Briefly, these benefits include:

- significant decrease in the number of higher-bandwidth interconnect PCB traces - enabling increased system reliability systems (most failures occur at points of interconnect)
- reduced PCB complexity - impacts both NRE costs and marginal production costs, very often the system can be implemented using fewer PCB layers
- opening of a critical bottleneck in the digital signal processing bandwidth of the system design - enables higher system performance

2. Higher lane rate to reduce IC package, PCB size and cost

The JESD204A 2008 specification defines an electrical or physical layer (PHY) that supports unidirectional, point-to-point, serial coded data rates from 312.5 Mbps to 3.125 Gbps between data converters and a logic device (FPGA, ASIC, microprocessor or DSP) separated by up 20 cm of standard FR-4 (FR402/4000-2 and FR406/4000-6) printed-circuit board material. The data converters and logic devices may be connected across a backplane using one or more impedance-controlled connectors or one or more cables.

The JESD204A PHY specification is similar to the OIF (Optical Internetworking Forum) SxI-5 and TFI-5 implementation agreements, generally referred to commercially as Current Mode Logic (CML). Compliant transmitters (TX) and receivers (RX) are expected to achieve Bit Error Rates (BER) of less than 1E−12; see Ref. 1 and Ref. 2.

The JESD204B draft specification additionally defines the OIF Common Electrical Interface (CEI) LV-6G-SR (Short Reach) as the 6.25 Gbps PHY (from 312.5 Mbps to 6.375 Gbps), and the OIF CEI-11G-SR as the 12.5 Gbps PHY. Note that LV-6G-SR compliant transmitters and receivers are expected to achieve BER of less than 1E−15; see Ref. 3.

Typically, TX pre-emphasis and RX equalization (EQ) on the converters and FPGAs/ASICs is an option at 12.5 Gbps, depending on the length of the transmission line. JESD204B retains the 20 cm “reach” (length) plus one or more impedance-controlled (100 Ω differential) connector transmission line characteristics as JESD204A. High quality PCB material such FR-4 Nelco 4000-13SI is also potentially necessary at 12.5 Gbps, again depending on the reach of the transmission line (transmission lines are called data “lanes” in JESD204A/B). Lanes less than 20 cm in length may not require TX pre-emphasis and RX EQ.

Altera Corporation has information on their web site relating to TX pre-emphasis and RX EQ; see Ref. 4.

Like JESD204A, 8B/10B is the coding scheme for JESD204B. Generally speaking, more efficient coders, such as 64B/65B, are used at higher line frequencies, however, it was considered “out of scope” to redefine the coding scheme for JESD204B by the JEDEC 150.01 task group. If there is sufficient industry interest, the coding scheme could be redefined as part of a future JESD204C revision.

The JESD204B specification includes new channel models for the 12.5 Gbps PHY specified as frequency-dependent Insertion Loss Deviation (ILD) masks required for 20 cm FR-4 (FR402/4000-2 and FR406/4000-6) and one or more impedance-controlled connectors or cables. Note that JESD204A specifies insertion loss more simply: the total insertion loss shall not exceed 6 dB from DC to 0.75 times the utilized baud rate.

JESD204A specifies TX and RX return loss (both single-ended and differential) with a single number: 7.5 dB minimum for TX, and 10 dB minimum for RX. In the JESD204B specification, the transmitter differential output return loss minimum (from 100 MHz to 0.75 times the utilized baud rate) is 8 dB, and the common mode return loss minimum (from 100 MHz to 0.75 times the utilized baud rate) is 6 dB. The receiver return loss minimums are the same.

JESD204A defines Total Jitter (TJ) as the sum of Deterministic Jitter (DJ) plus Random Jitter (RJ), measured in peak-to-peak normalized bit times or “unit intervals” (UI). In JESD204A with the 3.125 Gbps PHY, transmitter TJ = 0.35 (p-p) UI, DJ = 0.17 (p-p) UI and RJ = 0.08 (p-p) UI, where UI ranges from 3200 p/s to 320 p/s. The receiver TJ = 0.56 (p-p) UI, DJ = 0.32 (p-p) UI and RJ = 0.24 (p-p) UI over the same range of UI.

In the JESD204B specification, total jitter is defined the same way.

3. Deterministic latency – three new device subclasses in JESD204B

In the context of JESD204B, deterministic latency is measured from the parallel frame-based data input of a TX device (typically an ADC), to the parallel frame-based data output of an RX device (typically a DAC), measured within the frame clock domain. JESD204B latency is defined (and is programmable) in units of frame clock cycles or periods. The latency **must** be precisely repeatable from power-up cycle to power-up cycle, and across link resynchronization events.

JESD204B defines three normative Device Subclasses with respect to Deterministic Latency/Harmonic Clocking (DLHC):

Device Subclass 0 has no support for deterministic latency.

Device Subclass 1 defines a new source-synchronous “SYSREF signaling” high-resolution timing (deterministic up to approximately 2 GHz sampling clock frequencies) DLHC protocol, with either a periodic SYSREF, a one-shot (strobe-type) SYSREF or a “gapped periodic” SYSREF distributed to all ADCs/DACs and ASIC/FPGA logic devices. **The SYSREF signal synchronizes system-wide local TX and RX frame and multi-frame counters/dividers and the reading of RX FIFO output buffers in JESD204B**.

Device Subclass 2 uses the legacy SYNC~ signal, but in a system-synchronous “SYNC~ sampling” low-resolution timing DLHC protocol. This provides accurate deterministic latency up to approximately 500 MHz sampling frequencies, utilizing SYNC~ de-assertion to phase adjust ADC, DAC and logic device frame clock and multi-frame clock counters/dividers (combined with control interface-based triggering). **The SYNC~ signal conveys interface latency timing information in JESD204B, from the receiver back to the transmitter**.

JESD204B defines new physical clock signals:

Device clock: a global master clock signal synthesized by a system clock generator circuit from which all TX and RX devices (data converters and logic devices) generate their internal frame clock, and multi-frame clock signals. The device clock period is the absolute timing reference in a JESD204B system. Note that the device clock signal can be a harmonic multiple of the frame clock; **this relates directly to the harmonic clocking feature of JESD204B**.

SYSREF: a “global” timing reference signal that can be periodic, one-shot (strobe type), or “gapped” periodic and used to align frame clock and Local Multi-Frame Clock (LMFC) boundaries. SYSREF is an active HIGH signal that is sampled by the rising edge of the device clock. SYSREF is only used in Device Subclass 1 systems. The SYSREF source must be the same as the device clock source, typically a crystal oscillator time base, such as a low jitter TCXO or VCO/PLL.

It is helpful here to recall the definition of frame, multi-frame and LMFC from the JEDEC JESD204A specification:

Frame: a set of consecutive octets in which the position of each octet can be identified by reference to a frame alignment signal.

Multi-frame: a set of consecutive frames in which the position of each frame can be identified by reference to a multi-frame alignment signal.

LMFC: Local Multi-Frame Clock.

4. Harmonic frame clocking simplifies the PCB-level clock synthesis and distribution challenge

Simply put, harmonic clocking allows the use of, for example, a 2×, 3×, 4×, 5×, 6×, 7× or 8× sampling frequency (f_S) device clock as the only PCB-level data converter clock, without the need for an additional sampling frequency-based frame clock. The recovered clock from the JESD204B differential input data lane signals is used as the data interface "bit clock". With harmonic clocking, **or single clock system architecture**, TX and RX devices can generate all internal clocks from a single clock source, provided that the single clock source is a harmonic multiple of the frame clock.

As a practical example, in the case of a high-speed interpolating DAC architecture, assuming an internal PLL is not used, it is typically required to generate a high-quality device clock signal that is 2×, 4× or 8× the input data rate sampling frequency. This same 2×, 4×, or 8× clock can then be used as the device clock for the ADC, where it is internally divided to create the sampling clock and frame clock.

The advantages of single clock system architectures include reduced IC package pin count and lower risk of detrimental clock feed-through (or crosstalk) effects. In general, fewer clocks at the system PCB level reduce the potential for the disturbance of the ADC and DAC analog performance. At the system PCB level, the design engineer has only one data conversion clock to synthesize and distribute.

5. Unique system value enhancements from JESD204A/B

The new JEDEC JESD204A/B data converter interface definition has numerous system-level technical and commercial merits:

- Simplified PCB layout and routing, with the potential for PCB cost reduction (fewer signal layers, smaller PCB form factor, no data lane-to-clock skew management)
- Data converter and FPGA or ASIC pin count reduction, enabling higher channel count per FPGA or ASIC, with the potential for BOM cost reduction
- Increased system performance, enabling higher bandwidth digital signals over fewer PCB traces
- 8B/10B PHY is compatible with fibre optic signalling for long reach applications
- EMI/RFI radiation reduction, with the potential for easier device compliance test approval
- Reduced signal skew management, with the potential for reduced engineering development cost
- No PCB redesign for data converter resolution changes (12-bit to 16-bit), only FPGA logic reconfiguration/recoding, with the potential for reduced engineering development cost and faster end-product qualification
- Single bit error detection, by virtue of 8 B/10 B coding, with the potential for increased system reliability
- Multiple time-aligned and phase coherent data converter channels for system designs such as LTE MIMO base stations, with the potential for simplified system design and reduced engineering development cost
- Interoperability with SERDES-based FPGAs, with the major vendors offering compliant IP for their latest cost-effective programmable logic products
- Periodic frame alignment monitoring with the potential to maintain frame alignment without data loss for system reliability and robustness
- Optional data and control symbol scrambling to produce data independence across the JESD204A/B link, with the potential to reduce non-harmonic spurs in the data converter analog domain
- Optional embedded Pseudo-Random Bit Sequence (PRBS) generation (TX) and checking (RX) for simplified board-level Built-In Self Test (BIST)
- Elimination of CMOS parallel bus buffers, with BOM reduced and schematic/layout simplification

6. Conclusion – exciting backwards-compatible future path

As base station and other data acquisition and signal synthesis equipment designers drive relentlessly toward lower capital and operating expense goals, JESD204A interface high-speed data converters can help meet those goals. With the enhancements offered by JESD204B, system designers can save even more in the critical metrics of “dollars, Watts and square inches”, making this new data converter and logic device digital interface more compelling than ever. With the expected availability of JESD204B data converters in the second half of 2011, the widespread adoption of this interface in 2012 seems to be assured.

7. Abbreviations

Table 2. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
ASIC	Application-Specific Integrated Circuit
BOM	Bill Of Materials
DAC	Digital-to-Analog Converter
DSP	Digital Signal Processor
EMI	ElectroMagnetic Interference
FIFO	First-In-First-Out
FPGA	Field-Programmable Gate Array
IP	Intellectual Property
LTE	Long-Term Evolution
MIMO	Multiple-Input/Multiple-Output
NRE	Non-Recurring Engineering
OEM	Other Equipment Manufacturer
PCB	Print-Circuit Board
PHY	PHYsical layer protocol
PLL	Phase-Locked Loop
RFI	Radio Frequency Interference
SerDes	Serializer Deserializer
TCXO	Temperature-Controlled Crystal Oscillator
TDM	Time-Division Multiplexing
UI	Unit Interval
VCO	Voltage-Controlled Oscillator

8. References

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