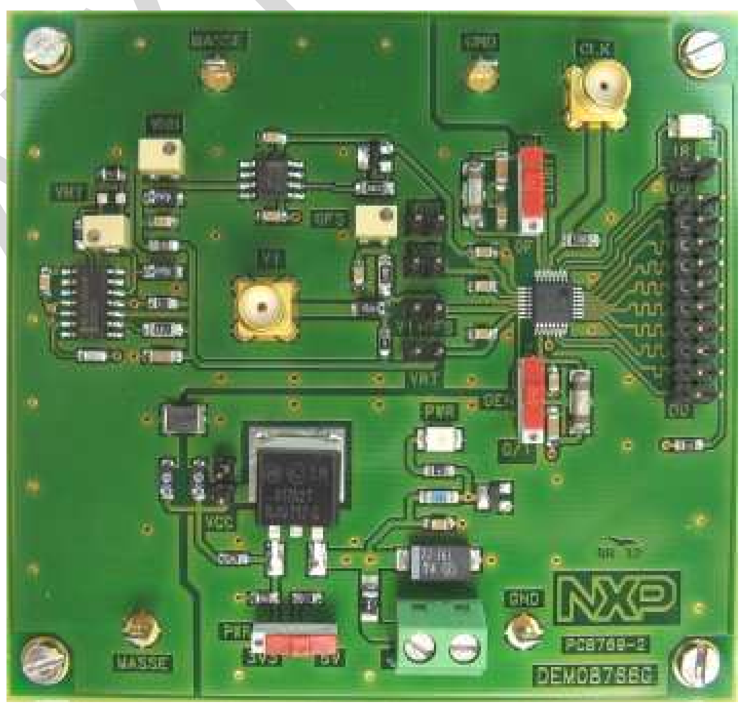
Quick Start ADC1002S020

Demonstration board for ADC1002S020

Rev. 2 — 11 octobre 2010 | Quick Start

Document information

Info	Content
Keywords	DEMO8766G, PCB769-2, Demonstration board, ADC, Converter, ADC1002S020
Abstract	This document describes how to use the demonstration board DEMO8766G for the analog-to-digital converter ADC1002S020.
Overview	

Revision history

Rev	Date	Description
1	20080612	Initial version.
2	20101011	Update for data acquisition system.

Contact information

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1. Overview of the ADC1002S020 demo board

1.1 ADC1002S020 demoboard

Figure 1 presents the connections to measure the ADC1002S020 based on DEMO8766G:

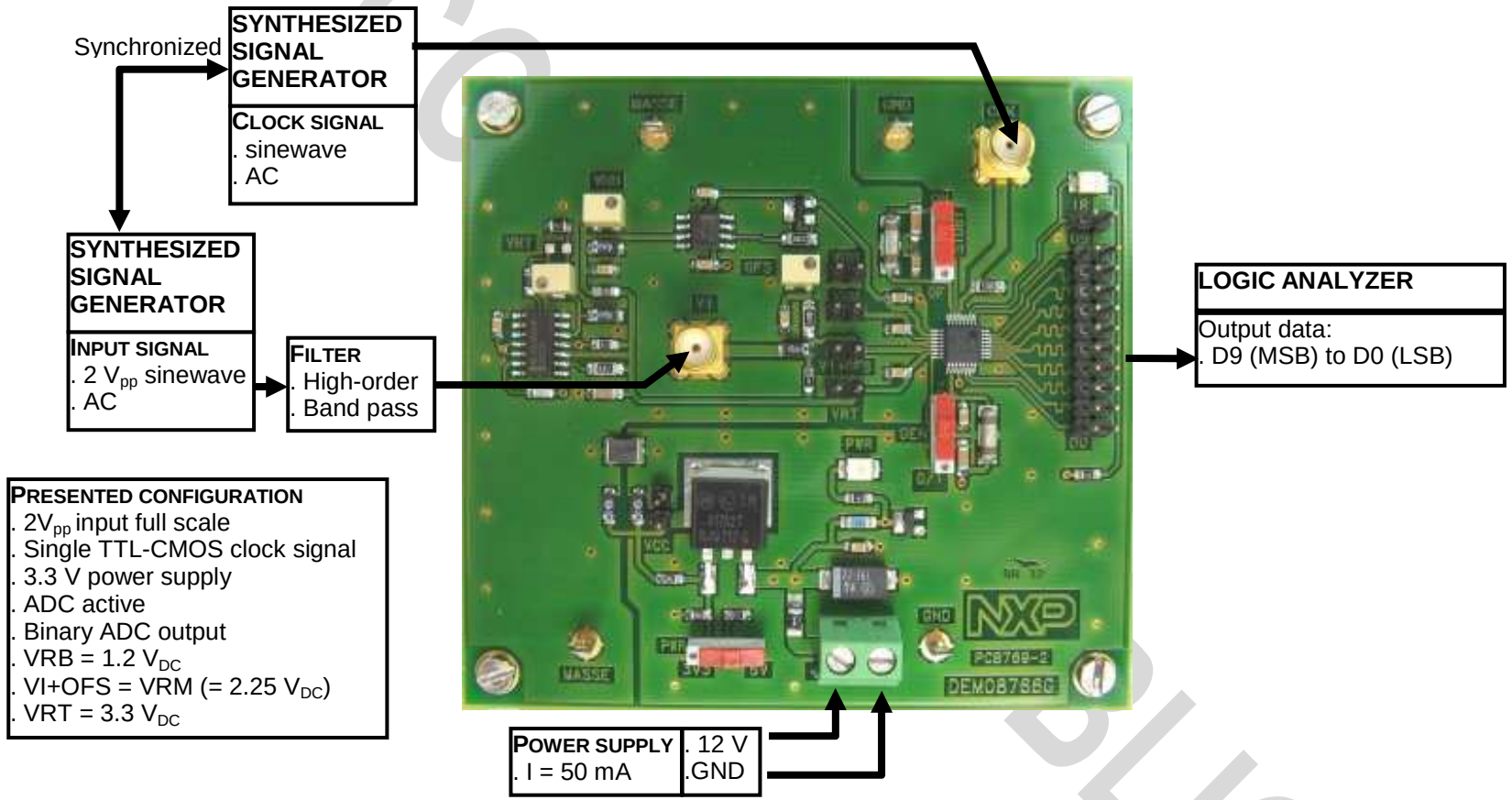
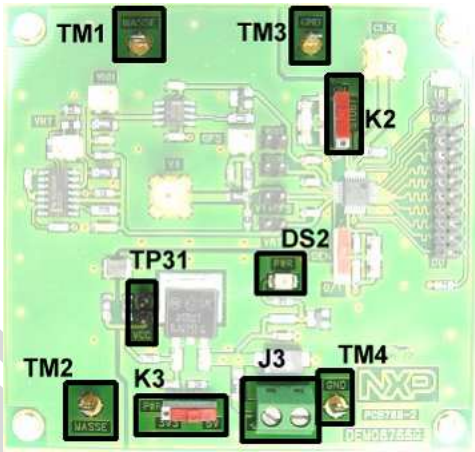


Fig 1. ADC1002S020 demoboard set-up

1.2 Power supply

The board is powered with a single 12 V_{DC} power supply. A power supply regulator is used to supply all the circuitry on the board.

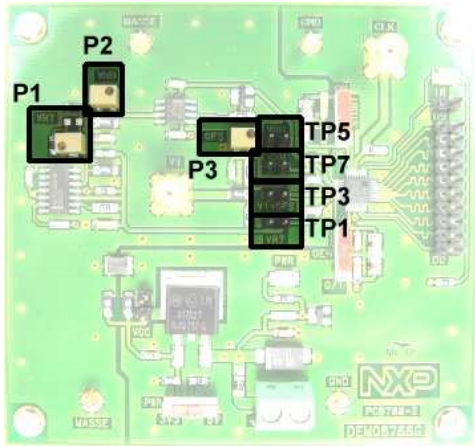
Table 1. General power supply

Name	Function	View
J3	Green connector – Power supply 12 V_{DC} / 50 mA.	
DS2	PWR green light – It indicates the good supply plugging	
K3	PWR switch – ADC power supply selection  3.3 V  5 V	
TP31	VCC test point – ADC power supply	
TM1, TM2	MASSE test point – Analog ground	
TM3, TM4	GND test point – Digital ground	
K2	STDBY switch – ADC stand-by activation ADC active  ADC OFF 	

1.3 DC voltage adjustments

The ADC1002S020 allows to adjust the full scale input signal from 1.6 V to 2.4 V.

Table 2. DC voltage adjustments

Name	Function	View
P1	VRT trimmer – TOP reference adjustment	
TP1	VRT test point – TOP reference value (typ 3.3 V)	
P2	VRB trimmer – BOT reference adjustment	
TP5	VRB test point – BOT reference value (typ 1.2 V)	
P3	OFS trimmer – Input signal DC offset adjustment	
TP3	VI+OFS test point – Input signal DC offset (typ 2.25 V)	
TP7	VRM test point – MIDDLE reference value (typ 2.25 V)	

1.4 Input signals (VI, CLK)

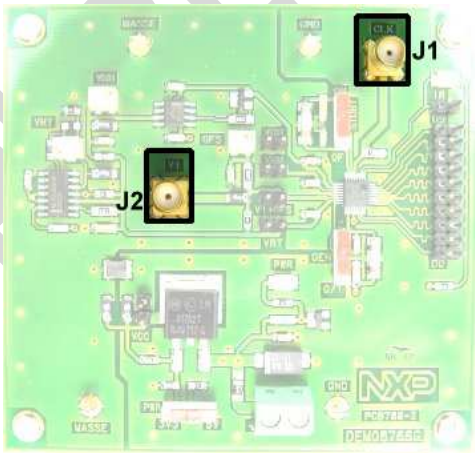
To ensure a good evaluation of the device, the input signal and the input clock must be synchronized together.

Moreover, the input frequency (Fi, MHz) and the clock frequency (Fclk, Msps) should follow the formula:

$$\frac{Fi}{Fclk} = \frac{M}{N}$$

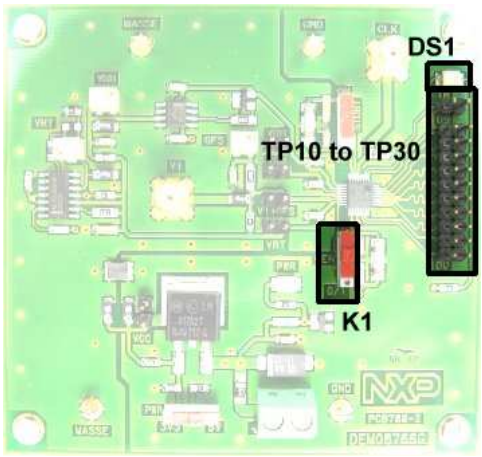
, where M is an odd number of period and N is the number of samples.

Table 3. Input signals

Name	Function	View
J2	VI connector – Analog input signal (50Ω matching)	
J3	CLK connector – Clock input signal (50Ω matching)	

1.5 Output signals (D0 to D9, IR)

Table 4. **Output signals**

Name	Function	View
TP10 to TP30	Array connector – ADC digital output(D0 to D9) and In range signal (IR)	
DS1	IR green light – It indicates that the analog input signal is in the full scale range	
K1	OEN switch – Output enable selection Active output  High impedance output 	

2. HSDC extension module: acquisition board

The figure 2 shows an overview of the extension module HSDC-EXTMOD01/DB acquisition board:

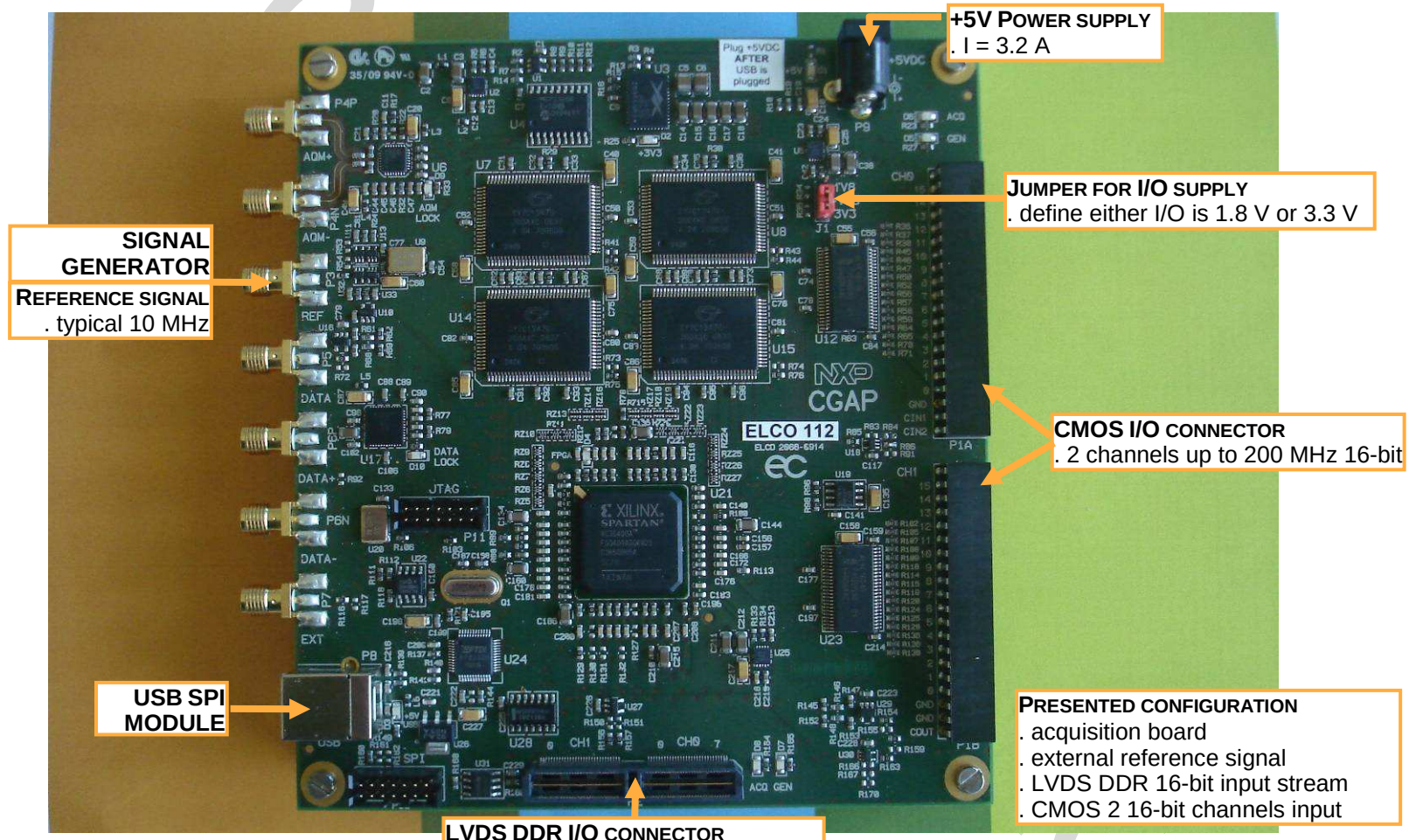


Fig 2. HSDC extension module: acquisition board

The HSDC extension module is intended for acquisition/generation and clock generation purpose. When connected to an ADC demo-board it is intended as an acquisition system for digital output bits delivered by ADC, either CMOS (HE14 P1 connector) or LVDS DDR (SAMTEC QTH_060_02 P2 connector).

The board brief specification is shown below:

- 8MB memory size for acquisition pattern;
- 2 16-bit channels CMOS up to 200 MHz;
- 16-bit LVDS DDR input data stream up to 320 MHz;
- On-board or external reference for signal generation.

In this section the specific requirement for the use with ADC1002S020 demo-board will be shown.

For more details on the HSDC-EXTMOD01/DB, please contact dataconverter-support@nxp.com.

2.1 HSDC extension module: hardware initialization

Before using the generation board, make sure that you connect the USB cable **prior to** the supply.

2.2 HSDC extension module: software initialization

Before using the generation board, the user needs to install software to control the board. The steps are described below.

Go to the installation directory “\HSDC-EXTMOD01\Software\USBConfigSetup v1.3 100212 1525” on the CD. Double click on the file “CDM 2.04.16.exe” file.

Run the application “\HSDC-EXTMOD01\Software\USBConfigSetup v1.3 100212 1525\USBConfigSetup.msi”, this will display the following window:

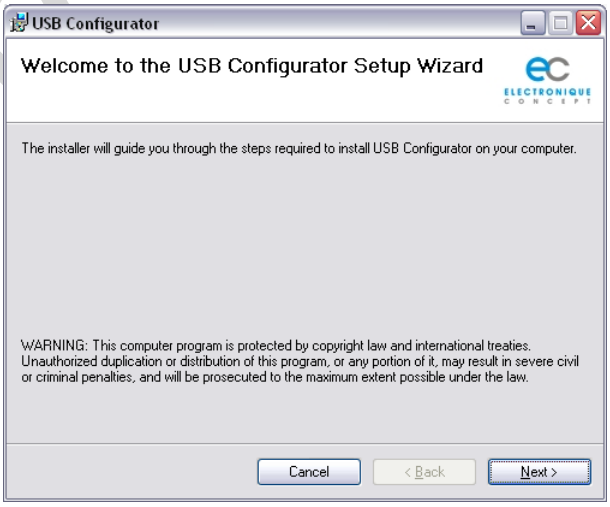


Fig 3. “USBConfigSetup” window: step 1

Click “Next” to proceed with installation process:

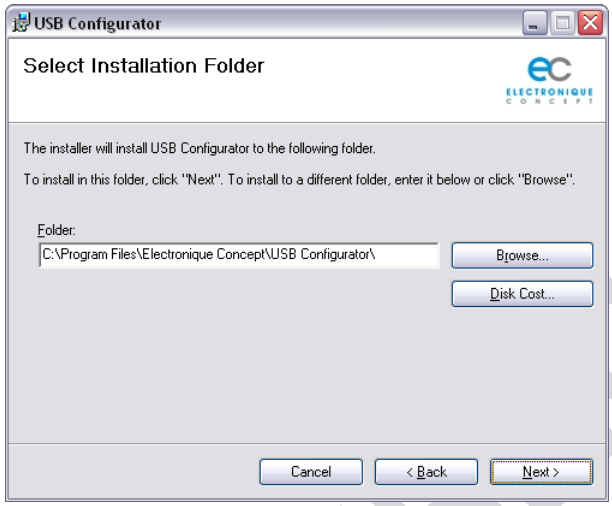


Fig 4. "USBConfigSetup" window: step 2

Click "Next" to continue:

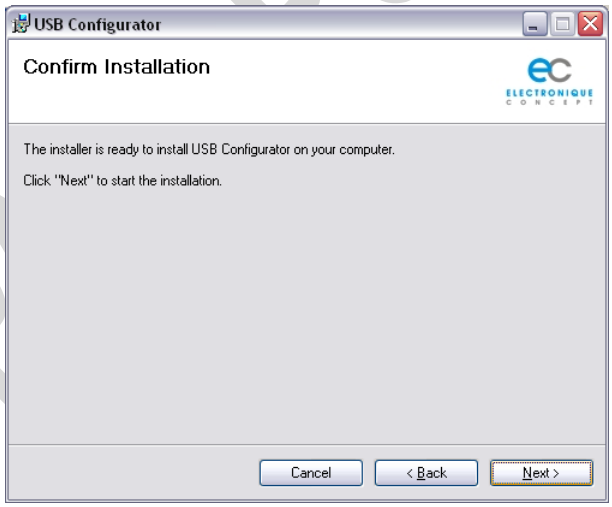


Fig 5. "USBConfigSetup" window: step 3

Click "Next" to finish the installation process.

The system is now ready to use the ADC1412D series board for evaluation purpose.

2.3 HSDC extension module: CMOS connector description

The figure 6 shows a brief description of the hardware connection on the HE14 connector:

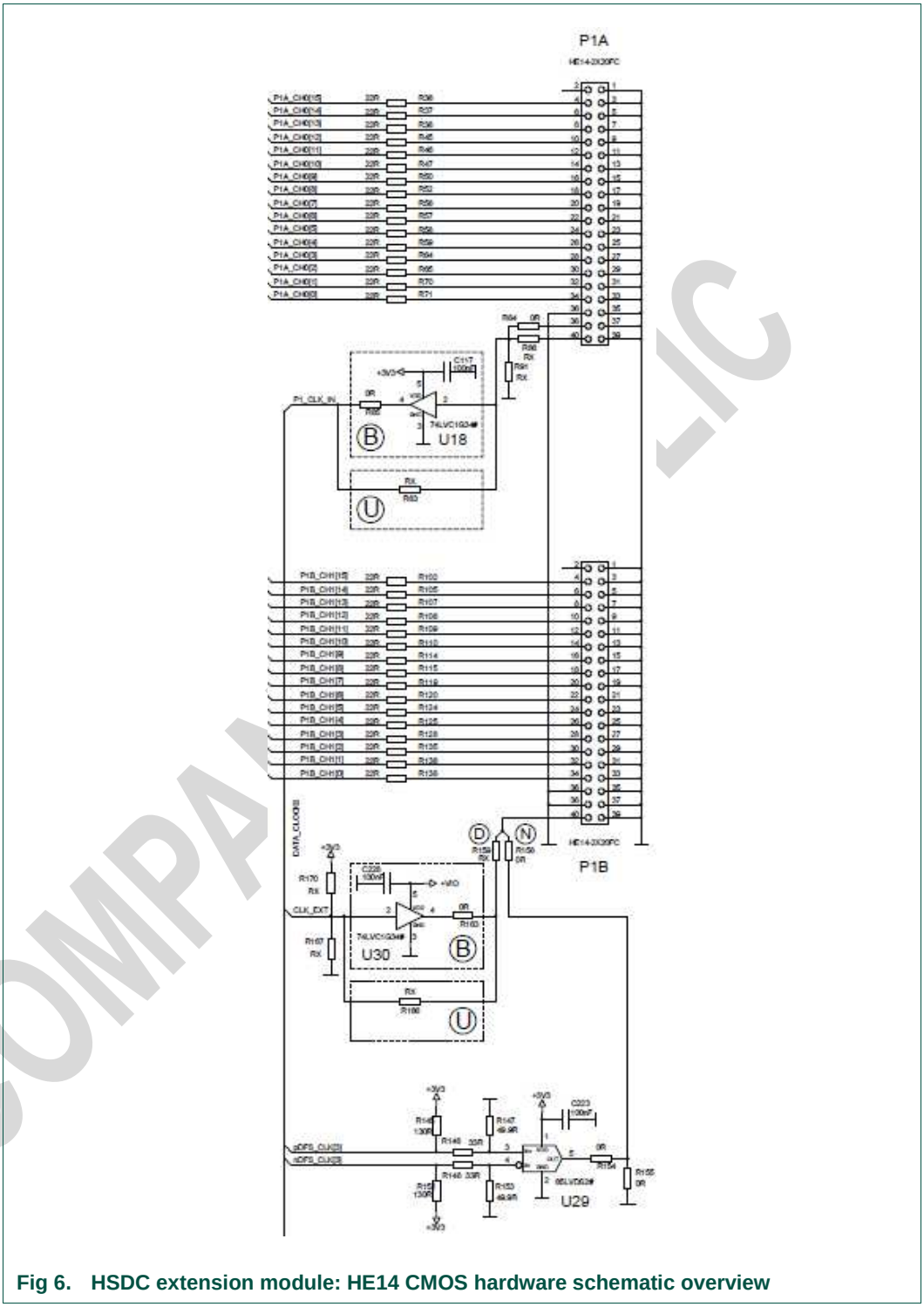


Fig 6. HSDC extension module: HE14 CMOS hardware schematic overview

The HSDC extension module can acquire data in CMOS level using:

- either the on-board clock generated by the internal PLL, refer to as pDFS_CLK[0]/nDFS_CLK[0] that will be used by the FPGA. In this case, the reference of the board should be delivered by the clock signal generator;

- or the clock provided by the ADC refer to as P1_CLK_IN. This is the preferred situation since the user will not deal with any set-up/hold timing for the acquisition.

Refer to section 3.2 for software configuration.

3. Combo ADC1002S020 and HSDC extension module

3.1 Measurement set-up overview

The figure 07 below shows an overview of the whole system ADC1002S020+HSDC extension module for which connection is done with the accessory (HSDC-ACC07/DB). The measurement set-up presented below shows 1 generator for input signal. Clock signal is delivered by the HSDC-EXTMOD for ADC clocking and data acquisition purpose:

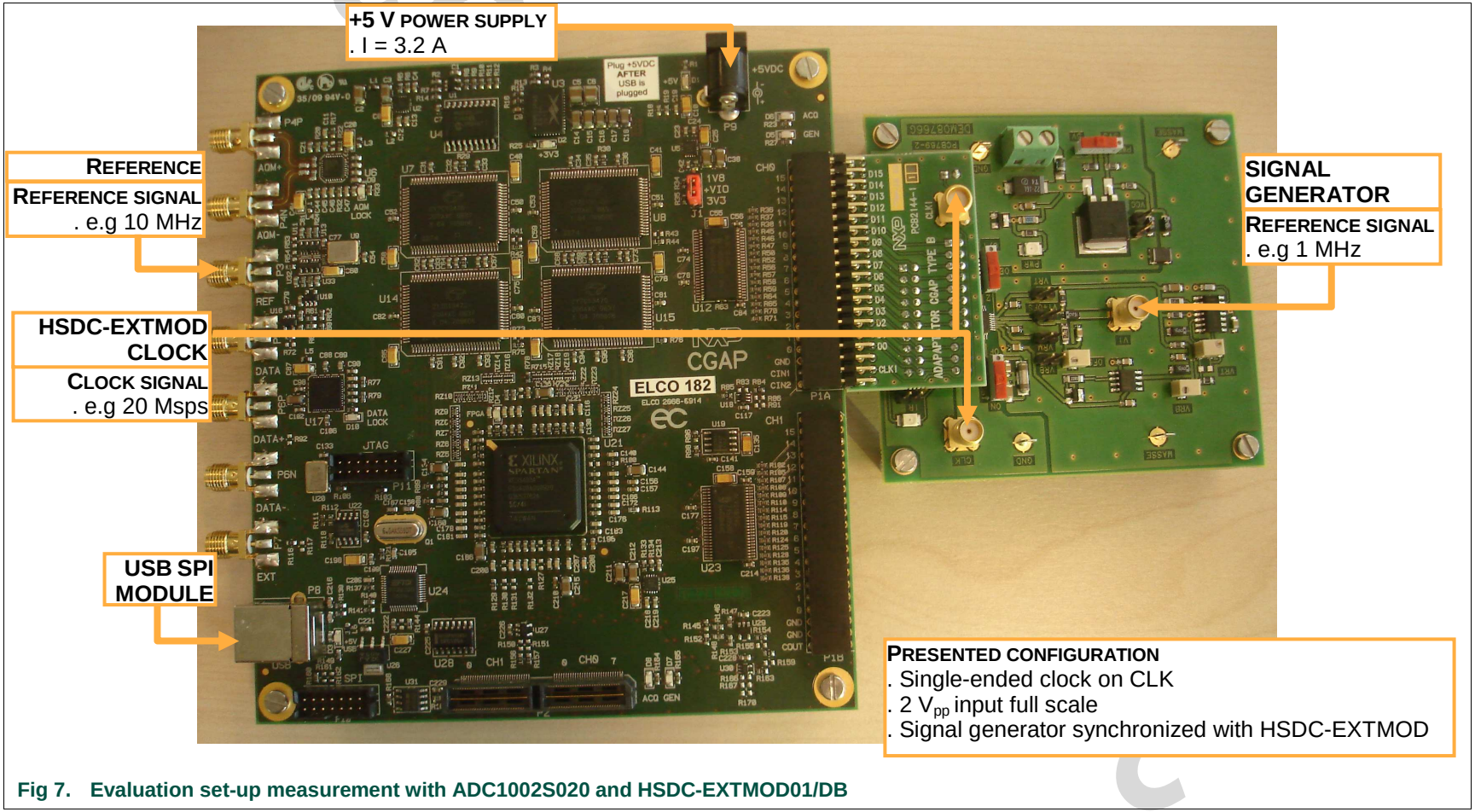


Fig 7. Evaluation set-up measurement with ADC1002S020 and HSDC-EXTMOD01/DB

3.2 HSDC extension module: FPGA flash

To get access to the software control of the generation system, run the “USB Configurator.exe”. It is located by default in the directory "C:\Program Files\Electronique Concept\USB Configurator\".

If a HSDC extension module is connected to the user system it will display the following window:

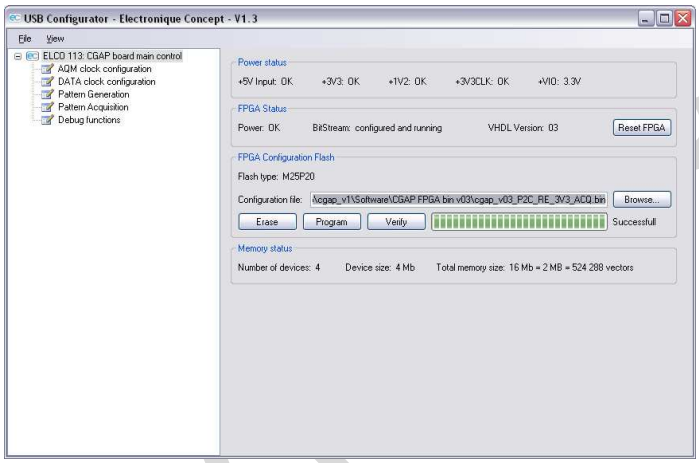


Fig 8. “USB Configurator” window: board main control

This window gives an overview of the current status of the board connected. If supply is not connected, a FAIL status appears on the Power status field.

Flash the FPGA with the appropriate bin file provided on the CD located at “\HSDC-EXTMOD01\Software\USBConfigSetup v1.3 100212 1525\HSDCEXTMOD FPGA bin v03”. Among the 8 files, 2 are considered here:

- “HSDCEXTMOD_v03_P1C_RE_3V3_GEN.bin”: the FPGA will use the rising edge of the clock delivered by connector P1C;
- “HSDCEXTMOD _v03_P1C_FE_3V3_ACQ.bin”: the FPGA will use the falling edge of the clock delivered by connector P1C.

For further details regarding the others file please contact dataconverter-support@nxp.com.

Browse to select the wanted bin file. Click “Erase” and “Program” buttons. Once the “Successful” message appears, click “Reset FPGA” button: board is programmed.

3.3 HSDC extension module: DATA clock configuration

To acquire the digital input pattern on P1 connector, the user needs to choose the wanted frequency. In our example, the frequency used for acquisition is 20 MHz and the reference signal is provided on external “REF” pin:

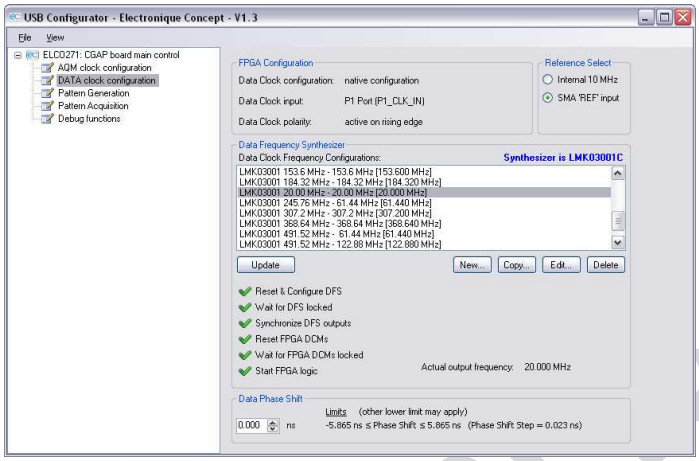


Fig 9. "USB Configurator" window: DATA clock configuration

The FPGA configuration indicates which configuration file has been programmed in FPGA, in the example shown it is the rising edge of the embedded clock.

In the directory "\HSDC-EXTMOD01\Software\USBConfigSetup v1.3 100212 1525\Config" of the CD, there are 2 configurations files that already defines frequencies for the DFS and AFS (AQM clock configuration that we don't use here). Copy these files to the directory "C:\Documents and Settings\All Users\Application Data\Electronique Concept\UsbConfig" to get access to these frequencies.

Select "LMK03001 20 MHz – 20 MHz (20.000 MHz)" to define the frequency to be 20 MHz. The pattern will be acquired as this sampling rate, meaning 20 MHz CMOS.

Click "Update", this should display 6 green check boxes and the value of the corresponding frequency being actually generated by the board.

The Data Phase Shift allows the user to shift the clock position wrt data by the amount of time indicated.

Note: you can edit the LMK file by clicking on the "Edit…" button to define your own frequency, as long as you respect the frequency range defined by the PLL. For other frequencies to generate, please contact dataconverter-support@nxp.com for more details.

3.4 HSDC extension module: pattern acquisition

The clock frequency is defined, and the board is ready to acquire the pattern.

In order to do the acquisition, the number of samples needs to be filled in the Pattern size field: this number is a power of 2 with a maximum of 8MB.

Select one-shot mode and source P1 to acquire data (see figure 10).

The hardware connection between the ADC1002S020 and the HSDC extension module has to be described to get correct results. This is done by using the fields in "Channel 0 Input Configuration" and in "Channel 1 Input Configuration".

The channel 0 receives the data from ADC where ADC MSB is connected to the 1st bit and ADC LSB is connected to the 10th bit of the HSDC extension module. Tune the fields "Input is located on file A between xx (MSB) and xx (LSB)" to describe this configuration (see figure 10).

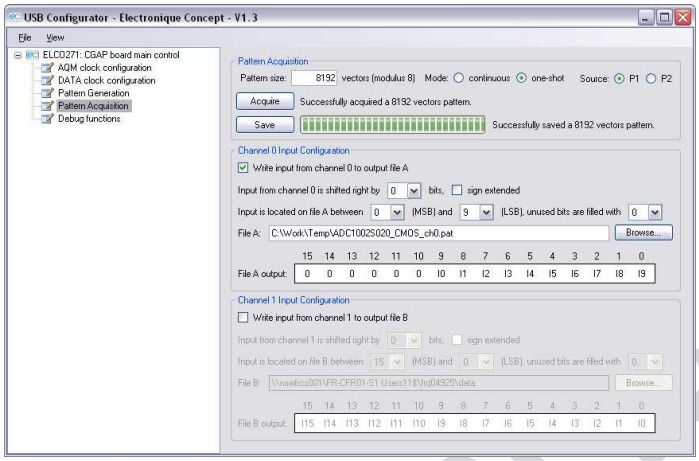


Fig 10. “USB Configurator” window: pattern acquisition for ADC1002S020

3.4.1 Pattern acquisition

Browse on both channel path configuration to select the file to store the data that will be acquired.

Click on “Acquire” and “Save” buttons to end the capture process.

3.5 FFT post-processing

Once acquisition is done, the captured data can now be processed for FFT results using the “NXP_ADC_Acquisition.exe” tool located under directory “\HSDC-EXTMOD01\Software\NXP_ADC_Acquisition” of the CD.

Run the application it will display the following window:

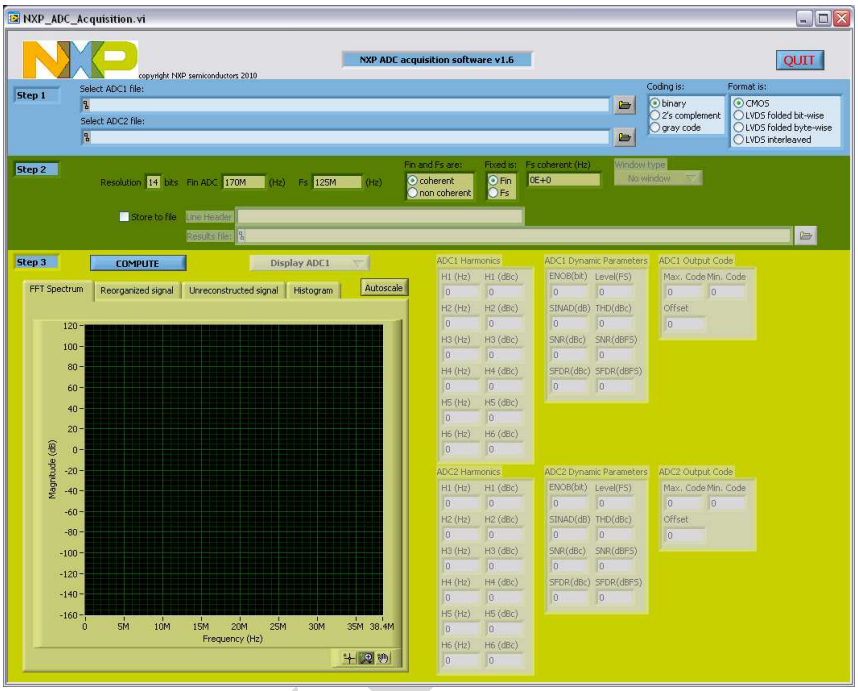


Fig 11. “NXP_ADC_Acquisition” window: start-up screen

3.5.1 Acquisition software: input files

The first step consists in delivering the files to be processed. Browse in field “Select ADC1 file:” to indicate the file to be used.

Indicate the data format (by default data are stored in binary format).

Note: both files needs to have the same data format and have the same input and clock frequency.

Indicate CMOS mode.

3.5.2 Acquisition software: frequency indication

The second step consists in indicating the relevant numbers for the FFT processing:

- the resolution N: 10 in this case;
- the input frequency Fin: 1.25 MHz in our example;
- the sampling frequency Fs: 20 Msps in our example;
- whether Fin or Fs are coherent or not:
  - if signals are coherent, selected which Fin or Fs are fixed for the calculation (see appendix A.1). The value of coherent frequency resulting from this calculation will be displayed (this corresponds to the value to be generated in front of the ADC);
  - if signals are not coherent, select the window for FFT processing to apply (the Blackman window gives better results).

The example shown below is for Fin = 1.25 MHz Fs = 20 Msps, with Fin and Fs coherent and Fs fixed value in CMOS mode:

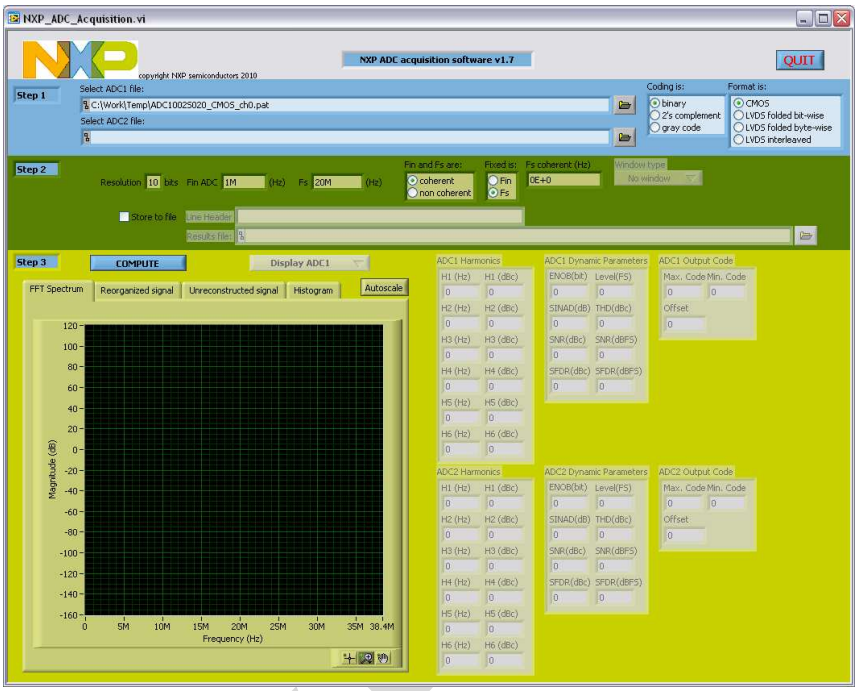


Fig 12. "NXP_ADC_Acquisition" window: frequency entry

3.5.3 Acquisition software: FFT results display

Press the "COMPUTE" button to display the results from the FFT processing. The results fields will be updated depending on the number of input files. If 2 files have been processed, it is possible to display both results on the same picture for all graphs using the "Display …" button ("Display ADC1" or "Display ADC2" or "Display ADC1 & ADC2").

3.5.3.1 FFT spectrum

The first graph to be displayed is the FFT spectrum of the digital pattern acquired:

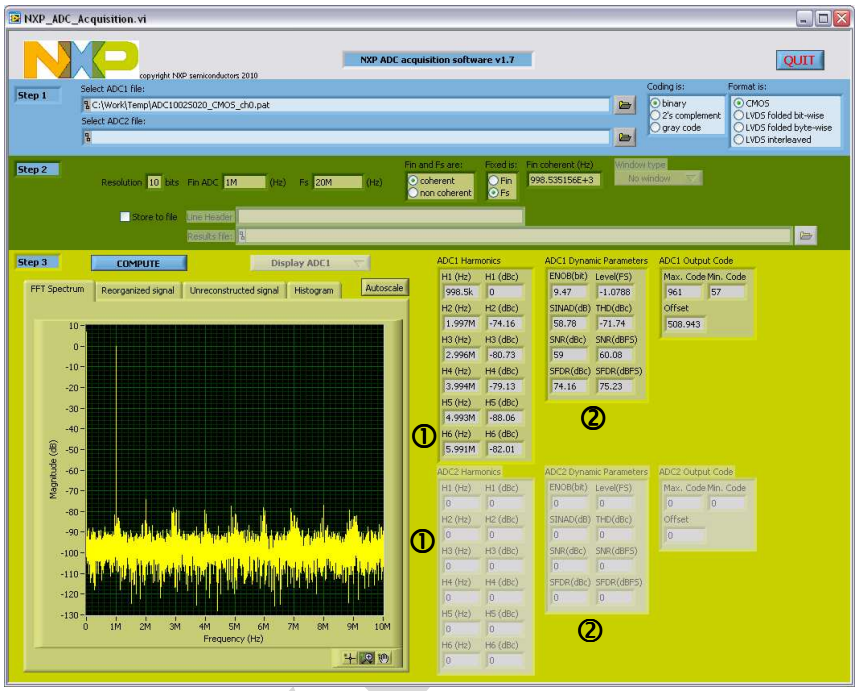


Fig 13. "NXP_ADC_Acquisition" window: FFT result

Press the "Autoscale" button to display the whole content.

The tables ① and ② give the relevant dynamic parameters:

- Table ①: first 6 harmonics frequencies and amplitude level;
- Table ②: dynamics parameters:
  - ENOB expressed in bit;
  - Level of the digital output signal relative to the full-scale;
  - SINAD in dBc;
  - THD in dBc calculated over first 6 harmonics;
  - SNR in dBc and dBFS;
  - SFDR in dBc and dBFS.

3.5.3.2 Reorganized signal

The Reorganized signal displays the reconstructed sine wave from coherency calculation corresponding to 1 period of the input signal:

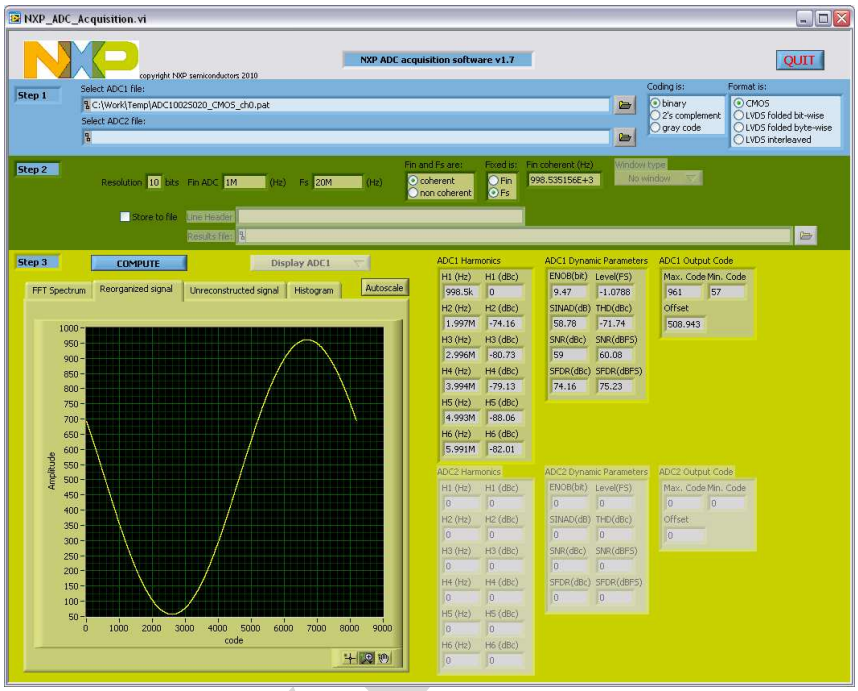


Fig 14. "NXP_ADC_Acquisition" window: reorganized signal

Press the "Autoscale" button to display the whole content.

3.5.3.3 Unreconstruted signal

The unreconstructed signal displays the unreconstructed sine wave corresponding to the whole number of period being acquired following the coherency rule:

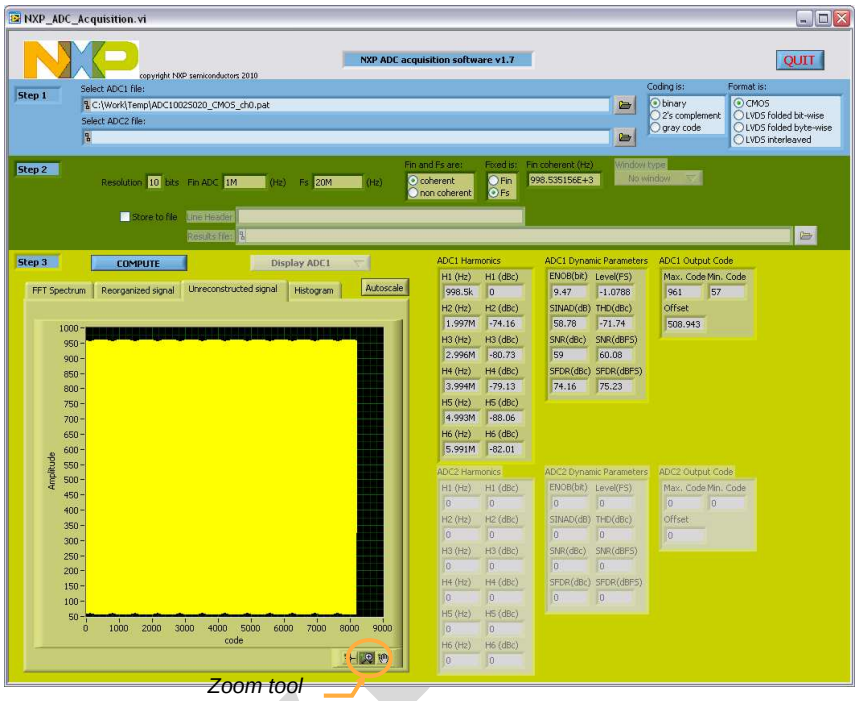


Fig 15. "NXP_ADC_Acquisition" window: unreconstruted signal

Press the "Autoscale" button to display the whole content.

Use the zoom tool to observe in more details all the captured data.

3.5.3.4 Histogram

The histogram graph shows the distribution of output codes. This graph allows to know which code is present and if there is any missing code in the conversion range:

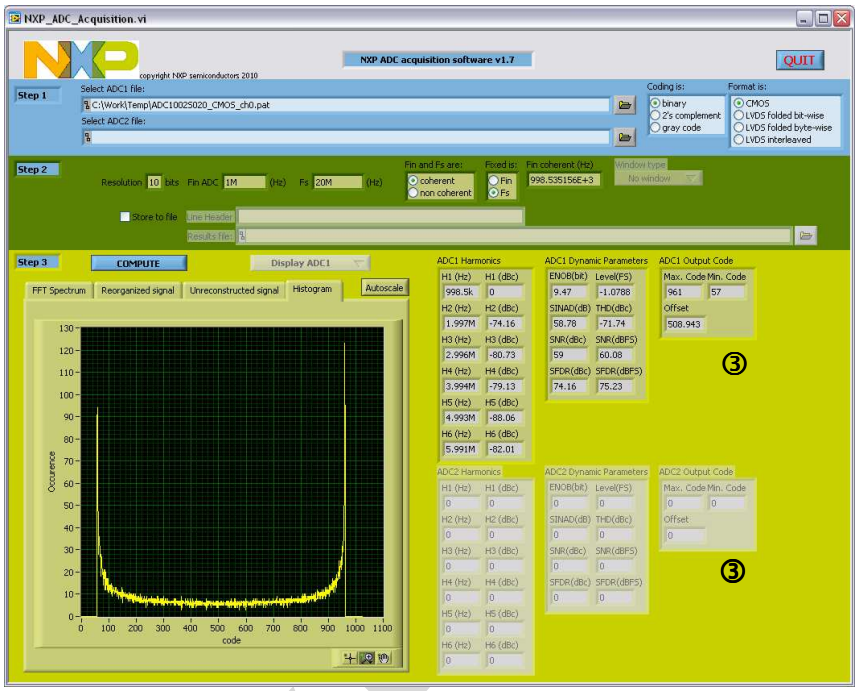


Fig 16. “NXP_ADC_Acquisition” window: code histogram

Press the “Autoscale” button to display the whole content.

The table ③ shows the range of output codes.

4. Appendix A.1: coherency calculation

The coherency relies on the fact that clock and analog input signal are synchronized and the first and last samples being captured are adjoining samples: it ensures a continuous digitized time process for the FFT processing.

To achieve this, one has to follow the equation:

$$\frac{F_{in}}{F_s} = \frac{M}{N}$$

where M is an odd integer equal to the number of periods being acquired and N the number of samples acquired.

With Fin, Fs and N known, M has to be chosen such that it follows the equation above. To do this iterative calculation, one has to decide whether Fin or Fs is fixed.

To illustrate this process, let's consider our current example with Fin = 1 MHz, Fs = 20 Msps and N = 8192 samples acquired:

- if Fin is fixed, this leads to M = 409 periods of input signal to be acquired and a real sampling frequency to be Fs = 20.0293399 MHz;
- if Fs is fixed, this leads to M = 409 periods of input signal to be acquired and a real input frequency to be Fin = 0.998535156 MHz.

Those values needs to be programmed in the signal generator and clock generator before capture is done, otherwise the FFT calculation will lead to a non-coherent result as shown below:

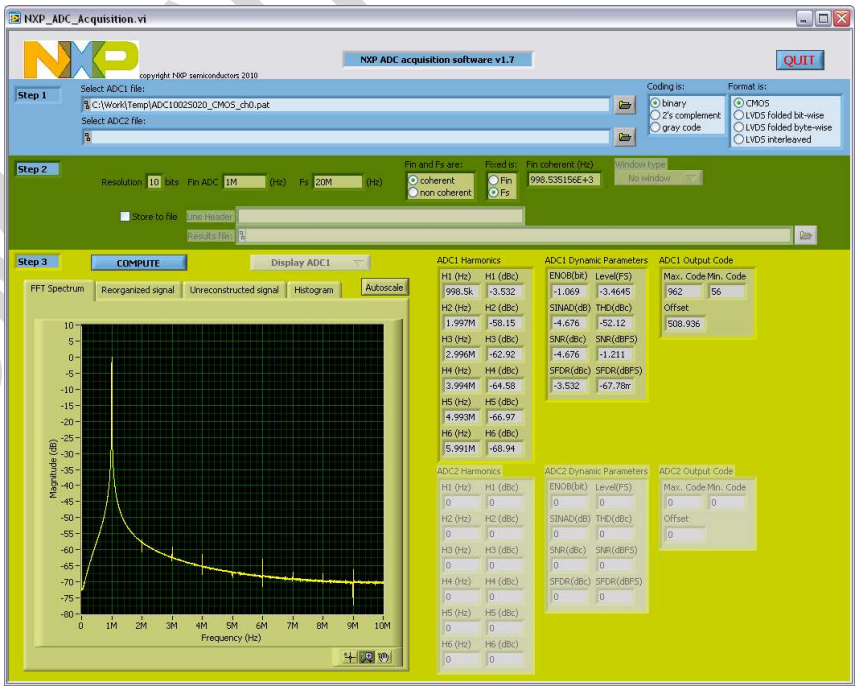


Fig 17. "NXP_ADC_Acquisition" window: non-coherent capture example

The numbers given for SNR, SFDR are completely wrong if coherency is not respected.

5. Notes

For any question, feel free to contact us at the following e-mail dataconverter-support@nxp.com.

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