



# Mobile SDRAM

**MT48H16M16LF – 4 Meg x 16 x 4 banks**

**MT48H8M32LF – 2 Meg x 32 x 4 banks**

## Features

- Fully synchronous; all signals registered on positive edge of system clock
- VDD/VDDQ = 1.70–1.95V
- Internal, pipelined operation; column address can be changed every clock cycle
- Four internal banks for concurrent operation
- Programmable burst lengths: 1, 2, 4, 8, or continuous page<sup>1</sup>
- Auto precharge, includes concurrent auto precharge
- Auto refresh and self refresh modes
- LVTTL-compatible inputs and outputs
- On-chip temperature sensor to control refresh rate
- Partial-array self refresh (PASR)
- Deep power-down (DPD)
- Selectable output drive (DS)
- 64ms refresh period (8,192 rows)

## Options

- VDD/VDDQ
  - 1.8V/1.8V
- Configuration
  - 16 Meg x 16 (4 Meg x 16 x 4 banks)
  - 8 Meg x 32 (2 Meg x 32 x 4 banks)
- Plastic “green” package
  - 54-ball VFBGA (8mm x 9mm)
  - 90-ball VFBGA (8mm x 13mm)
- Timing – cycle time
  - 7.5ns at CL = 3
  - 8ns at CL = 3
- Power
  - Standard IDD2P/IDD7
  - Low IDD2P/IDD7
- Operating temperature range
  - Commercial (0° to +70°C)
  - Industrial (–40°C to +85°C)
- Design revision

## Marking

H

16M16

8M32

BF

B5

–75

–8

None

L

None

IT

:G

**Table 1: Addressing**

	<b>16 Meg x 16</b>	<b>8 Meg x 32</b>
Configuration	4 Meg x 16 x 4 banks	2 Meg x 32 x 4 banks
Refresh count	8K	8K
Row addressing	8K (A0–A12)	4K (A0–A11)
Bank addressing	4 (BA0, BA1)	4 (BA0, BA1)
Column addressing	512 (A0–A8)	512 (A0–A8)

**Table 2: Key Timing Parameters**

CL = CAS (READ) latency

Speed Grade	Clock Rate (MHz)		Access Time		Data Setup Time	Data Hold Time
	CL = 2	CL = 3	CL = 2	CL = 3		
–75	104	133	8ns	6ns	1.5ns	1ns
–8	100	125	9ns	7ns	2.5ns	1ns

Notes: 1. For continuous page burst, contact factory for availability.

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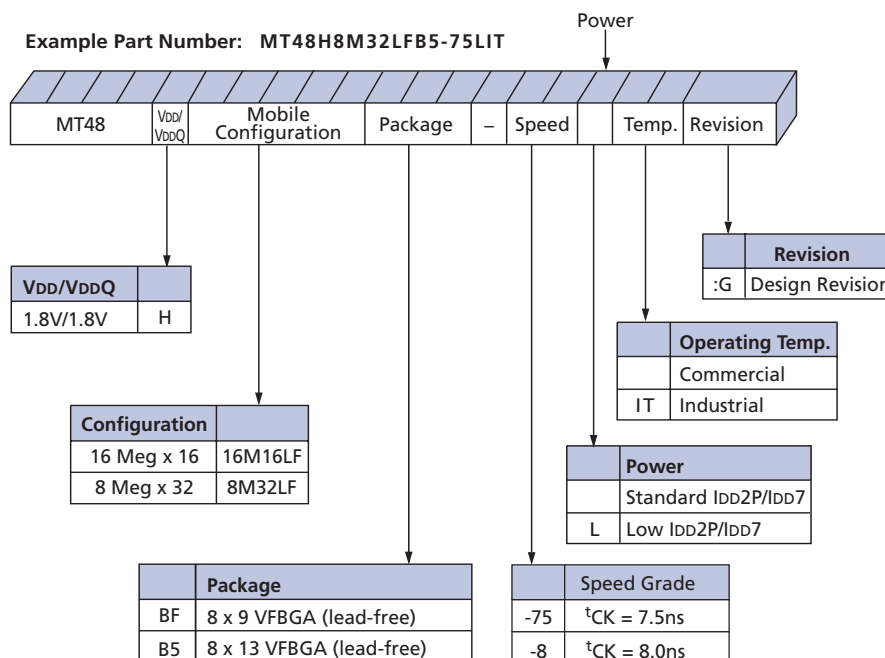
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**Figure 1: 256Mb Mobile SDRAM Part Numbering**



## General Description

The Micron® 256Mb Mobile SDRAM is a high-speed CMOS, dynamic random-access memory containing 268,435,456-bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x16's 67,108,864-bit banks is organized as 8,192 rows by 512 columns by 16 bits. Each of the x32's 67,108,864-bit banks is organized as 4,096 rows by 512 columns by 32 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable read or write burst lengths (BLs) of 1, 2, 4, or 8 page locations with a read burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

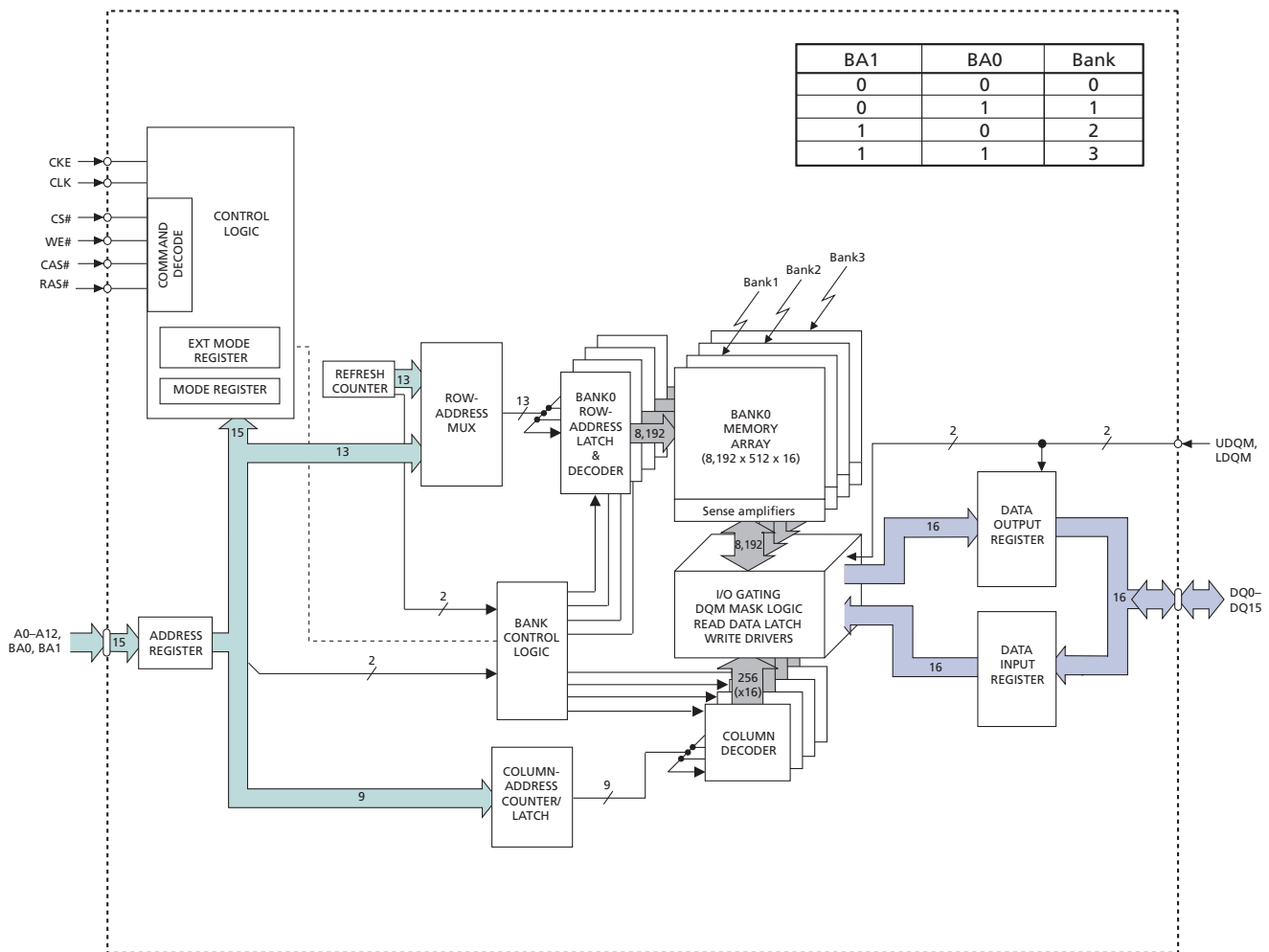
The 256Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. It also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless high-speed, random-access operation.

The 256Mb SDRAM is designed to operate in 1.8V low-power memory systems. An auto refresh mode is provided, along with a power-saving deep power-down mode. All inputs and outputs are LVTTTL-compatible.

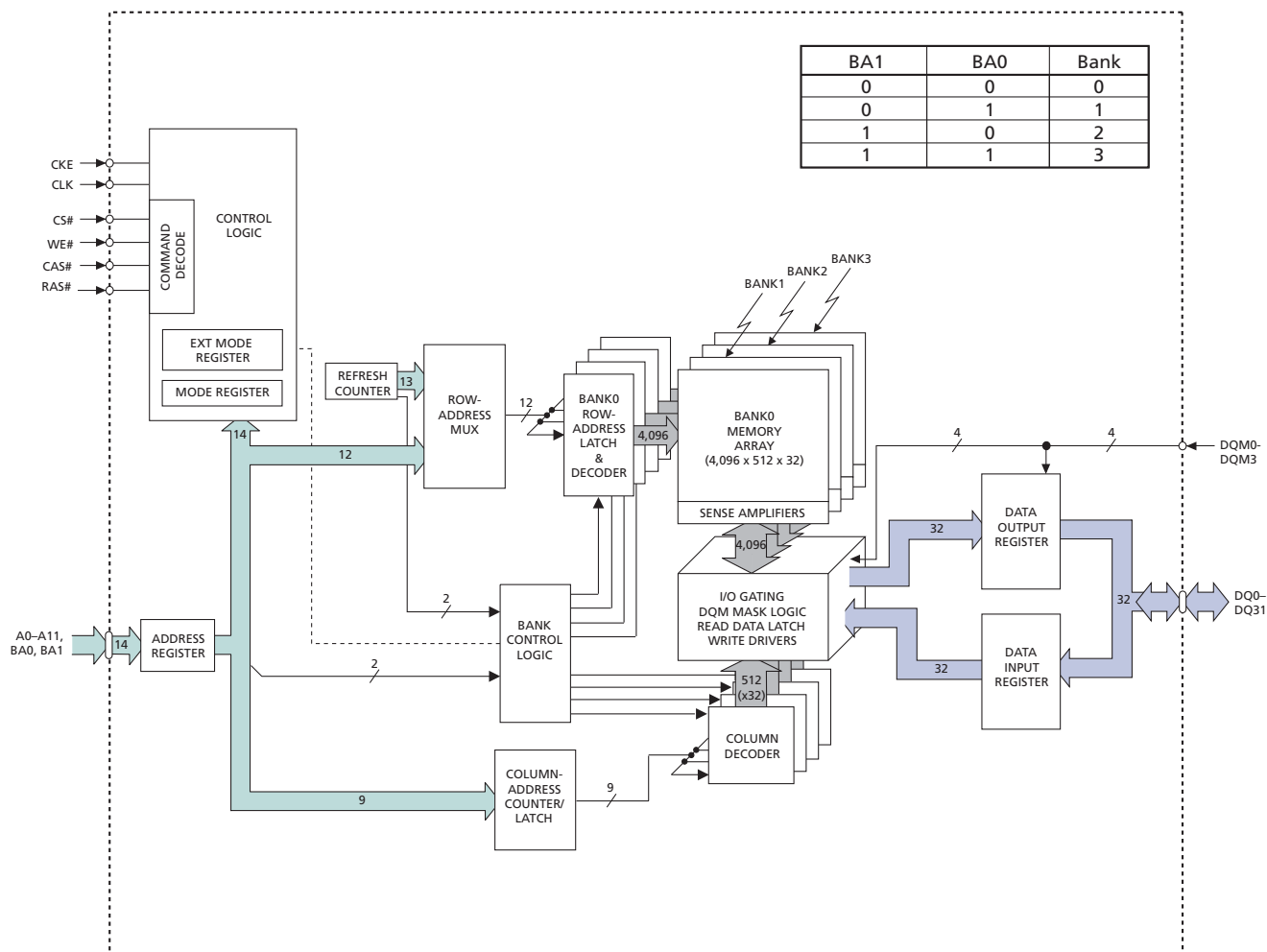
SDRAM offers substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

## Functional Block Diagrams

**Figure 2: 16 Meg x 16 SDRAM**

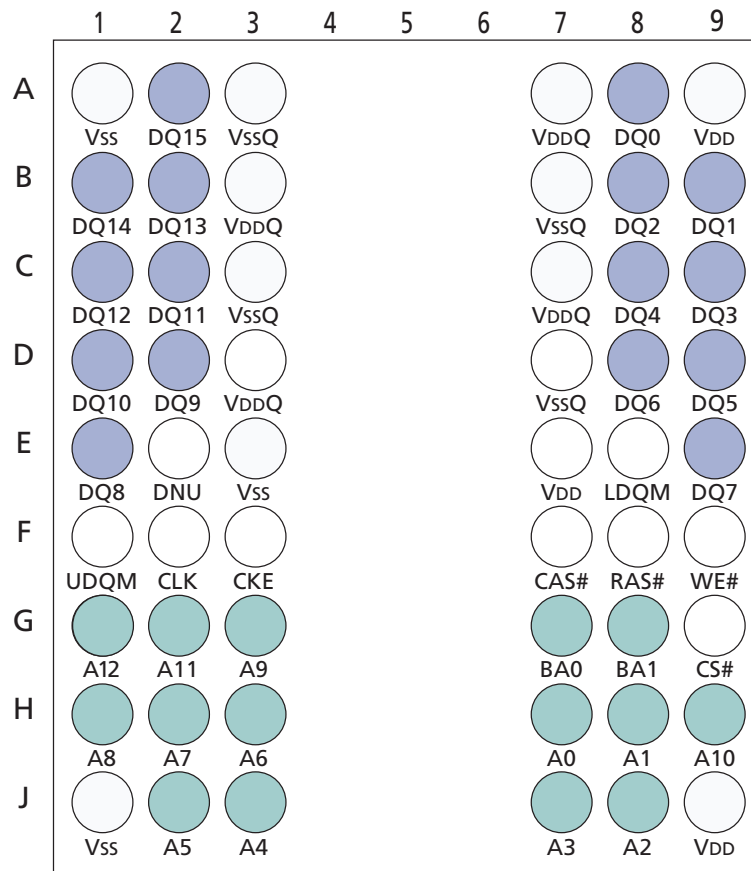


**Figure 3: 8 Meg x 32 SDRAM**





























































































## Ball Assignments

**Figure 4: 54-Ball FBGA (Top View) – 8mm x 9mm**



**Figure 5: 90-Ball VFBGA (Top View) – 8mm x 13mm**

	1	2	3	4	5	6	7	8	9
A	 DQ26	 DQ24	 Vss				 VDD	 DQ23	 DQ21
B	 DQ28	 VDDQ	 VssQ				 VDDQ	 VssQ	 DQ19
C	 VssQ	 DQ27	 DQ25				 DQ22	 DQ20	 VDDQ
D	 VssQ	 DQ29	 DQ30				 DQ17	 DQ18	 VDDQ
E	 VDDQ	 DQ31	 NC				 NC	 DQ16	 VssQ
F	 Vss	 DQM3	 A3				 A2	 DQM2	 VDD
G	 A4	 A5	 A6				 A10	 A0	 A1
H	 A7	 A8	 NC				 NC	 BA1	 A11
J	 CLK	 CKE	 A9				 BA0	 CS#	 RAS#
K	 DQM1	 DNU	 NC				 CAS#	 WE#	 DQM0
L	 VDDQ	 DQ8	 Vss				 VDD	 DQ7	 VssQ
M	 VssQ	 DQ10	 DQ9				 DQ6	 DQ5	 VDDQ
N	 VssQ	 DQ12	 DQ14				 DQ1	 DQ3	 VDDQ
P	 DQ11	 VDDQ	 VssQ				 VDDQ	 VssQ	 DQ4
R	 DQ13	 DQ15	 Vss				 VDD	 DQ0	 DQ2

## Ball Descriptions

**Table 3: VFBGA Ball Descriptions**

54-Ball VFBGA	90-Ball VFBGA	Symbol	Type	Description
F2	J1	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
F3	J2	CKE	Input	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides precharge power-down and SELF REFRESH operation (all banks idle), ACTIVE power-down (row active in any bank), Deep power-down (all banks idle), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power.
G9	J8	CS#	Input	Chip select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
F7, F8, F9	K7, J9, K8	CAS#, RAS#, WE#	Input	Command inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
F1, E8	K9, K1, F8, F2	UDQM LDQM, DQM0– DQM3	Input	Input/output mask: DQM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) during a READ cycle. For the x16, LDQM corresponds to DQ0–DQ7 and UDQM corresponds to DQ8–DQ16. For the x32, DQM0 corresponds to DQ0–DQ7, DQM1 corresponds to DQ8–DQ15, DQM2 corresponds to DQ16–DQ23, and DQM3 corresponds to DQ24–DQ31. DQM0–DQM3 (or LDQM and UDQM if x16) are considered same state when referenced as DQM. DQM loading is designed to match that of DQ balls.
G7, G8	J7, H8	BA0, BA1	Input	Bank address input(s): BA0 and BA1 define to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied. These balls also provide the op-code during a LOAD MODE REGISTER (LMR) command. BA0 and BA1 become “Don’t Care” when registering an ALL BANK PRECHARGE (A10 HIGH).
H7, H8, J8, J7, J3, J2, H3, H2, H1, G3, H9, G2, G1	G8, G9, F7, F3, G1, G2, G3, H1, H2, J3, G7, H9	A0–A12	Input	Address inputs: A0–A12 are sampled during the ACTIVE command (row-address A0–A12) and READ/WRITE command (column-address A0–A8 [x32]; column-address A0–A8 [x16]; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1. The address inputs also provide the op-code during a LMR command.

**Table 3: VFBGA Ball Descriptions (Continued)**

54-Ball VFBGA	90-Ball VFBGA	Symbol	Type	Description
A8, B9, B8, C9, C8, D9, D8, E9, E1, D2, D1, C2, C1, B2, B1, A2	R8, N7, R9, N8, P9, M8, M7, L8, L2, M3, M2, P1, N2, R1, N3, R2, E8, D7, D8, B9, C8, A9, C7, A8, A2, C3, A1, C2, B1, D2, D3, E2	DQ0–DQ31	I/O	Data input/output: Data bus.
A7, B3, C7, D3	B2, B7, C9, D9, E1, L1, M9, N9, P2, P7	VDDQ	Supply	DQ power: Provide isolated power to DQ for improved noise immunity.
A3, B7, C3, D7	B8, B3, C1, D1, E9, L9, M1, N1, P3, P8	VssQ	Supply	DQ ground: Provide isolated ground to DQ for improved noise immunity.
A9, E7, J9	A7, F9, L7, R7	VDD	Supply	Core power supply.
A1, E3, J1	A3, F1, L3, R3	Vss	Supply	Ground.
–	E3, E7, H3, H7, K3	NC	–	Internally not connected: These could be left unconnected, but it is recommended they be connected to Vss.
E2	K2	DNU	Input	E2 is a TEST pin that must be tied to Vss or VssQ in normal operation.

## Functional Description

In general, a 256Mb SDRAM is quad-bank DRAM that operates at 1.8V and includes a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK).

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 and BA1 select the bank, A0–A12 select the row for x16, and A0–A11 select the row for x32). The address bits (A0–A8 for x16 and A0–A8 for x32) registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

## Initialization

SDRAM must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. The initialization for mobile SDRAM is as follows.

1. Simultaneously apply power to VDD and VDDQ.
2. After power supplies have settled, apply a stable clock signal. Stable clock is defined as a signal cycling within timing constraints specified for the clock pin.
3. Wait at least 100µs. During this period NOP or COMMAND INHIBIT commands should be applied. No other command other than NOP or COMMAND INHIBIT is allowed during this period.
4. Perform a PRECHARGE ALL command to place the SDRAM into an all banks idle state.
5. Wait at least  $t_{RP}$  time. During this time NOP or COMMAND INHIBIT commands must be applied.
6. Issue an AUTO REFRESH command.
7. Wait at least  $t_{RFC}$  time, during which only NOP or COMMAND INHIBIT commands are allowed.
8. Issue an Auto Refresh command.
9. Wait at least  $t_{RFC}$  time, during which only NOP or COMMAND INHIBIT commands are allowed.
10. Issue a LOAD MODE REGISTER command with BA1=0, and BA0=0, to program the mode register with desired values.
11. Wait  $t_{MRD}$  time. Only NOP or COMMAND INHIBIT commands may be applied during this time.
12. Issue a LOAD MODE REGISTER command with BA1=1, and BA0=0, to program the extended mode register with desired values.
13. Wait  $t_{MRD}$  time. Only NOP or COMMAND INHIBIT commands may be applied during this time.

The Mobile SDRAM is now initialized and can accept any valid command.

## Register Definition

### Mode Register

There are two MRs in the component: mode register and extended mode register (EMR). The mode register is illustrated in Figure 6 on page 14. The mode register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length (BL), a burst type, a CAS latency (CL), an operating mode and a write burst mode, as shown in Figure 6 on page 14. The mode register is programmed via the LMR command and will retain the stored information until it is programmed again or the device loses power.

M0–M2 mode register bits specify the BL, M3 specifies the type of burst, M4–M6 specify the CL, M7 and M8 specify the operating mode, M9 specifies the write burst mode, and M10 and M11 should be set to zero.

The mode register must be loaded when all banks are idle, and the controller must wait  $t_{MRD}$  before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

### Burst Length (BL)

Read and write accesses to the SDRAM are burst oriented, with the BL being programmable, as shown in Figure 6 on page 14. The BL determines the maximum number of column locations that can be accessed for a given READ or WRITE command. BL = 1, 2, 4, 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

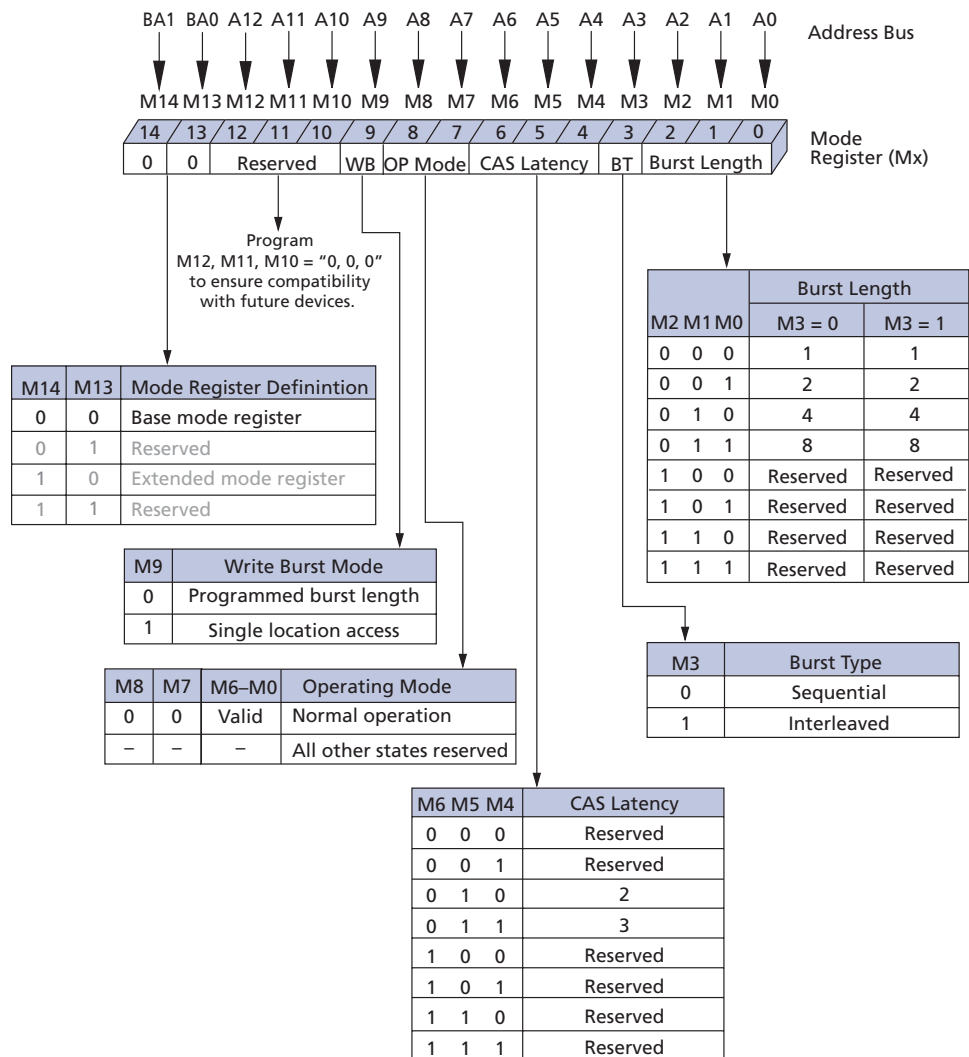
When a READ or WRITE command is issued, a block of columns equal to the BL is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1–A8 when BL = 2, A2–A8 when BL = 4, and A3–A8 when BL = 8. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block.

### Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the BL, the burst type, and the starting column address, as shown in Table 4 on page 15.

**Figure 6: Mode Register Definition**



**Table 4: Burst Definition Table**

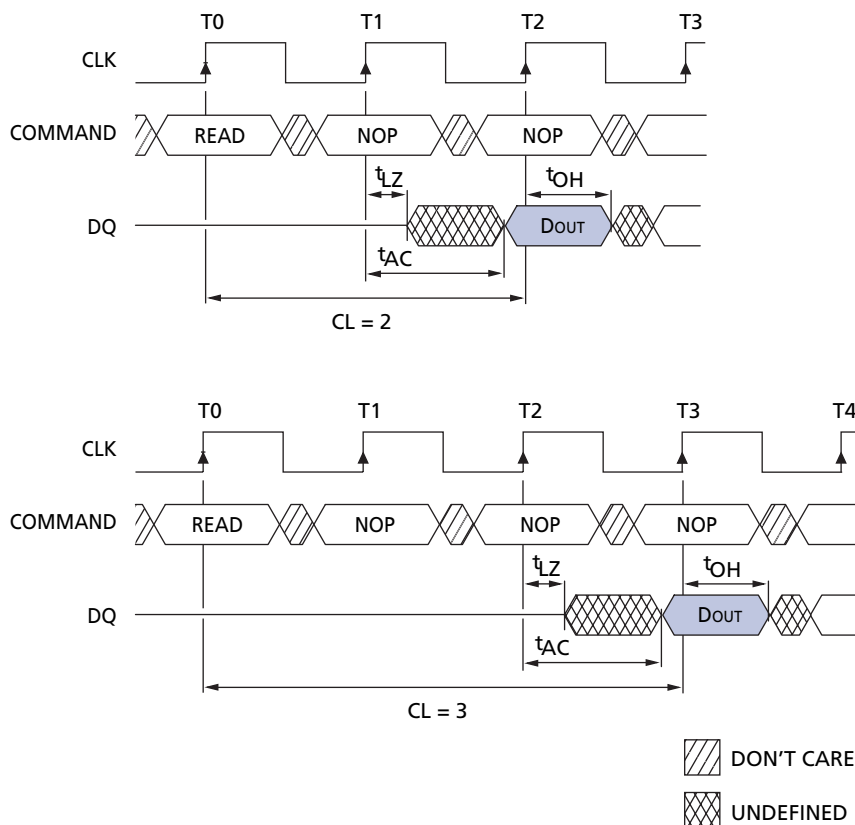
Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2			A0		
			0	0-1	0-1
			1	1-0	1-0
4		A1	A0		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

### CAS Latency (CL)

The CL is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks.

If a READ command is registered at clock edge  $n$ , and the latency is  $m$  clocks, the data will be available by clock edge  $n + m$ . The DQs will start driving as a result of the clock edge one cycle earlier ( $n + m - 1$ ), and provided that the relevant access times are met, the data will be valid by clock edge  $n + m$ . For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the DQs will start driving after T1 and the data will be valid by T2, as shown in Figure 7 on page 16.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

**Figure 7: CAS Latency**


## Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

## Write Burst Mode

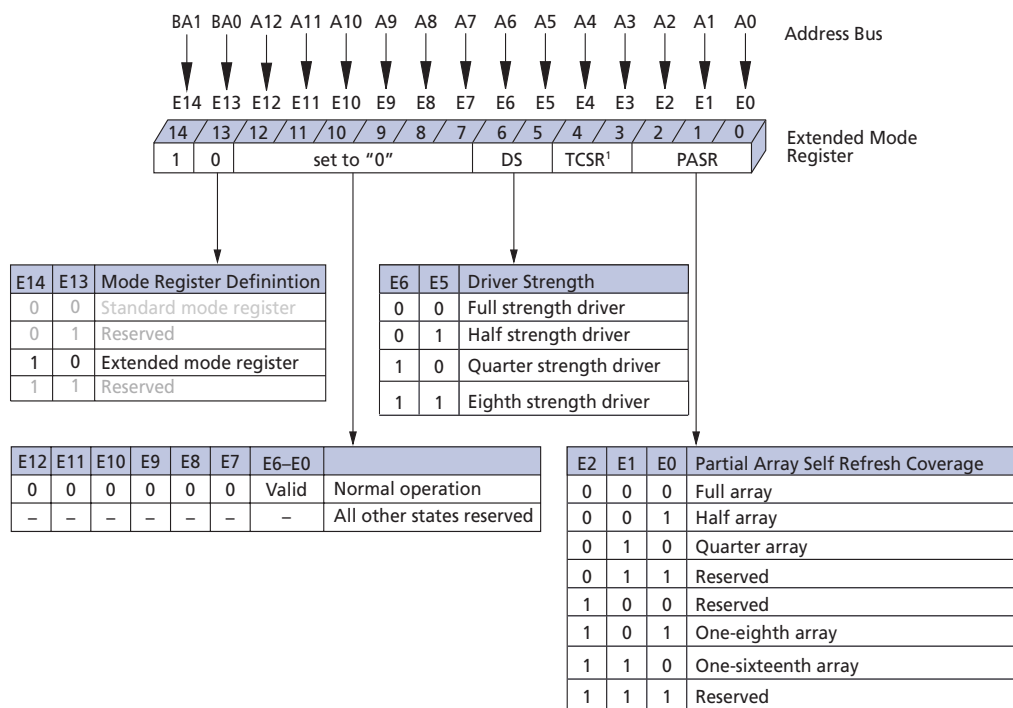
When M9 = 0, the BL programmed via M0–M2 applies to both READ and WRITE bursts; when M9 = 1, the programmed BL applies to READ bursts, but write accesses are single-location accesses.

## Extended Mode Register (EMR)

The low-power EMR controls the functions beyond those controlled by the MR. These additional functions are special features of the mobile device. They include temperature-compensated self refresh (TCSR) control, partial-array self refresh (PASR), and output drive strength.

The low-power EMR is programmed via the MODE REGISTER SET command and retains the stored information until it is programmed again or the device loses power.

**Figure 8: EMR Definition**



Notes: 1. On-die temperature sensor is used in place of TCSR. Setting these bits will have no effect.

The EMR must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements results in unspecified operation. Once the values are entered, the EMR settings will be retained even after exiting deep power-down mode.

## Temperature-Compensated Self Refresh (TCSR)

On this version of the Mobile SDR SDRAM, a temperature sensor is implemented for automatic control of the self refresh oscillator on the device. Therefore, it is recommended not to program or use the temperature-compensated self refresh control bits in the extended mode register.

Programming of the TCSR bits has no effect on the device. The self refresh oscillator will continue refresh at the factory programmed optimal rate for the device temperature.

**Partial-Array Self Refresh (PASR)**

For further power savings during self refresh, the partial-array self refresh (PASR) feature allows the controller to select the amount of memory that will be refreshed during self refresh. The following refresh options are available.

1. All banks (banks 0, 1, 2, and 3).
2. Two banks (banks 0 and 1; BA1=0).
3. One bank (bank 0; BA1 = BA0 = 0).
4. Half bank (bank 0; BA1 = BA0 = row address MSB = 0).
5. Quarter bank (bank 0; BA1 = BA0; row address MSB = row address MSB - 1 = 0).

WRITE and READ commands occur to any bank selected during standard operation, but only the selected banks in PASR will be refreshed during self refresh. It is important to note that data in banks 2 and 3 will be lost when the two-bank option is used.

**Driver Strength**

Bits E5 and E6 of the EMR can be used to select the driver strength of the DQ outputs. This value should be set according to the application's requirements.

## Commands

Table 5 provides a quick reference of available commands. This is followed by a written description of each command. Three additional Truth Tables appear following “Operations” on page 23. These tables provide current state/next state information.

**Table 5: Truth Table – Commands and DQM Operation**

Notes 1 and 2 apply to all commands

Name (Function)	CS#	RAS#	CAS#	WE#	DQM	ADDR	DQs	Notes
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	4
NO OPERATION (NOP)	L	H	H	H	X	X	X	4
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	5
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H	Bank/Col	X	6
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H	Bank/Col	Valid	6
BURST TERMINATE or deep power-down (Enter deep power-down mode)	L	H	H	L	X	X	X	3, 7, 8
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	9
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	10, 11
LOAD MODE REGISTER	L	L	L	L	X	Op-Code	X	12
Write enable/output enable	X	X	X	X	L	X	Active	
Write inhibit/output High-Z	X	X	X	X	H	X	High-Z	

- Notes:
1. CKE is HIGH for all commands shown except SELF REFRESH and deep power-down.
  2. All states and sequences not shown are reserved and/or illegal.
  3. The purpose of the BURST TERMINATE command is to stop a data burst, thus the command could coincide with data on the bus. However, the DQs column reads a don't care state to illustrate that the BURST TERMINATE command can occur when there is no data present.
  4. DESELECT and NOP are functionally interchangeable.
  5. BA0–BA1 provide bank address and A0–A12 provide row address.
  6. BA0–BA1 provide bank address; A0–A9 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), and A10 LOW disables the auto precharge feature.
  7. Applies only to read bursts with auto precharge disabled; this command is undefined (and should not be used) for READ bursts with auto precharge enabled and for WRITE bursts.
  8. This command is a BURST TERMINATE if CKE is HIGH, deep power-down if CKE is LOW.
  9. A10 LOW: BA0–BA1 determine which bank is precharged. A10 HIGH: all banks are precharged and BA0–BA1 are “Don't Care.”
  10. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
  11. Internal refresh counter controls row addressing; all inputs and I/Os are “Don't Care” except for CKE.
  12. BA0–BA1 select either the standard mode register or the extended mode register (BA0 = 0, BA1 = 0 select the standard mode register; BA0 = 0, BA1 = 1 select extended mode register; other combinations of BA0–BA1 are reserved.) A0–A12 provide the op-code to be written to the selected mode register.

## COMMAND INHIBIT

The COMMAND INHIBIT function prevents new commands from being executed by the SDRAM, regardless of whether the CLK signal is enabled. The SDRAM is effectively deselected. Operations already in progress are not affected.

**NO OPERATION (NOP)**

The NO OPERATION (NOP) command is used to perform a NOP to an SDRAM which is selected (CS# is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

**LOAD MODE REGISTER (LMR)**

The MR is loaded via inputs A0–A12, BA0, and BA1. (See “Mode Register” on page 13.) The LMR and LOAD EXTENDED MODE REGISTER (LEMR) commands can only be issued when all banks are idle, and a subsequent executable command cannot be issued until  $t_{MRD}$  is met.

**ACTIVE**

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

**READ**

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the read burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Read data appears on the DQs subject to the logic level on the DQM inputs two clocks earlier. If a given DQM signal was registered HIGH, the corresponding DQs will be High-Z two clocks later; if the DQM signal was registered LOW, the DQs will provide valid data.

**WRITE**

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provides the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the write burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered LOW, the corresponding data will be written to memory; if the DQM signal is registered HIGH, the corresponding data inputs will be ignored, and a write will not be executed to that byte/column location.

**PRECHARGE**

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time ( $t_{RP}$ ) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

## **BURST TERMINATE**

The BURST TERMINATE command is used to truncate fixed-length bursts. The most recently registered READ or WRITE command prior to the BURST TERMINATE command will be truncated, as shown in “Operations” on page 23.

## **AUTO REFRESH**

AUTO REFRESH is used during normal operation of the SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) refresh in conventional DRAM. This command is non persistent, so it must be issued each time a refresh is required. All active banks must be PRECHARGED prior to issuing an AUTO REFRESH command. The AUTO REFRESH command should not be issued until the minimum  $t_{RP}$  has been met after the PRECHARGE command, as shown in “Operations” on page 23.

The addressing is generated by the internal refresh controller. This makes the address bits “Don’t Care” during an AUTO REFRESH command. The 256Mb SDRAM requires 8,192 AUTO REFRESH cycles every 64ms ( $t_{REF}$ ). Providing a distributed AUTO REFRESH command every 7.8125 $\mu$ s will meet the refresh requirement and ensure that each row is refreshed. Alternatively, 8,192 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate ( $t_{RFC}$ ), once every 64ms.

## **SELF REFRESH**

The SELF REFRESH command can be used to retain data in the SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command, except CKE is disabled (LOW). Once the SELF REFRESH command is registered, all the inputs to the SDRAM become “Don’t Care” with the exception of CKE, which must remain LOW.

Once self refresh mode is engaged, the SDRAM provides its own internal clocking, causing it to perform its own auto refresh cycles. The SDRAM must remain in self refresh mode for a minimum period equal to  $t_{RAS}$  and may remain in self refresh mode for an indefinite period beyond that.

The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable (stable clock is defined as a signal cycling within timing constraints specified for the clock ball) prior to CKE going back HIGH. Once CKE is HIGH, the SDRAM must have NOP commands issued (a minimum of two clocks) for  $t_{XSR}$  because time is required for the completion of any internal refresh in progress.

Upon exiting the self refresh mode, AUTO REFRESH commands must be issued every 7.8125 $\mu$ s or less as both SELF REFRESH and AUTO REFRESH utilize the row refresh counter.

## **Auto Precharge**

Auto precharge is a feature which performs the same individual-bank precharge function described above, without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. Auto precharge is non persistent in that it is either enabled or disabled for each individual READ or WRITE command.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time ( $t_{RP}$ ) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in “Operations” on page 23.

### **Deep Power-Down**

Deep power-down is an operating mode used to achieve maximum power reduction by eliminating the power to the memory array. Data will not be retained once the device enters deep power-down mode.

## Operations

### Bank/Row Activation

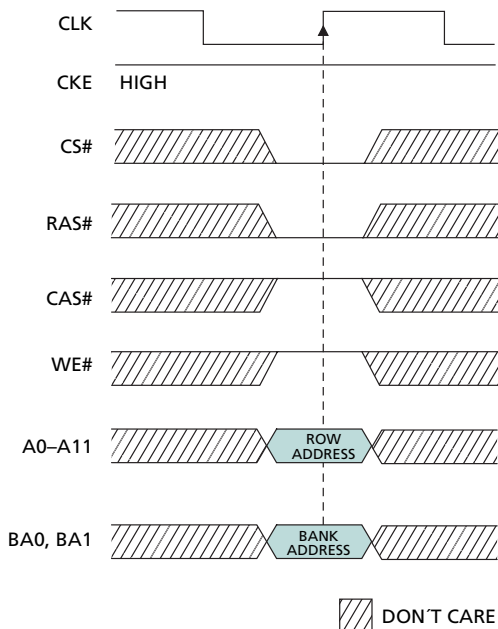
Before any READ or WRITE commands can be issued to a bank within the SDRAM, a row in that bank must be “opened.” This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated (see Figure 9).

After opening a row (issuing an ACTIVE command), a READ or WRITE command may be issued to that row, subject to the  $t_{RCD}$  specification.  $t_{RCD}(\text{MIN})$  should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a  $t_{RCD}$  specification of 20ns with a 125 MHz clock (8ns period) results in 2.5 clocks, rounded to 3. This is reflected in Figure 10 on page 24, which covers any case where  $2 < t_{RCD}(\text{MIN})/t_{CK} \leq 3$ . (The same procedure is used to convert other specification limits from time units to clock cycles.)

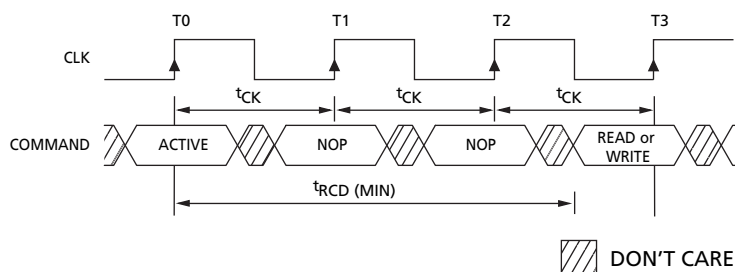
A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been “closed” (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by  $t_{RC}$ .

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by  $t_{RRD}$ .

**Figure 9: Activating a Specific Row in a Specific Bank**



**Figure 10: Example: Meeting  $t_{RCD} (MIN)$  When  $2 < t_{RCD} (MIN)/t_{CK} \leq 3$**



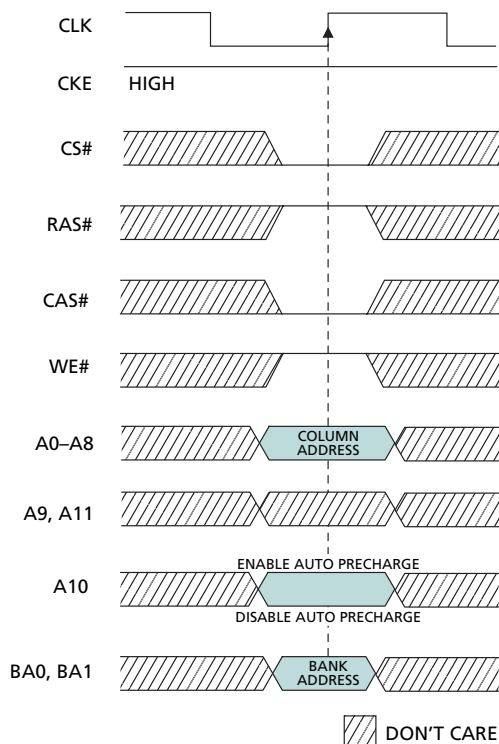
## READs

READ bursts are initiated with a READ command, as shown in Figure 11.

The starting column and bank addresses are provided with the READ command, and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic READ commands used in the following illustrations, auto precharge is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CL after the READ command. Each subsequent data-out element will be valid by the next positive clock edge. Figure 7 on page 16 shows general timing for each possible CL setting.

**Figure 11: READ Command**

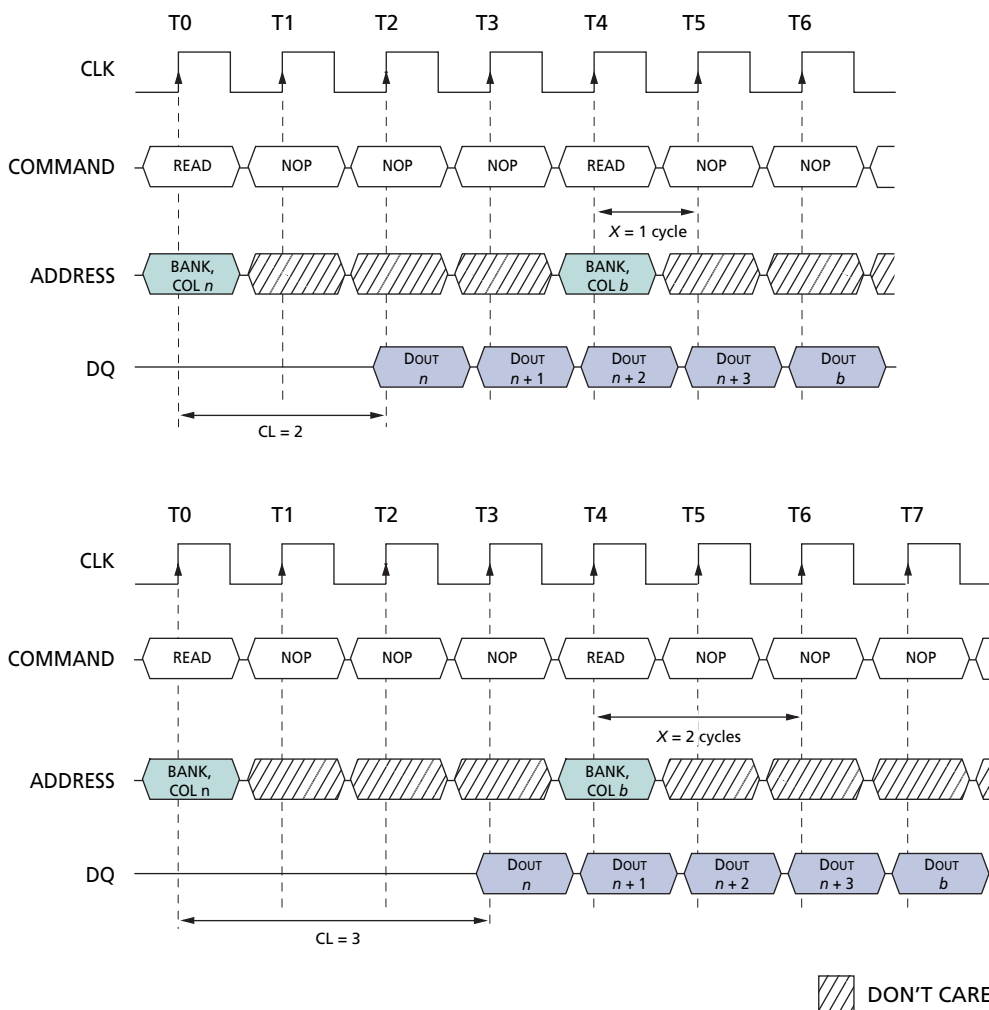


Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z.

Data from any READ burst may be truncated with a subsequent READ command, and data from a fixed-length READ burst may be immediately followed by data from a READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst that is being truncated. The new READ command should be issued  $x$  cycles before the clock edge at which the last desired data element is valid, where  $x = CL - 1$ .

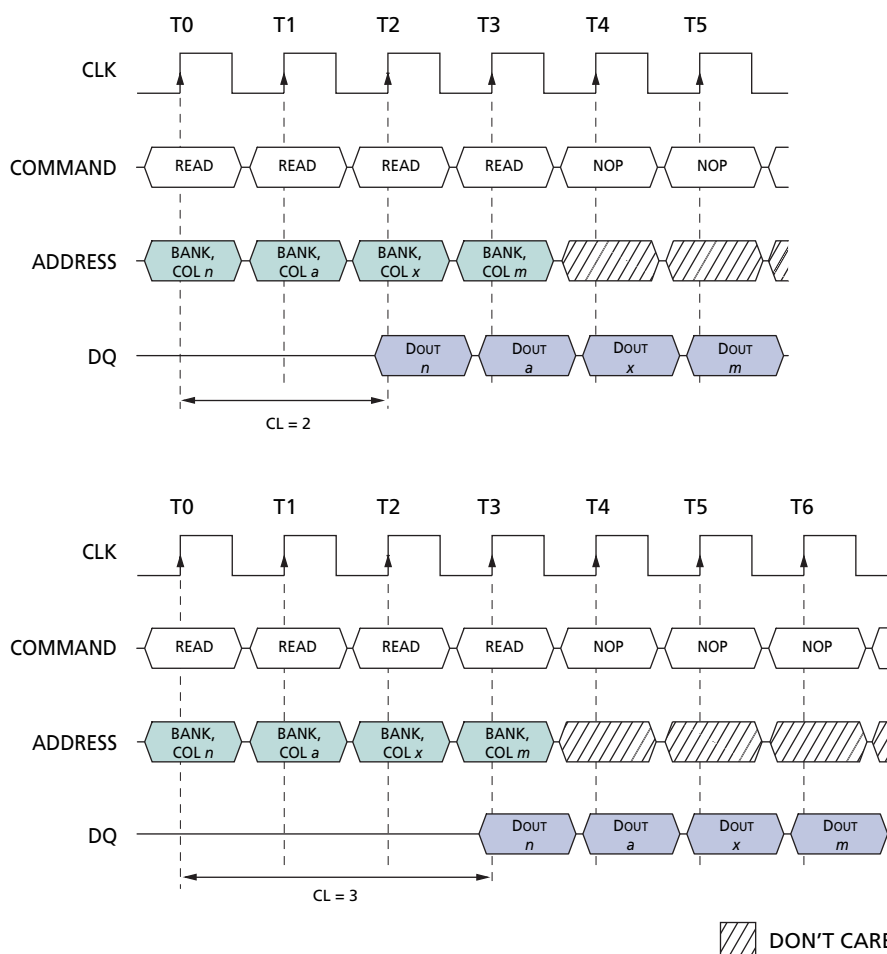
Figure 7 on page 16 shows for CL of two and three; data element  $n + 3$  is either the last of a burst of four or the last desired data element of a longer burst. The 256Mb SDRAM uses a pipelined architecture. A READ command can be initiated on any clock cycle following a previous READ command. Full-speed random read accesses can be performed to the same bank, as shown in Figure 12 on page 25, or each subsequent READ may be performed to a different bank.

**Figure 12: Consecutive READ Bursts**



**Note:** Each READ command may be to either bank. DQM is LOW.

**Figure 13: Random READ Accesses**



**Note:** Each READ command may be to either bank. DQM is LOW.

Data from any READ burst may be truncated with a subsequent WRITE command, and data from a fixed-length READ burst may be immediately followed by data from a WRITE command (subject to bus turnaround limitations). The WRITE burst may be initiated on the clock edge immediately following the last (or last desired) data element from the READ burst, provided that I/O contention can be avoided. In a given system design, there may be a possibility that the device driving the input data will go Low-Z before the SDRAM DQs go High-Z. In this case, at least a single-cycle delay should occur between the last read data and the WRITE command.

The DQM input is used to avoid I/O contention, as shown in Figure 14 on page 27 and Figure 15 on page 28. The DQM signal must be asserted (HIGH) at least two clocks prior to the WRITE command (DQM latency is two clocks for output buffers) to suppress data-out from the READ. Once the WRITE command is registered, the DQs will go High-Z (or remain High-Z), regardless of the state of the DQM signal, provided the DQM was active on the clock just prior to the WRITE command that truncated the READ command. If

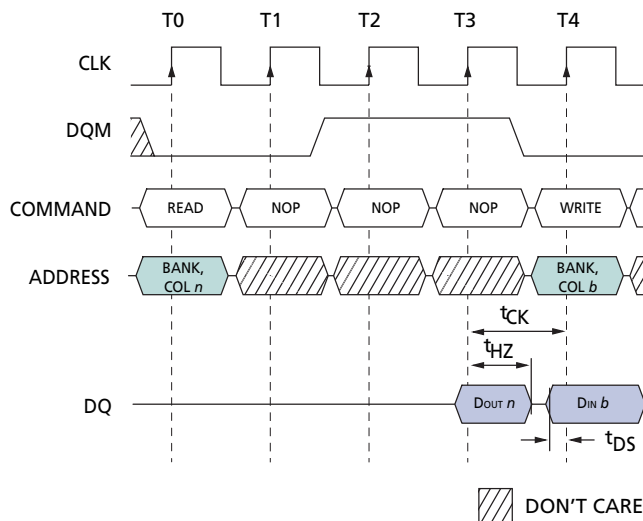
not, the second WRITE will be an invalid WRITE. For example, if DQM was LOW during T4 (as in Figure 15 on page 28) then the WRITES at T5 and T7 would be valid, while the WRITE at T6 would be invalid.

The DQM signal must be de-asserted prior to the WRITE command (DQM latency is zero clocks for input buffers) to ensure that the written data is not masked. Figure 12 on page 25 shows the case where the clock frequency allows for bus contention to be avoided without adding a NOP cycle, and Figure 13 on page 26 shows the case where the additional NOP is needed.

A fixed-length READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that auto precharge was not activated). The PRECHARGE command should be issued  $x$  cycles before the clock edge at which the last desired data element is valid, where  $x = CL - 1$ . This is shown in Figure 16 on page 28 for each possible CL; data element  $n + 3$  is either the last of a burst of four or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until  $t_{RP}$  is met. Note that part of the row precharge time is hidden during the access of the last data element(s).

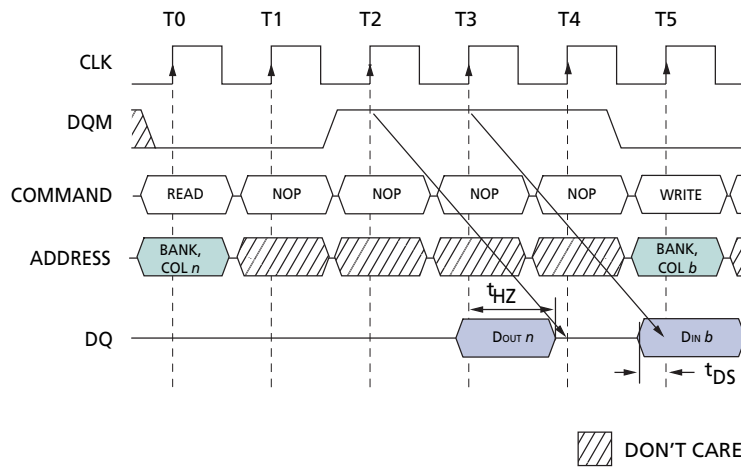
In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the PRECHARGE command is that it can be used to truncate fixed-length page bursts.

**Figure 14: READ-to-WRITE**



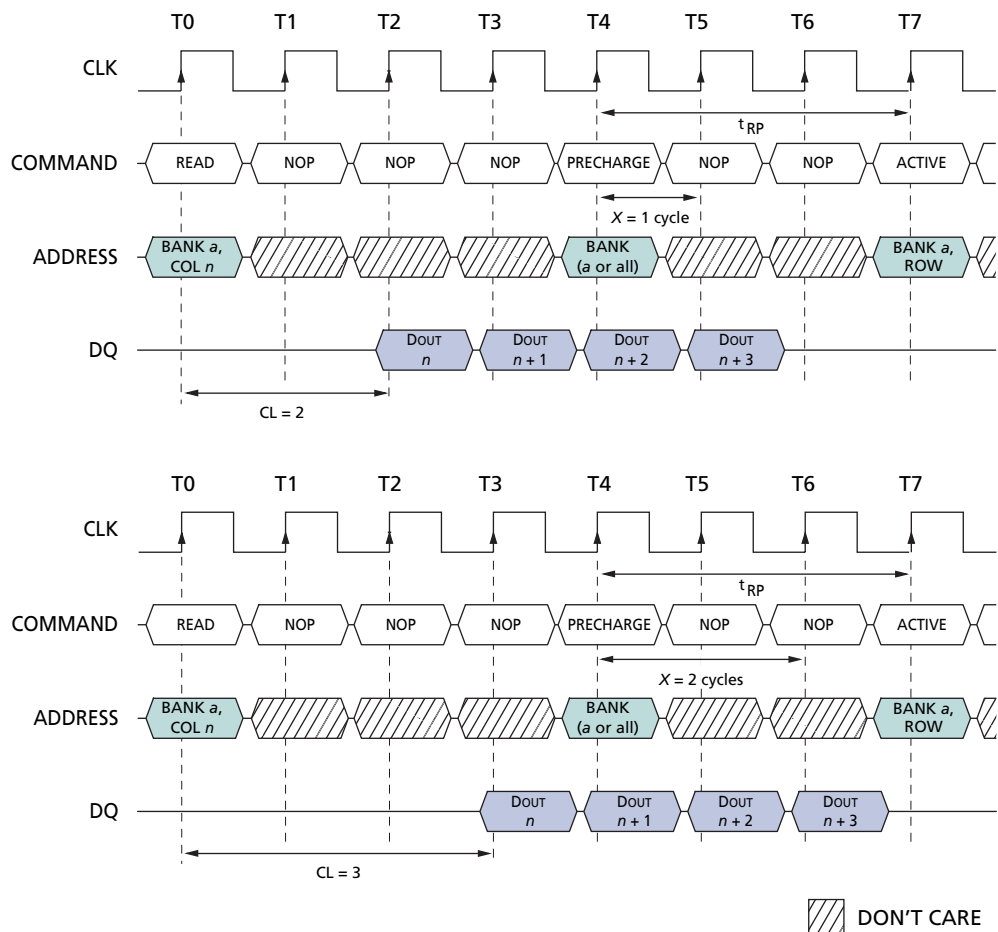
**Note:** CL = 3. The READ command may be to any bank, and the WRITE command may be to any bank. If a burst of one is used, then DQM is not required.

**Figure 15: READ-to-WRITE with Extra Clock Cycle**



Note: CL = 3. The READ command may be to any bank, and the WRITE command may be to any bank.

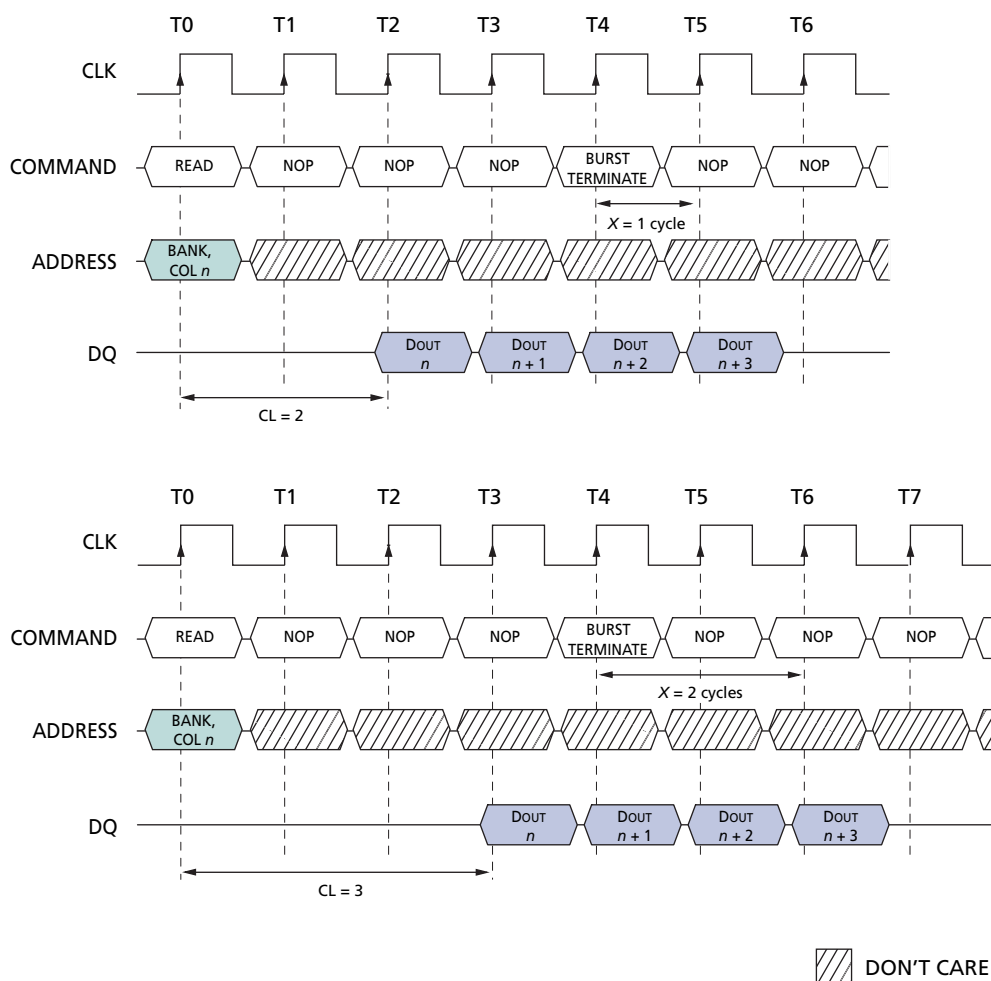
**Figure 16: READ-to-PRECHARGE**



Note: DQM is LOW.

Fixed-length READ bursts may be truncated with a BURST TERMINATE command, provided that auto precharge was not activated. The BURST TERMINATE command should be issued  $x$  cycles before the clock edge at which the last desired data element is valid, where  $x = CL - 1$ . This is shown in Figure 17 for each possible CL; data element  $n + 3$  is the last desired data element of a longer burst.

**Figure 17: Terminating a READ Burst**



Note: DQM is LOW.

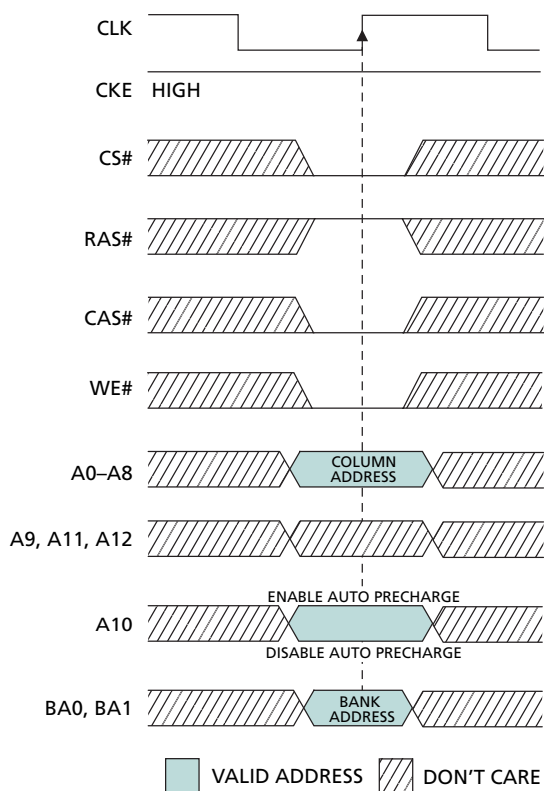
## WRITES

WRITE bursts are initiated with a WRITE command, as shown in Figure 18 on page 30.

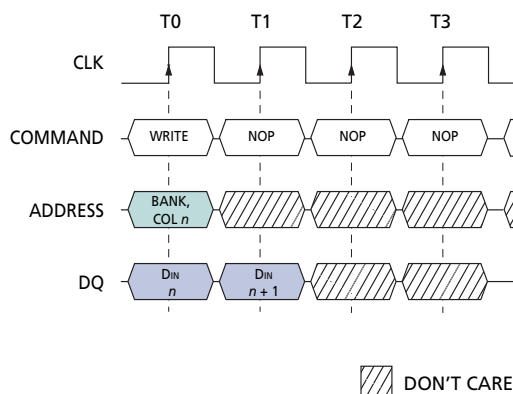
The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, auto precharge is disabled.

During WRITE bursts, the first valid data-in element will be registered coincident with the WRITE command. Subsequent data elements will be registered on each successive positive clock edge. Upon completion of a fixed-length burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data will be ignored (see Figure 19).

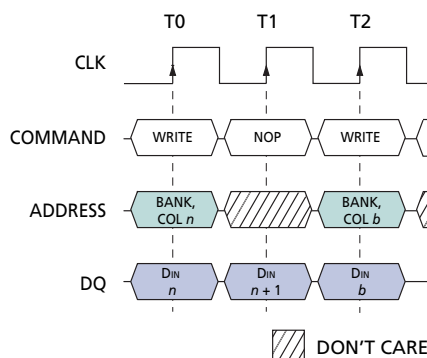
**Figure 18: WRITE Command**



Data for any WRITE burst may be truncated with a subsequent WRITE command, and data for a fixed-length WRITE burst may be immediately followed by data for a WRITE command. The new WRITE command can be issued on any clock following the previous WRITE command, and the data provided coincident with the new command applies to the new command. An example is shown in Figure 20 on page 31. Data  $n + 1$  is either the last of a burst of two or the last desired of a longer burst. The 256Mb SDRAM uses a pipelined architecture. A WRITE command can be initiated on any clock cycle following a previous WRITE command. Full-speed random write accesses within a page can be performed to the same bank, as shown in Figure 19 on page 31, or each subsequent WRITE may be performed to a different bank.

**Figure 19: WRITE Burst**


Note: BL = 2. DQM is LOW.

**Figure 20: WRITE-to-WRITE**


Note: BL = 2. DQM is LOW. Each WRITE command may be to any bank.

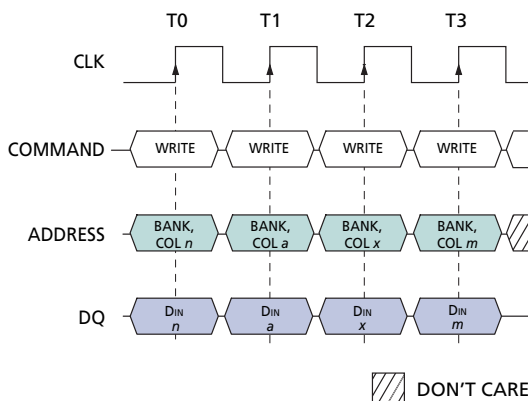
Data for any WRITE burst may be truncated with a subsequent READ command, and data for a fixed-length WRITE burst may be immediately followed by a READ command. Once the READ command is registered, the data inputs will be ignored, and WRITES will not be executed. An example is shown in Figure 21 on page 32. Data  $n + 1$  is either the last of a burst of two or the last desired of a longer burst.

Data for a fixed-length WRITE burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that auto precharge was not activated). The PRECHARGE command should be issued  $t_{WR}$  after the clock edge at which the last desired input data element is registered. The auto precharge mode requires a  $t_{WR}$  of at least one clock plus time (see note 24 on page 52), regardless of frequency.

In addition, when truncating a WRITE burst, the DQM signal must be used to mask input data for the clock edge prior to, and the clock edge coincident with, the PRECHARGE command. An example is shown in Figure 21 on page 32. Data  $n + 1$  is either the last of a burst of two or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until  $t_{RP}$  is met.

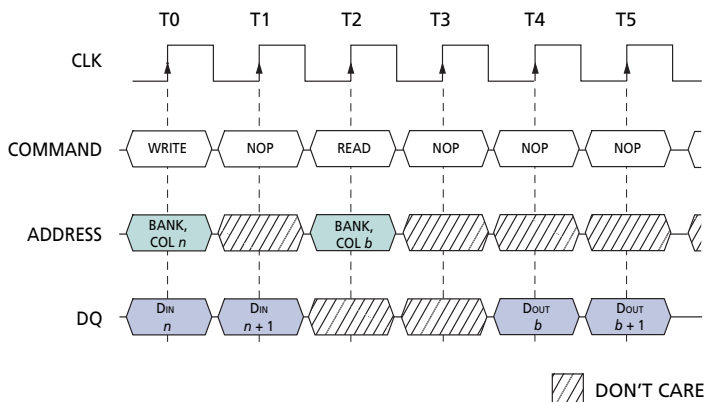
In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the PRECHARGE command is that it can be used to truncate fixed-length bursts.

**Figure 21: Random WRITE Cycles**



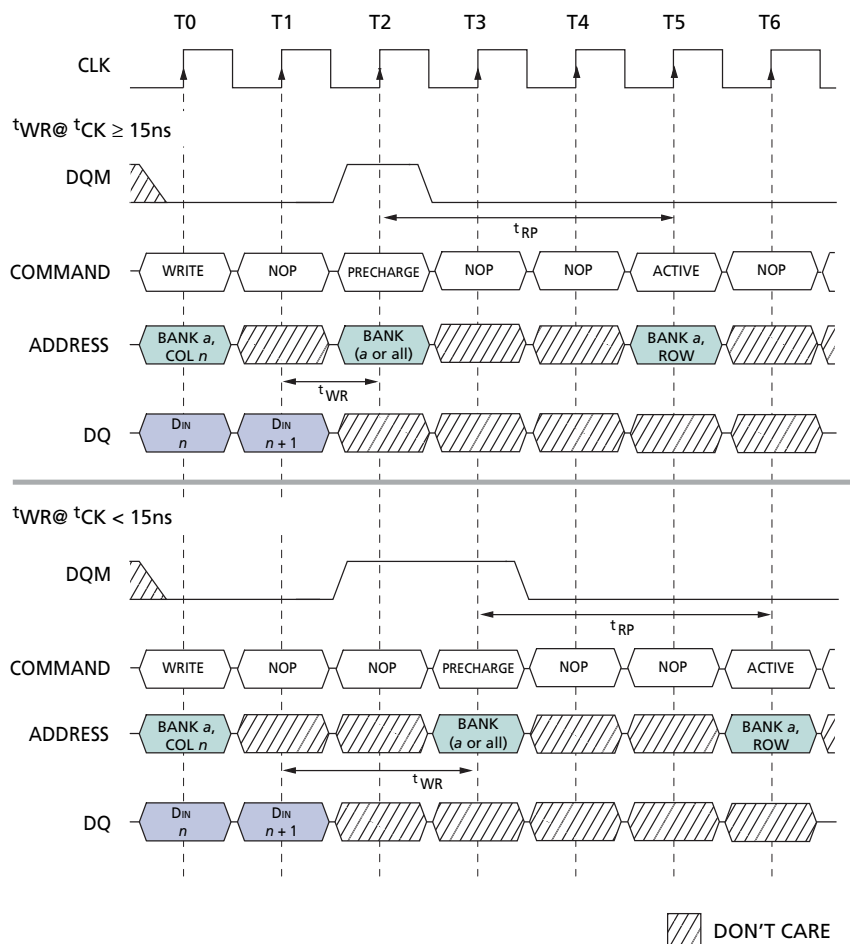
Note: Each WRITE command may be to any bank. DQM is LOW.

**Figure 22: WRITE-to-READ**



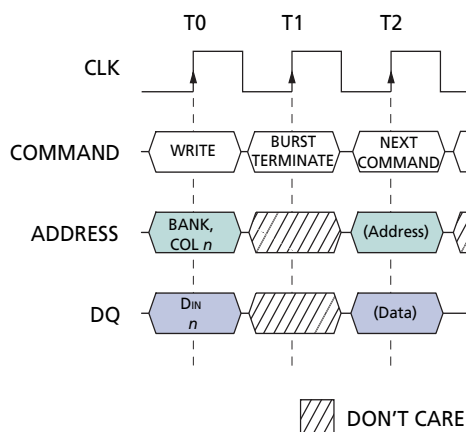
Note: BL = 2. The WRITE command may be to any bank, and the READ command may be to any bank. DQM is LOW. CL = 2 for illustration.

**Figure 23: WRITE-to-PRECHARGE**



Note: DQM could remain LOW in this example if the WRITE burst is a fixed length of two.

**Figure 24: Terminating a WRITE Burst**



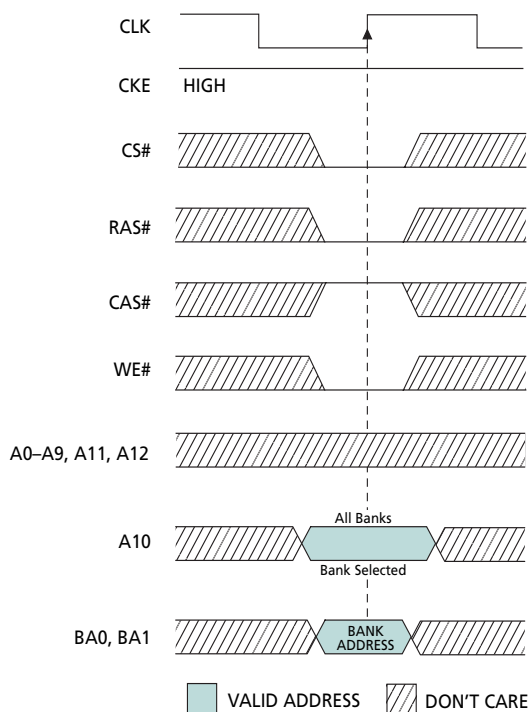
Note: DQMs are LOW.

Fixed-length or WRITE bursts can be truncated with the BURST TERMINATE command. When truncating a WRITE burst, the input data applied coincident with the BURST TERMINATE command will be ignored. The last data written (provided that DQM is LOW at that time) will be the input data applied one clock previous to the BURST TERMINATE command. This is shown in Figure 22 on page 32, where data  $n$  is the last desired data element of a longer burst.

## PRECHARGE

The PRECHARGE command (see Figure 25) is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time ( $t_{RP}$ ) after the precharge command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

**Figure 25: PRECHARGE Command**

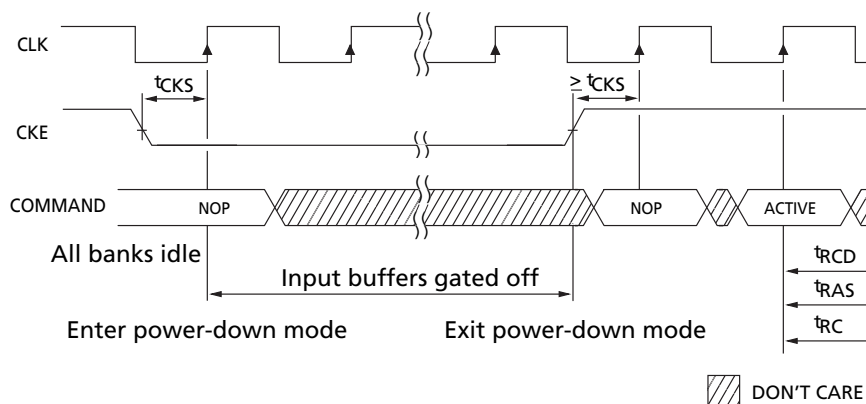


## Power-Down

Power-down occurs if CKE is registered LOW coincident with a NOP or COMMAND INHIBIT when no accesses are in progress. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CKE, for maximum power savings while in standby. The device may not remain in the power-down state longer than the refresh period (64ms) since no REFRESH operations are performed in this mode.

The power-down state is exited by registering a NOP or COMMAND INHIBIT and CKE HIGH at the desired clock edge (meeting  $t_{CKS}$ ). See Figure 24.

**Figure 26: Power-Down**



## Deep Power-Down

Deep power-down mode is a maximum power savings feature achieved by shutting off the power to the entire memory array of the device. Data in the memory array will not be retained once deep power-down mode is executed. Deep power-down mode is entered by having all banks idle then CS# and WE# held LOW with RAS# and CAS# HIGH at the rising edge of the clock, while CKE is LOW. CKE must be held LOW during deep power-down.

To exit deep power-down mode, CKE must be asserted HIGH. Upon exit of Deep Power-Down mode, at least 200 $\mu$ s of valid clocks with either NOP or COMMAND INHIBIT commands are applied to the command bus, followed by a full Mobile SDRAM initialization sequence, is required.

## Clock Suspend

The clock suspend mode occurs when a column access/burst is in progress and CKE is registered LOW. In the clock suspend mode, the internal clock is deactivated, "freezing" the synchronous logic.

For each positive clock edge on which CKE is sampled LOW, the next internal positive clock edge is suspended. Any command or data present on the input balls at the time of a suspended internal clock edge is ignored; any data present on the DQ balls remains driven; and burst counters are not incremented, as long as the clock is suspended. (See examples in Figure 27 and Figure 28 on page 37.)

Clock suspend mode is exited by registering CKE HIGH; the internal clock and related operation will resume on the subsequent positive clock edge.

## Burst Read/Single Write

The burst read/single write mode is entered by programming the write burst mode bit (M9) in the MR to a logic 1. In this mode, all WRITE commands result in the access of a single column location (burst of one), regardless of the programmed BL. READ commands access columns according to the programmed BL and sequence, just as in the normal mode of operation (M9 = 0).

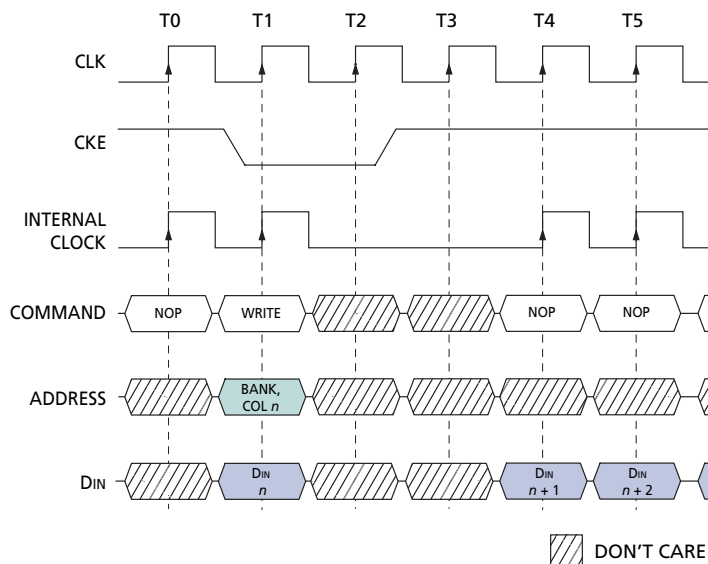
## Concurrent Auto Precharge

An access command (READ or WRITE) to a second bank while an access command with auto precharge enabled on a first bank is executing is not allowed by SDRAM, unless the SDRAM supports concurrent auto precharge. Micron SDRAM support concurrent auto precharge. Four cases where concurrent auto precharge occurs are defined in the “READ with Auto Precharge” and “WRITE with Auto Precharge” sections.

## READ with Auto Precharge

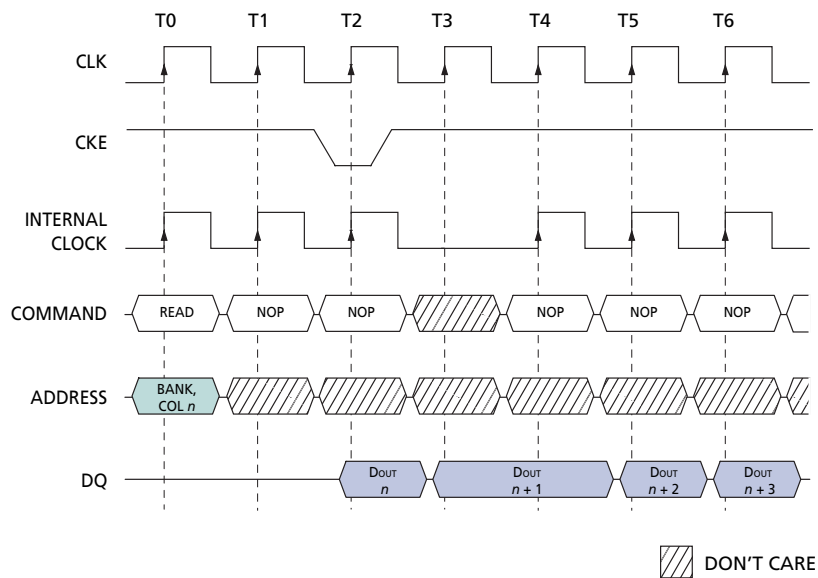
1. Interrupted by a READ (with or without auto precharge): A READ to bank  $m$  will interrupt a READ on bank  $n$ , CL later. The precharge to bank  $n$  will begin when the READ to bank  $m$  is registered (see Figure 29 on page 37).
2. Interrupted by a WRITE (with or without auto precharge): A WRITE to bank  $m$  will interrupt a READ on bank  $n$  when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The precharge to bank  $n$  will begin when the WRITE to bank  $m$  is registered (see Figure 30 on page 38).

**Figure 27: Clock Suspend During WRITE Burst**



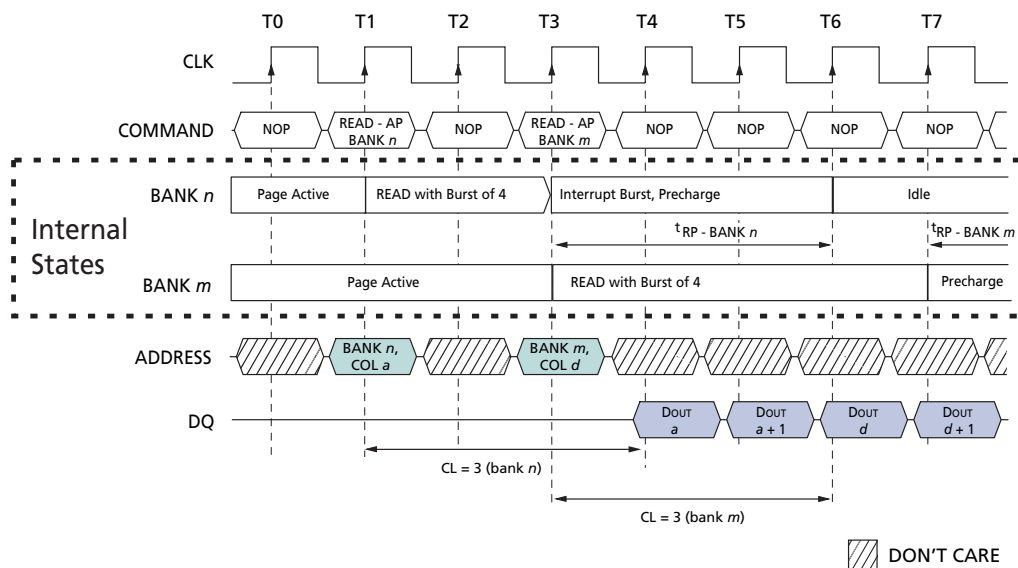
Note: For this example, BL = 4 or greater, and DM is LOW.

**Figure 28: Clock Suspend During READ Burst**



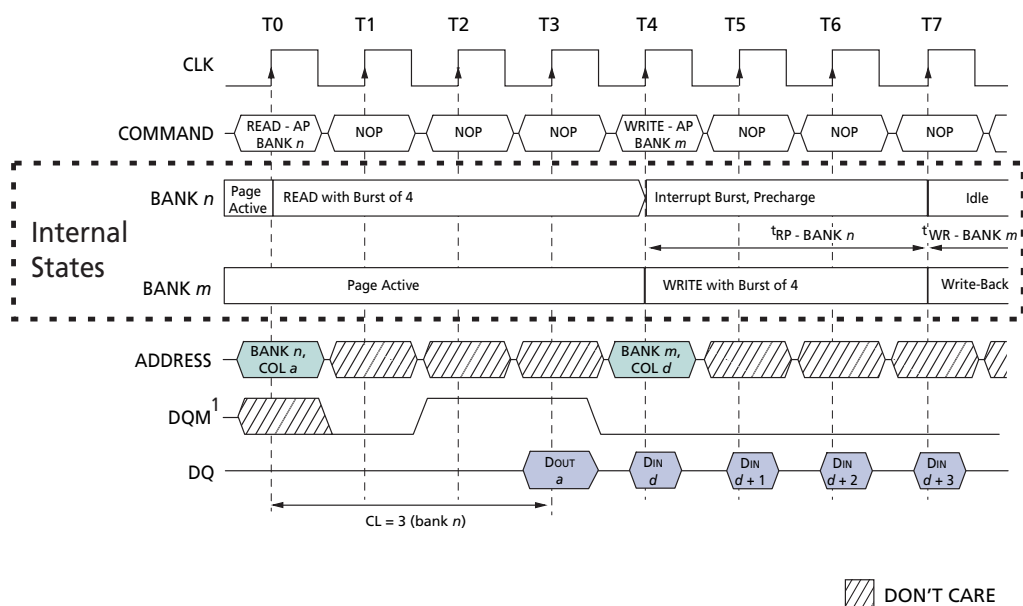
Note: For this example, CL = 2, BL = 4 or greater, and DQM is LOW.

**Figure 29: READ with Auto Precharge Interrupted by a READ**



Note: DQM is LOW.

**Figure 30: READ with Auto Precharge Interrupted by a WRITE**

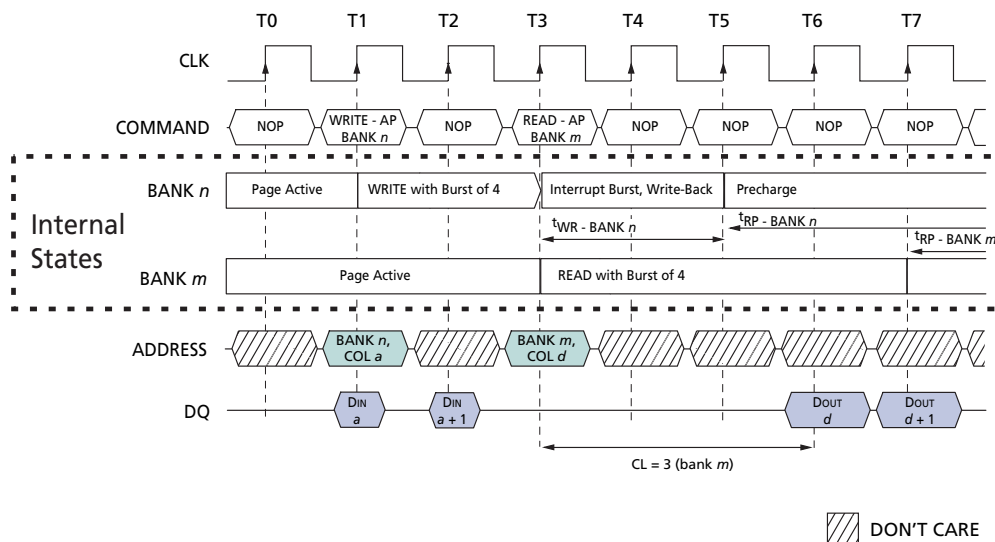


Note: DQM is HIGH at T2 to prevent DOUT  $a+1$  from contending with DIN  $d$  at T4.

## WRITE with Auto Precharge

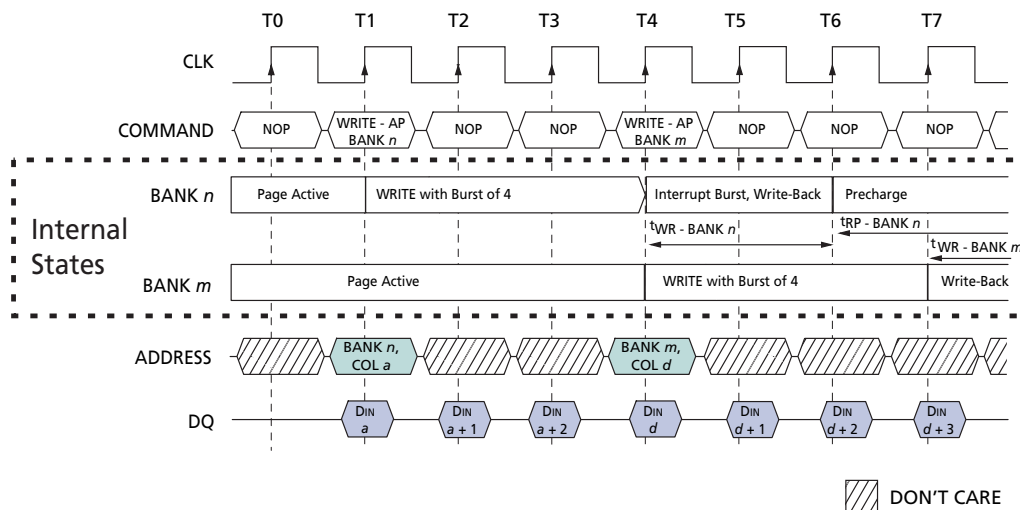
1. Interrupted by a READ (with or without auto precharge): A READ to bank  $m$  will interrupt a WRITE on bank  $n$  when registered, with the data-out appearing CL later. The precharge to bank  $n$  will begin after  $t_{WR}$  is met, where  $t_{WR}$  begins when the READ to bank  $m$  is registered. The last valid WRITE to bank  $n$  will be data-in registered one clock prior to the READ to bank  $m$  (see Figure 31 on page 39).
2. Interrupted by a WRITE (with or without auto precharge): A WRITE to bank  $m$  will interrupt a WRITE on bank  $n$  when registered. The precharge to bank  $n$  will begin after  $t_{WR}$  is met, where  $t_{WR}$  begins when the WRITE to bank  $m$  is registered. The last valid data WRITE to bank  $n$  will be data registered one clock prior to a WRITE to bank  $m$  (see Figure 32 on page 39).

**Figure 31: WRITE with Auto Precharge Interrupted by a READ**



Note: DQM is LOW.

**Figure 32: WRITE with Auto Precharge Interrupted by a WRITE**



Note: DQM is LOW.

## Truth Tables

**Table 6: Truth Table – CKE**

Notes: 1–4

$CKE_{n-1}$	$CKE_n$	Current State	Command <sub>n</sub>	Action <sub>n</sub>	Notes
L	L	Power-down	X	Maintain power-down	
		Self refresh	X	Maintain self refresh	
		Clock suspend	X	Maintain clock suspend	
		Deep power-down	X	Maintain deep power-down	8
L	H	Power-down	COMMAND INHIBIT or NOP	Exit power-down	5
		Deep power-down	X	Exit deep power-down	8
		Self refresh	COMMAND INHIBIT or NOP	Exit self refresh	6
		Clock suspend	X	Exit clock suspend	7
H	L	All banks idle	COMMAND INHIBIT or NOP	Power-down entry	
		All banks idle	BURST TERMINATE	Deep power-down entry	8
		All banks idle	AUTO REFRESH	Self refresh entry	
		Reading or writing	VALID	Clock suspend entry	
H	H		See Table 8 on page 43		

- Notes:
1.  $CKE_n$  is the logic state of CKE at clock edge  $n$ ;  $CKE_{n-1}$  was the state of CKE at the previous clock edge.
  2. Current state is the state of the SDRAM immediately prior to clock edge  $n$ .
  3.  $COMMAND_n$  is the command registered at clock edge  $n$ , and  $ACTION_n$  is a result of  $COMMAND_n$ .
  4. All states and sequences not shown are illegal or reserved.
  5. Exiting power-down at clock edge  $n$  will put the device in the all banks idle state in time for clock edge  $n + 1$  (provided that  $t_{CKS}$  is met).
  6. Exiting self refresh at clock edge  $n$  will put the device in the all banks idle state once  $t_{XSR}$  is met.  $COMMAND$  INHIBIT or NOP commands should be issued on any clock edges occurring during the  $t_{XSR}$  period. A minimum of two NOP commands must be provided during  $t_{XSR}$  period.
  7. After exiting clock suspend at clock edge  $n$ , the device will resume operation and recognize the next command at clock edge  $n + 1$ .
  8. Deep power-down is power savings feature of this Mobile SDRAM device. This command is BURST TERMINATE when CKE is HIGH and deep power-down when CKE is LOW.

**Table 7: Truth Table – Current State Bank  $n$ , Command to Bank  $n$** 

Notes: 1–6; notes appear below table

Current State	CS#	RAS#	CAS#	WE#	Command (Action)	Notes
Any	H	X	X	X	COMMAND INHIBIT (NOP/Continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/Continue previous operation)	
Idle	L	L	H	H	ACTIVE (Select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	LMR	7
	L	L	H	L	PRECHARGE	11
Row active	L	H	L	H	READ (Select column and start READ burst)	10
	L	H	L	L	WRITE (Select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (Deactivate row in bank or banks)	8
Read (auto precharge disabled)	L	H	L	H	READ (Select column and start new READ burst)	10
	L	H	L	L	WRITE (Select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (Truncate READ burst, start PRECHARGE)	8
	L	H	H	L	BURST TERMINATE	9
Write (auto precharge disabled)	L	H	L	H	READ (Select column and start READ burst)	10
	L	H	L	L	WRITE (Select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (Truncate WRITE burst, start PRECHARGE)	8
	L	H	H	L	BURST TERMINATE	9

- Notes:
- This table applies when  $\text{CKE}_{n-1}$  was HIGH and  $\text{CKE}_n$  is HIGH (see Table 6 on page 40) and after  $t_{\text{XSR}}$  has been met (if the previous state was self refresh).
  - This table is bank-specific, except where noted; i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.
  - Current state definitions:
    - Idle: The bank has been precharged, and  $t_{\text{RP}}$  has been met.
    - Row active: A row in the bank has been activated, and  $t_{\text{RCD}}$  has been met. No data bursts/accesses and no register accesses are in progress.
    - Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
    - Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
  - The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Table 7, and according to Table 8 on page 43.
    - Precharging: Starts with registration of a PRECHARGE command and ends when  $t_{\text{RP}}$  is met. Once  $t_{\text{RP}}$  is met, the bank will be in the idle state.
    - Row activating: Starts with registration of an ACTIVE command and ends when  $t_{\text{RCD}}$  is met. Once  $t_{\text{RCD}}$  is met, the bank will be in the row active state.
    - Read w/auto-precharge enabled: Starts with registration of a READ command with auto precharge enabled and ends when  $t_{\text{RP}}$  has been met. Once  $t_{\text{RP}}$  is met, the bank will be in the idle state.
    - Write w/auto-precharge enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when  $t_{\text{RP}}$  has been met. Once  $t_{\text{RP}}$  is met, the bank will be in the idle state.

5. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.
 

Refreshing:	Starts with registration of an AUTO REFRESH command and ends when $t_{RFC}$ is met. Once $t_{RFC}$ is met, the Mobile SDRAM will be in the all banks idle state.
Accessing MR:	Starts with registration of an LMR command and ends when $t_{MRD}$ has been met. Once $t_{MRD}$ is met, the Mobile SDRAM will be in the all banks idle state.
Precharging all:	Starts with registration of a PRECHARGE ALL command and ends when $t_{RP}$ is met. Once $t_{RP}$ is met, all banks will be in the idle state.
6. All states and sequences not shown are illegal or reserved
7. Not bank-specific; requires that all banks are idle.
8. May or may not be bank-specific; if all banks are to be precharged, all must be in a valid state for precharging.
9. Not bank-specific; BURST TERMINATE affects the most recent READ or WRITE burst, regardless of bank.
10. READs or WRITEs listed in the Command (Action) column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
11. Does not affect the state of the bank and acts as a NOP to that bank.

**Table 8: Truth Table – Current State Bank *n*, Command to Bank *m***

Notes: 1–6; notes appear below and on next page

Current State	CS#	RAS#	CAS#	WE#	Command (Action)	Notes
Any	H	X	X	X	COMMAND INHIBIT (NOP/Continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/Continue previous operation)	
Idle	X	X	X	X	Any command otherwise allowed to bank <i>m</i>	
Row activating, active, or precharging	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	7
	L	H	L	L	WRITE (Select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (auto precharge disabled)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start new READ burst)	7, 8
	L	H	L	L	WRITE (Select column and start WRITE burst)	7, 9
	L	L	H	L	PRECHARGE	10
Write (auto precharge disabled)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	7, 11
	L	H	L	L	WRITE (Select column and start new WRITE burst)	7, 12
	L	L	H	L	PRECHARGE	10
Read (with auto precharge)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start new READ burst)	7, 13, 14
	L	H	L	L	WRITE (Select column and start WRITE burst)	7, 13, 15
	L	L	H	L	PRECHARGE	10
Write (with auto precharge)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	7, 13, 16
	L	H	L	L	WRITE (Select column and start new WRITE burst)	7, 13, 17
	L	L	H	L	PRECHARGE	10

- Notes:
- This table applies when CKE<sub>*n-1*</sub> was HIGH and CKE<sub>*n*</sub> is HIGH (see Table 6 on page 40) and after <sup>t</sup>XSR has been met (if the previous state was self refresh).
  - This table describes alternate bank operation, except where noted; i.e., the current state is for bank *n* and the commands shown are those allowed to be issued to bank *m* (assuming that bank *m* is in such a state that the given command is allowable). Exceptions are covered in the notes below.
  - Current state definitions:
    - Idle: The bank has been precharged, and <sup>t</sup>RP has been met.
    - Row active: A row in the bank has been activated, and <sup>t</sup>RCD has been met. No data bursts/accesses and no register accesses are in progress.
    - Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
    - Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
    - Read w/auto-precharge enabled: Starts with registration of a READ command with auto precharge enabled and ends when <sup>t</sup>RP has been met. Once <sup>t</sup>RP is met, the bank will be in the idle state.
    - Write w/auto-precharge enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when <sup>t</sup>RP has been met. Once <sup>t</sup>RP is met, the bank will be in the idle state.
  - AUTO REFRESH, SELF REFRESH and LMR commands may only be issued when all banks are idle.

5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs to bank *m* listed in the Command (Action) column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
8. For a READ without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the READ on bank *n*, CL later (see Figure 11 on page 24).
9. For a READ without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the READ on bank *n* when registered (see Figure 12 on page 25 and Figure 13 on page 26). DQM should be used one clock prior to the WRITE command to prevent bus contention.
10. Burst in bank *n* continues as initiated.
11. For a WRITE without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the WRITE on bank *n* when registered (see Figure 20 on page 31), with the data-out appearing CL later. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m*.
12. For a WRITE without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank will interrupt the WRITE on bank *n* when registered (see Figure 18 on page 30). The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m*.
13. Concurrent auto precharge: Bank *n* will initiate the auto precharge command when its burst has been interrupted by bank *m* burst.
14. For a READ with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the READ on bank *n*, CL later. The PRECHARGE to bank *n* will begin when the READ to bank *m* is registered.
15. For a READ with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the READ on bank *n* when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The PRECHARGE to bank *n* will begin when the WRITE to bank *m* is registered.
16. For a WRITE with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the WRITE on bank *n* when registered, with the data-out appearing CL later. The PRECHARGE to bank *n* will begin after  $t_{WR}$  is met, where  $t_{WR}$  begins when the READ to bank *m* is registered. The last valid WRITE bank *n* will be data-in registered one clock prior to the READ to bank *m*.
17. For a WRITE with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* interrupt the WRITE on bank *n* when registered. The PRECHARGE to bank *n* will begin after  $t_{WR}$  is met, where  $t_{WR}$  begins when the WRITE to bank *m* is registered. The last valid WRITE to bank *n* will be data registered one clock to the WRITE to bank *m*.

## Electrical Specifications

### Absolute Maximum Ratings

Stresses greater than those listed in Table 9 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Table 9: Absolute Maximum Ratings**

Voltage/Temperature	Min	Max	Units
Voltage on V <sub>DD</sub> /V <sub>DDQ</sub> supply relative to V <sub>SS</sub> (1.8V)	-0.3	+2.7	V
Voltage on inputs, NC or I/O balls relative to V <sub>SS</sub> (1.8V)	-0.3	+2.7	
Storage temperature plastic	-55	+150	

**Table 10: DC Electrical Characteristics and Operating Conditions**

Notes: 1, 5, 6; notes appear on page 51 and 52; V<sub>DD</sub>/V<sub>DDQ</sub> = 1.7–1.95V

Parameter/Condition	Symbol	Min	Max	Units	Notes
Supply voltage	V <sub>DD</sub>	1.7	1.95	V	
I/O supply voltage	V <sub>DDQ</sub>	1.7	1.95	V	
Input high voltage: Logic 1; All inputs	V <sub>IH</sub>	0.8 × V <sub>DDQ</sub>	V <sub>DDQ</sub> + 0.3	V	22
Input low voltage: Logic 0; All inputs	V <sub>IL</sub>	-0.3	+0.3	V	22
Output high voltage: All inputs: I <sub>out</sub> = -4mA	V <sub>OH</sub>	0.9 × V <sub>DDQ</sub>	–	V	
Output low voltage: All inputs: I <sub>out</sub> = 4mA	V <sub>OL</sub>	–	0.2	V	
Input leakage current: Any input 0V ≤ V <sub>IN</sub> ≤ V <sub>DD</sub> (All other balls not under test = 0V)	I <sub>I</sub>	-1.0	1.0	μA	
<b>Operating temperature</b>					
T <sub>A</sub> (commercial)		+70	°C		
T <sub>A</sub> (industrial)		+85			

**Table 11: Electrical Characteristics and Recommended AC Operating Conditions**

Notes: 5, 6, 8, 9, 11; notes appear on page 51 and 52

AC Characteristics		Symbol	-75		-8		Units	Notes
Parameter			Min	Max	Min	Max		
Access time from CLK (pos. edge)	CL = 3	$t_{AC}^{(3)}$		6		7	ns	9
	CL = 2	$t_{AC}^{(2)}$		8		9	ns	
Address hold time		$t_{AH}$	1		1		ns	
Address setup time		$t_{AS}$	1.5		2.5		ns	
CLK high-level width		$t_{CH}$	3		3		ns	
CLK low-level width		$t_{CL}$	3		3		ns	
Clock cycle time	CL = 3	$t_{CK}^{(3)}$	7.5		8		ns	23
	CL = 2	$t_{CK}^{(2)}$	9.6		10		ns	23
CKE hold time		$t_{CKH}$	1		1		ns	
CKE setup time		$t_{CKS}$	2.5		2.5		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		$t_{CMH}$	1		1		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		$t_{CMS}$	1.5		2.5		ns	
Data-in hold time		$t_{DH}$	1		1		ns	
Data-in setup time		$t_{DS}$	1.5		2.5		ns	
Data-out High-Z time	CL = 3	$t_{HZ}^{(3)}$		6		7	ns	10
	CL = 2	$t_{HZ}^{(2)}$		9		9	ns	10
Data-out Low-Z time		$t_{LZ}$	1		1		ns	
Data-out hold time (load)		$t_{OH}$	2.5		2.5		ns	
Data-out hold time (no load)		$t_{OHn}$	1.8		1.8		ns	25
ACTIVE-to-PRECHARGE command		$t_{RAS}$	44	120,000	48	120,000	ns	
ACTIVE-to-ACTIVE command period		$t_{RC}$	67.5		72		ns	
ACTIVE-to-READ or WRITE delay		$t_{RCD}$	19		20		ns	
Refresh period (8,192 rows)		$t_{REF}$		64		64	ms	
AUTO REFRESH period		$t_{RFC}$	80		80		ns	
PRECHARGE command period		$t_{RP}$	19		19		ns	
ACTIVE bank <i>a</i> to ACTIVE bank <i>b</i> command		$t_{RRD}$	2		2		$t_{CK}$	
Transition time		$t_T$	0.3	1.2	0.5	1.2	ns	7
WRITE recovery time		$t_{WR}$	15		15		ns	31
Exit SELF REFRESH to ACTIVE command		$t_{XSR}$	80		80		ns	20

**Table 12: AC Functional Characteristics**

Notes: 5, 6, 8, 9, 11 notes appear on page 51 and 52

Parameter	Symbol	-75	-8	Units	Notes
READ/WRITE command to READ/WRITE command	$t_{CCD}$	1	1	$t_{CK}$	17
CKE to clock disable or power-down entry mode	$t_{CKED}$	1	1	$t_{CK}$	14
CKE to clock enable or power-down exit setup mode	$t_{PED}$	1	1	$t_{CK}$	14
DQM to input data delay	$t_{DQD}$	0	0	$t_{CK}$	17
DQM to data mask during WRITES	$t_{DQM}$	0	0	$t_{CK}$	17
DQM to data High-Z during READs	$t_{DQZ}$	2	2	$t_{CK}$	17
WRITE command to input data delay	$t_{DWD}$	0	0	$t_{CK}$	17
Data-in to ACTIVE command	$t_{DAL}$	5	5	$t_{CK}$	15, 21
Data-in to PRECHARGE command	$t_{DPL}$	2	2	$t_{CK}$	16, 21
Last data-in to burst STOP command	$t_{BDL}$	1	1	$t_{CK}$	17
Last data-in to new READ/WRITE command	$t_{CDL}$	1	1	$t_{CK}$	17
Last data-in to PRECHARGE command	$t_{RDL}$	2	2	$t_{CK}$	16, 21
LMR command to ACTIVE or REFRESH command	$t_{MRD}$	2	2	$t_{CK}$	25
Data-out High-Z from PRECHARGE command	CL = 3	$t_{ROH(3)}$	3	$t_{CK}$	17
	CL = 2	$t_{ROH(2)}$	2	$t_{CK}$	17

**Table 13: IDD Specifications and Conditions (x16)**

 Notes: 1, 5, 6, 11, 13; notes appear on page 51 and 52;  $V_{DD}/V_{DDQ} = 1.7-1.95V$ 

Parameter/Condition	Symbol	Max		Units	Notes
		-75	-8		
Operating current: Active mode; BL = 1; READ or WRITE; $t_{RC} = t_{RC}(\text{MIN})$	IDD1	65	60	mA	1, 18, 19
Standby current: Power-down mode; All banks idle; CKE = LOW	IDD2P	300	300	$\mu A$	30
Standby current: Non-power-down mode; All banks idle; CKE = HIGH	IDD2N	20	20	mA	
Standby current: Active mode; CKE = LOW; CS# = HIGH; All banks active; No accesses in progress	IDD3P	5	5	mA	1, 12, 19
Standby current: Active mode; CKE = HIGH; CS# = HIGH; All banks active after $t_{RCD}$ met; No accesses in progress	IDD3N	25	25	mA	1, 12, 19
Operating current: Burst mode; READ or WRITE; All banks active, half DQs toggling every cycle	IDD4	90	85	mA	1, 18, 19
Auto refresh current: CKE = HIGH; CS# = HIGH	$t_{RFC} = t_{RFC}(\text{MIN})$	100	95	mA	1, 12, 18 19, 26
	$t_{RFC} = 7.8125\mu s$	5	5	mA	
Deep power-down	Izz	10	10	$\mu A$	29, 30

**Table 14: IDD Specifications and Conditions (x32)**

Notes: 1, 5, 6, 11, 13; notes appear on page 51 and 52; VDD/VDDQ = 1.7–1.95V

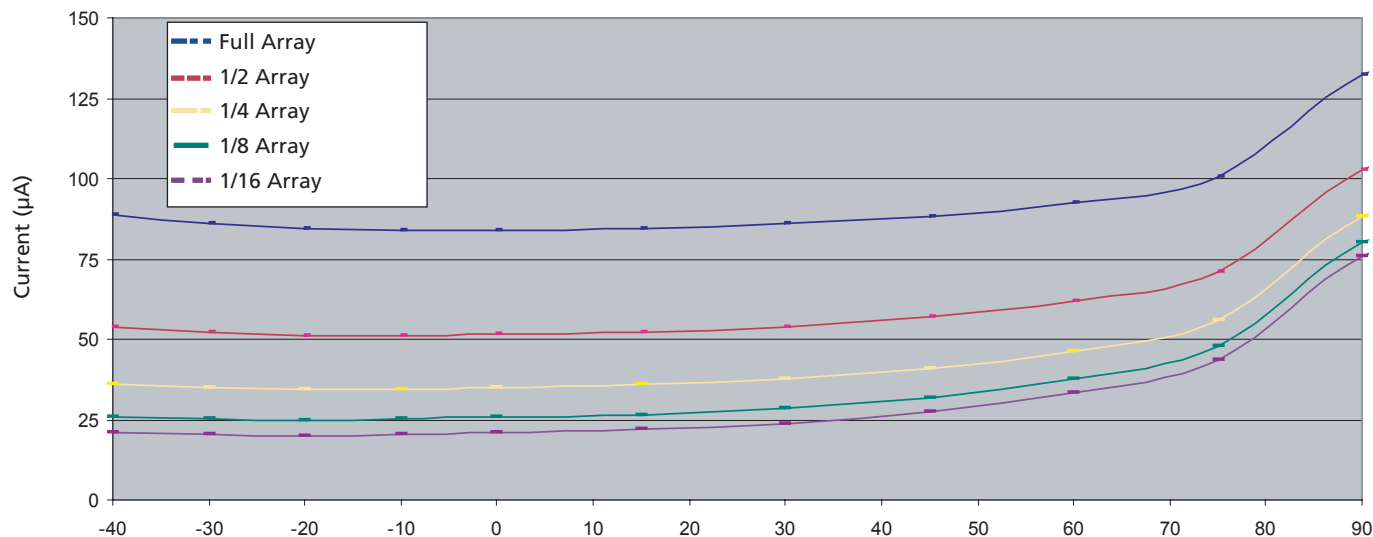
Parameter/Condition	Symbol	Max		Units	Notes
		-75	-8		
Operating current: Active mode; BL = 1; READ or WRITE; $t_{RC} = t_{RC}(\text{MIN})$	IDD1	95	90	mA	1, 18, 19
Standby current: Power-down mode; All banks idle; CKE = LOW	IDD2P	300	300	$\mu\text{A}$	30
Standby current: Non-power-down mode; All banks idle; CKE = HIGH	IDD2N	20	20	mA	
Standby current: Active mode; CKE = LOW; CS# = HIGH; All banks active; No accesses in progress	IDD3P	5	5	mA	1, 12, 19
Standby current: Active mode; CKE = HIGH; CS# = HIGH; All banks active after $t_{RCD}$ met; No accesses in progress	IDD3N	25	25	mA	1, 12, 19
Operating current: Burst mode; READ or WRITE; All banks active, half DQs toggling every cycle	IDD4	120	115	mA	1, 18, 19
Auto refresh current: CKE = HIGH; CS# = HIGH	$t_{RFC} = t_{RFC}(\text{MIN})$	100	95	mA	1, 12, 18, 26
	$t_{RFC} = 7.8125\mu\text{s}$	5	5	mA	19, 27
Deep power-down	Izz	10	10	$\mu\text{A}$	29, 30

**Table 15: Idd7 – Self Refresh Current Options**

Notes: 2, 28, 30; notes appear on page 51 and page 52

Temperature-Compensated Self Refresh Parameter/Condition	Maximum Temperature	Low Idd7 Option "L"	Standard Idd7	Units
Self refresh current: CKE = LOW – 4-bank refresh	85°C	220	300	μA
	70°C	175	210	μA
	45°C	140	190	μA
	15°C	125	180	μA
Self refresh current: CKE = LOW – 2-bank refresh	85°C	200	275	μA
	70°C	150	180	μA
	45°C	130	160	μA
	15°C	115	150	μA
Self refresh current: CKE = LOW – 1-bank refresh	85°C	185	265	μA
	70°C	140	160	μA
	45°C	120	140	μA
	15°C	115	140	μA
Self refresh current: CKE = LOW – Half-bank refresh	85°C	175	255	μA
	70°C	125	150	μA
	45°C	115	130	μA
	15°C	110	125	μA
Self refresh current: CKE = LOW – Quarter-bank refresh	85°C	170	250	μA
	70°C	120	140	μA
	45°C	110	120	μA
	15°C	105	115	μA

**Figure 33: Typical Self Refresh Current vs. Temperature**



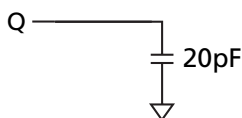
**Table 16: Capacitance**

Note: 2; notes appear on page 51 and 52

Parameter	Symbol	Min	Max	Units
Input capacitance: CLK	C <sub>I1</sub>	1.5	4.5	pF
Input capacitance: All other input-only balls	C <sub>I2</sub>	2.0	4.5	pF
Input/output capacitance: DQs	C <sub>IO</sub>	2.0	6.0	pF

## Notes

1. All voltages referenced to VSS.
2. This parameter is sampled. VDD, VDDQ = +1.8V;  $T_A = 25^\circ\text{C}$ ; ball under test biased at 0.9V;  $f = 1\text{ MHz}$ .
3. IDD is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ( $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$  for  $T_A$  on IT parts) is ensured.
6. An initial pause of 100 $\mu\text{s}$  is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (VDD and VDDQ must be powered up simultaneously. VSS and VSSQ must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the  $t_{\text{REF}}$  refresh requirement is exceeded.
7. AC characteristics assume  $t_T = 1\text{ ns}$ .
8. In addition to meeting the transition rate specification, the clock and CKE must transit between  $V_{\text{IH}}$  and  $V_{\text{IL}}$  (or between  $V_{\text{IL}}$  and  $V_{\text{IH}}$ ) in a monotonic manner.
9. Outputs measured for 1.8V at 0.9V with equivalent load:



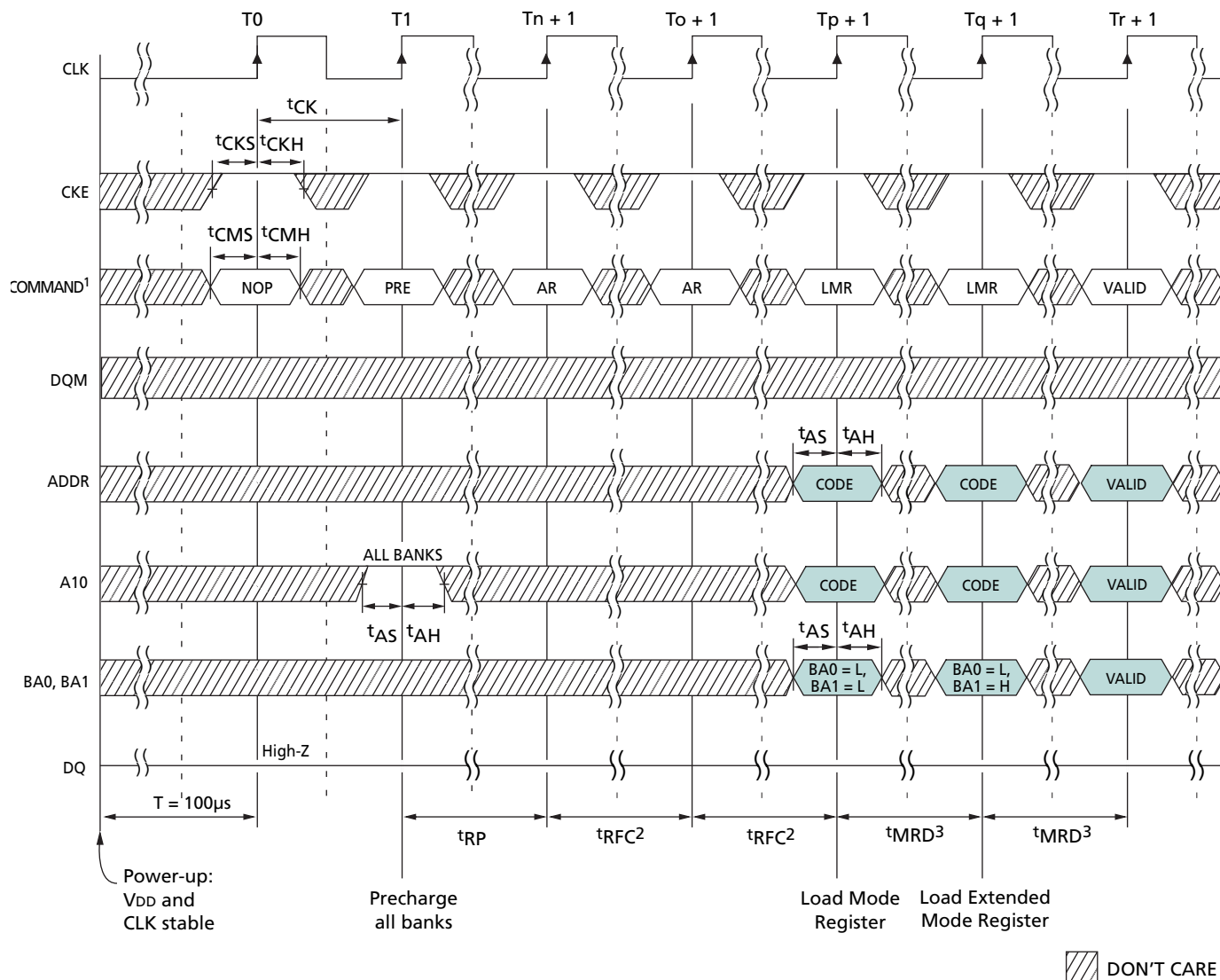
Test loads with full DQ driver strength. Performance will vary with actual system DQ bus capacitive loading, termination, and programmed drive strength.

10.  $t_{\text{HZ}}$  defines the time at which the output achieves the open circuit condition; it is not a reference to  $V_{\text{OH}}$  or  $V_{\text{OL}}$ . The last valid data element will meet  $t_{\text{OH}}$  before going High-Z.
11. AC timing and IDD tests have  $V_{\text{IL}}$  and  $V_{\text{IH}}$ , with timing referenced to  $V_{\text{IH}}/2 =$  crossover point. If the input transition time is longer than  $t_T$  (MAX), then the timing is referenced at  $V_{\text{IL}}$  (MAX) and  $V_{\text{IH}}$  (MIN) and no longer at the  $V_{\text{IH}}/2$  crossover point.
12. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid  $V_{\text{IH}}$  or  $V_{\text{IL}}$  levels.
13. IDD specifications are tested after the device is properly initialized.
14. Timing actually specified by  $t_{\text{CKS}}$ ; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by  $t_{\text{WR}}$  plus  $t_{\text{RP}}$ ; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by  $t_{\text{WR}}$ .
17. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The IDD current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
19. Address transitions average one transition every two clocks.
20. CLK must be toggled a minimum of two times during this period.
21. Based on  $t_{\text{CK}} = 7.5\text{ ns}$  for -75,  $t_{\text{CK}} = 8\text{ ns}$  for -8, at  $\text{CL} = 3$ .

22. VIH overshoot:  $V_{IH} (MAX) = V_{DDQ} + 2V$  for a pulse width  $\leq 3ns$ , and the pulse width cannot be greater than one third of the cycle rate. VIL undershoot:  $V_{IL} (MIN) = -2V$  for a pulse width  $\leq 3ns$ .
23. The clock frequency can only be changed during clock stop, power-down, or while in a self-refresh mode.
24. Auto precharge mode only. The precharge timing budget ( $t_{RP}$ ) begins at 7ns for -8 after the first clock delay, after the last WRITE is executed. May not exceed limit set for precharge mode. The clock frequency can only be changed during
25. Parameter guaranteed by design.
26. CKE is HIGH during refresh command period  $t_{RFC} (MIN)$  else CKE is LOW.
27. The IDD6 limit is actually a nominal value and does not result in a fail value.
28. Values for IDD7 for 70°C, 45°C, 15°C, and IDD7 1/2-bank and 1/4-bank are sampled only. Values for IDD7 4-bank, 2-bank, and 1-bank for 85°C are 100 percent tested.
29. Deep power-down current is a nominal value at 25°C. This parameter is not tested.
30. Test conditions include 500ms delay prior to measurement.
31. Auto precharge mode only. The precharge timing budget ( $t_{RP}$ ) begins at 7.5ns for -75 and 7ns for -8 after the first clock delay, after the last WRITE is executed. For auto precharge mode, at least one clock cycle is required during  $t_{WR}$ .

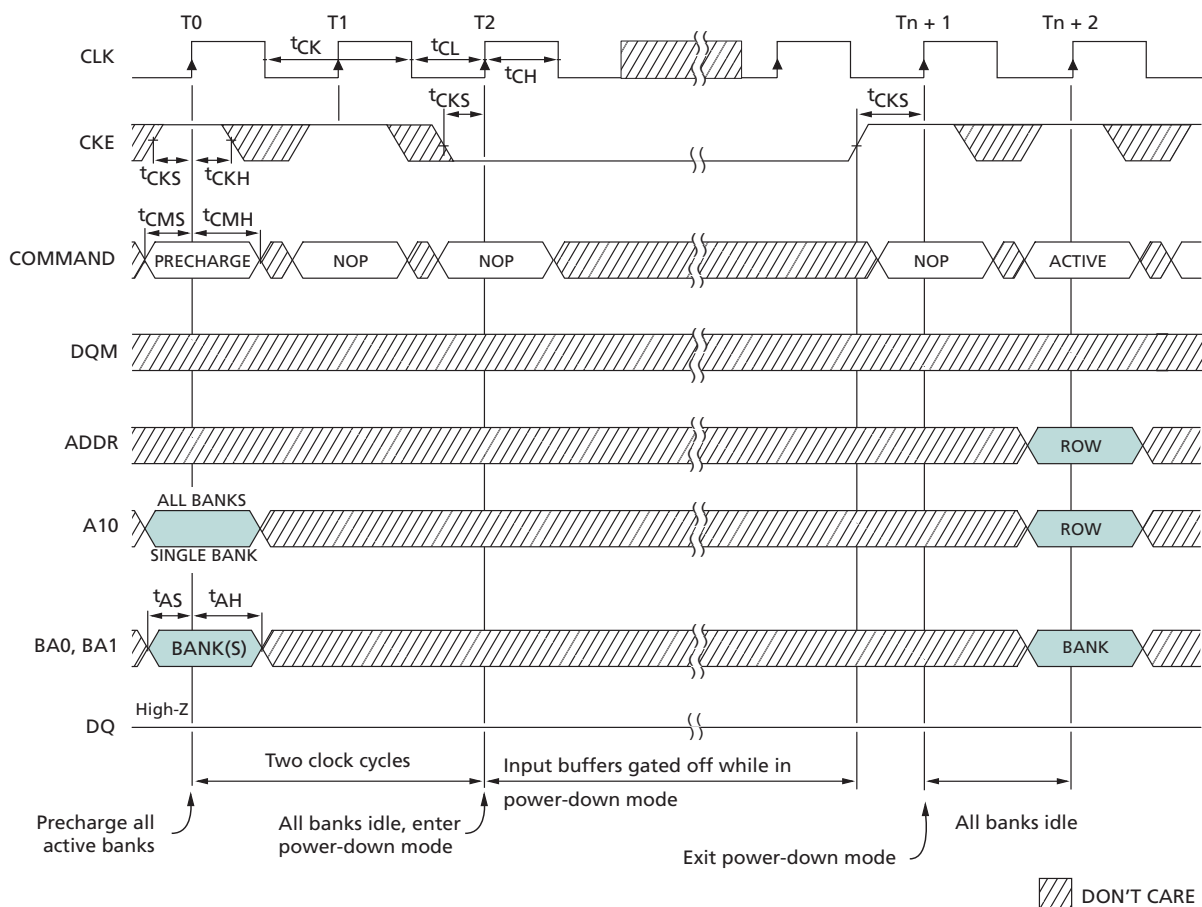
## Timing Diagrams

**Figure 34: Initialize and Load Mode Register**



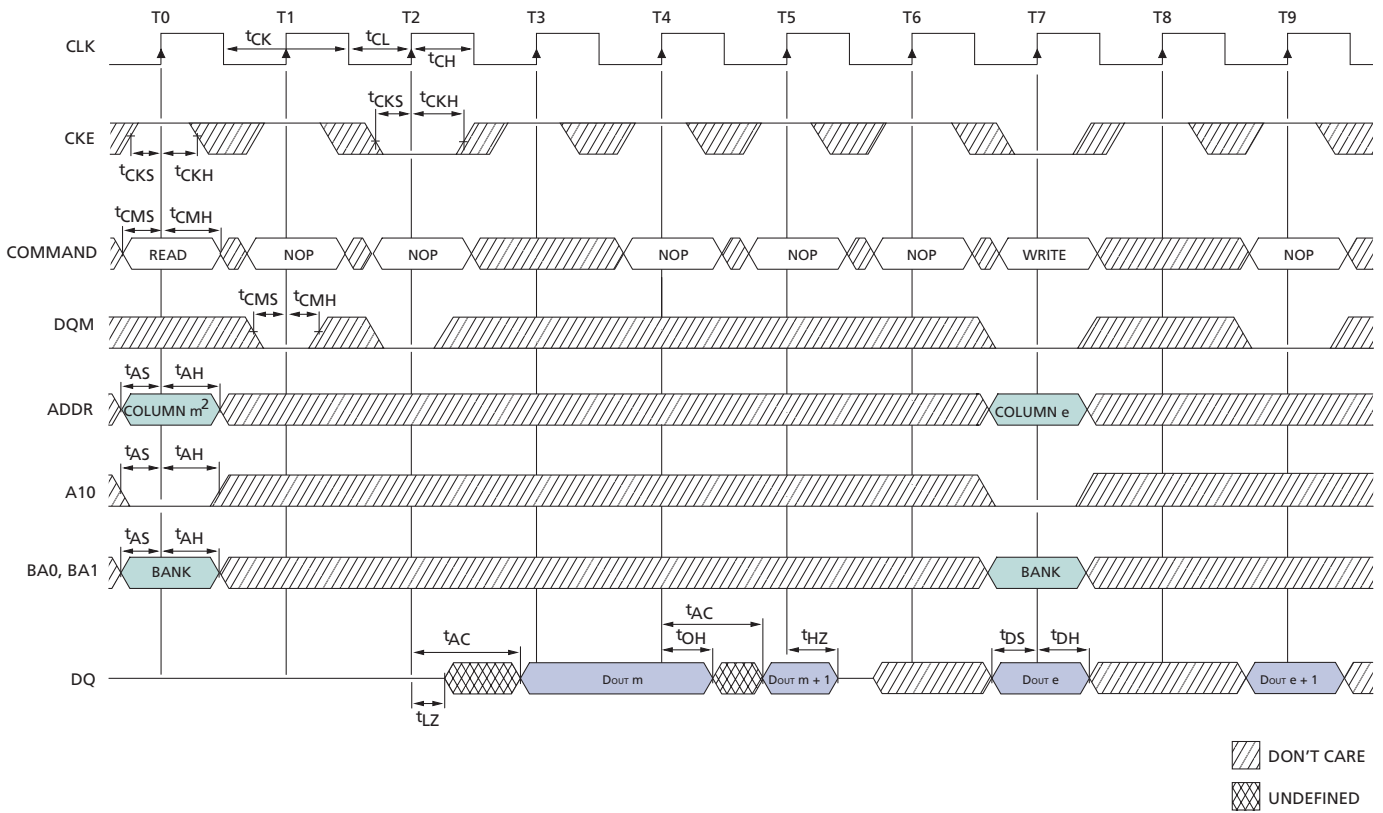
- Notes:
1. PRE = PRECHARGE command; AR = AUTO REFRESH command; LMR = LOAD MODE REGISTER command.
  2. Only NOPs or COMMAND INHIBITS may be issued during  $t_{RFC}^2$  time.
  3. At least one NOP or COMMAND INHIBIT is required during  $t_{MRD}^3$  time.

**Figure 35: Power-Down Mode**



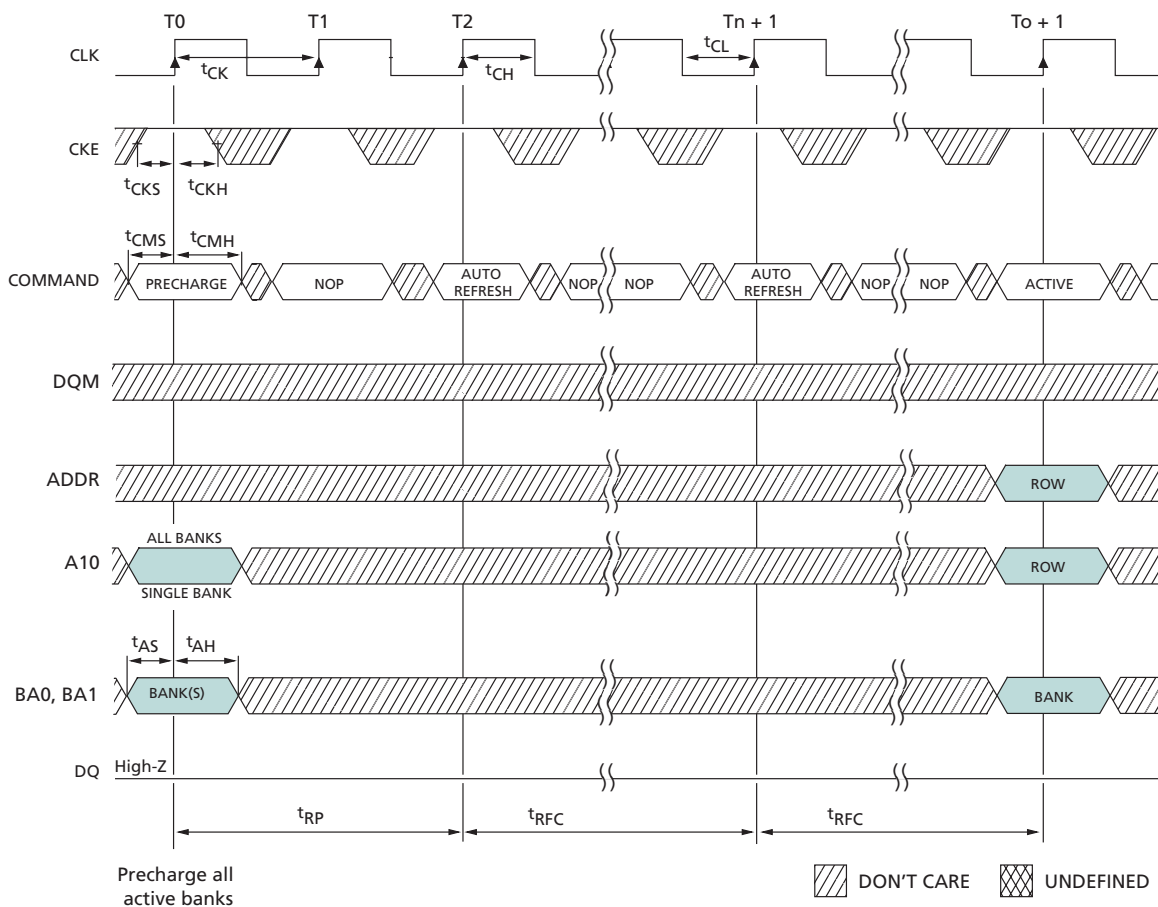
Notes: 1. Violating refresh requirements during power-down may result in a loss of data. See Table 11 on page 46.

**Figure 36: Clock Suspend Mode**



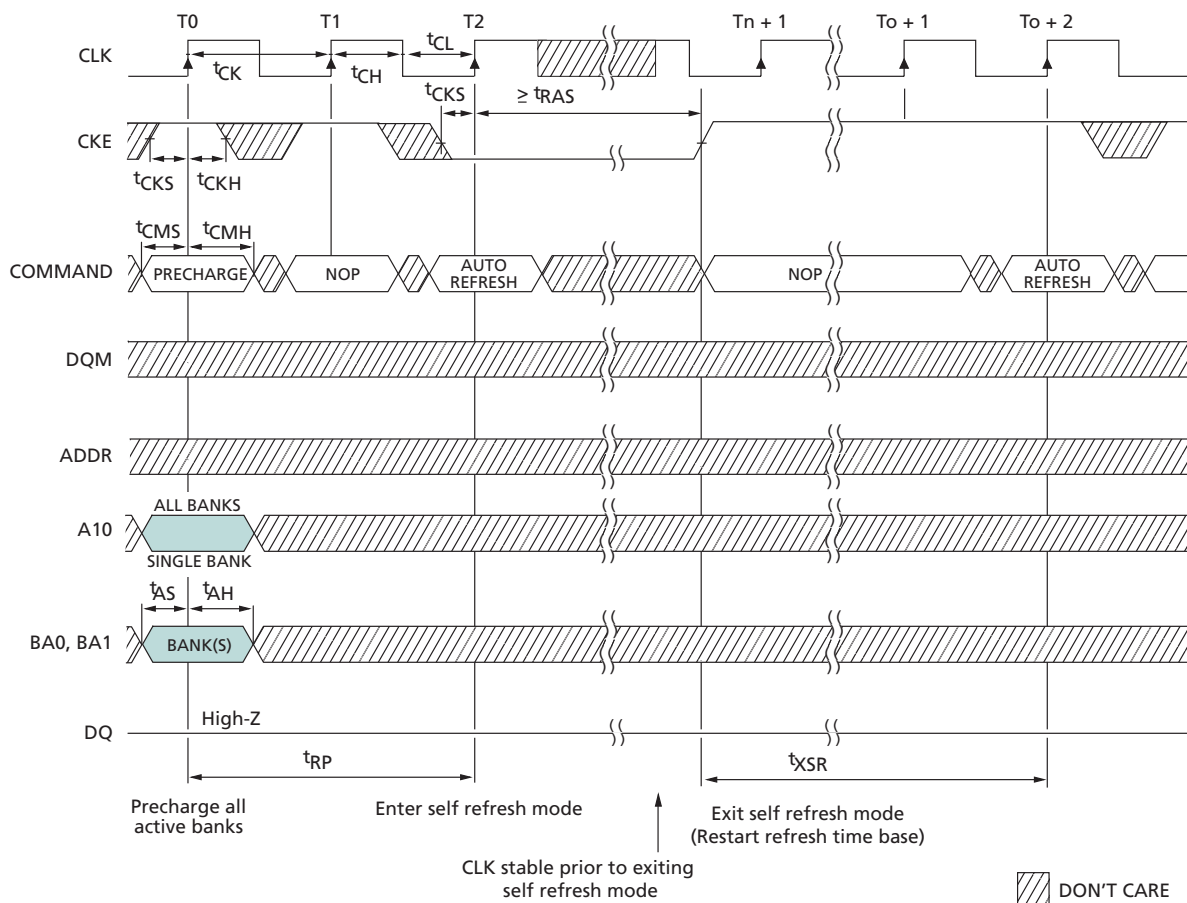
Notes: 1. For this example, BL = 2, CL = 3, and auto precharge is disabled.

**Figure 37: Auto Refresh Mode**

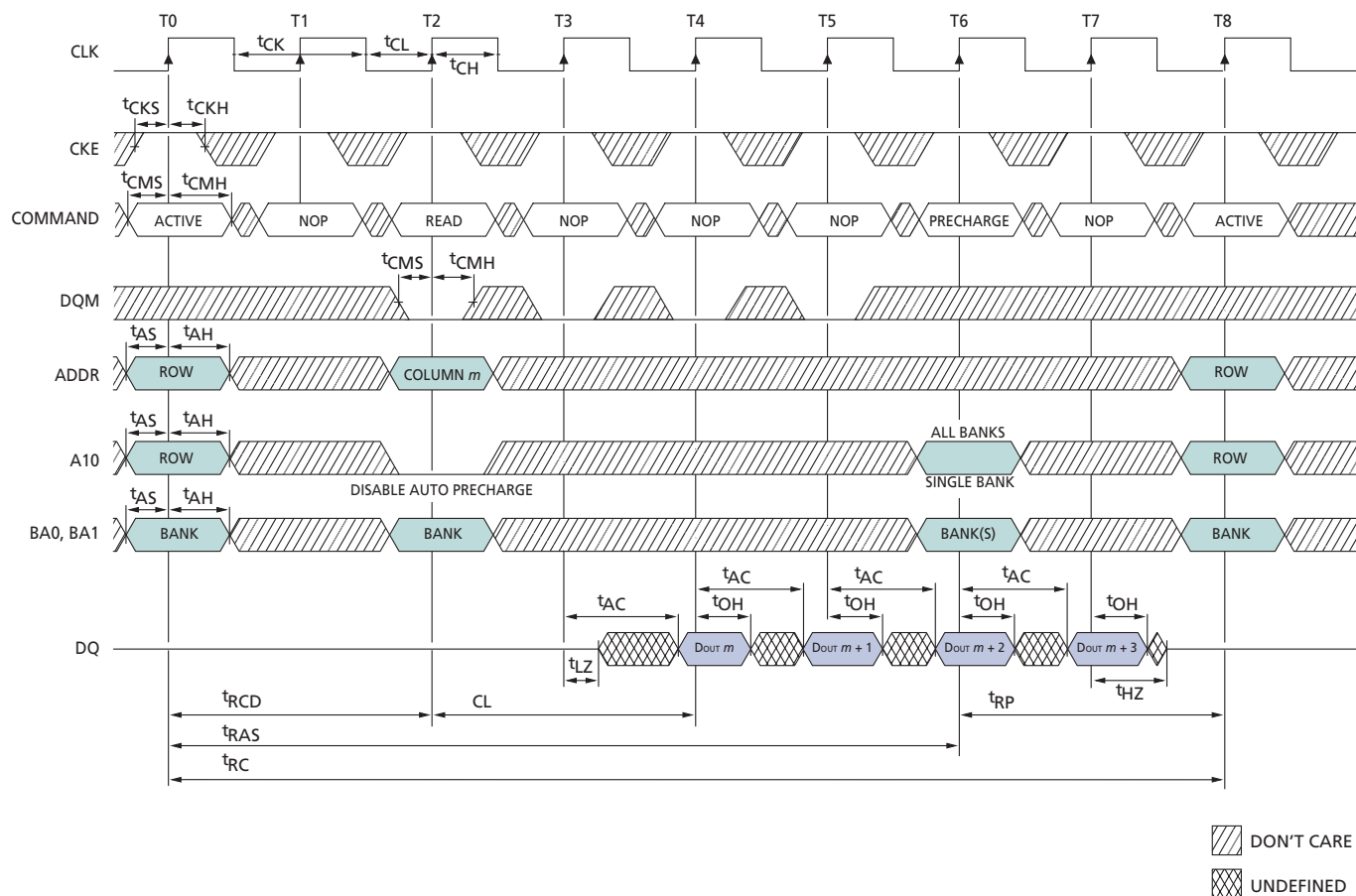


Notes: 1. Each AUTO REFRESH command performs a REFRESH cycle. Back-to-back commands are not required.  
See Table 11 on page 46.

**Figure 38: Self Refresh Mode**

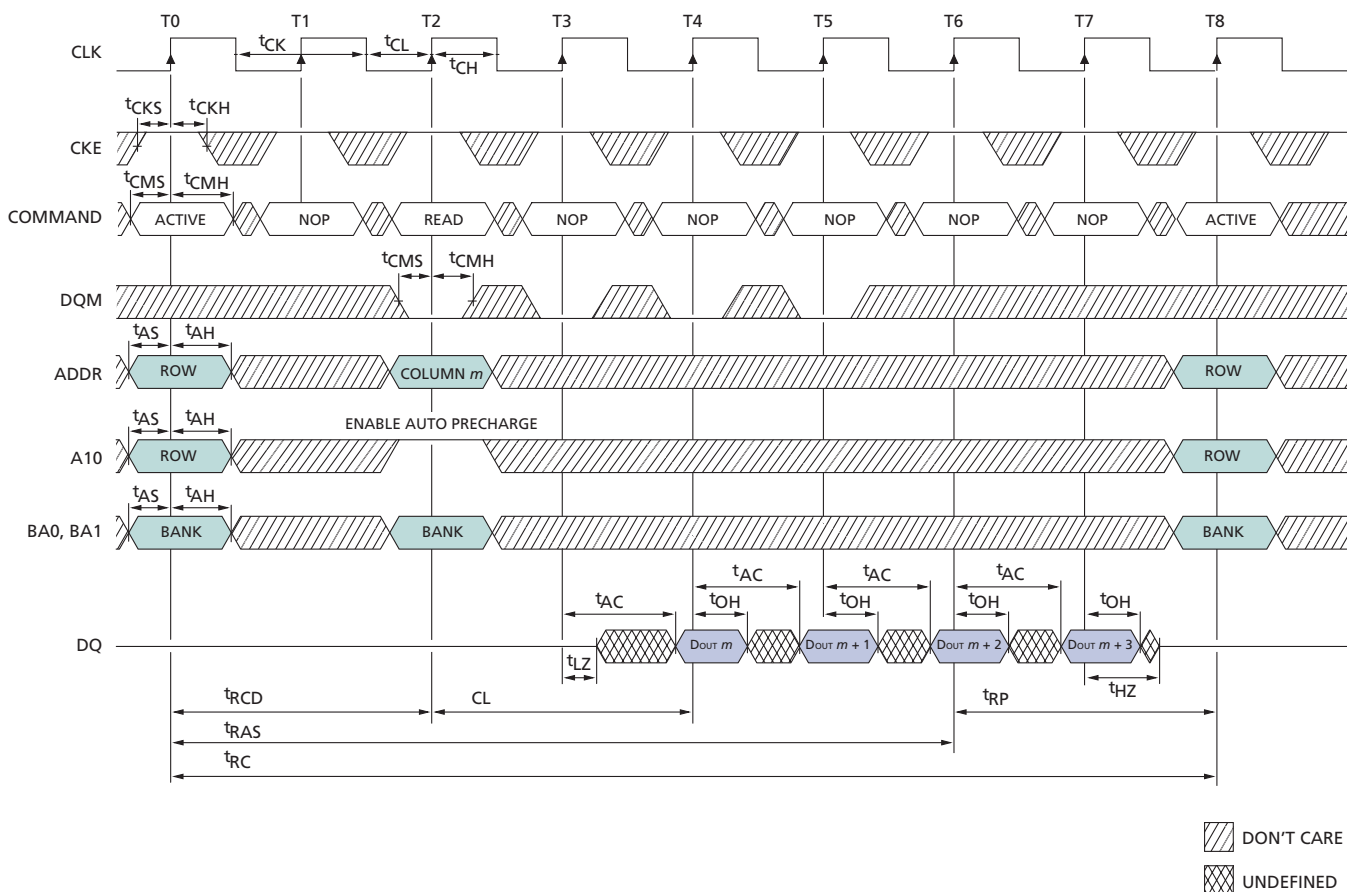


**Figure 39: READ – without Auto Precharge**



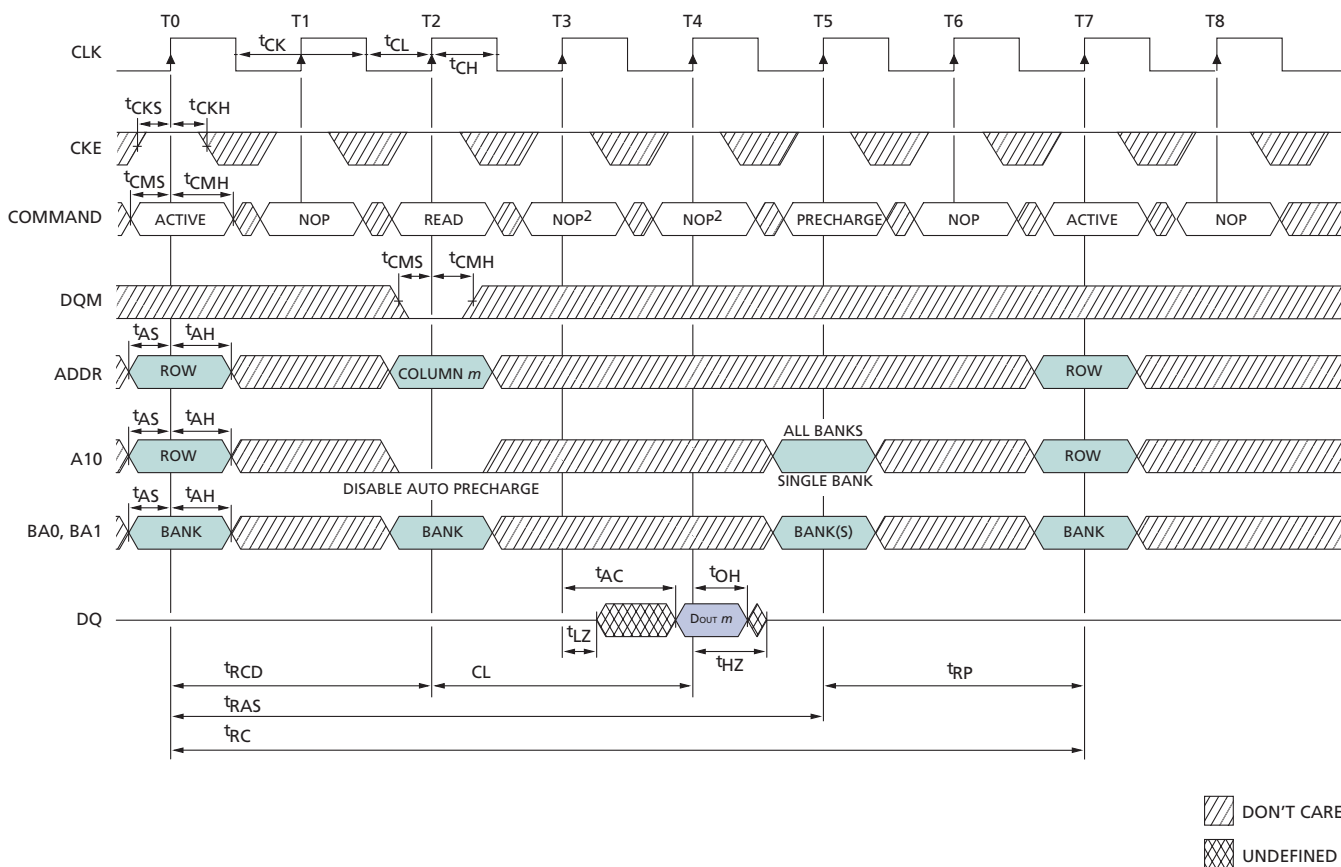
Notes: 1. For this example, BL = 4, CL = 2, and the READ burst is followed by a manual PRECHARGE.

**Figure 40: READ – with Auto Precharge**



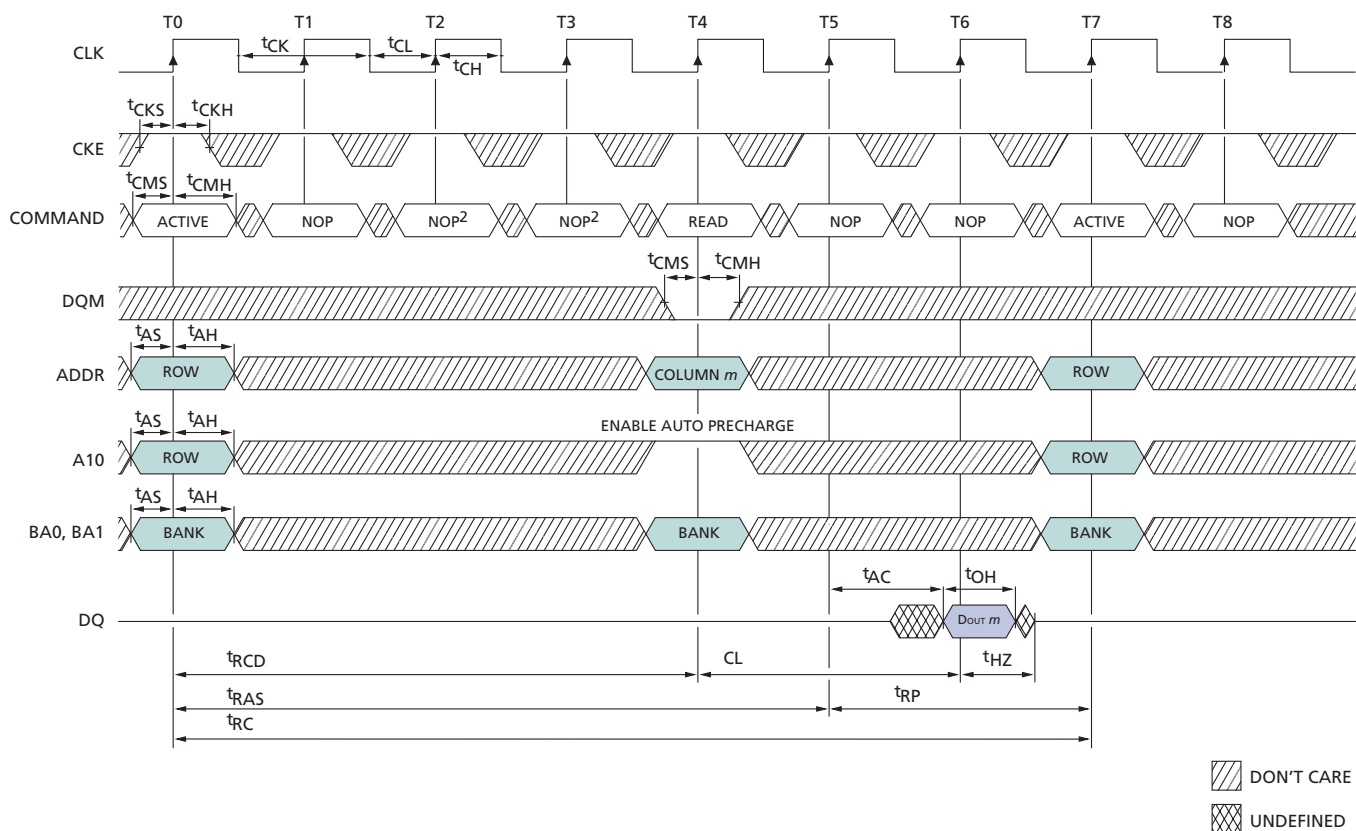
Notes: 1. For this example, BL = 4, CL = 2.

**Figure 41: Single READ – without Auto Precharge**



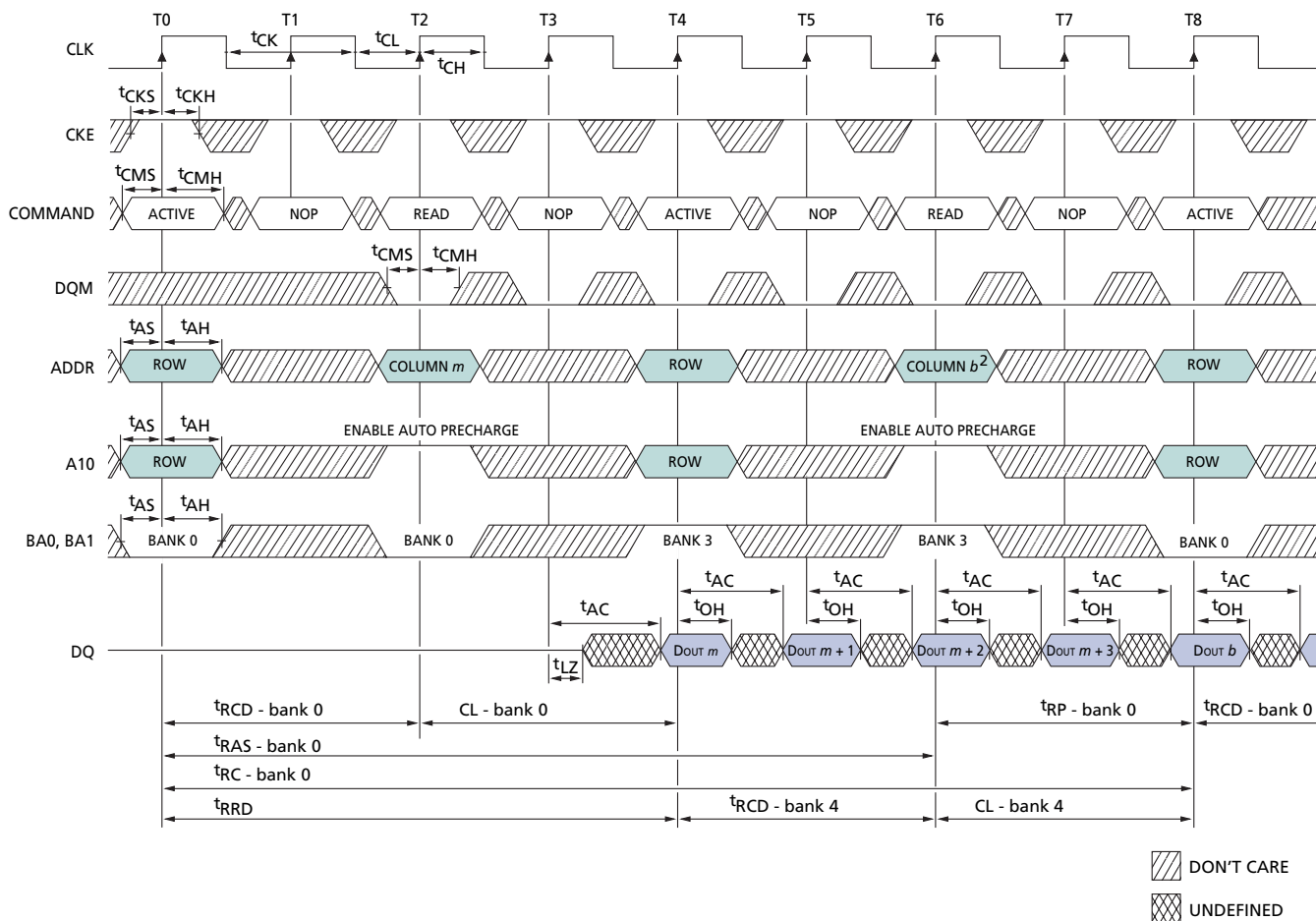
- Notes:
1. For this example, BL = 4, CL = 2, and the READ burst is followed by a manual PRECHARGE.
  2. PRECHARGE command not allowed or  $t_{RAS}$  would be violated.  
See Table 11 on page 46.

**Figure 42: Single READ – with Auto Precharge**



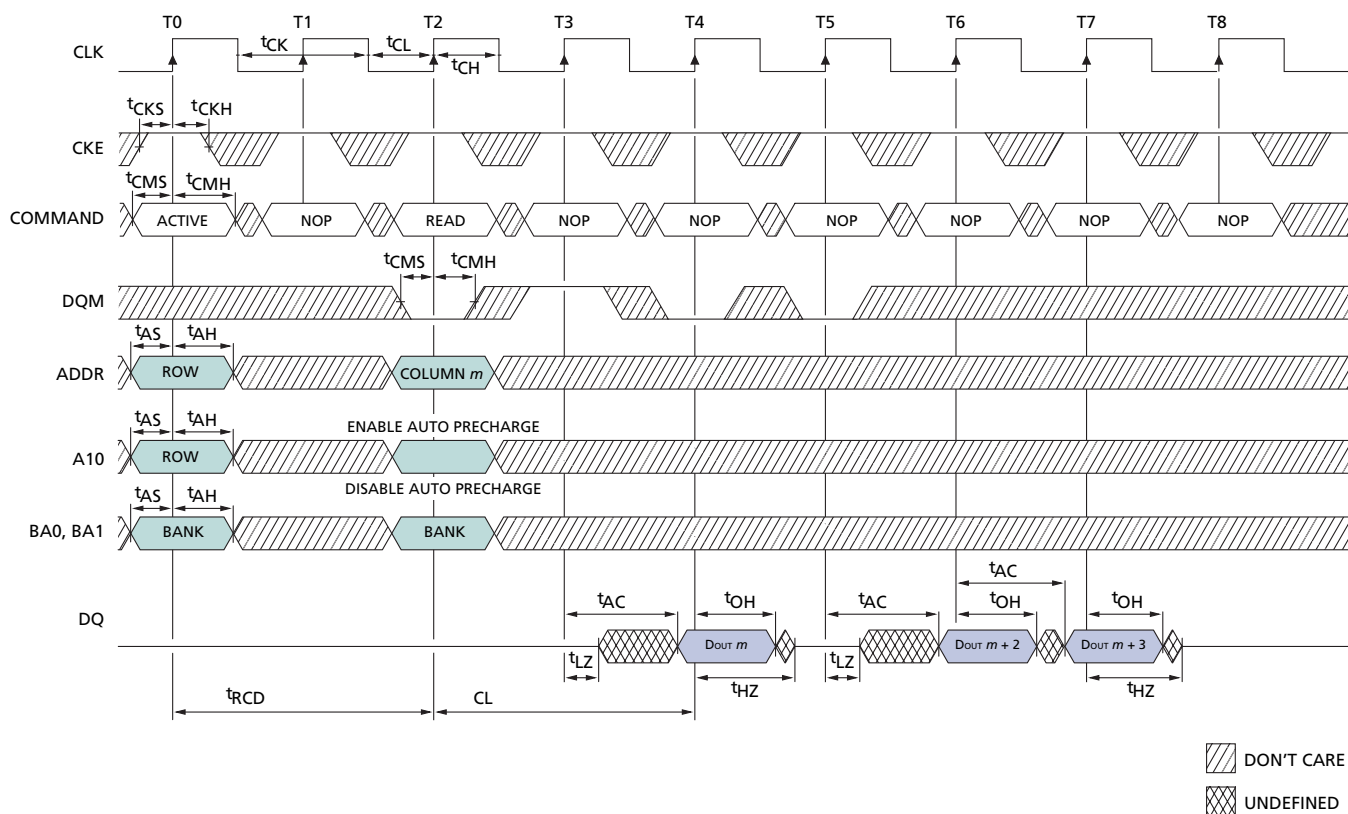
- Notes:
1. For this example, BL = 4, CL = 2, and the READ burst is followed by a manual PRECHARGE.
  2. PRECHARGE command not allowed or  $t_{RAS}$  would be violated.
- See Table 11 on page 46.

**Figure 43: Alternating Bank Read Accesses**



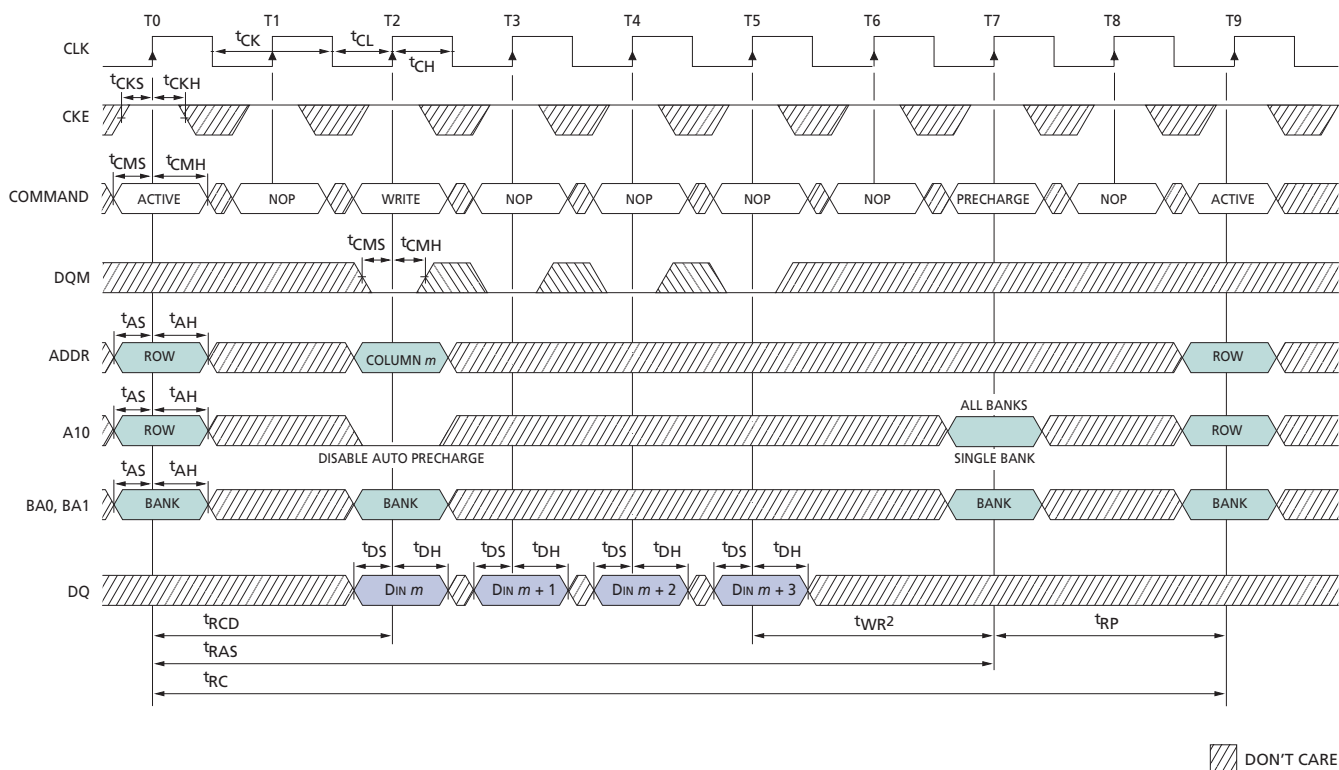
Notes: 1. For this example, BL = 4, CL = 2.

**Figure 44: READ – DQM Operation**



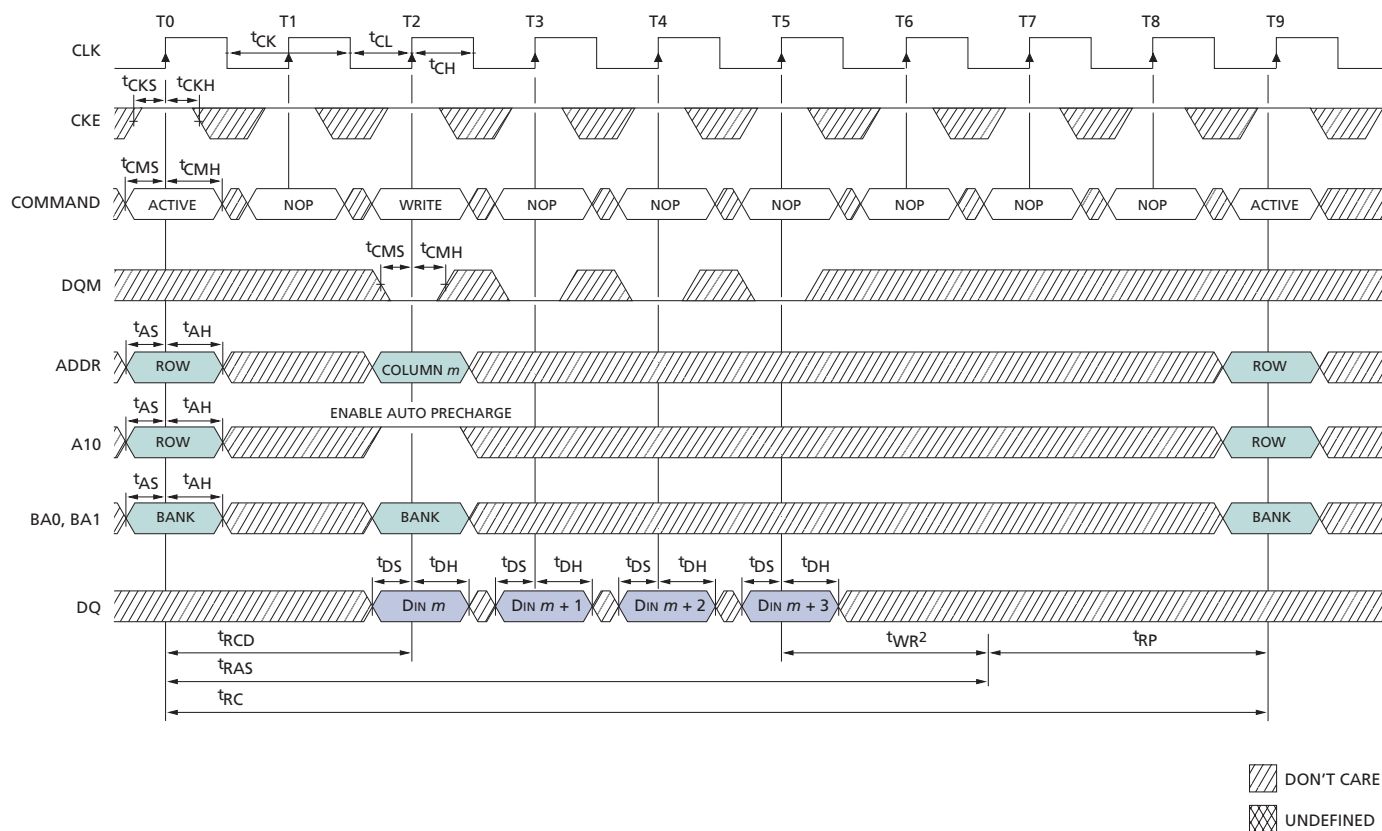
Notes: 1. For this example, CL = 2.

**Figure 45: WRITE – without Auto Precharge**



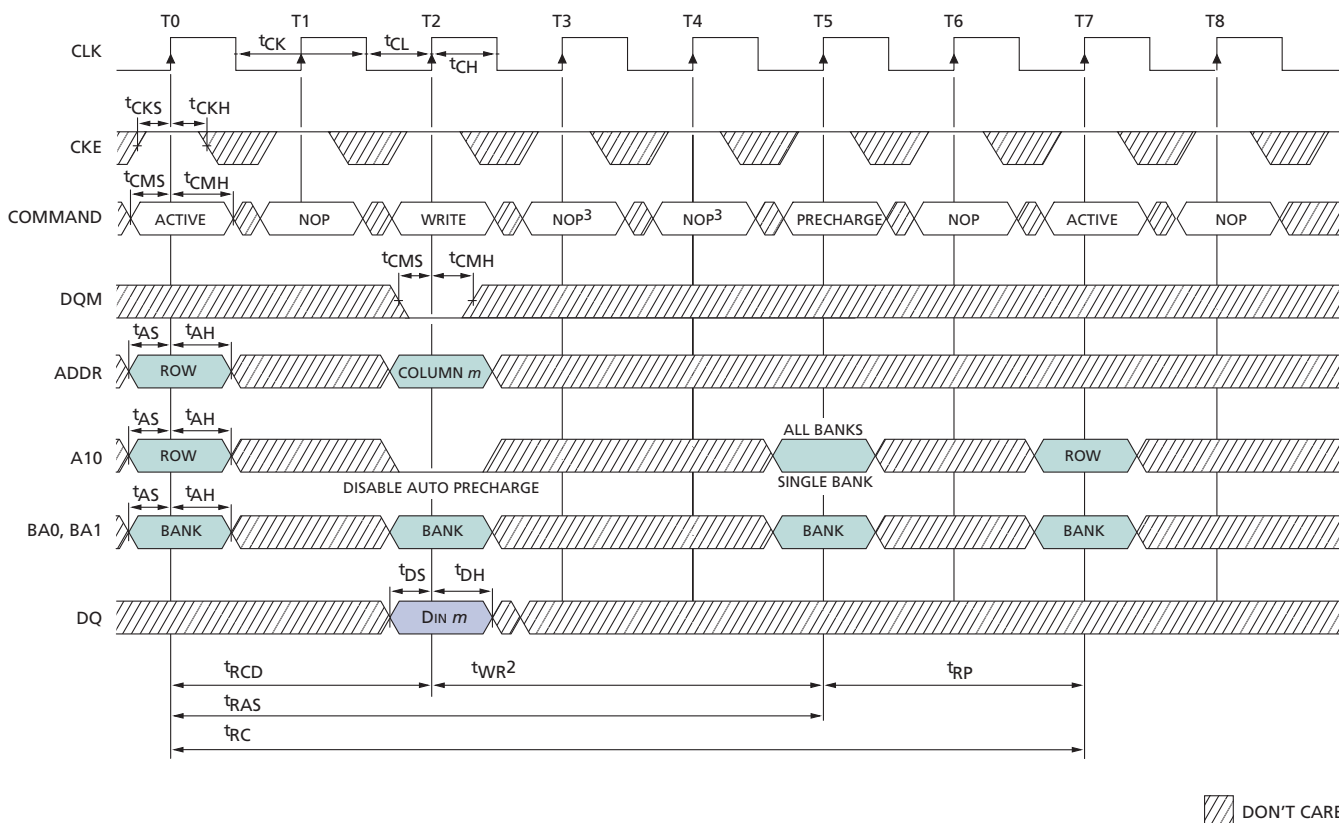
- Notes:
1. For this example, BL = 4, and the WRITE burst is followed by a manual PRECHARGE.
  2. 15ns is required between <DIN m + 3> and the PRECHARGE command, regardless of frequency.

**Figure 46: WRITE – with Auto Precharge**



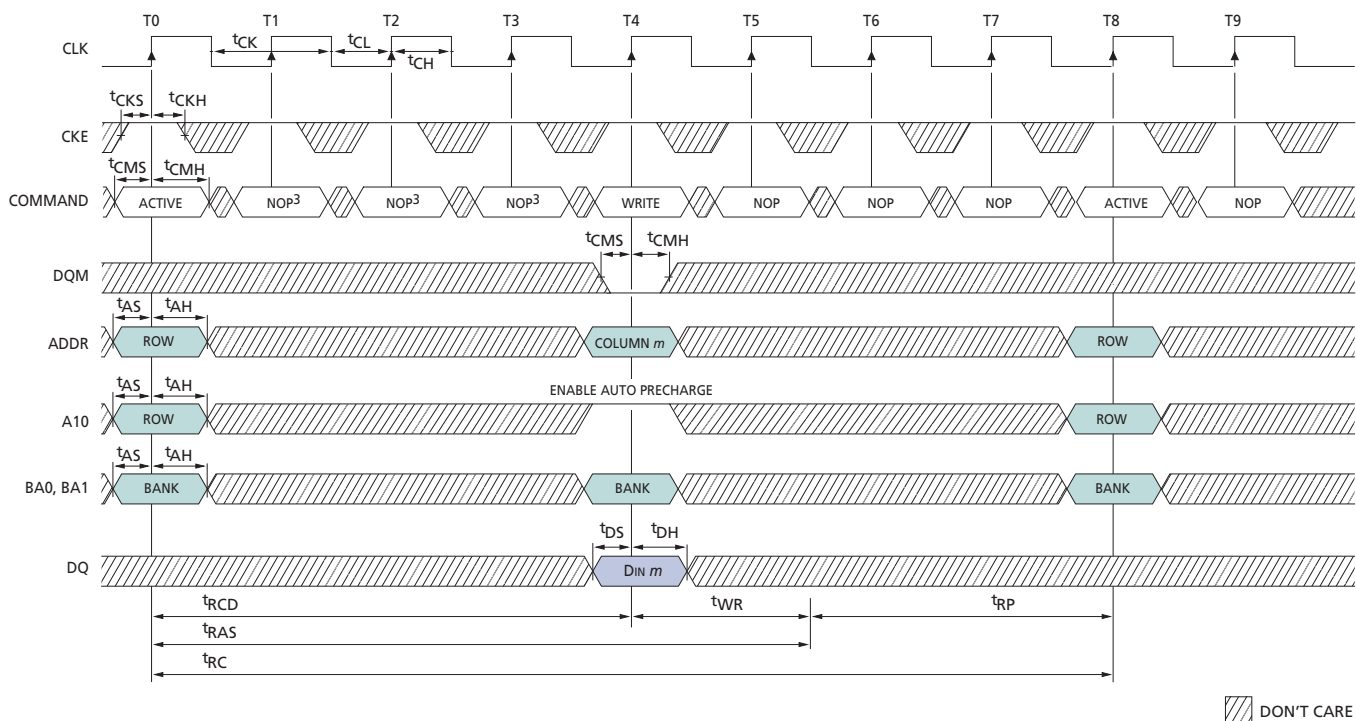
Notes: 1. For this example, BL = 4.

**Figure 47: Single WRITE – without Auto Precharge**



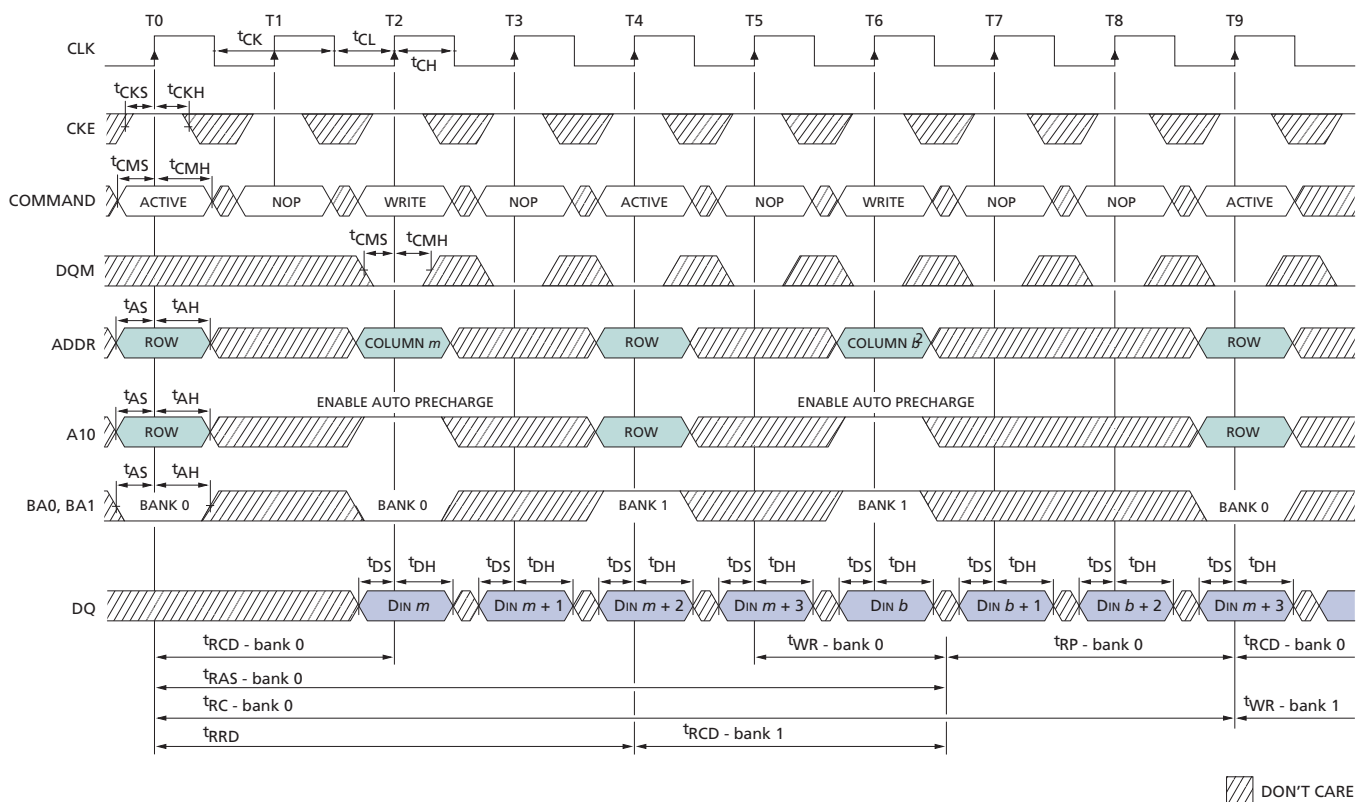
- Notes:
1. For this example, BL = 1, and the WRITE burst is followed by a manual PRECHARGE.
  2. 15ns is required between <DIN m> and the PRECHARGE command, regardless of frequency.
  3. PRECHARGE command not allowed or tRAS would be violated. See Table 11 on page 46.

**Figure 48: Single WRITE – with Auto Precharge**



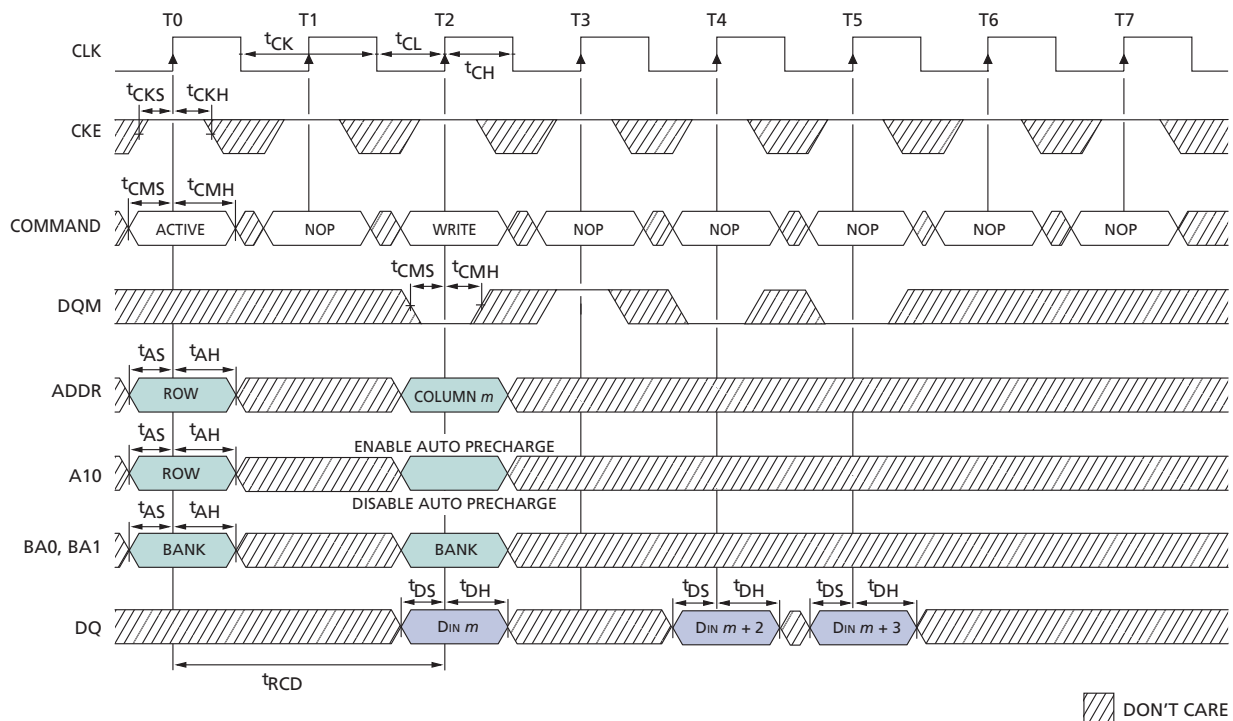
- Notes:
1. For this example, BL = 1, and the WRITE burst is followed by a manual PRECHARGE.
  2. 15ns is required between <DIN m> and the PRECHARGE command, regardless of frequency.
  3. WRITE command not allowed or  $t_{RAS}$  would be violated.  
See Table 11 on page 46.

**Figure 49: Alternating Bank Write Accesses**



Notes: 1. For this example, BL = 4.

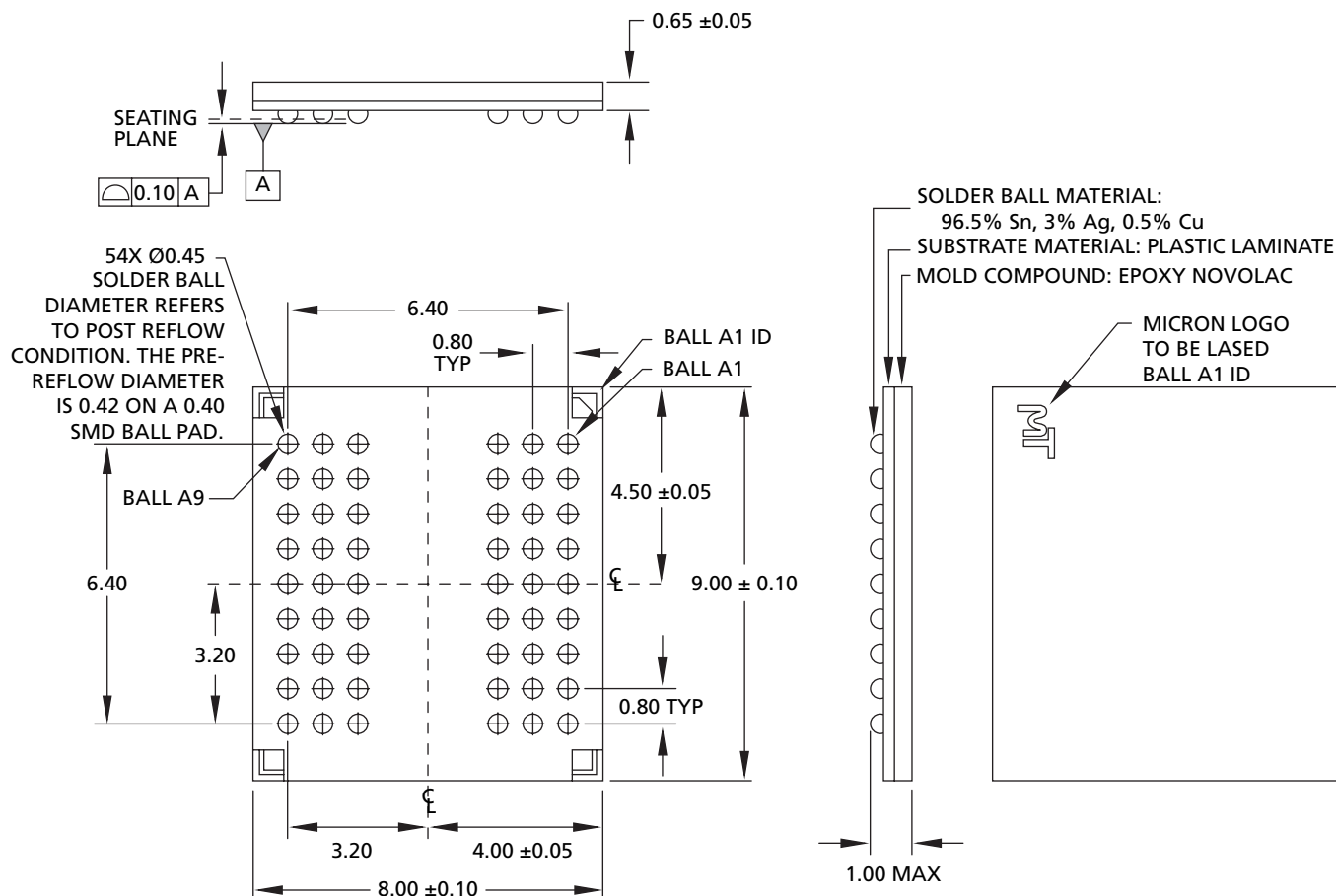
**Figure 50: WRITE – DQM Operation**



Notes: 1. For this example, BL = 4.

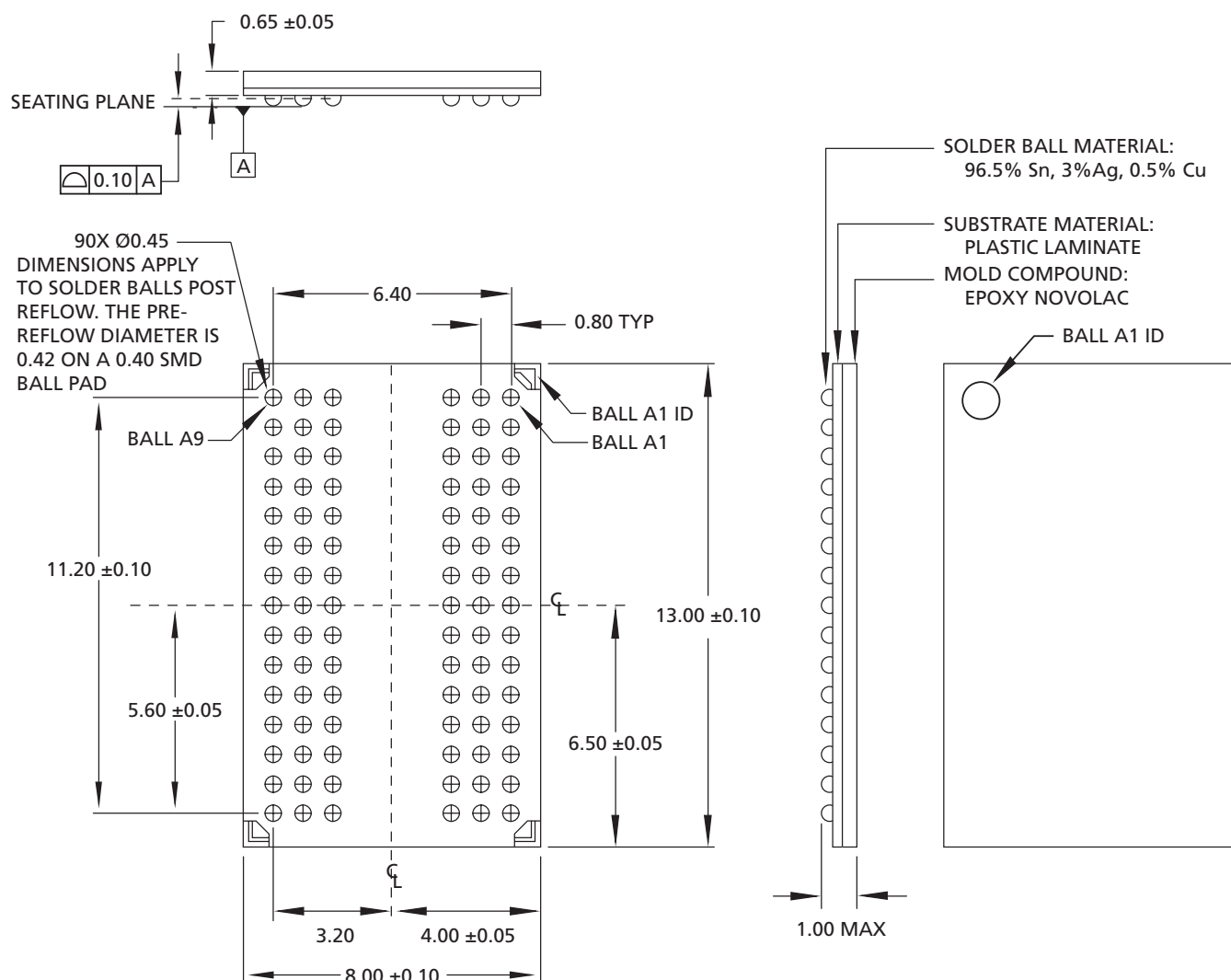
## Package Dimensions

**Figure 51: 54-Ball VFBGA (8mm x 9mm)**



Notes: 1. All dimensions are in millimeters.

**Figure 52: 90-Ball VFBGA (8mm x 13mm)**



Notes: 1. All dimensions are in millimeters.



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