



**16 MEG: x4, x8  
SDRAM**

# SYNCHRONOUS DRAM

**MT48LC4M4A1/A2 S - 2 Meg x 4 x 2 banks**  
**MT48LC2M8A1/A2 S - 1 Meg x 8 x 2 banks**

For the latest data sheet revisions, please refer to the  
Micron Web site: [www.micron.com/datasheets](http://www.micron.com/datasheets).

## FEATURES

- PC100-compliant; includes CONCURRENT AUTO PRECHARGE
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode
- 64ms, 4,096-cycle refresh
- LVTTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply
- Longer lead TSOP for improved reliability (OCPL\*)
- One- and two-clock WRITE recovery (<sup>t</sup>WR) versions

## OPTIONS

- Configurations
 

4 Meg x 4 (2 Meg x 4 x 2 banks)	4M4
2 Meg x 8 (1 Meg x 8 x 2 banks)	2M8
- WRITE Recovery (<sup>t</sup>WR/<sup>t</sup>DPL)
 

<sup>t</sup> WR = 1 CLK	A1
<sup>t</sup> WR = 2 CLK (Contact factory for availability.)	A2
- Plastic Package - OCPL\*
 

44-pin TSOP (400 mil)	TG
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- Timing (Cycle Time)
 

8ns; <sup>t</sup> AC = 6ns @ CL = 3	-8B
10ns; <sup>t</sup> AC = 9ns @ CL = 2	-10

## MARKING

**NOTE:** The 16Mb SDRAM base number differentiates the offerings in two places: MT48LC2M8A1 S. The fourth field distinguishes the architecture offering: 4M4 designates 4 Meg x 4, and 2M8 designates 2 Meg x 8. The fifth field distinguishes the WRITE recovery offering: A1 designates one CLK and A2 designates two CLKs.

Part Number Example:

**MT48LC2M8A1TG-10 S**

## 16Mb (x4/x8) SDRAM PART NUMBERS

PART NUMBER	ARCHITECTURE
MT48LC4M4A1TG S	4 Meg x 4 ( <sup>t</sup> WR = 1 CLK)
MT48LC2M8A1TG S	2 Meg x 8 ( <sup>t</sup> WR = 1 CLK)

## PIN ASSIGNMENT (Top View)

### 44-Pin TSOP

x4	x8			x8	x4
-	VDD	1		44	VSS
NC	DQ0	2		43	DQ7
-	VSSQ	3		42	VSSQ
DQ0	DQ1	4		41	DQ6
-	VDDQ	5		40	VDDQ
NC	DQ2	6		39	DQ5
-	VSSQ	7		38	VSSQ
DQ1	DQ3	8		37	DQ4
-	VDDQ	9		36	VDDQ
-	NC	10		35	NC
-	NC	11		34	NC
-	WE#	12		33	DQM
-	CAS#	13		32	CLK
-	RAS#	14		31	CKE
-	CS#	15		30	NC
-	BA	16		29	A9
-	A10	17		28	A8
-	A0	18		27	A7
-	A1	19		26	A6
-	A2	20		25	A5
-	A3	21		24	A4
-	VDD	22		23	VSS

**NOTE:** The # symbol indicates signal is active LOW. A dash (-) indicates x4 pin function is same as x8 pin function.

	4 MEG x 4	2 MEG x 8
Configuration	2 Meg x 4 x 2 banks	1 Meg x 8 x 2 banks
Refresh Count	4K	4K
Row Addressing	2K (A0-A10)	2K (A0-A10)
Bank Addressing	2 (BA)	1 (BA)
Column Addressing	1K (A0-A9)	512 (A0-A8)

## KEY TIMING PARAMETERS

SPEED GRADE	CLOCK FREQUENCY	ACCESS TIME		SETUP TIME	HOLD TIME
		CL = 2**	CL = 3**		
-8B	125 MHz	-	6ns	2ns	1ns
-10	100 MHz	-	7.5ns	3ns	1ns
-8B	83 MHz	9ns	-	2ns	1ns
-10	66 MHz	9ns	-	3ns	1ns

\* Off-center parting line

\*\*CL = CAS (READ) latency

## GENERAL DESCRIPTION

The Micron 16Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 16,777,216 bits. It is internally configured as a dual memory array (the 4 Meg x 4 is a dual 2 Meg x 4, and the 2 Meg x 8 is a dual 1 Meg x 8) with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the two internal banks is organized with 2,048 rows and either 1,024 columns by 4 bits (4 Meg x 4) or 512 columns by 8 bits (2 Meg x 8).

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA selects the bank, A0-A10 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable READ or WRITE burst lengths of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option. An auto precharge

function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The Micron 16Mb SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the  $2n$  rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing the alternate bank will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

The Micron 16Mb SDRAM is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTTL-compatible.

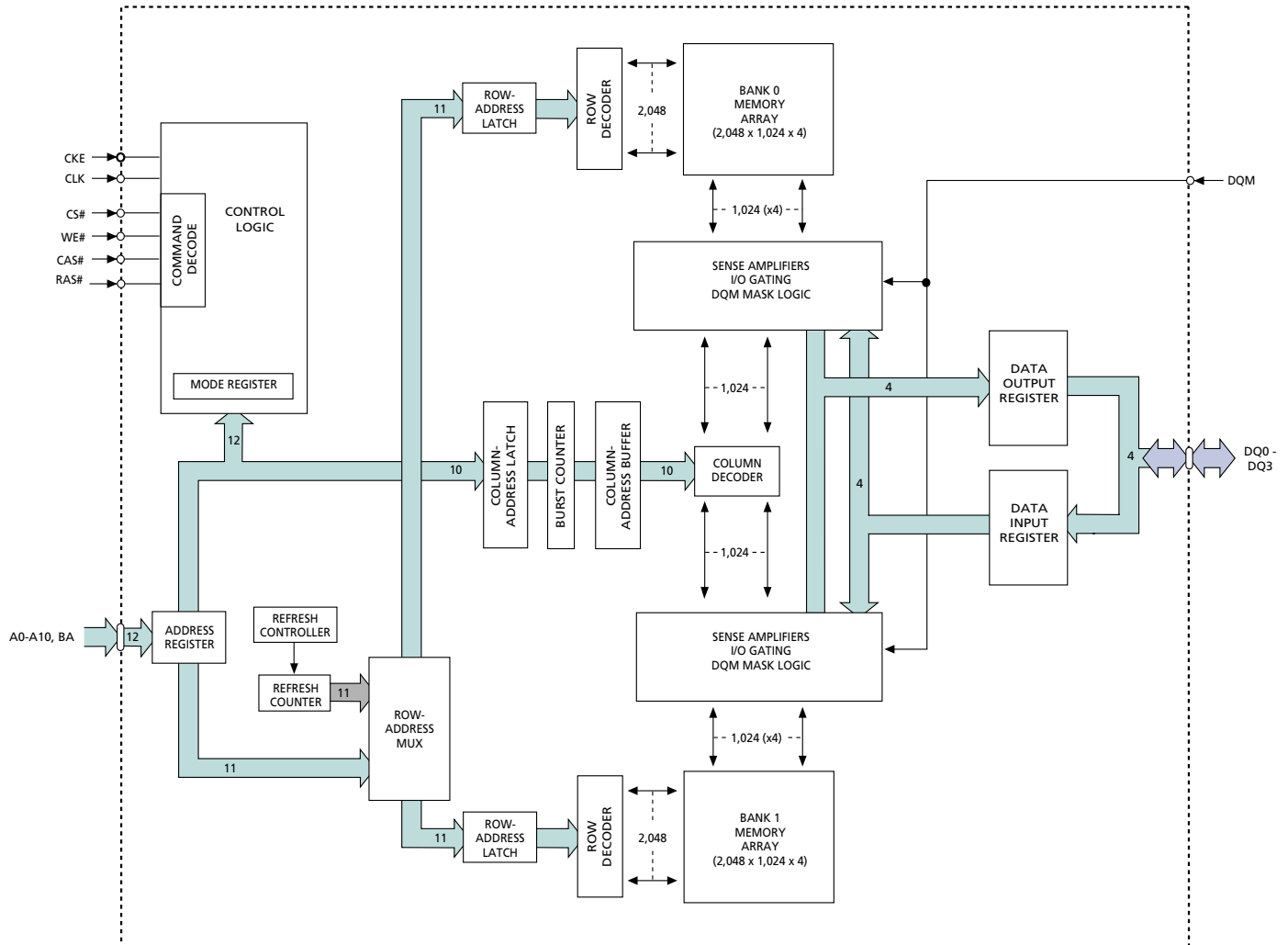
SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

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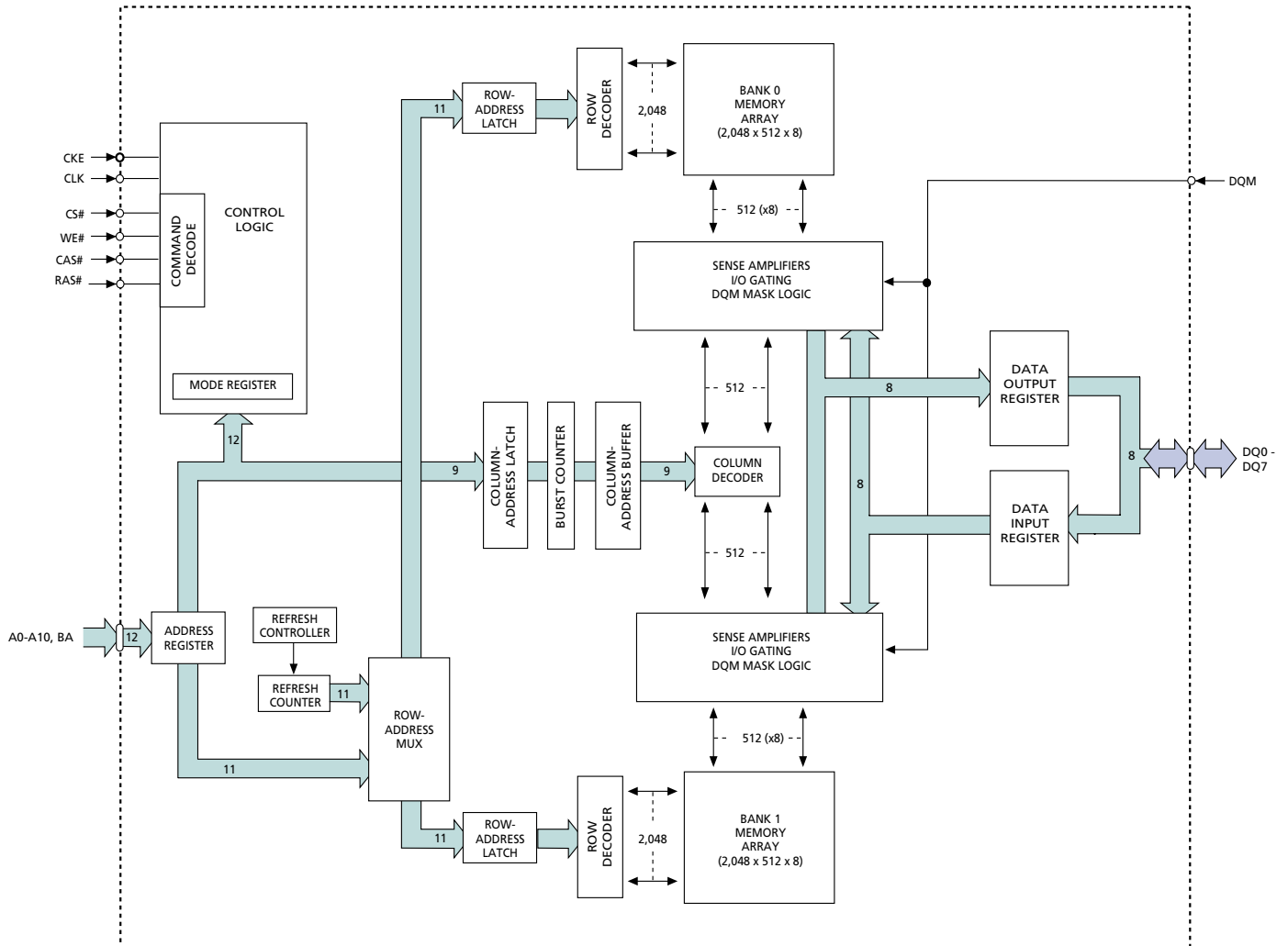
## FUNCTIONAL BLOCK DIAGRAM

### 4 Meg x 4 SDRAM



## FUNCTIONAL BLOCK DIAGRAM

### 2 Meg x 8 SDRAM



## PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
32	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
31	CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), ACTIVE POWER-DOWN (row active in either bank), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
15	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
14, 13, 12	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
33	DQM	Input	Input/Output Mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (after a two-clock latency) when DQM is sampled HIGH during a READ cycle.
16	BA	Input	Bank Address: BA defines to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA is also used to program the twelfth bit of the Mode Register.
18-21, 24-29, 17	A0-A10	Input	Address Inputs: A0-A10 are sampled during the ACTIVE command (row-address A0-A10) and READ/WRITE command (column-address A0-A9 [x4]; A0-A8 [x8], with A9 as a "Don't Care;" and with A10 defining AUTO PRECHARGE) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if both banks are to be precharged (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
4, 8, 37, 41	x4: DQ0, 1, 2, 3 x8: DQ1, 3, 4, 6	Input	Data I/O: Data bus.
2, 6, 39, 43	x4: NC	–	No Connect: These pins should be left unconnected.
	x8: DQ0, 2, 5, 7	Input	Data I/O: Data bus.
10, 11, 30, 34, 35	NC	–	No Connect: These pins should be left unconnected.
5, 9, 36, 40	V <sub>DD</sub> Q	Supply	DQ Power.
3, 7, 38, 42	V <sub>SS</sub> Q	Supply	DQ Ground.
1, 22	V <sub>DD</sub>	Supply	Power Supply: +3.3V ±0.3V.
23, 44	V <sub>SS</sub>	Supply	Ground.

## FUNCTIONAL DESCRIPTION

In general, the SDRAM is a dual memory array (the 4 Meg x 4 is a dual 2 Meg x 4, and the 2 Meg x 8 is a dual 1 Meg x 8) which operates at 3.3V and includes a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the two internal banks is organized with 2,048 rows and either 1,024 columns by 4 bits (4 Meg x 4) or 512 columns by 8 bits (2 Meg x 8).

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA selects the bank, A0-A10 select the row). The address bits (A0-A9; A9 is a "Don't Care" for x8) registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

### Initialization

SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Once power is applied to V<sub>DD</sub> and V<sub>DDQ</sub> (simultaneously) and the clock is stable, the SDRAM requires a 100µs delay prior to applying an executable command. The RAS#, CAS#, WE# and CS# inputs should be held HIGH during this phase of power-up.

Once the 100µs delay has been satisfied, CKE HIGH and the PRECHARGE command can be applied (set up and held with respect to a positive edge of CLK). Both banks must then be precharged, thereby placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for Mode Register programming. Because the Mode Register will power up in an unknown state, it should be loaded prior to applying any operational command.

### Register Definition

#### MODE REGISTER

The Mode Register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, an

operating mode, and a write burst mode, as shown in Figure 1. The Mode Register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode Register bits M0-M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4-M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the write burst mode, and M10 and M11 are reserved for future use.

The Mode Register must be loaded when both banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

#### Burst Length

Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 1. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4 or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

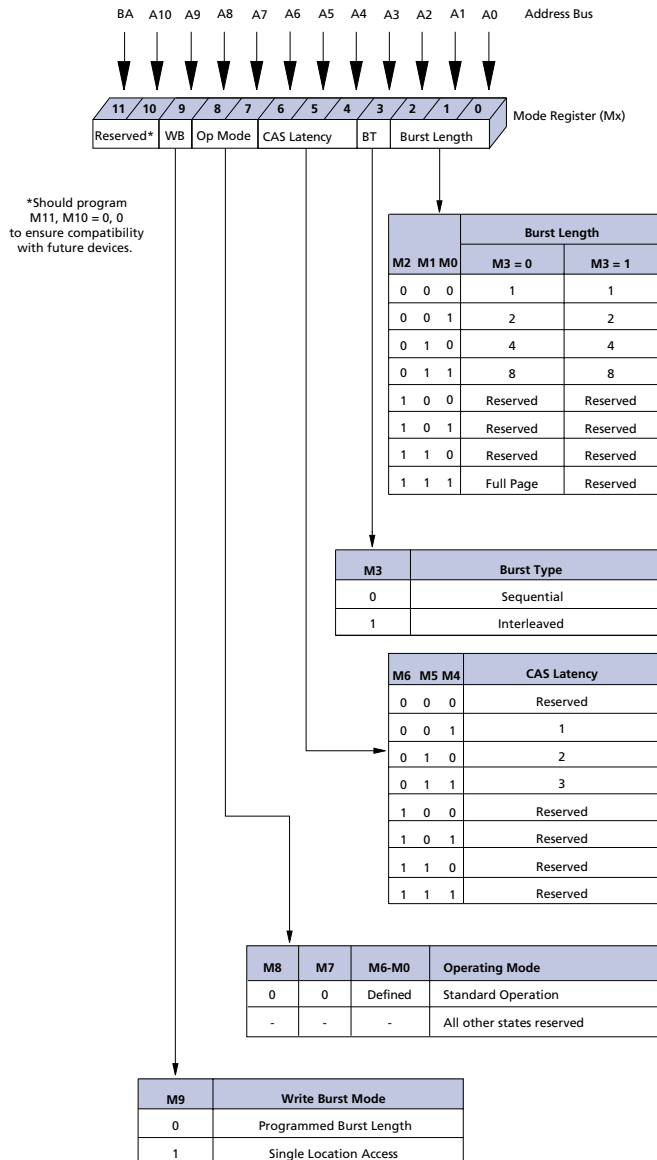
When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-A9 (A9 is "Don't Care" for x8) when the burst length is set to two; by A2-A9 (A9 is "Don't Care" for x8) when the burst length is set to four; and by A3-A9 (A9 is "Don't Care" for x8) when the burst length is set to eight. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached.

#### Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 1.

**Figure 1  
Mode Register Definition**



**Table 1  
Burst Definition**

Burst Length	Starting Column Address:	Order of Accesses Within a Burst	
		Type = Sequential	Type = Interleaved
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (x4: 1,024) (x8: 512)	x4: n = A0-A9 x8: n = A0-A8 (location 0-1,023) (location 0-511)	Cn, Cn+1, Cn+2 Cn+3, Cn+4... ...Cn-1, Cn...	Not supported

- NOTE:**
- For a burst length of two, A1-A9 select the block of two burst (A9 is a "Don't Care" for x8); A0 selects the starting column within the block.
  - For a burst length of four, A2-A9 select the block of four burst (A9 is a "Don't Care" for x8); A0-A1 select the starting column within the block.
  - For a burst length of eight, A3-A9 select the block of eight burst (A9 is a "Don't Care" for x8); A0-A2 select the starting column within the block.
  - For a full-page burst, the full row is selected and A0-A9 select the starting column (A9 is a "Don't Care" for x8).
  - Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
  - For a burst length of one, A0-A9 select the unique column to be accessed (A9 is a "Don't Care" for x8), and Mode Register bit M3 is ignored.

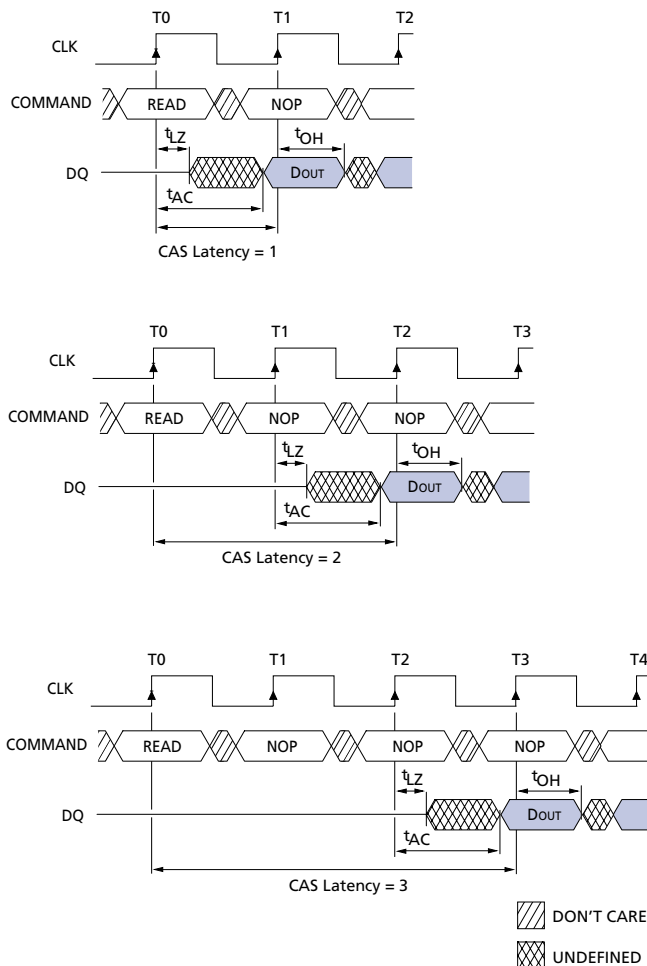


### CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to 1, 2, or 3 clocks.

If a READ command is registered at clock edge  $n$ , and the latency is  $m$  clocks, the data will be available by clock edge  $n + m$ . The DQs will start driving as a result of the clock edge one cycle earlier ( $n + m - 1$ ) and, provided that the relevant access times are met, the data will be valid by clock edge  $n + m$ . For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at  $T_0$ , and the latency is programmed to two clocks, the DQs will start driving after  $T_1$  and the data will be valid by  $T_2$ , as shown in Figure 2. Table 2 below indicates the operating frequencies at which each CAS latency setting can be used.

**Figure 2  
CAS LATENCY**



Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

### Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both READ and WRITE bursts.

Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

### Write Burst Mode

When M9 = 0, the burst length programmed via M0-M2 applies to both READ and WRITE bursts; when M9 = 1, the programmed burst length applies to READ bursts, but write accesses are single-location (nonburst) accesses.

**Table 2  
CAS LATENCY**

SPEED	ALLOWABLE OPERATING FREQUENCY (MHz)		
	CAS LATENCY = 1	CAS LATENCY = 2	CAS LATENCY = 3
-8D/E	≤ 33	≤ 100	≤ 125
-8A/B/C	≤ 33	≤ 83	≤ 125
-10	≤ 33	≤ 66	≤ 100

## COMMANDS

Truth Table 1 provides a quick reference of available commands. This is followed by a written description of each command. Two additional Truth Tables appear

following the Operation section; these tables provide current state/next state information.

### TRUTH TABLE 1 – Commands and DQM Operation

(Note: 1)

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	DQM	ADDR	DQs	NOTES
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	3
READ (Select bank and column and start READ burst)	L	H	L	H	X	Bank/Col	X	4
WRITE (Select bank and column and start WRITE burst)	L	H	L	L	X	Bank/Col	Valid	4
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op-code	X	2
Write Enable/Output Enable	–	–	–	–	L	–	Active	8
Write Inhibit/Output High-Z	–	–	–	–	H	–	High-Z	8

- NOTE:**
1. CKE is HIGH for all commands shown except SELF REFRESH.
  2. A0-A10 and BA define the op-code written to the Mode Register.
  3. A0-A10 provide row address, and BA determines which bank is made active (BA LOW = Bank 0; BA HIGH = Bank 1).
  4. A0-A9 (A9 is a "Don't Care" for x8) provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA determines which bank is being read from or written to (BA LOW = Bank 0; BA HIGH = Bank 1).
  5. For A10 LOW, BA determines which bank is being precharged (BA LOW = Bank 0; BA HIGH = Bank 1); for A10 HIGH, both banks are precharged and BA is a "Don't Care."
  6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
  7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
  8. Activates or deactivates the DQs during WRITES (zero-clock delay) and READs (two-clock delay).

## COMMAND INHIBIT

The COMMAND INHIBIT function prevents new commands from being executed by the SDRAM, regardless of whether the CLK signal is enabled. The SDRAM is effectively deactivated, or deselected.

## NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to perform a NOP to an SDRAM which is selected (CS# is LOW). This prevents unwanted commands from being registered during idle or wait states.

## LOAD MODE REGISTER

The Mode Register is loaded via inputs A0-A10 and BA. See Mode Register heading in Register Definition section. The LOAD MODE REGISTER command can only be issued when both banks are idle, and a subsequent executable command cannot be issued until <sup>t</sup>MRD is met.

## ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA input selects the bank, and the address provided on inputs A0-A10 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

## READ

The READ command is used to initiate a burst read access to an active row. The value on the BA input selects the bank, and the address provided on inputs A0-A9 (A9 is a “Don’t Care” on x8) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Read data appears on the DQs, subject to the logic level on the DQM input, two clocks earlier. If the DQM signal was registered HIGH, the DQs will be High-Z two clocks later; if the DQM signal was registered LOW, the DQs will provide valid data.

## WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA input selects the bank, and the address provided on inputs A0-A9 (A9 is a “Don’t Care” on x8) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected,

the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DQM input logic level appearing coincident with the data. If the DQM signal is registered LOW, the corresponding data will be written to memory; if the DQM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that location.

## PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in both banks. The bank(s) will be available for a subsequent row access some specified time (<sup>t</sup>RP) after the PRECHARGE command is issued. Input A10 determines whether one or both banks are to be precharged, and in the case where only one bank is to be precharged, input BA selects the bank. Otherwise BA is treated as a “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

## AUTO PRECHARGE

Auto precharge is a feature which performs the same individual-bank PRECHARGE function described above, without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A PRECHARGE of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst, except in the full-page burst mode, where auto precharge does not apply. Auto precharge is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command.

Auto precharge ensures that the PRECHARGE is initiated at the earliest valid stage within a burst. The user must not issue another command until the precharge time (<sup>t</sup>RP) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in the Operation section of this data sheet.

## BURST TERMINATE

The BURST TERMINATE command is used to truncate either fixed-length or full-page bursts. The most recently registered READ or WRITE command prior to the BURST TERMINATE command will be truncated, as shown in the Operation section of this data sheet.

**AUTO REFRESH**

AUTO REFRESH is used during normal operation of the SDRAM and is analagous to CAS#-BEFORE-RAS# (CBR) REFRESH in conventional DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required.

The addressing is generated by the internal refresh controller. This makes the address bits “Don’t Care” during an AUTO REFRESH command. The Micron 16Mb SDRAM requires all of its 4,096 rows to be refreshed every 64ms ( $t_{REF}$ ). Providing a distributed AUTO REFRESH command every 15.6 $\mu$ s will meet the refresh requirement and ensure that each row is refreshed. Alternatively, all 4,096 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate ( $t_{RC}$ ) once every 64ms.

**SELF REFRESH**

The SELF REFRESH command can be used to retain data in the SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the SDRAM retains data without external clocking. The SELF RE-

FRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). Once the SELF REFRESH command is registered, all the inputs to the SDRAM become “Don’t Care,” with the exception of CKE, which must remain LOW.

Once self refresh mode is engaged, the SDRAM provides its own internal clocking, causing it to perform its own AUTO REFRESH cycles. The SDRAM must remain in self refresh mode for a minimum period equal to  $t_{RAS}$  and may remain in self refresh mode for an indefinite period beyond that.

The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable prior to CKE going back HIGH. Once CKE is HIGH, the SDRAM must have NOP commands issued (a minimum of two clocks) for  $t_{XSR}$  because time is required for the completion of any internal refresh in progress.

A burst of 4,096 AUTO REFRESH cycles should be completed just prior to entering and just after exiting the self refresh mode.

## OPERATION

### BANK/ROW ACTIVATION

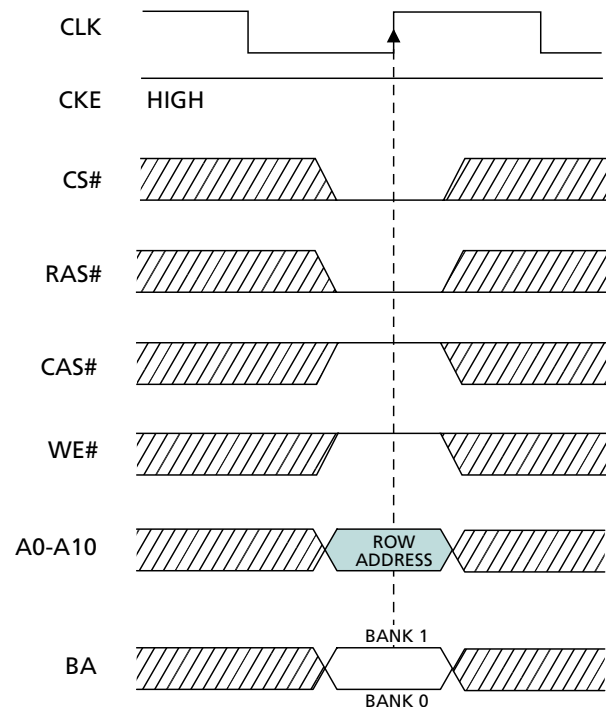
Before any READ or WRITE commands can be issued to a bank within the SDRAM, a row in that bank must be “opened.” This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated.

After opening a row (issuing an ACTIVE command), a READ or WRITE command may be issued to that row, subject to the  $t_{RCD}$  specification.  $t_{RCD}$  (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a  $t_{RCD}$  specification of 30ns with a 90 MHz clock (11.11ns period) results in 2.7 clocks, rounded to 3. This is reflected in Figure 4, which covers any case where  $2 < t_{RCD} \text{ (MIN)} / t_{CK} < 3$ . (The same procedure is used to convert other specification limits from time units to clock cycles.)

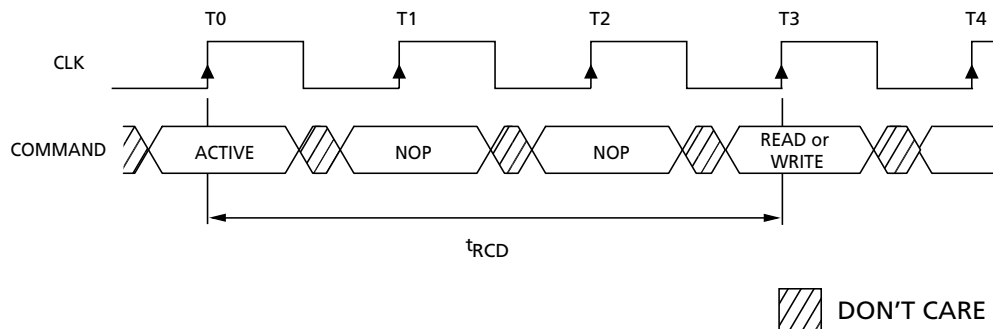
A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been “closed” (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by  $t_{RC}$ .

A subsequent ACTIVE command to the other bank can be issued while the first bank is being accessed, resulting in a reduction of total row access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by  $t_{RRD}$ .

**Figure 3**  
**Activating a Specific Row in a Specific Bank**



**Figure 4**  
**EXAMPLE: MEETING  $t_{RCD}$  (MIN) WHEN  $2 < t_{RCD} \text{ (MIN)} / t_{CK} < 3$**



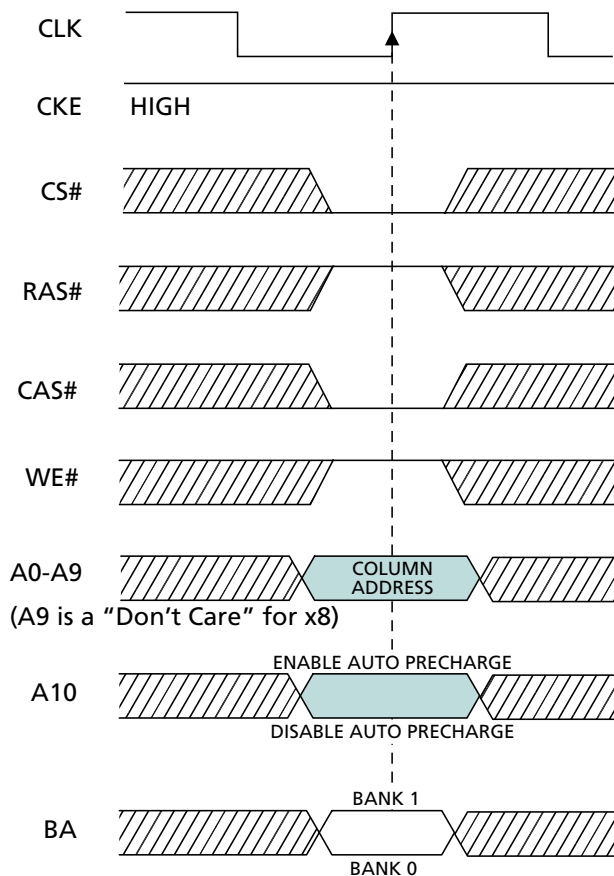
## READs

READ bursts are initiated with a READ command, as shown in Figure 5 (A9 is a "Don't Care" on x8).

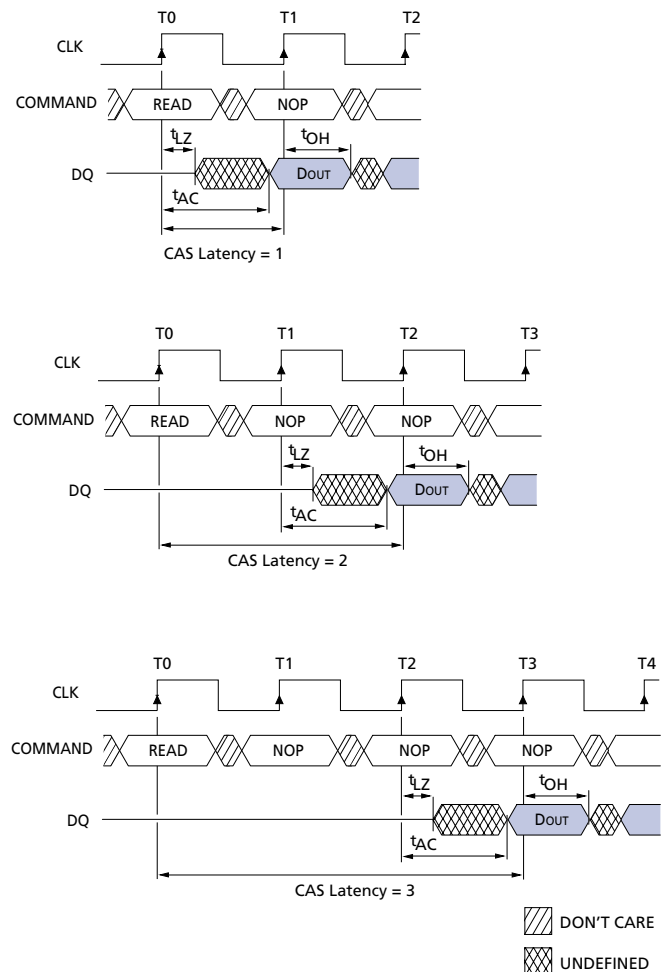
The starting column and bank addresses are provided with the READ command, and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic READ commands used in the following illustrations, auto precharge is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid by the next positive clock edge. Figure 6 shows general timing for each possible CAS latency setting.

**Figure 5  
READ Command**



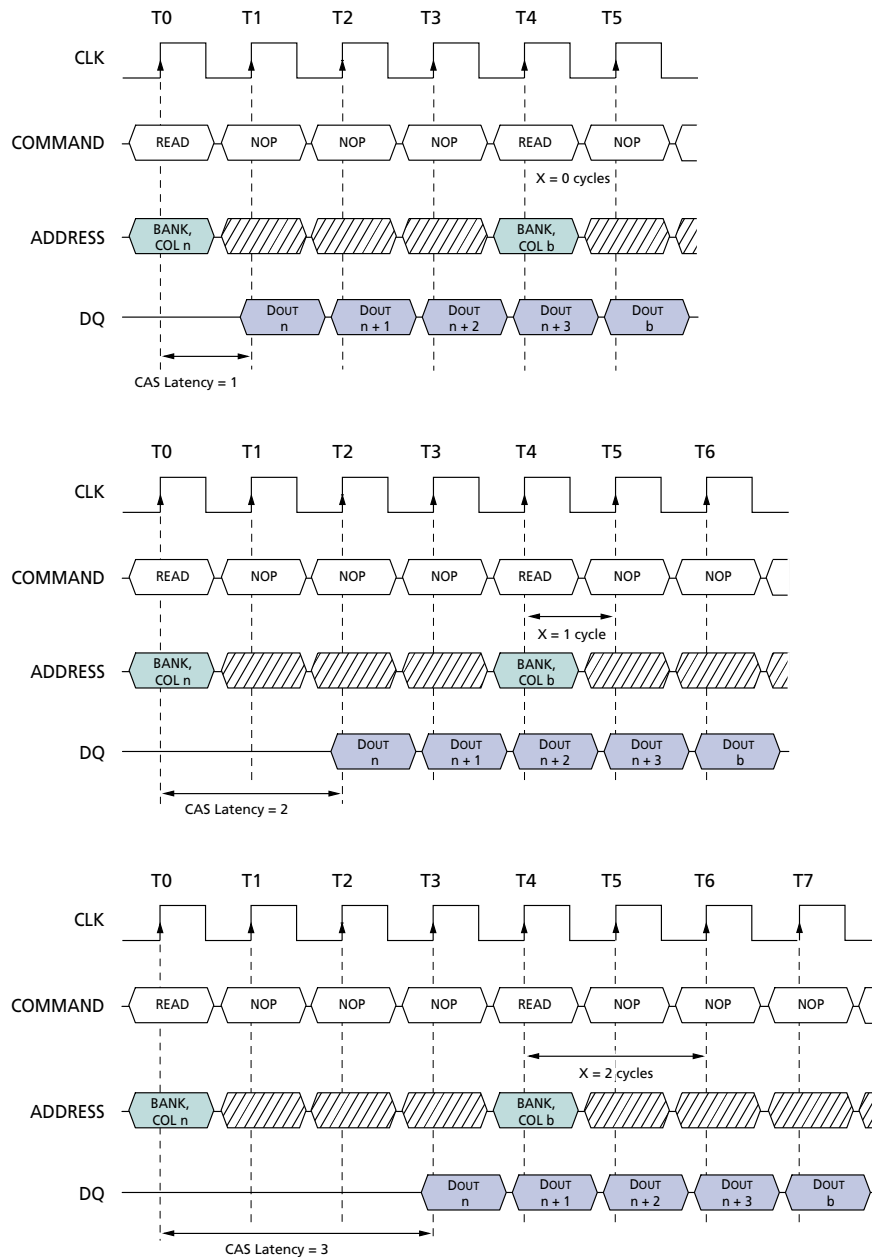
**Figure 6  
CAS Latency**



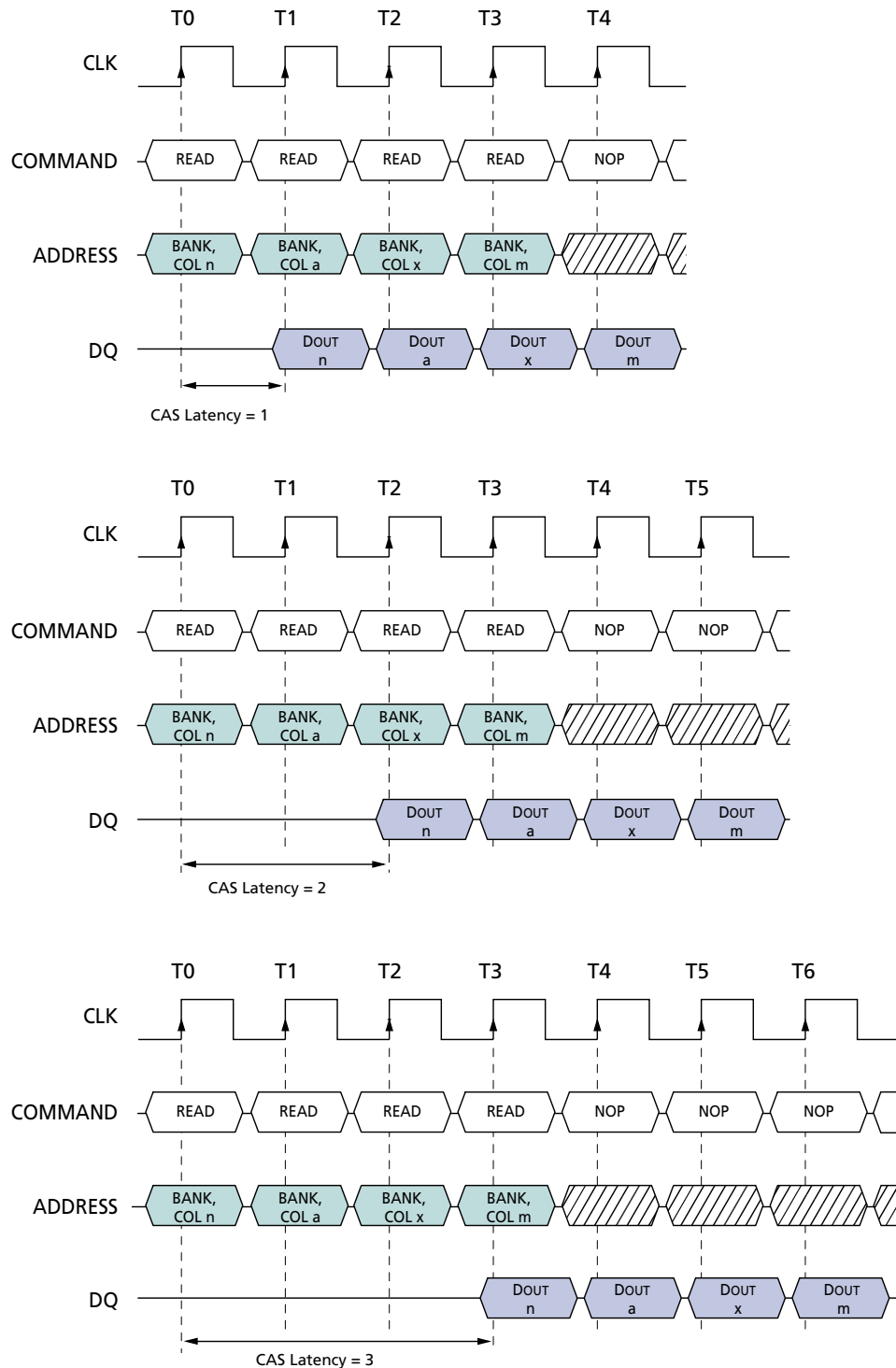
shown in Figure 7 for CAS latencies of one, two and three; data element  $n + 3$  is either the last of a burst of four or the last desired of a longer burst. The Micron 16Mb SDRAM uses a pipelined architecture and therefore does not require the  $2n$  rule associated with a prefetch architec-

ture. A READ command can be initiated on any clock cycle following a previous READ command. Full-speed random read accesses can be performed to the same bank, as shown in Figure 8, or each subsequent READ may be performed to a different bank.

**Figure 7**  
**Consecutive READ Bursts**



**Figure 8**  
**Random READ Accesses**



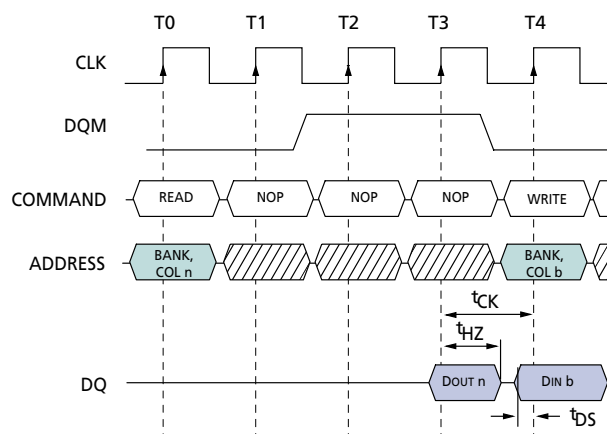


A fixed-length READ burst may be followed by, or truncated with, a WRITE burst (provided that AUTO PRECHARGE was not activated), and a full-page READ burst may be truncated by a WRITE burst. The WRITE burst may be initiated on the clock edge immediately following the last (or last desired) data element from the READ burst, provided that I/O contention can be avoided. In a given system design, there may be a possibility that the device driving the input data will go Low-Z before the SDRAM DQs go High-Z. In this case, a single-cycle delay should occur between the last read data and the WRITE command.

The DQM input is used to avoid I/O contention, as shown in Figures 9 and 10. The DQM signal must be

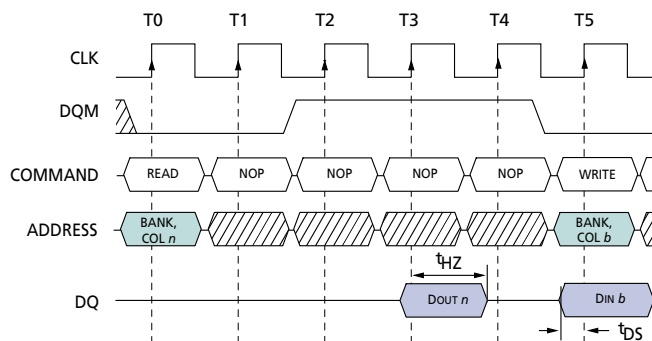
asserted (HIGH) at least two clocks prior to the WRITE command (DQM latency is two clocks for output buffers) to suppress data-out from the READ. Once the WRITE command is registered, the DQs will go High-Z (or remain High-Z) regardless of the state of the DQM signal. The DQM signal must be de-asserted prior to the WRITE command (DQM latency is zero clocks for input buffers) to ensure that the written data is not masked. Figure 9 shows the case where the clock frequency allows for bus contention to be avoided without adding a NOP cycle, and Figure 10 shows the case where the additional NOP is needed.

**Figure 9  
READ to WRITE**



**NOTE:** A CAS latency of three and a burst of two or more is used for illustration. The READ command may be to either bank, and the WRITE command may be to either bank. If a burst of one is used, then DQM is not required.

**Figure 10  
READ to WRITE with Extra Clock Cycle**



**NOTE:** A CAS latency of three is used for illustration. The READ command may be to either bank, and the WRITE command may be to either bank.

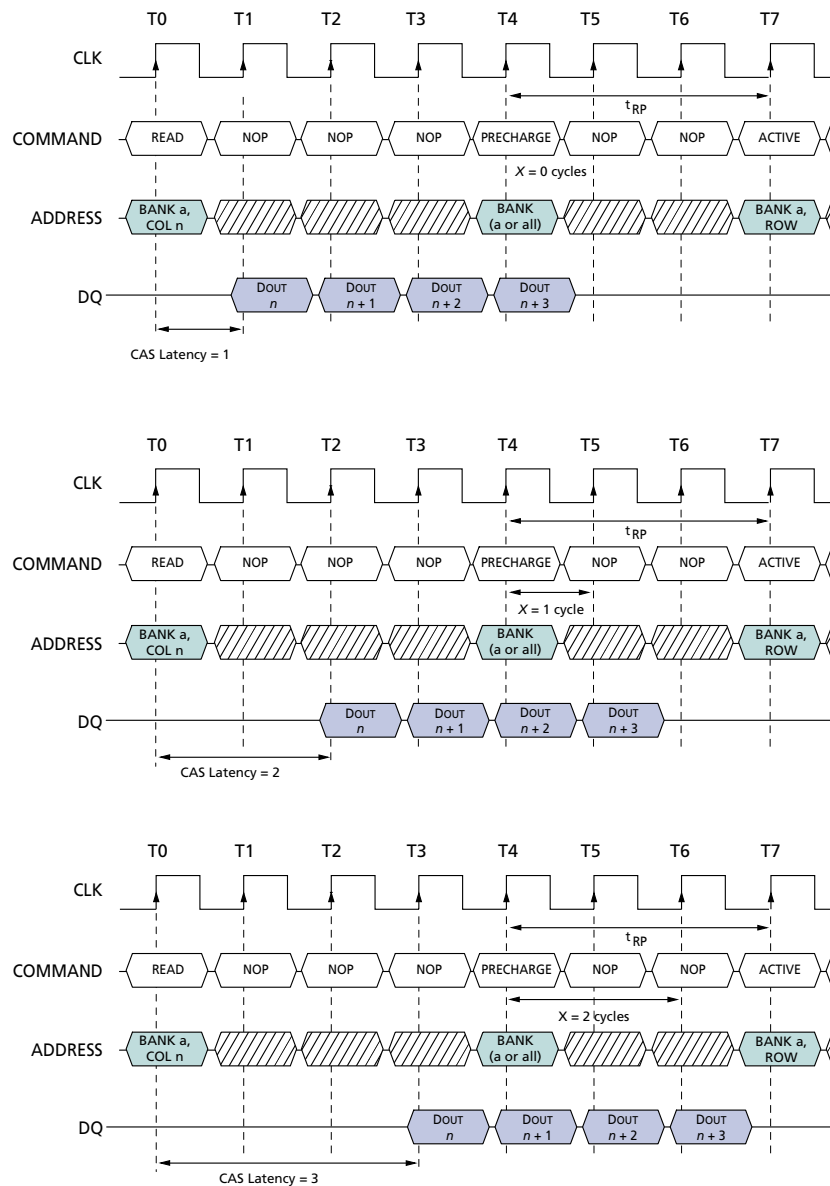
DON'T CARE

A fixed-length READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that auto precharge was not activated), and a full-page burst may be truncated with a PRECHARGE command to the same bank. The PRECHARGE command should be issued  $x$  cycles before the clock edge at which the last desired data element is valid, where  $x$  equals the CAS latency minus one. This is shown in Figure 11 for each possible CAS latency; data

element  $n+3$  is either the last of a burst of four or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until  $t_{RP}$  is met. Note that part of the row precharge time is hidden during the access of the last data element(s).

In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same op-

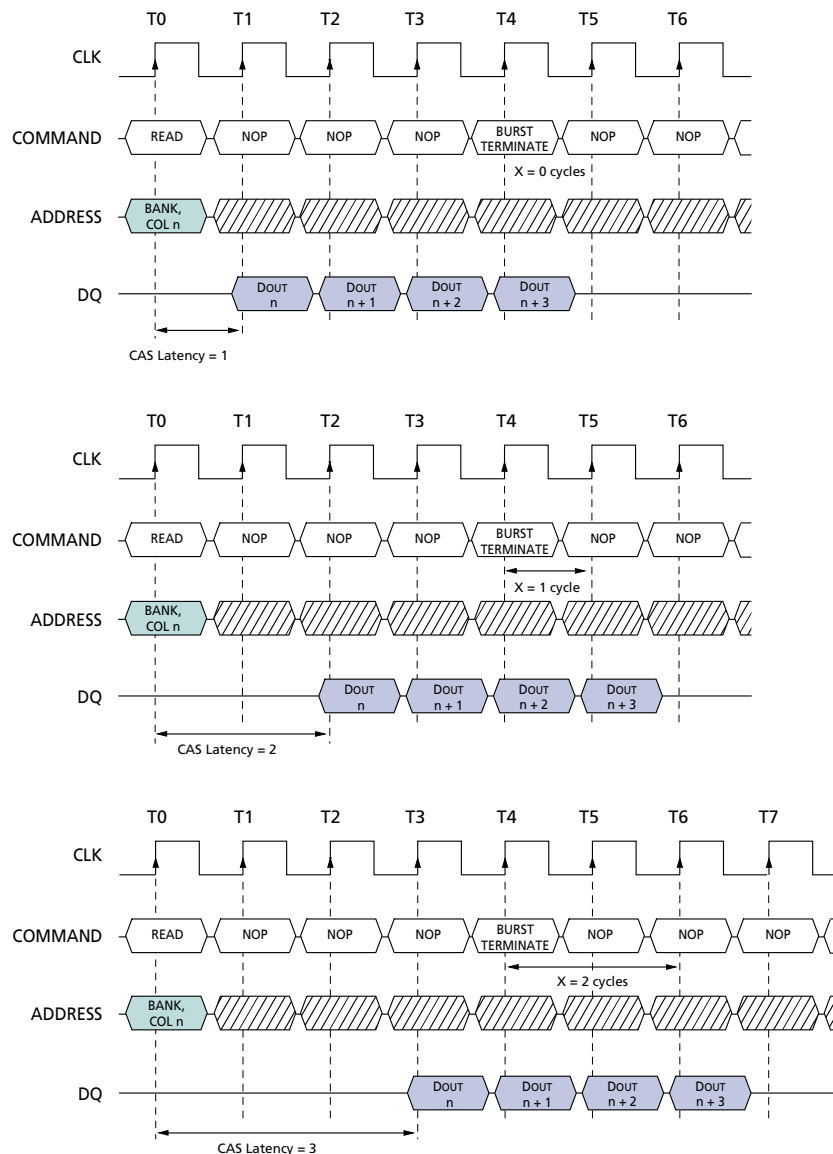
**Figure 11  
READ to PRECHARGE**



eration that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the PRECHARGE command is that it can be used to truncate fixed-length or full-page bursts. The auto precharge command does not truncate fixed-length bursts and does not apply to full-page bursts.

Full-page READ bursts can be truncated with the BURST TERMINATE command, and fixed-length READ bursts may be truncated with a BURST TERMINATE command, provided that auto precharge was not activated. The BURST TERMINATE command should be issued  $x$  cycles before the clock edge at which the last desired data element is valid, where  $x$  equals the CAS latency minus one. This is shown in Figure 12 for each possible CAS latency; data element  $n + 3$  is the last desired data element of a longer burst.

**Figure 12**  
**Terminating a READ Burst**



NOTE: DQM is LOW.

DON'T CARE

## WRITES

WRITE bursts are initiated with a WRITE command, as shown in Figure 13 (A9 is a "Don't Care" on x8).

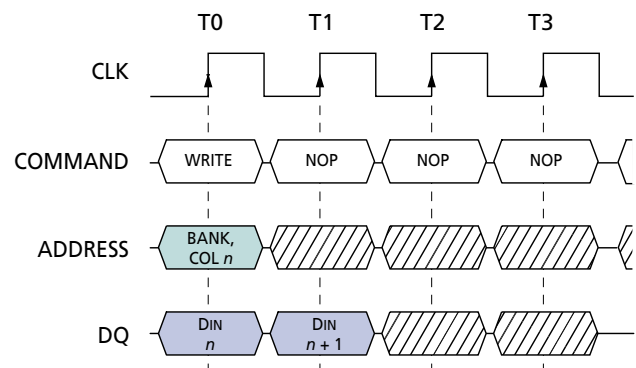
The starting column and bank addresses are provided with the WRITE command and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, auto precharge is disabled.

During WRITE bursts, the first valid data-in element will be registered coincident with the WRITE command. Subsequent data elements will be registered on each successive positive clock edge. Upon completion of a fixed-length burst, assuming no other commands have been initiated, the DQs will remain High-Z, and any additional input data will be ignored (see Figure 14). A full-page burst will continue until terminated. (At the end of the page, it will wrap to column 0 and continue.)

A fixed-length WRITE burst may be followed by, or truncated with, a WRITE burst (provided that AUTO PRECHARGE was not activated), and a full-page WRITE burst can be truncated with a subsequent WRITE burst. The new WRITE command can be issued on any clock cycle following the previous WRITE command, and the data

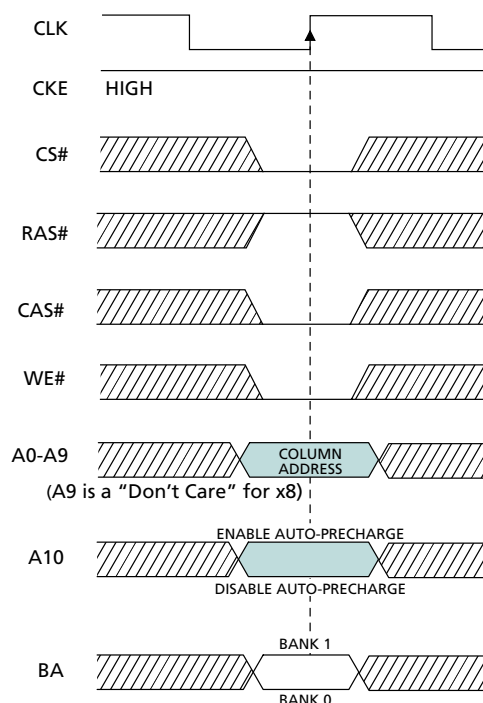
provided coincident with the new command applies to the new command. An example is shown in Figure 15. Data  $n + 1$  is either the last of a burst of two or the last desired of a longer burst. The Micron 16Mb SDRAM uses a pipelined architecture and therefore does not require the  $2n$  rule associated with a prefetch architecture. A WRITE command can be initiated on any clock cycle

**Figure 14  
WRITE Burst**

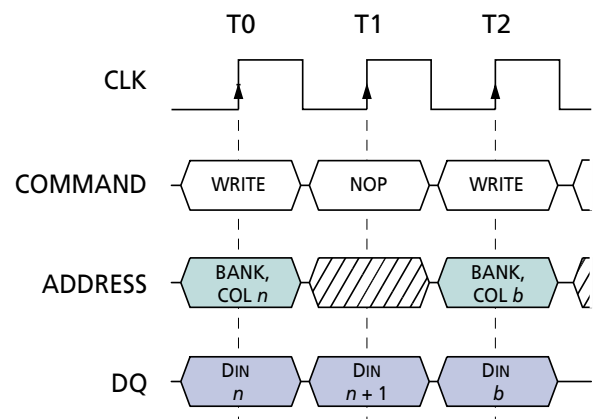


NOTE: Burst length = 2. DQM is LOW.

**Figure 13  
WRITE Command**



**Figure 15  
WRITE to WRITE**



NOTE: DQM is LOW. Each WRITE command may be to either bank.

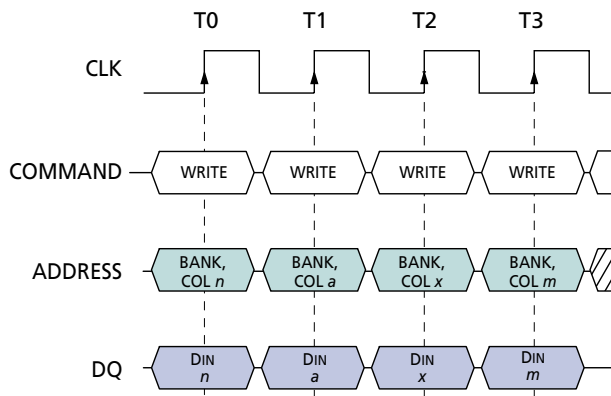
DON'T CARE

following a previous WRITE command. Full-speed random write accesses can be performed to the same bank, as shown in Figure 16, or each subsequent WRITE may be performed to a different bank.

A fixed-length WRITE burst may be followed by, or truncated with, a READ burst (provided that auto precharge was not activated), and a full-page WRITE burst can be truncated with a subsequent READ burst. Once the READ command is registered, the data inputs will be ignored, and WRITES will not be executed. An example is shown in Figure 17. Data  $n + 1$  is either the last of a burst of two or the last desired of a longer burst.

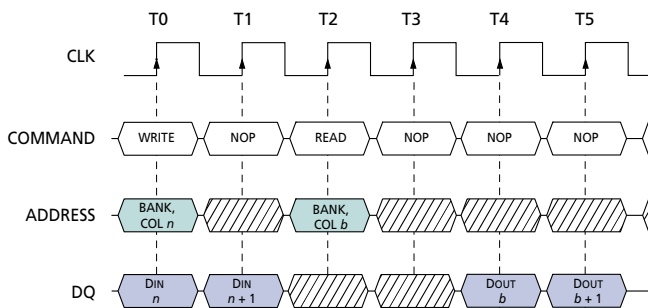
A fixed-length WRITE burst may be followed by, or truncated with, a PRECHARGE command to the same

**Figure 16  
RANDOM WRITE Cycles**



NOTE: Each WRITE command may be to either bank. DQM is LOW.

**Figure 17  
WRITE to READ**

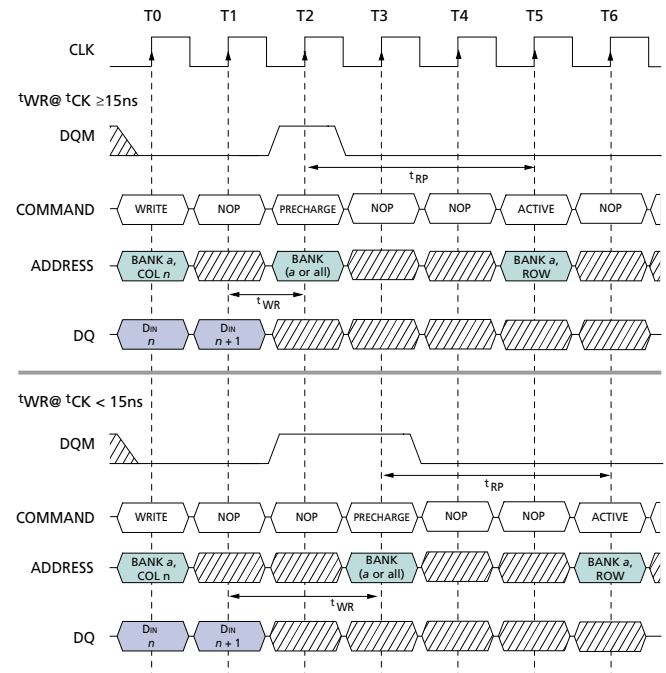


NOTE: The WRITE command may be to either bank, and the READ command may be to either bank. DQM is LOW. CAS latency = 2 for illustration.

bank (provided that auto precharge was not activated), and a full-page WRITE burst may be truncated with a PRECHARGE command to the same bank. The PRECHARGE command should be issued  $t_{WR}$  after the clock edge at which the last desired input data element is registered. The two-clock WRITE recovery version (A2) requires at least two clocks, regardless of frequency, as well as  $t_{WR}$  being met. In addition, when truncating a WRITE burst, the DQM signal must be used to mask input data for the clock edge on which the PRECHARGE command is entered. An example is shown in Figure 18. Data  $n + 1$  is either the last of a burst of two or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until  $t_{RP}$  is met.

In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the PRECHARGE command is that it can be used to truncate

**Figure 18  
WRITE to PRECHARGE**



NOTE: DQM could remain LOW in this example if the WRITE burst is a fixed length of two.

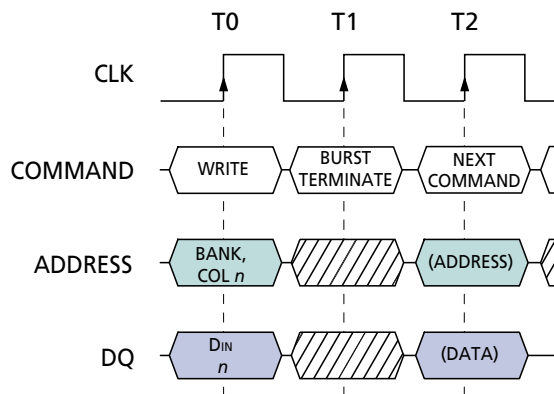
DON'T CARE

fixed-length or full-page bursts. The AUTO PRECHARGE command does not truncate fixed-length bursts and does not apply to full page bursts.

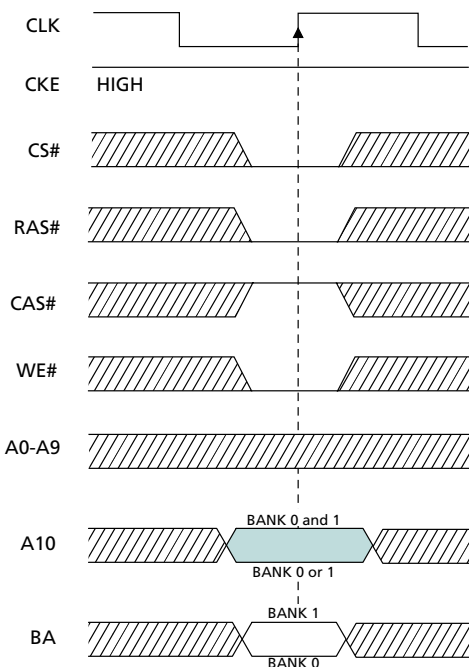
Fixed-length or full-page WRITE bursts can be truncated with the BURST TERMINATE command. When truncating a WRITE burst, the input data applied coincident with the BURST TERMINATE command will be ignored. The last data written (provided that DQM is

LOW at that time) will be the input data applied one clock previous to the BURST TERMINATE command. This is shown in Figure 19, where data  $n$  is the last desired data element of a longer burst.

**Figure 19  
Terminating a WRITE Burst**



**Figure 20  
PRECHARGE Command**



### PRECHARGE

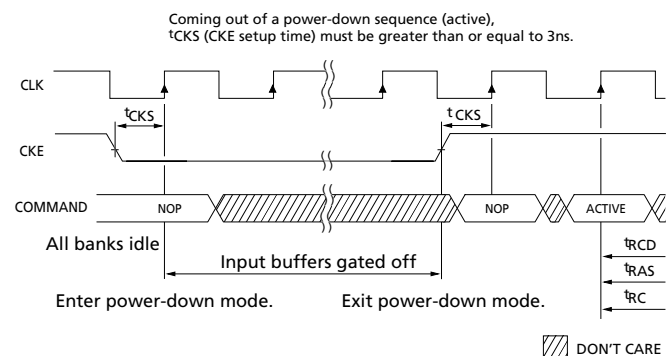
The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in both banks. The bank(s) will be available for a subsequent row access some specified time ( $t_{RP}$ ) after the PRECHARGE command is issued. Input A10 determines whether one or both banks are to be precharged, and in the case where only one bank is to be precharged, input BA selects the bank. When both banks are to be precharged, input BA is treated as a “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

### POWER-DOWN

Power-down occurs if CKE is registered LOW coincident with a NOP or COMMAND INHIBIT, when no accesses are in progress. If power-down occurs when both banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in either bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CKE, for maximum power savings while in standby. The device may not remain in the power-down state longer than the refresh period (64ms) since no refresh operations are performed in this mode.

The power-down state is exited by registering a NOP or COMMAND INHIBIT and CKE HIGH at the desired clock edge (meeting  $t_{CKS}$ ).

**Figure 21  
Power-Down**

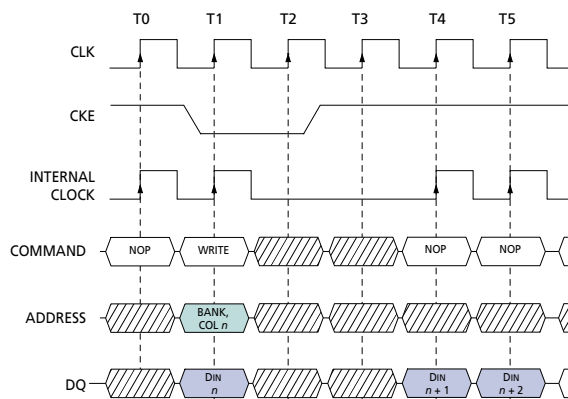


## CLOCK SUSPEND

The clock suspend mode occurs when a column access/burst is in progress and CKE is registered LOW. In the clock suspend mode, the internal clock is deactivated, “freezing” the synchronous logic.

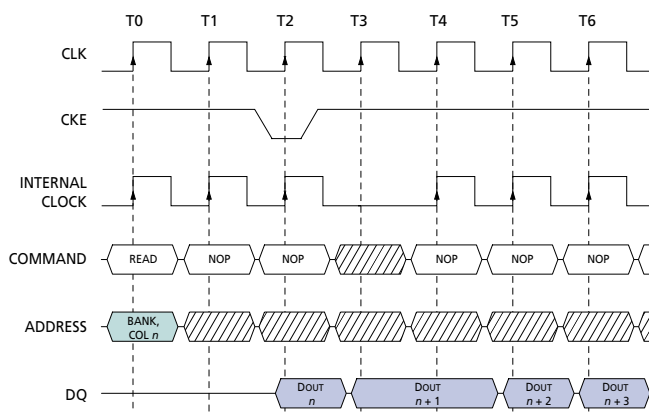
For each positive clock edge on which CKE is sampled LOW, the next internal positive clock edge is suspended. Any command or data present on the input pins at the time of a suspended internal clock edge is ignored; any data present on the DQ pins remains driven; and burst counters are not incremented, as long as the clock is suspended (see examples in Figures 22 and 23).

**Figure 22**  
**CLOCK SUSPEND During WRITE Burst**



NOTE: For this example, burst length = 4 or greater, and DQM is LOW.

**Figure 23**  
**CLOCK SUSPEND During READ Burst**



NOTE: For this example, CAS latency = 2, burst length = 4 or greater, and DQM is LOW.

DON'T CARE

### CONCURRENT AUTO PRECHARGE

An access command (READ or WRITE) to another bank while an access command with auto precharge enabled is executing is not allowed by SDRAMs, unless the SDRAM supports CONCURRENT AUTO PRECHARGE. Micron SDRAMs support CONCURRENT AUTO PRECHARGE. Four cases where CONCURRENT AUTO PRECHARGE occurs are defined below.

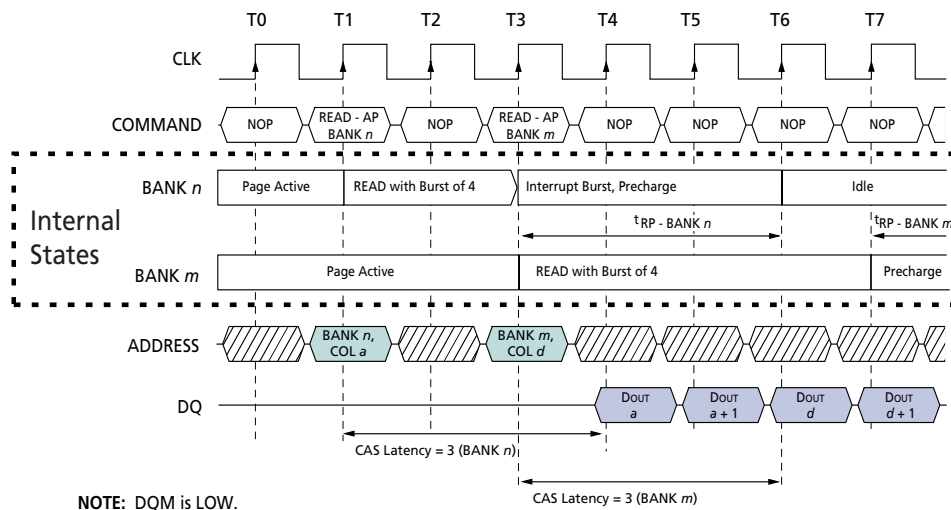
READ with auto precharge

1. Interrupted by a READ (with or without auto precharge): A READ to bank *m* will interrupt a READ

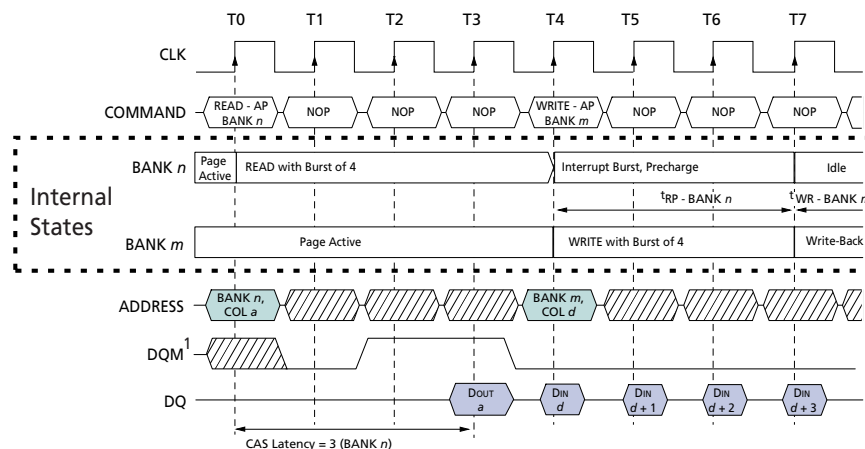
on bank *n*, CAS latency later. The PRECHARGE to bank *n* will begin when the READ to bank *m* is registered (Figure 24).

2. Interrupted by a WRITE (with or without auto precharge): A WRITE to bank *m* will interrupt a READ on bank *n* when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The PRECHARGE to bank *n* will begin when the WRITE to bank *m* is registered (Figure 25).

**Figure 24**  
**READ with Auto Precharge Interrupted by a READ**



**Figure 25**  
**READ with Auto Precharge Interrupted by a WRITE**



DON'T CARE

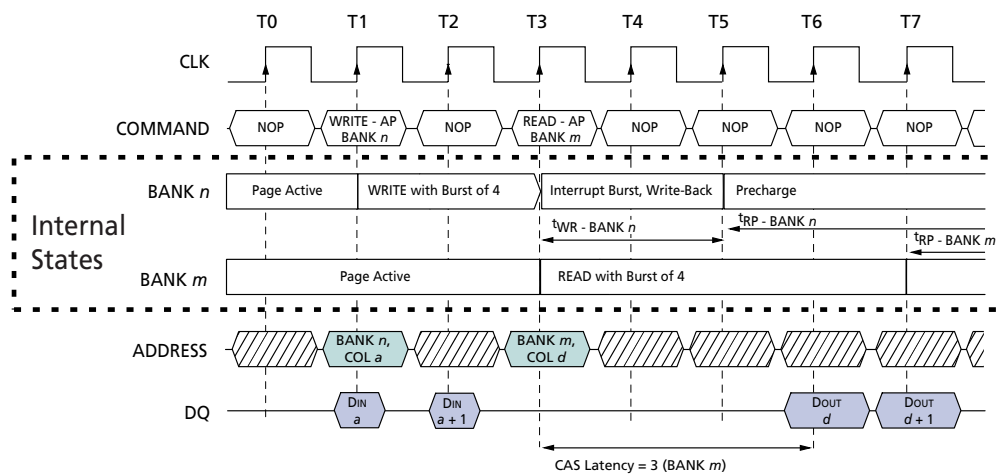


### WRITE with auto precharge

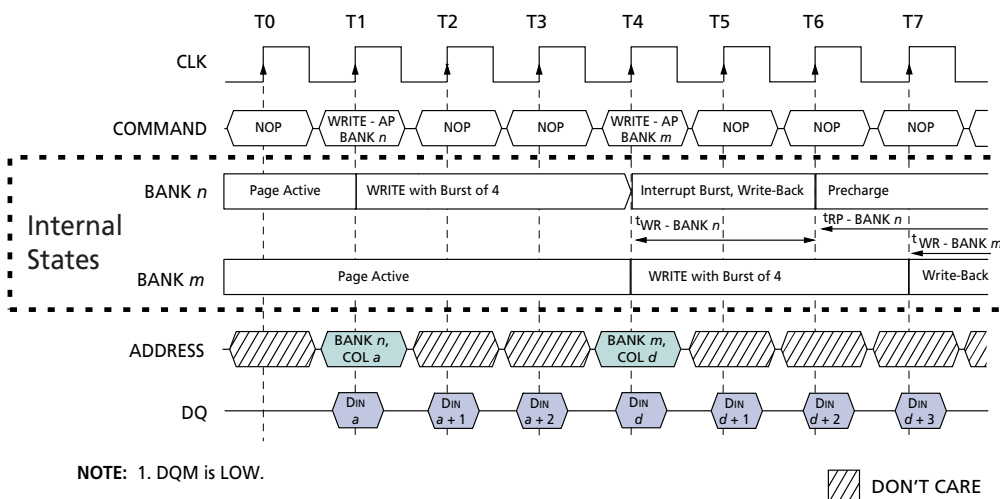
3. Interrupted by a READ (with or without auto precharge): A READ to bank  $m$  will interrupt a WRITE on bank  $n$  when registered, with the data-out appearing CAS latency later. The PRECHARGE to bank  $n$  will begin after  $t_{WR}$  is met, where  $t_{WR}$  begins when the READ to bank  $m$  is registered. The last valid WRITE to bank  $n$  will be data-in registered one clock prior to the READ to bank  $m$  (Figure 26).

4. Interrupted by a WRITE (with or without auto precharge): A WRITE to bank  $m$  will interrupt a WRITE on bank  $n$  when registered. The PRECHARGE to bank  $n$  will begin after  $t_{WR}$  is met, where  $t_{WR}$  begins when the WRITE to bank  $m$  is registered. The last valid data WRITE to bank  $n$  will be data registered one clock prior to a WRITE to bank 1 (Figure 27).

**Figure 26**  
**WRITE with Auto Precharge Interrupted by a READ**



**Figure 27**  
**WRITE with Auto Precharge Interrupted by a WRITE**



**TRUTH TABLE 2 – CKE**

(Notes: 1-4)

CKE <sub>n-1</sub>	CKE <sub>n</sub>	CURRENT STATE	COMMAND <sub>n</sub>	ACTION <sub>n</sub>	NOTES
L	L	Power-Down	X	Maintain Power-Down	
		Self Refresh	X	Maintain Self Refresh	
		Clock Suspend	X	Maintain Clock Suspend	
L	H	Power-Down	COMMAND INHIBIT or NOP	Exit Power-Down	5
		Self Refresh	COMMAND INHIBIT or NOP	Exit Self Refresh	6
		Clock Suspend	X	Exit Clock Suspend	7
H	L	Both Banks Idle	COMMAND INHIBIT or NOP	Power-Down Entry	
		Both Banks Idle	AUTO REFRESH	Self Refresh Entry	
		Reading or Writing	VALID	Clock Suspend Entry	
H	H		See Truth Table 3		

- NOTE:**
1. CKE<sub>n</sub> is the logic state of CKE at clock edge *n*; CKE<sub>n-1</sub> was the state of CKE at the previous clock edge.
  2. Current state is the state of the SDRAM immediately prior to clock edge *n*.
  3. COMMAND<sub>n</sub> is the command registered at clock edge *n* and ACTION<sub>n</sub> is a result of COMMAND<sub>n</sub>.
  4. All states and sequences not shown are illegal or reserved.
  5. Exiting power-down at clock edge *n* will put the device in the all banks idle state in time for clock edge *n* + 1 (provided that <sup>t</sup>CKS is met).
  6. Exiting self refresh at clock edge *n* will put the device in the all banks idle state once <sup>t</sup>XSR is met. COMMAND INHIBIT or NOP commands should be issued on any clock edges occurring during the <sup>t</sup>XSR period. A minimum of two NOP commands must be provided during the <sup>t</sup>XSR period.
  7. After exiting clock suspend at clock edge *n*, the device will resume operation and recognize the next command at clock edge *n* + 1.

**TRUTH TABLE 3 – Current State Bank *n* - Command to Bank *n***

(Notes: 1-6; notes appear below and on next page)

CURRENT STATE	CS#	RAS#	CAS#	WE#	COMMAND (ACTION)	NOTES
Any	H	X	X	X	COMMAND INHIBIT (NOP/Continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/Continue previous operation)	
Idle	L	L	H	H	ACTIVE (Select bank and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	LOAD MODE REGISTER	7
	L	L	H	L	PRECHARGE	11
Row Active	L	H	L	H	READ (Select bank and column and start READ burst)	10
	L	H	L	L	WRITE (Select bank and column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (Deactivate row in bank or banks)	8
Read (Auto- Precharge Disabled)	L	H	L	H	READ (Select bank and column and start new READ burst)	10
	L	H	L	L	WRITE (Select bank and column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (Truncate READ burst, start PRECHARGE)	8
	L	H	H	L	BURST TERMINATE	9
Write (Auto- Precharge Disabled)	L	H	L	H	READ (Select bank and column and start READ burst)	10
	L	H	L	L	WRITE (Select bank and column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (Truncate WRITE burst, start PRECHARGE)	8
	L	H	H	L	BURST TERMINATE	9

- NOTE:**
1. This table applies when  $\text{CKE}_{n-1}$  was HIGH and  $\text{CKE}_n$  is HIGH (see Truth Table 2) and after  $t_{\text{XSR}}$  has been met (if the previous state was self refresh).
  2. This table is bank-specific, except where noted; i.e., the current state is for a specific bank, and the commands shown are those allowed to be issued to that bank when it is in that state. Exceptions are covered in the notes below.
  3. Current state definitions:
    - Idle: The bank has been precharged and  $t_{\text{RP}}$  has been met.
    - Row Active: A row in the bank has been activated and  $t_{\text{RCD}}$  has been met. No data bursts/accesses and no register accesses are in progress.
    - Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
    - Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
  4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Truth Table 3, and according to Truth Table 4.
    - Precharging: Starts with registration of a PRECHARGE command and ends when  $t_{\text{RP}}$  is met. Once  $t_{\text{RP}}$  is met, the bank will be in the idle state.
    - Row Activating: Starts with registration of an ACTIVE command and ends when  $t_{\text{RCD}}$  is met. Once  $t_{\text{RCD}}$  is met, the bank will be in the row active state.
    - Read w/Auto-Precharge Enabled: Starts with registration of a READ command with auto precharge enabled, and ends when  $t_{\text{RP}}$  has been met. Once  $t_{\text{RP}}$  is met, the bank will be in the idle state.
    - Write w/Auto-Precharge Enabled: Starts with registration of a WRITE command with auto precharge enabled, and ends when  $t_{\text{RP}}$  has been met. Once  $t_{\text{RP}}$  is met, the bank will be in the idle state.

**NOTE (continued):**

5. The following states must not be interrupted by any executable command; COMMAND INHIBIT or NOP commands must be applied on each positive clock edge during these states.

Refreshing: Starts with registration of an AUTO REFRESH command and ends when  $t_{RC}$  is met. Once  $t_{RC}$  is met, the SDRAM will be in the all banks idle state.

Accessing Mode

Register: Starts with registration of a LOAD MODE REGISTER command and ends when  $t_{MRD}$  has been met. Once  $t_{MRD}$  is met, the SDRAM will be in the all banks idle state.

6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that both banks are idle.
8. May or may not be bank-specific; if both banks are to be precharged, both must be in a valid state for precharging.
9. Not bank-specific; BURST TERMINATE affects the most recent READ or WRITE burst, regardless of bank.
10. READs or WRITEs listed in the Command (Action) column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
11. Does not affect the state of the bank and acts as a NOP to that bank.

**TRUTH TABLE 4 – Current State Bank *n* - Command to Bank *m***

(Notes: 1-6; notes appear below and on next page)

CURRENT STATE	CS#	RAS#	CAS#	WE#	COMMAND (ACTION)	NOTES
Any	H	X	X	X	COMMAND INHIBIT (NOP/Continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/Continue previous operation)	
Idle	X	X	X	X	Any command otherwise allowed to bank m	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	7
	L	H	L	L	WRITE (Select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (Auto- Precharge Disabled)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start new READ burst)	7, 10
	L	H	L	L	WRITE (Select column and start WRITE burst)	7, 11
	L	L	H	L	PRECHARGE	9
Write (Auto- Precharge Disabled)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	7, 12
	L	H	L	L	WRITE (Select column and start new WRITE burst)	7, 13
	L	L	H	L	PRECHARGE	9
Read (With Auto- Precharge)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start new READ burst)	7, 8, 14
	L	H	L	L	WRITE (Select column and start WRITE burst)	7, 8, 15
	L	L	H	L	PRECHARGE	9
Write (With Auto- Precharge)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	7, 8, 16
	L	H	L	L	WRITE (Select column and start new WRITE burst)	7, 8, 17
	L	L	H	L	PRECHARGE	9

- NOTE:**
1. This table applies when CKE<sub>*n-1*</sub> was HIGH and CKE<sub>*n*</sub> is HIGH (see Truth Table 2) and after <sup>t</sup>XSR has been met (if the previous state was self refresh).
  2. This table describes alternate bank operation, except where noted; i.e., the current state is for bank *n* and the commands shown are those allowed to be issued to bank *m* (assuming that bank *m* is in such a state that the given command is allowable). Exceptions are covered in the notes below.
  3. Current state definitions:
    - Idle: The bank has been precharged, and <sup>t</sup>RP has been met.
    - Row Active: A row in the bank has been activated, and <sup>t</sup>RCD has been met. No data bursts/accesses and no register accesses are in progress.
    - Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
    - Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
    - Read w/Auto-Precharge Enabled: Starts with registration of a READ command with auto precharge enabled, and ends when <sup>t</sup>RP has been met. Once <sup>t</sup>RP is met, the bank will be in the idle state.
    - Write w/Auto-Precharge Enabled: Starts with registration of a WRITE command with auto precharge enabled, and ends when <sup>t</sup>RP has been met. Once <sup>t</sup>RP is met, the bank will be in the idle state.

**NOTE (continued):**

4. AUTO REFRESH, SELF REFRESH, and LOAD MODE REGISTER commands may only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs to bank *m* listed in the Command (Action) column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
8. CONCURRENT AUTO PRECHARGE: Bank *n* will initiate the auto precharge command when its burst has been interrupted by bank *m*'s burst.
9. Burst in bank *n* continues as initiated.
10. For a READ without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the READ on bank *n*, CAS latency later (Figure 7).
11. For a READ without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the READ on bank *n* when registered (Figures 9 and 10). DQM should be used one clock prior to the WRITE command to prevent bus contention.
12. For a WRITE without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the WRITE on bank *n* when registered (Figure 17), with the data-out appearing CAS latency later. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m*.
13. For a WRITE without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the WRITE on bank *n* when registered (Figure 15). The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m*.
14. For a READ with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the READ on bank *n*, CAS latency later. The PRECHARGE to bank *n* will begin when the READ to bank *m* is registered (Figure 24).
15. For a READ with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the READ on bank *n* when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The PRECHARGE to bank *n* will begin when the WRITE to bank *m* is registered (Figure 25).
16. For a WRITE with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the WRITE on bank *n* when registered, with the data-out appearing CAS latency later. The PRECHARGE to bank *n* will begin after  $t_{WR}$  is met, where  $t_{WR}$  begins when the READ to bank *m* is registered. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m* (Figure 26).
17. For a WRITE with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the WRITE on bank *n* when registered. The PRECHARGE to bank *n* will begin after  $t_{WR}$  is met, where  $t_{WR}$  begins when the WRITE to bank *m* is registered. The last valid WRITE to bank *n* will be data registered one clock prior to the WRITE to bank *m* (Figure 27).

## ABSOLUTE MAXIMUM RATINGS\*

Voltage on V <sub>DD</sub> /V <sub>DDQ</sub> Supply	
Relative to V <sub>SS</sub> .....	-1V to +4.6V
Voltage on Inputs, NC or I/O Pins	
Relative to V <sub>SS</sub> .....	-1V to +4.6V
Operating Temperature, T <sub>A</sub> (ambient) .....	0°C to +70°C
Storage Temperature (plastic) .....	-55°C to +150°C
Power Dissipation .....	1W

\*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 6; notes appear on page 34) (0°C ≤ T<sub>A</sub> ≤ 70°C; V<sub>DD</sub>/V<sub>DDQ</sub> = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V <sub>DD</sub> /V <sub>DDQ</sub>	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs	V <sub>IH</sub>	2	V <sub>DD</sub> + 0.3	V	23
INPUT LOW VOLTAGE: Logic 0; All inputs	V <sub>IL</sub>	-0.5	0.8	V	23
INPUT LEAKAGE CURRENT: Any input 0V ≤ V <sub>IN</sub> ≤ V <sub>DD</sub> (All other pins not under test = 0V)	I <sub>I</sub>	-5	5	μA	
OUTPUT LEAKAGE CURRENT: DQs are disabled; 0V ≤ V <sub>OUT</sub> ≤ V <sub>DDQ</sub>	I <sub>OZ</sub>	-5	5	μA	
OUTPUT LEVELS: Output High Voltage (I <sub>OUT</sub> = -2mA)	V <sub>OH</sub>	2.4	–	V	
Output Low Voltage (I <sub>OUT</sub> = 2mA)	V <sub>OL</sub>	–	0.4	V	

## I<sub>CC</sub> SPECIFICATIONS AND CONDITIONS

(Notes: 1, 6, 11, 13; notes appear on page 34) (0°C ≤ T<sub>A</sub> ≤ 70°C; V<sub>DD</sub>/V<sub>DDQ</sub> = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MAX		UNITS	NOTES
		-8B	-10		
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; t <sub>RC</sub> = t <sub>RC</sub> (MIN); CAS latency = 3; t <sub>CK</sub> = 10ns (15ns for -10)	I <sub>CC1</sub>	105	90	mA	3, 18, 19
STANDBY CURRENT: Power-Down Mode; All banks idle; CKE = LOW; t <sub>CK</sub> = 10ns (15ns for -10)	I <sub>CC2</sub>	3	2	mA	
STANDBY CURRENT: Active Mode; CKE = HIGH; CS# = HIGH; t <sub>CK</sub> = 10ns (15ns for -10); All banks active after t <sub>RCD</sub> met; No accesses in progress	I <sub>CC3</sub>	45	40	mA	3, 12, 19
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; t <sub>CK</sub> = 10ns (15ns for -10); All banks active; CAS latency = 3	I <sub>CC4</sub>	125	85	mA	3, 18, 19
AUTO REFRESH CURRENT: t <sub>RC</sub> = t <sub>RC</sub> (MIN); CAS latency = 3; CKE = HIGH; CS# = HIGH; t <sub>CK</sub> = 10ns (15ns for -10)	I <sub>CC5</sub>	95	85	mA	3, 12, 18, 19
SELF REFRESH CURRENT: CKE ≤ 0.2V	I <sub>CC6</sub>	1	2	mA	4

## CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: CLK	C <sub>I1</sub>	2.5	4.0	pF	2
Input Capacitance: All other input-only pins	C <sub>I2</sub>	2.5	5.0	pF	2
Input/Output Capacitance: DQs	C <sub>IO</sub>	4.0	6.5	pF	2

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 5, 6, 8, 9, 11; notes appear on page 34) (0°C ≤ T<sub>A</sub> ≤ +70°C)

AC CHARACTERISTICS		SYMBOL	-8B		-10		UNITS	NOTES
PARAMETER			MIN	MAX	MIN	MAX		
Access time from CLK (pos. edge)	CL = 3	t <sub>AC</sub> (3)		6		7.5	ns	
	CL = 2	t <sub>AC</sub> (2)		9		9	ns	22
	CL = 1	t <sub>AC</sub> (1)		27		27	ns	22
Address hold time		t <sub>AH</sub>	1		1		ns	
Address setup time		t <sub>AS</sub>	2		3		ns	
CLK high-level width		t <sub>CH</sub>	3		3.5		ns	
CLK low-level width		t <sub>CL</sub>	3		3.5		ns	
Clock cycle time	CL = 3	t <sub>CK</sub> (3)	8		10		ns	24
	CL = 2	t <sub>CK</sub> (2)	12		15		ns	22, 24
	CL = 1	t <sub>CK</sub> (1)	30		30		ns	24
CKE hold time		t <sub>CKH</sub>	1		1		ns	
CKE setup time		t <sub>CKS</sub>	2		3		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		t <sub>CMH</sub>	1		1		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		t <sub>CMS</sub>	2		3		ns	
Data-in hold time		t <sub>DH</sub>	1		1		ns	
Data-in setup time		t <sub>DS</sub>	2		3		ns	
Data-out high-impedance time	CL = 3	t <sub>HZ</sub> (3)		6		8	ns	10
	CL = 2	t <sub>HZ</sub> (2)		7		10	ns	10
	CL = 1	t <sub>HZ</sub> (1)		15		15	ns	10
Data-out low-impedance time		t <sub>LZ</sub>	1		2		ns	
Data-out hold time		t <sub>OH</sub>	3		3		ns	
ACTIVE to PRECHARGE command		t <sub>RAS</sub>	50	120,000	60	120,000	ns	
AUTO REFRESH, ACTIVE command period		t <sub>RC</sub>	80		90		ns	22
ACTIVE to READ or WRITE delay		t <sub>RCD</sub>	20		30		ns	22
Refresh period (2,048 or 4,096 rows)		t <sub>REF</sub>		64		64	ms	
PRECHARGE command period		t <sub>RP</sub>	24		30		ns	22
ACTIVE bank A to ACTIVE bank B command		t <sub>RRD</sub>	20		20		ns	
Transition time		t <sub>T</sub>	0.3	1.2	1	1.2	ns	7
WRITE recovery time	A1 version	t <sub>WR</sub>	1		1		t <sub>CK</sub>	25
			10		10		ns	26
	A2 version	t <sub>WR</sub>	2		2		t <sub>CK</sub>	25
			15		15		ns	26
Exit SELF REFRESH to ACTIVE command		t <sub>XSR</sub>	80		90		ns	20



## AC FUNCTIONAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 11; notes appear on page 34) ( $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ )

PARAMETER		SYMBOL	-8B	-10	UNITS	NOTES
READ/WRITE command to READ/WRITE command		$t_{\text{CCD}}$	1	1	$t_{\text{CK}}$	17
CKE to clock disable or power-down entry mode		$t_{\text{CKED}}$	1	1	$t_{\text{CK}}$	14
CKE to clock enable or power-down exit setup mode		$t_{\text{PED}}$	1	1	$t_{\text{CK}}$	14
DQM to input data delay		$t_{\text{DQD}}$	0	0	$t_{\text{CK}}$	17
DQM to data mask during WRITES		$t_{\text{DQM}}$	0	0	$t_{\text{CK}}$	17
DQM to data high-impedance during READs		$t_{\text{DQZ}}$	2	2	$t_{\text{CK}}$	17
WRITE command to input data delay		$t_{\text{DWD}}$	0	0	$t_{\text{CK}}$	17
Data-in to ACTIVE command	A1 version	$t_{\text{DAL}}$	4	3	$t_{\text{CK}}$	15, 21
	A2 version	$t_{\text{DAL}}$	5	4	$t_{\text{CK}}$	15, 21
Data-in to PRECHARGE command	A1 version	$t_{\text{DPL}}$	1	1	$t_{\text{CK}}$	16, 21
	A2 version	$t_{\text{DPL}}$	2	2	$t_{\text{CK}}$	16, 21
Last data-in to burst STOP command		$t_{\text{BDL}}$	1	1	$t_{\text{CK}}$	17
Last data-in to new READ/WRITE command		$t_{\text{CDL}}$	1	1	$t_{\text{CK}}$	17
Last data-in to PRECHARGE command	A1 version	$t_{\text{RDL}}$	1	1	$t_{\text{CK}}$	16, 21
	A2 version	$t_{\text{RDL}}$	2	2	$t_{\text{CK}}$	16, 21
LOAD MODE REGISTER command to ACTIVE or REFRESH command		$t_{\text{MRD}}$	2	2	$t_{\text{CK}}$	27
Data-out to high-impedance from PRECHARGE command	CL = 3	$t_{\text{ROH}} (3)$	3	3	$t_{\text{CK}}$	17
	CL = 2	$t_{\text{ROH}} (2)$	2	2	$t_{\text{CK}}$	17
	CL = 1	$t_{\text{ROH}} (1)$	1	1	$t_{\text{CK}}$	17

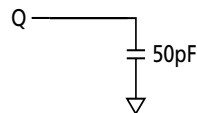
## ELECTRICAL TIMING CHARACTERISTICS BETWEEN -8 SPEED OPTIONS

(Notes: 5, 6, 8, 9, 11, 24; notes appear on page 34) ( $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ )

AC CHARACTERISTICS PARAMETER		SYM	-8E		-8D		-8C		-8B		-8A		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Access time from CLK (pos. edge)	CL = 3	<sup>t</sup> AC (3)		6		6		6		6		6	ns	22
	CL = 2	<sup>t</sup> AC (2)		6		7		9		9		9	ns	22
	CL = 1	<sup>t</sup> AC (1)		27		27		27		27		27	ns	22
Clock cycle time	CL = 3	<sup>t</sup> CK (3)	8		8		8		8		8		ns	22
	CL = 2	<sup>t</sup> CK (2)	10		10		12		12		12		ns	22
	CL = 1	<sup>t</sup> CK (1)	30		30		30		30		30		ns	22
ACTIVE to READ or WRITE delay		<sup>t</sup> RCD	20		20		20		20		24		ns	22
PRECHARGE command period		<sup>t</sup> RP	20		20		20		24		24		ns	22
AUTO REFRESH, ACTIVE command period		<sup>t</sup> RC	70		70		70		80		80		ns	22
WRITE recovery time	A1 version	<sup>t</sup> WR	na		na		1		1		1		<sup>t</sup> CK	21
	A2 version	<sup>t</sup> WR	2		2		2		2		2		<sup>t</sup> CK	21
100 MHz Speed Reference (CL- <sup>t</sup> RCD- <sup>t</sup> RP)			2-2-2		2-2-2		3-2-2		3-2-3		3-3-3		CLKs	

## NOTES

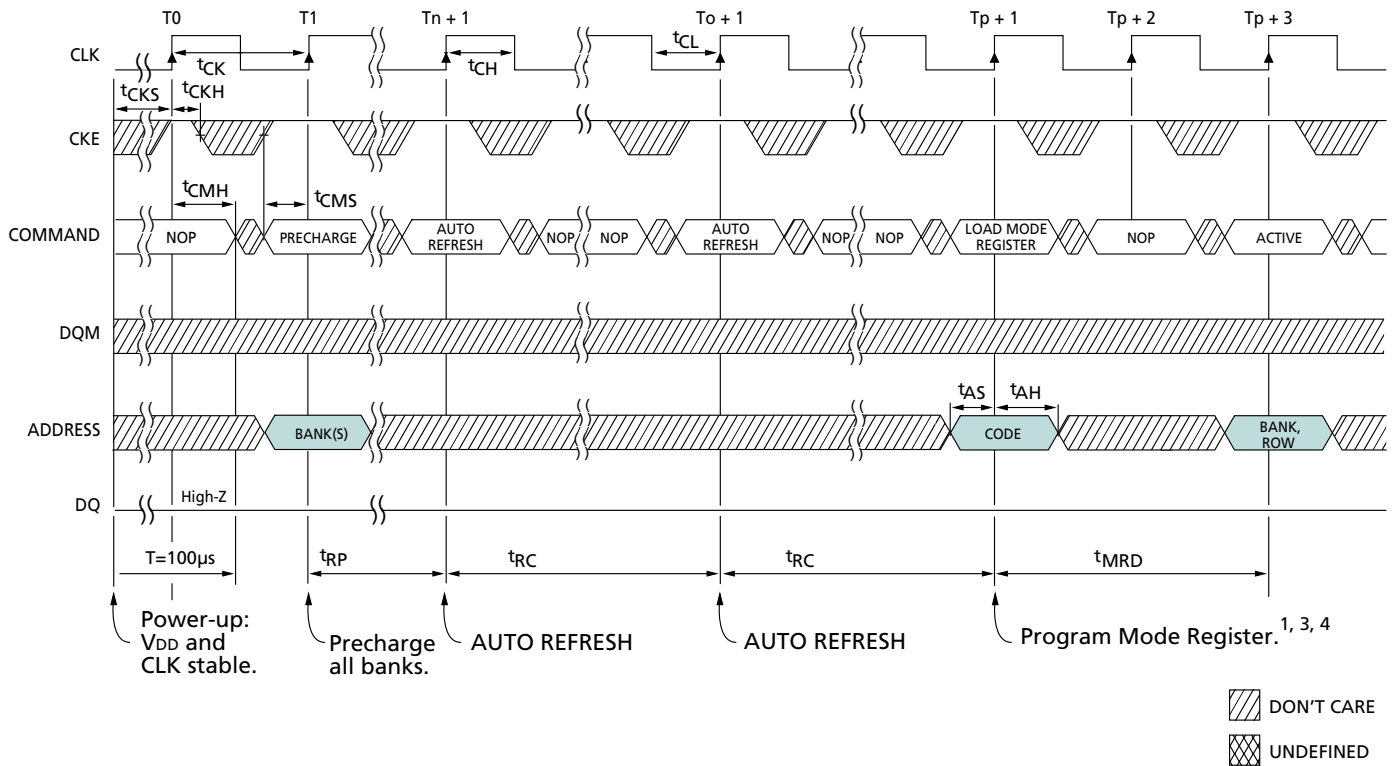
1. All voltages referenced to Vss.
2. This parameter is sampled.  $V_{DD}$ ,  $V_{DDQ} = +3.3V$ ;  $f = 1\text{ MHz}$ ,  $T_A = 25^\circ\text{C}$ ; pin under test biased at 1.4V.
3.  $I_{CC}$  is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ( $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ ) is ensured.
6. An initial pause of 100 $\mu\text{s}$  is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. ( $V_{DD}$  and  $V_{DDQ}$  must be powered up simultaneously.  $V_{SS}$  and  $V_{SSQ}$  must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the  $t_{REF}$  refresh requirement is exceeded.
7. AC characteristics assume  $t_T = 1\text{ns}$ .
8. In addition to meeting the transition rate specification, the clock and CKE must transit between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a monotonic manner.
9. Outputs measured at 1.5V with equivalent load:



10.  $t_{HZ}$  defines the time at which the output achieves the open circuit condition; it is not a reference to  $V_{OH}$  or  $V_{OL}$ . The last valid data element will meet  $t_{OH}$  before going High-Z.
11. AC timing and  $I_{CC}$  tests have  $V_{IL} = 0V$  and  $V_{IH} = 3V$ , with timing referenced to 1.5V crossover point.

12. Other input signals are allowed to transition no more than once in any 30ns period (20ns on -8) and are otherwise at valid  $V_{IH}$  or  $V_{IL}$  levels.
13.  $I_{CC}$  specifications are tested after the device is properly initialized.
14. Timing actually specified by  $t_{CKS}$ ; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by  $t_{WR}$  plus  $t_{RP}$ ; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by  $t_{WR}$ .
17. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The  $I_{CC}$  current will decrease as the CAS latency is reduced. This is due to the fact that the maximum cycle rate is slower as the CAS latency is reduced.
19. Address transitions average one transition every 30ns (20ns on -8).
20. CLK must be toggled a minimum of two times during this period.
21. Based on  $t_{CK} = 100\text{ MHz}$  for -8 and 66 MHz for -10.
22. These five parameters vary between speed grades and define the differences between the -8 SDRAM speeds: -8A, -8B, -8C, -8D, and -8E. All other -8 timing parameters remain constant.
23.  $V_{IH}$  overshoot:  $V_{IH}(\text{MAX}) = V_{DDQ} + 2V$  for a pulse width  $\leq 10\text{ns}$ , and the pulse width cannot be greater than one third of the cycle rate.  $V_{IL}$  undershoot:  $V_{IL}(\text{MIN}) = -2V$  for a pulse width  $\leq 10\text{ns}$ , and the pulse width cannot be greater than one third of the cycle rate.
24. The clock frequency must remain constant during access or precharge states (READ, WRITE, including  $t_{WR}$ , and PRECHARGE commands). CKE may be used to reduce the data rate.
25. Auto precharge mode only.
26. Precharge mode only.
27. JEDEC and PC100 specify three clocks.

## INITIALIZE AND LOAD MODE REGISTER



## TIMING PARAMETERS

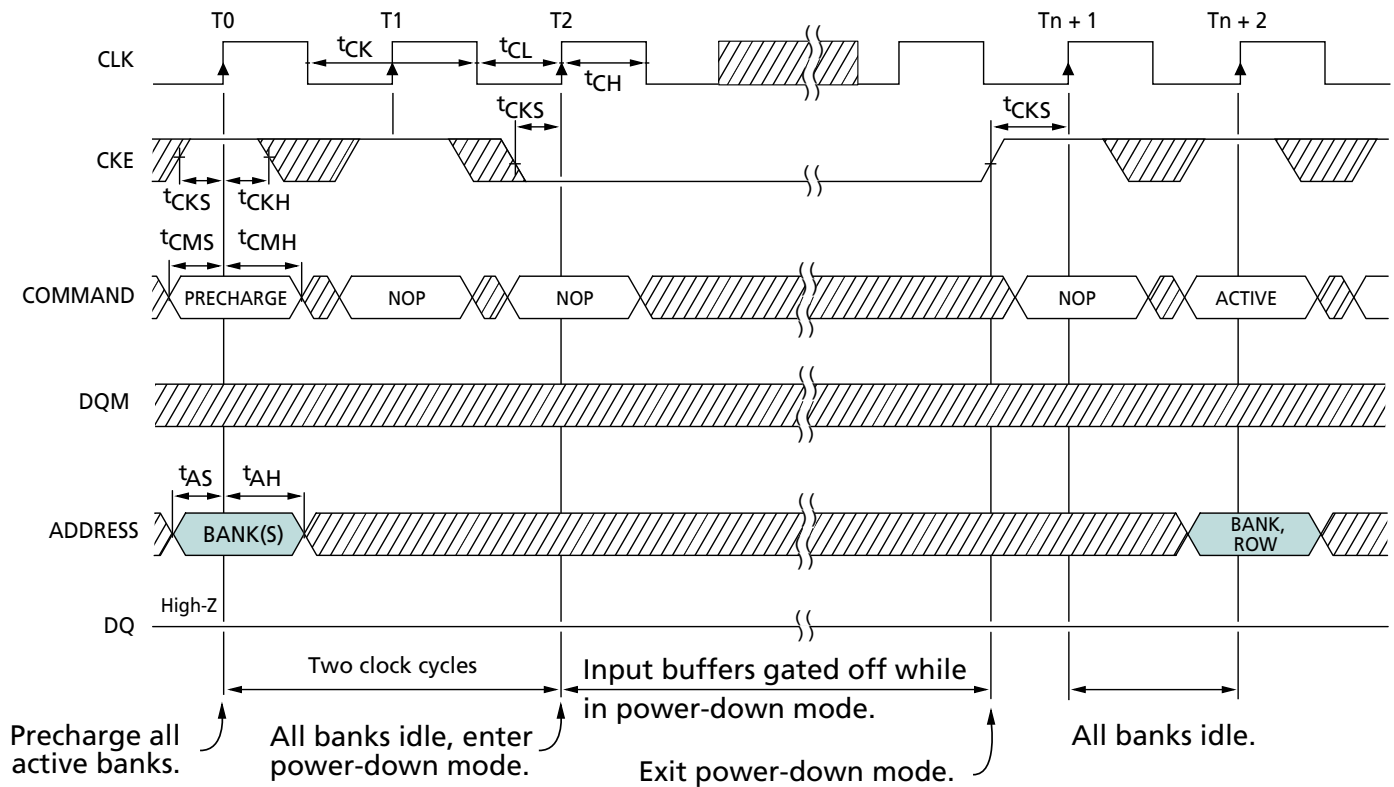
SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
t <sub>AH</sub>	1		1		ns
t <sub>AS</sub>	2		3		ns
t <sub>CH</sub>	3		3.5		ns
t <sub>CL</sub>	3		3.5		ns
t <sub>CK</sub> (3)	8		10		ns
t <sub>CK</sub> (2)	12		15		ns
t <sub>CKH</sub>	1		1		ns

SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
t <sub>CKS</sub>	2		3		ns
t <sub>CMH</sub>	1		1		ns
t <sub>CMS</sub>	2		3		ns
t <sub>MRD</sub> <sup>3</sup>	2		2		t <sub>CK</sub>
t <sub>RC</sub>	80		90		ns
t <sub>RP</sub>	24		30		ns

\*CAS latency indicated in parentheses.

- NOTE:**
1. The Mode Register may be loaded prior to the AUTO REFRESH cycles if desired.
  2. If CS is HIGH at clock high time, all commands applied are NOP, with CKE a "Don't Care."
  3. JEDEC and PC100 specify three clocks.
  4. Outputs are guaranteed High-Z after command is issued.

# **POWER-DOWN MODE <sup>1</sup>**



DON'T CARE  
 UNDEFINED

## **TIMING PARAMETERS**

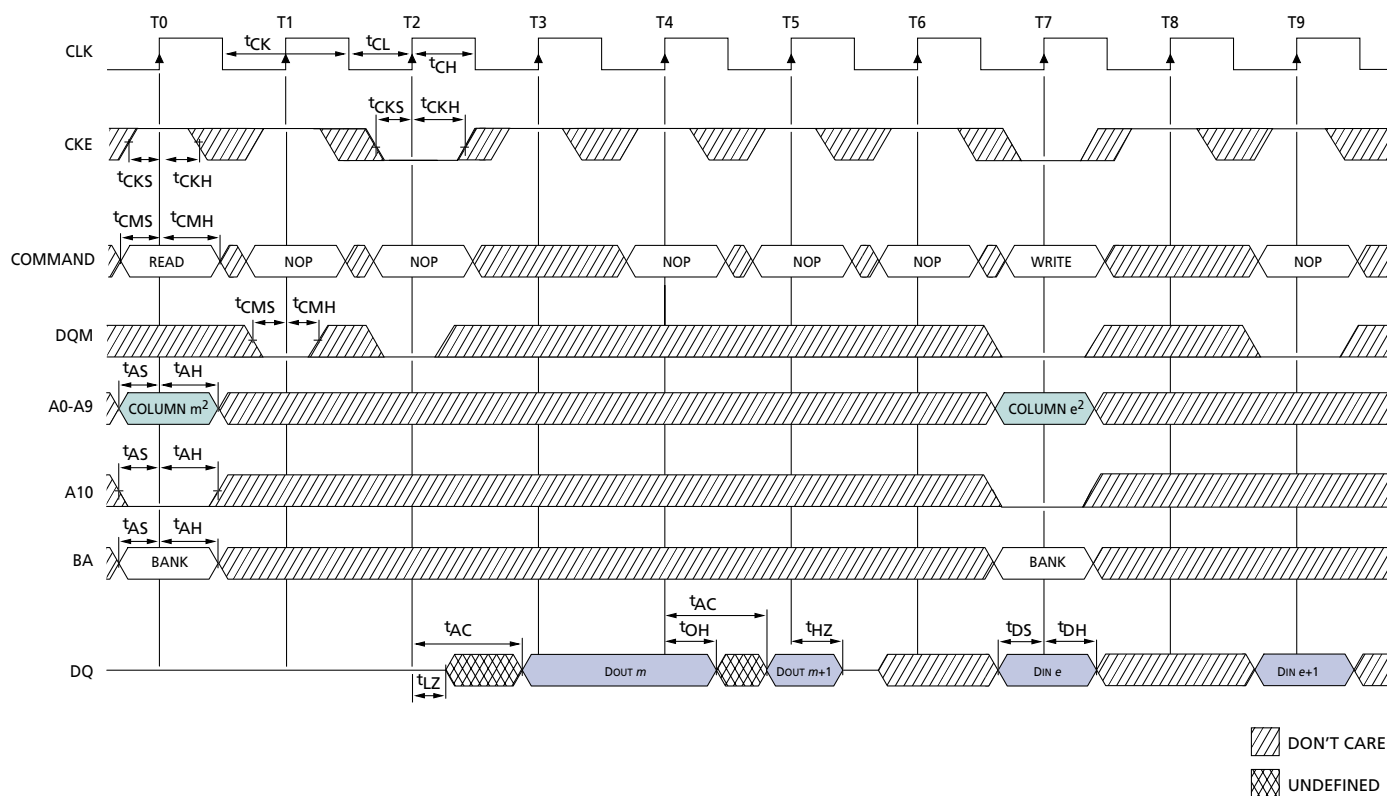
SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
t <sub>AH</sub>	1		1		ns
t <sub>AS</sub>	2		3		ns
t <sub>CH</sub>	3		3.5		ns
t <sub>CL</sub>	3		3.5		ns
t <sub>CK</sub> (3)	8		10		ns

SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
t <sub>CK</sub> (2)	12		15		ns
t <sub>CKH</sub>	1		1		ns
t <sub>CKS</sub>	2		3		ns
t <sub>CMH</sub>	1		1		ns
t <sub>CMS</sub>	2		3		ns

\*CAS latency indicated in parentheses.

**NOTE:** 1. Violating refresh requirements during power-down may result in a loss of data.

## CLOCK SUSPEND MODE <sup>1</sup>



### TIMING PARAMETERS

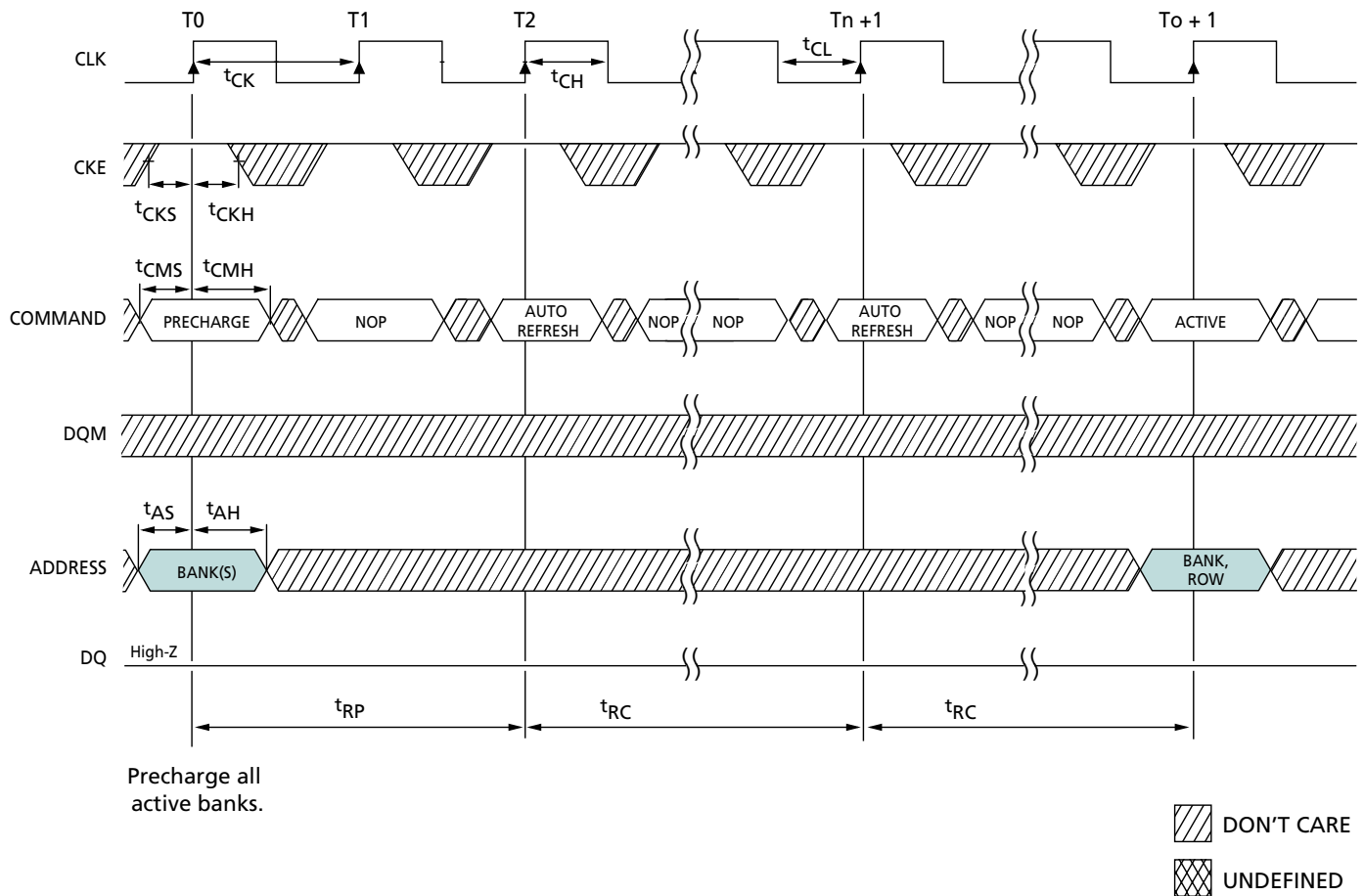
SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
$t_{AC(3)}$		6		7.5	ns
$t_{AC(2)}$		9		9	ns
$t_{AH}$	1		1		ns
$t_{AS}$	2		3		ns
$t_{CH}$	3		3.5		ns
$t_{CL}$	3		3.5		ns
$t_{CK(3)}$	8		10		ns
$t_{CK(2)}$	12		15		ns
$t_{CKH}$	1		1		ns

SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
$t_{CKS}$	2		3		ns
$t_{CMH}$	1		1		ns
$t_{CMS}$	2		3		ns
$t_{DH}$	1		1		ns
$t_{DS}$	2		3		ns
$t_{HZ(3)}$		6		8	ns
$t_{HZ(2)}$		7		10	ns
$t_{LZ}$	1		2		ns
$t_{OH}$	3		3		ns

\*CAS latency indicated in parentheses.

**NOTE:** 1. For this example, the burst length = 2, the CAS latency = 3, and AUTO PRECHARGE is disabled.  
2. Column-address A9 is a "Don't Care" on x8 version.

### AUTO REFRESH MODE



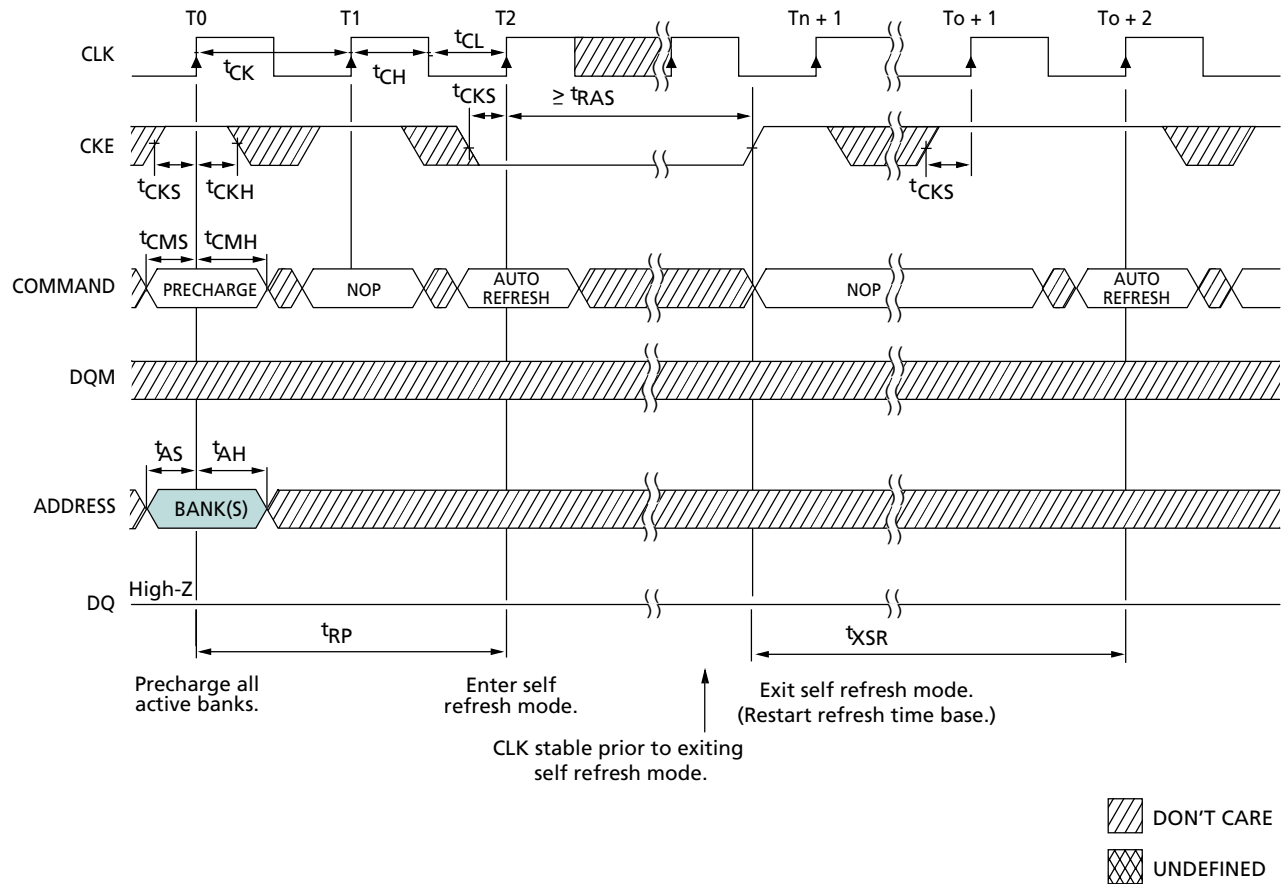
### TIMING PARAMETERS

SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
$t_{AH}$	1		1		ns
$t_{AS}$	2		3		ns
$t_{CH}$	3		3.5		ns
$t_{CL}$	3		3.5		ns
$t_{CK} (3)$	8		10		ns
$t_{CK} (2)$	12		15		ns

SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
$t_{CKH}$	1		1		ns
$t_{CKS}$	2		3		ns
$t_{CMH}$	1		1		ns
$t_{CMS}$	2		3		ns
$t_{RC}$	80		90		ns
$t_{RP}$	24		30		ns

\*CAS latency indicated in parentheses.

## SELF REFRESH MODE

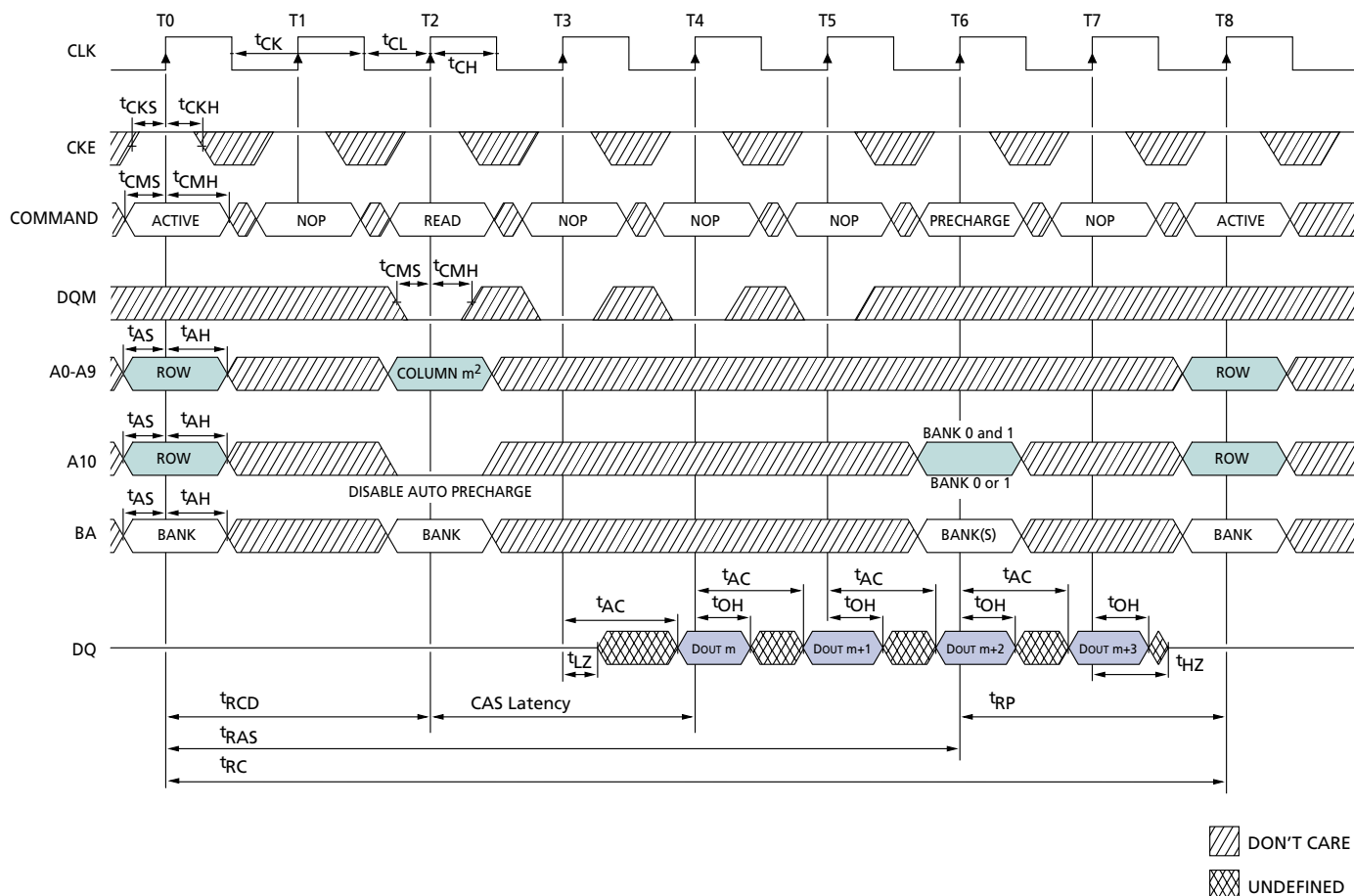


## TIMING PARAMETERS

SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
$t_{AH}$	1		1		ns
$t_{AS}$	2		3		ns
$t_{CH}$	3		3.5		ns
$t_{CL}$	3		3.5		ns
$t_{CK}$ (3)	8		10		ns
$t_{CK}$ (2)	12		15		ns
$t_{CKH}$	1		1		ns

SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
$t_{CKS}$	2		3		ns
$t_{CMH}$	1		1		ns
$t_{CMS}$	2		3		ns
$t_{RAS}$	50	120,000	60	120,000	ns
$t_{RP}$	24		30		ns
$t_{XSR}$	80		90		ns

\*CAS latency indicated in parentheses.

**READ – WITHOUT AUTO PRECHARGE <sup>1</sup>**

**TIMING PARAMETERS**

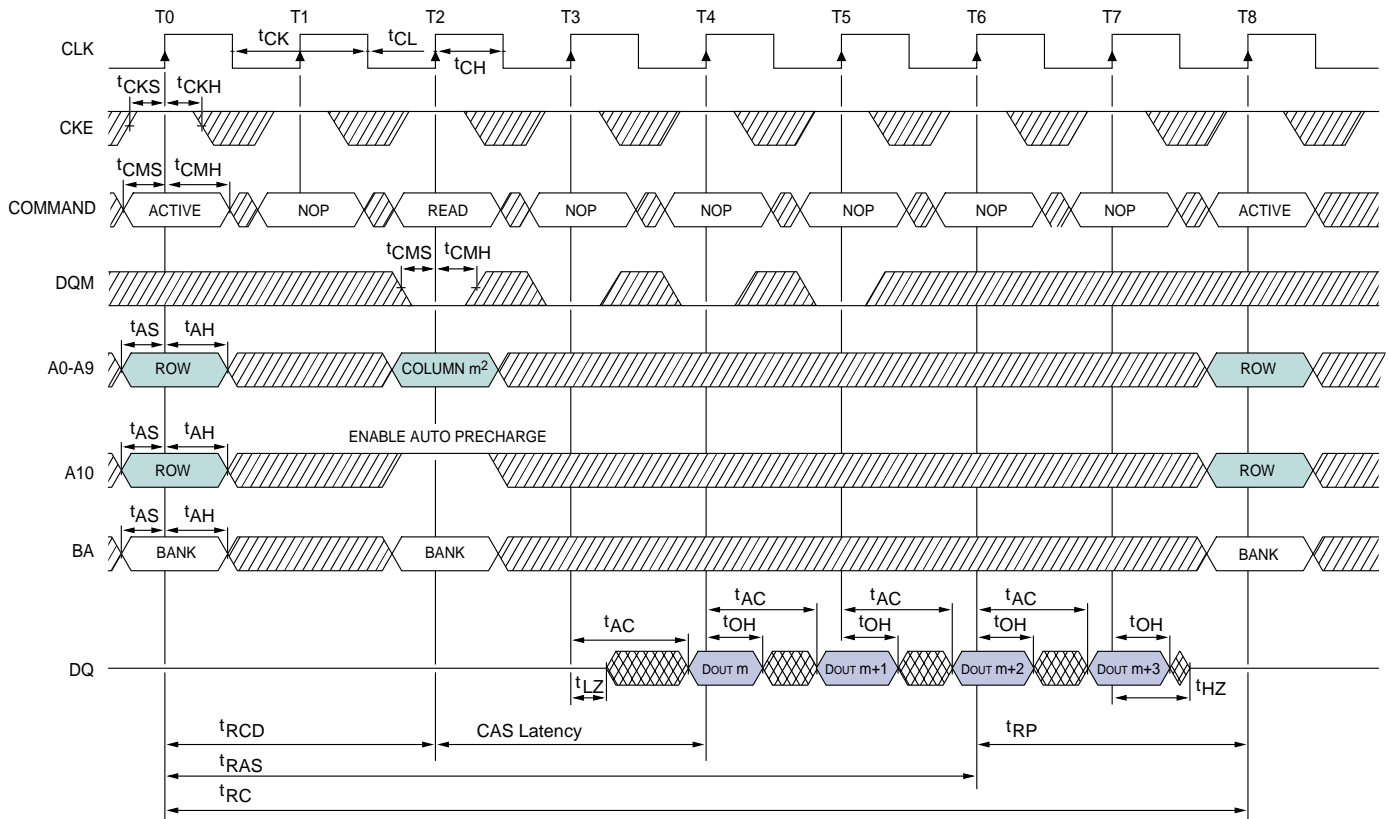
SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
$t_{AC(3)}$		6		7.5	ns
$t_{AC(2)}$		9		9	ns
$t_{AH}$	1		1		ns
$t_{AS}$	2		3		ns
$t_{CH}$	3		3.5		ns
$t_{CL}$	3		3.5		ns
$t_{CK(3)}$	8		10		ns
$t_{CK(2)}$	12		15		ns
$t_{CKH}$	1		1		ns
$t_{CKS}$	2		3		ns

SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
$t_{CMH}$	1		1		ns
$t_{CMS}$	2		3		ns
$t_{HZ(3)}$		6		8	ns
$t_{HZ(2)}$		7		10	ns
$t_{LZ}$	1		2		ns
$t_{OH}$	3		3		ns
$t_{RAS}$	50	120,000	60	120,000	ns
$t_{RC}$	80		90		ns
$t_{RCD}$	20		30		ns
$t_{RP}$	24		30		ns

\*CAS latency indicated in parentheses.

**NOTE:** 1. For this example, the burst length = 4, the CAS latency = 2, and the READ burst is followed by a “manual” PRECHARGE.  
2. Column-address A9 is a “Don’t Care” on x8 version.



**READ – WITH AUTO PRECHARGE <sup>1</sup>**


DON'T CARE  
 UNDEFINED

**TIMING PARAMETERS**

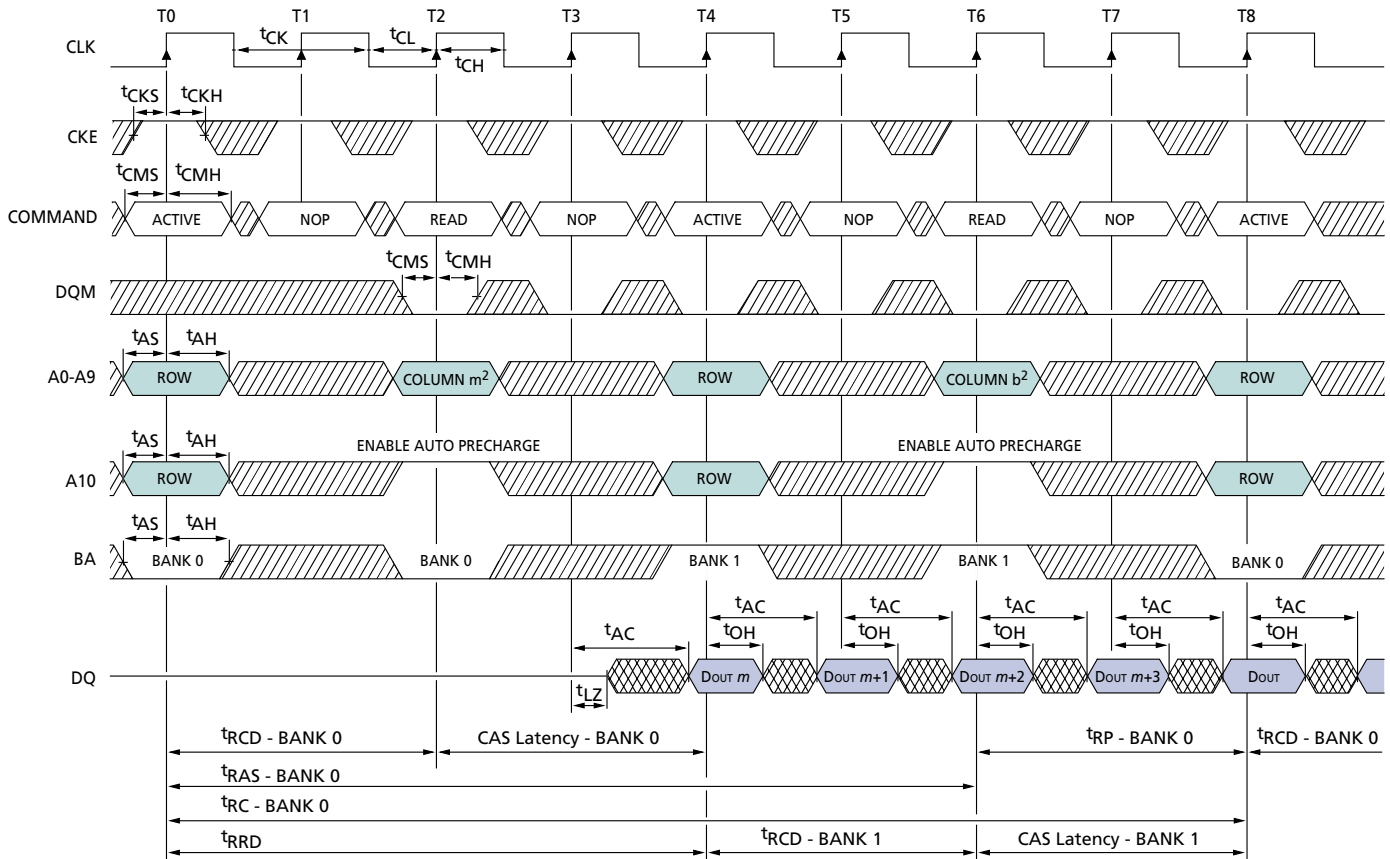
SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
$t_{AC(3)}$		6		7.5	ns
$t_{AC(2)}$		9		9	ns
$t_{AH}$	1		1		ns
$t_{AS}$	2		3		ns
$t_{CH}$	3		3.5		ns
$t_{CL}$	3		3.5		ns
$t_{CK(3)}$	8		10		ns
$t_{CK(2)}$	12		15		ns
$t_{CKH}$	1		1		ns
$t_{CKS}$	2		3		ns

SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
$t_{CMH}$	1		1		ns
$t_{CMS}$	2		3		ns
$t_{HZ(3)}$		6		8	ns
$t_{HZ(2)}$		7		10	ns
$t_{LZ}$	1		2		ns
$t_{OH}$	3		3		ns
$t_{RAS}$	50	120,000	60	120,000	ns
$t_{RC}$	80		90		ns
$t_{RCD}$	20		30		ns
$t_{RP}$	24		30		ns

\*CAS latency indicated in parentheses.

**NOTE:** 1. For this example, the burst length = 4, and the CAS latency = 2.  
 2. Column-address A9 is a "Don't Care" on x8 version.

# **ALTERNATING BANK READ ACCESSES <sup>1</sup>**



DON'T CARE  
 UNDEFINED

## **TIMING PARAMETERS**

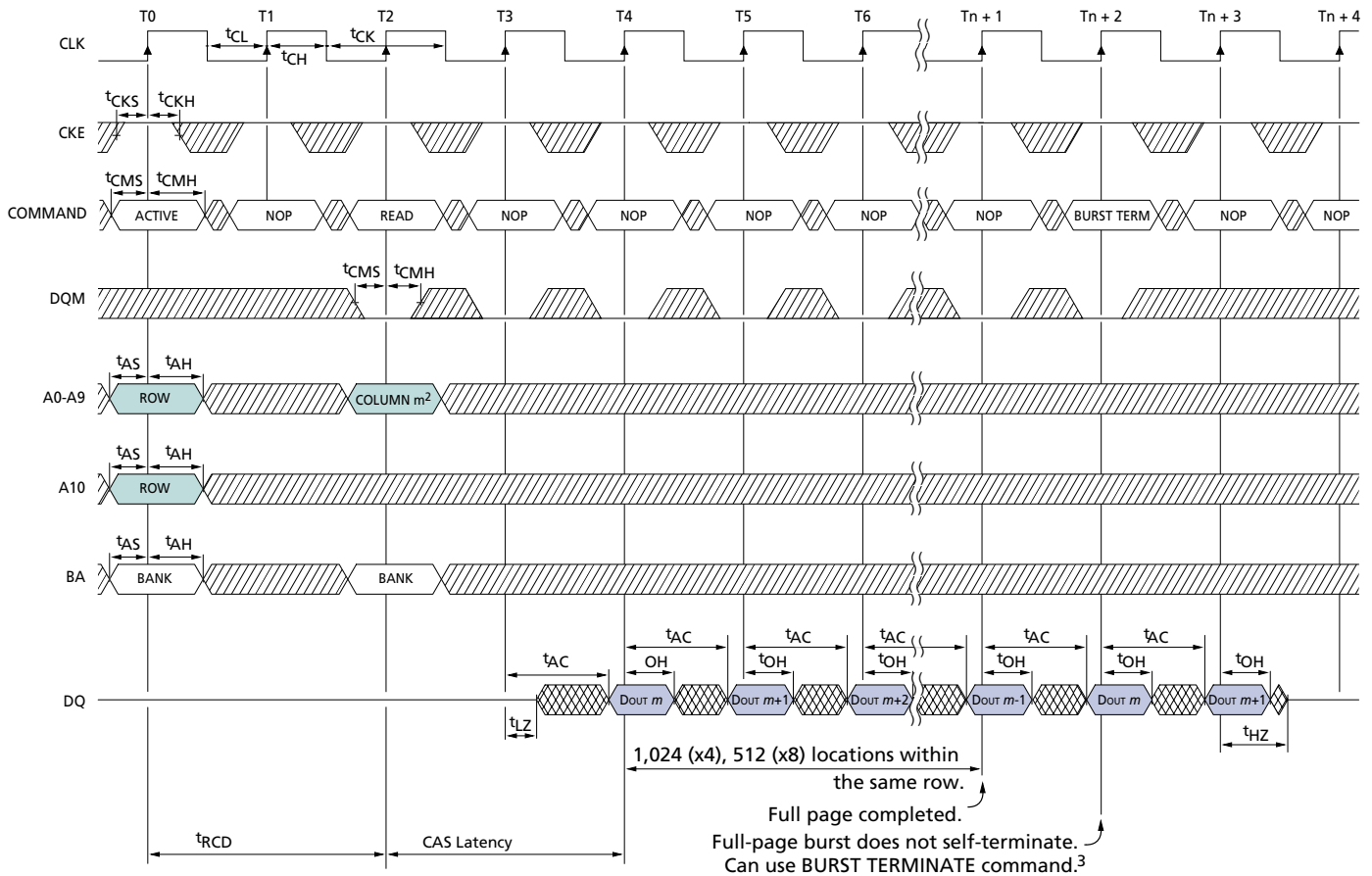
SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
t <sub>AC</sub> (3)		6		7.5	ns
t <sub>AC</sub> (2)		9		9	ns
t <sub>AH</sub>	1		1		ns
t <sub>AS</sub>	2		3		ns
t <sub>CH</sub>	3		3.5		ns
t <sub>CL</sub>	3		3.5		ns
t <sub>CK</sub> (3)	8		10		ns
t <sub>CK</sub> (2)	12		15		ns
t <sub>CKH</sub>	1		1		ns
t <sub>CKS</sub>	2		3		ns

SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
t <sub>CMH</sub>	1		1		ns
t <sub>CMS</sub>	2		3		ns
t <sub>LZ</sub>	1		2		ns
t <sub>OH</sub>	3		3		ns
t <sub>RAS</sub>	50	120,000	60	120,000	ns
t <sub>RC</sub>	80		90		ns
t <sub>RCD</sub>	20		30		ns
t <sub>RP</sub>	24		30		ns
t <sub>RRD</sub>	20		20		ns

\*CAS latency indicated in parentheses.

**NOTE:** 1. For this example, the burst length = 4, and the CAS latency = 2.  
 2. Column-address A9 is a "Don't Care" on x8 version.

## READ – FULL-PAGE BURST <sup>1</sup>



DON'T CARE  
 UNDEFINED

## TIMING PARAMETERS

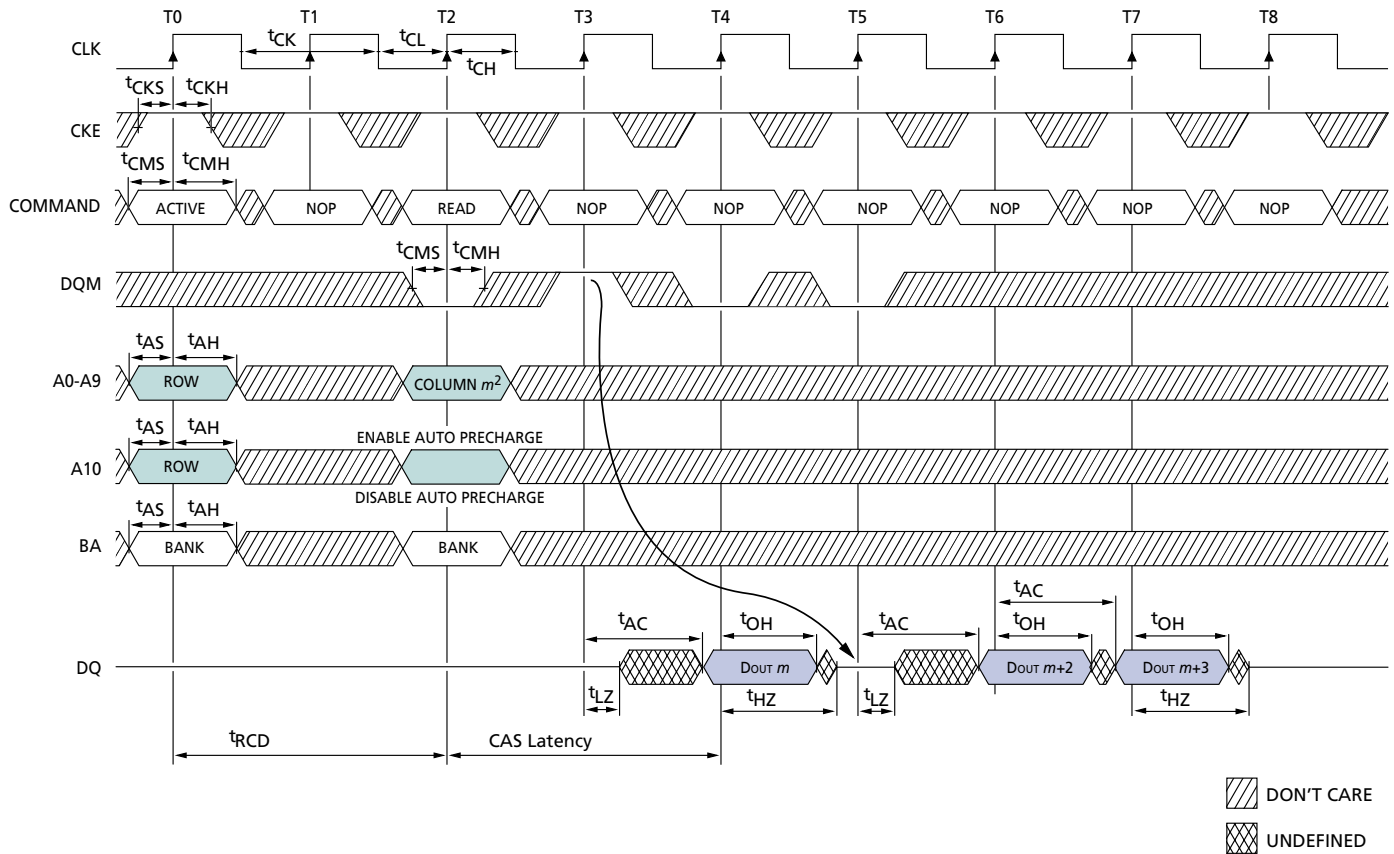
SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
t <sub>AC</sub> (3)		6		7.5	ns
t <sub>AC</sub> (2)		9		9	ns
t <sub>AH</sub>	1		1		ns
t <sub>AS</sub>	2		3		ns
t <sub>CH</sub>	3		3.5		ns
t <sub>CL</sub>	3		3.5		ns
t <sub>CK</sub> (3)	8		10		ns
t <sub>CK</sub> (2)	12		15		ns
t <sub>CKH</sub>	1		1		ns

SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
t <sub>CKS</sub>	2		3		ns
t <sub>CMH</sub>	1		1		ns
t <sub>CMS</sub>	2		3		ns
t <sub>HZ</sub> (3)		6		8	ns
t <sub>HZ</sub> (2)		7		10	ns
t <sub>LZ</sub>	1		2		ns
t <sub>OH</sub>	3		3		ns
t <sub>RCD</sub>	20		30		ns

\*CAS latency indicated in parentheses.

**NOTE:** 1. For this example, the CAS latency = 2.  
 2. Column-address A9 is a "Don't Care" on x8 version.  
 3. Page left open; no t<sub>RP</sub>.

## READ – DQM OPERATION <sup>1</sup>



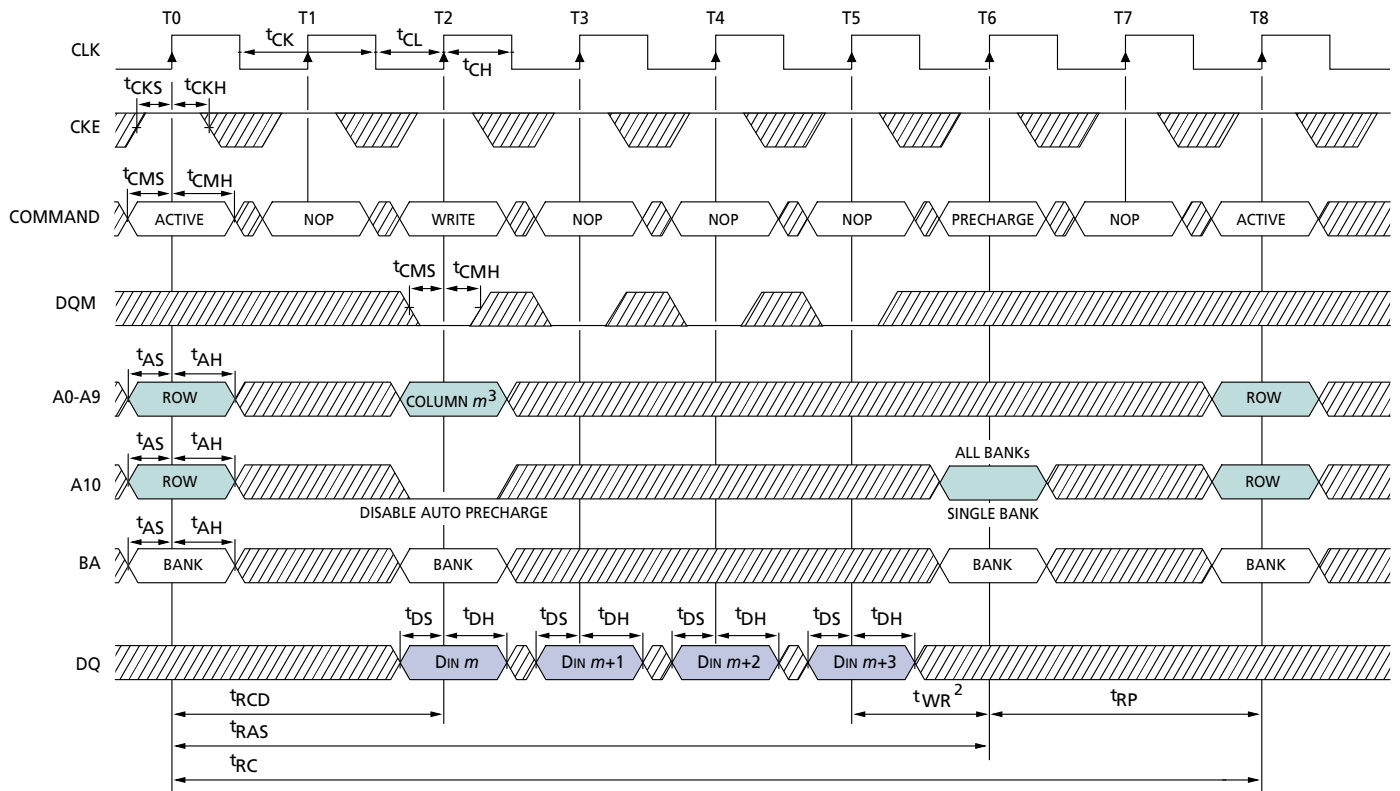
## TIMING PARAMETERS

SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
$t_{AC(3)}$		6		7.5	ns
$t_{AC(2)}$		9		9	ns
$t_{AH}$	1		1		ns
$t_{AS}$	2		3		ns
$t_{CH}$	3		3.5		ns
$t_{CL}$	3		3.5		ns
$t_{CK(3)}$	8		10		ns
$t_{CK(2)}$	12		15		ns
$t_{CKH}$	1		1		ns

SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
$t_{CKS}$	2		3		ns
$t_{CMH}$	1		1		ns
$t_{CMS}$	2		3		ns
$t_{HZ(3)}$		6		8	ns
$t_{HZ(2)}$		7		10	ns
$t_{LZ}$	1		2		ns
$t_{OH}$	3		3		ns
$t_{RCD}$	20		30		ns

\*CAS latency indicated in parentheses.

**NOTE:** 1. For this example, the burst length = 4, and the CAS latency = 2.  
2. Column-address A9 is a "Don't Care" on x8 version.

**WRITE – WITHOUT AUTO PRECHARGE <sup>1</sup>**


DON'T CARE  
 UNDEFINED

**TIMING PARAMETERS**

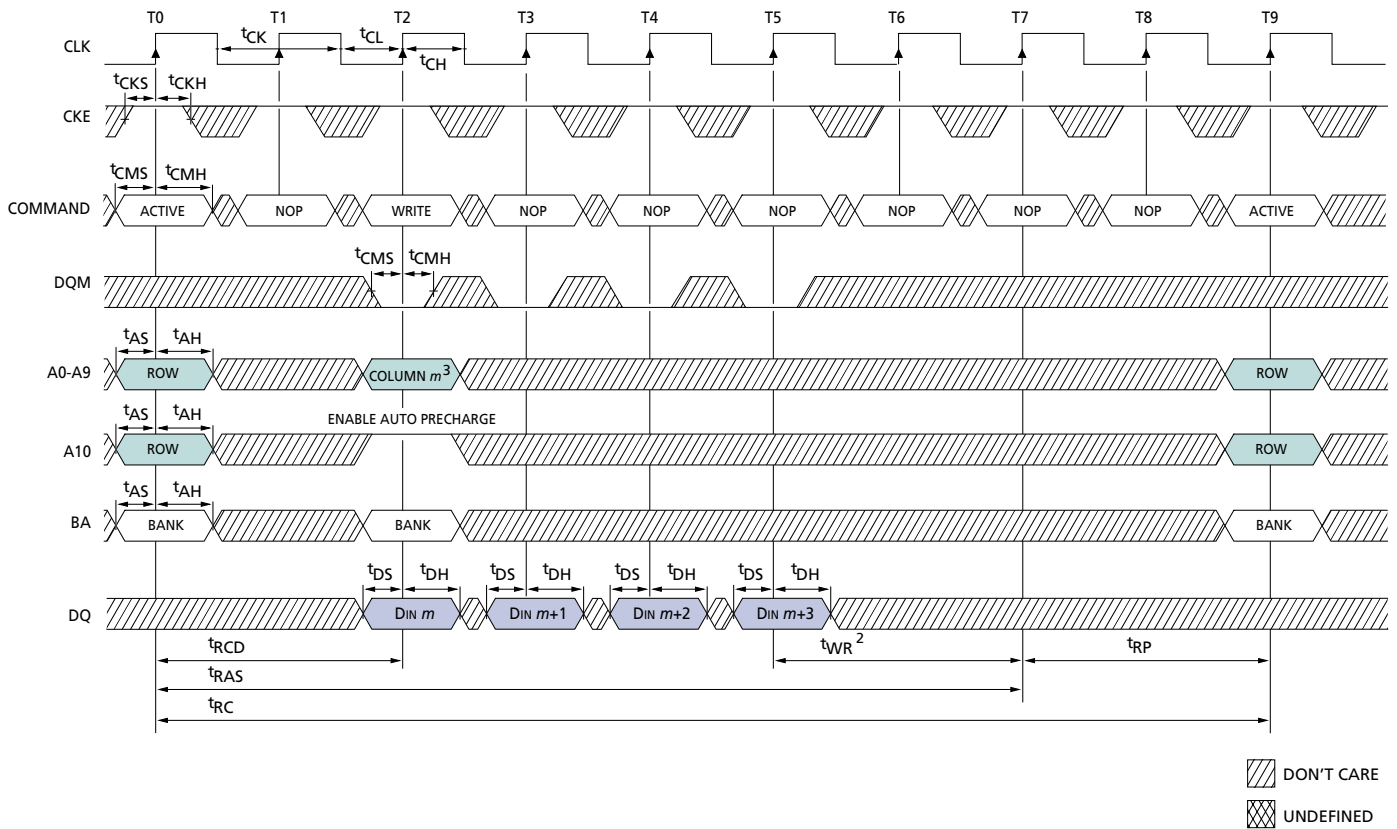
SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
t <sub>AH</sub>	1		1		ns
t <sub>AS</sub>	2		3		ns
t <sub>CH</sub>	3		3.5		ns
t <sub>CL</sub>	3		3.5		ns
t <sub>CK</sub> (3)	8		10		ns
t <sub>CK</sub> (2)	12		15		ns
t <sub>CKH</sub>	1		1		ns
t <sub>CKS</sub>	2		3		ns
t <sub>CMH</sub>	1		1		ns

SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
t <sub>CMS</sub>	2		3		ns
t <sub>DH</sub>	1		1		ns
t <sub>DS</sub>	2		3		ns
t <sub>RAS</sub>	50	120,000	60	120,000	ns
t <sub>RC</sub>	80		90		ns
t <sub>RCD</sub>	20		30		ns
t <sub>RP</sub>	24		30		ns
t <sub>WR</sub> [A1]	10		10		ns
t <sub>WR</sub> [A2]	15		15		ns

\*CAS latency indicated in parentheses.

**NOTE:** 1. For this example, the burst length = 4, and the WRITE burst is followed by a “manual” PRECHARGE with the A1 version.  
 2. 10ns (A1) or 15ns (A2) are required between <DIN m+3> and the PRECHARGE command, regardless of frequency.  
 3. Column-address A9 is a “Don’t Care” on x8 version.

## WRITE – WITH AUTO PRECHARGE <sup>1</sup>



### TIMING PARAMETERS

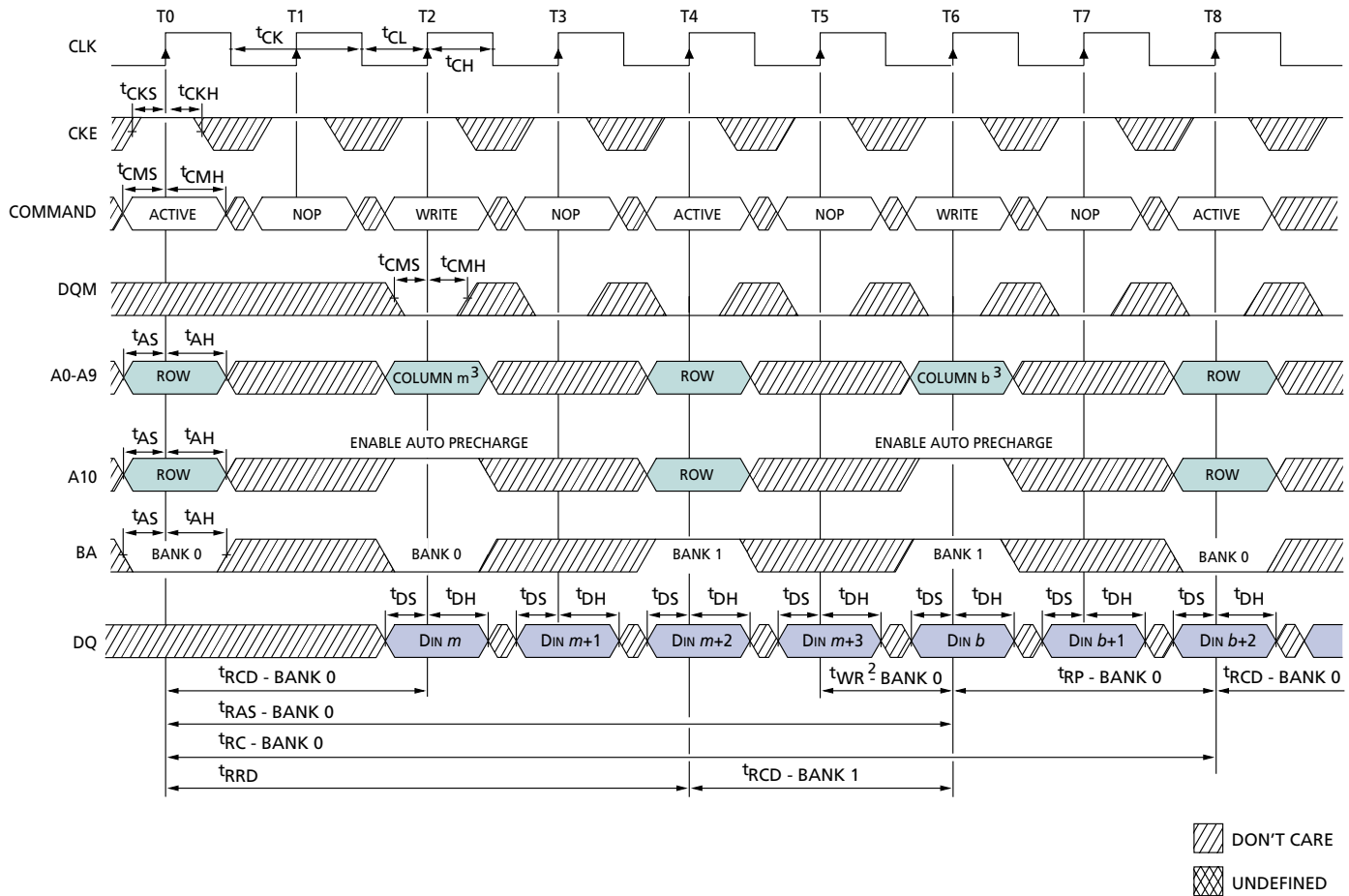
SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
$t_{AH}$	1		1		ns
$t_{AS}$	2		3		ns
$t_{CH}$	3		3.5		ns
$t_{CL}$	3		3.5		ns
$t_{CK} (3)$	8		10		ns
$t_{CK} (2)$	12		15		ns
$t_{CKH}$	1		1		ns
$t_{CKS}$	2		3		ns
$t_{CMH}$	1		1		ns

SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
$t_{CMS}$	2		3		ns
$t_{DH}$	1		1		ns
$t_{DS}$	2		3		ns
$t_{RAS}$	50	120,000	60	120,000	ns
$t_{RC}$	80		90		ns
$t_{RCD}$	20		30		ns
$t_{RP}$	24		30		ns
$t_{WR} [A1]$	1		1		$t_{CK}$
$t_{WR} [A2]$	2		2		$t_{CK}$

\*CAS latency indicated in parentheses.

- NOTE:**
- For this example, the burst length = 4 with the A2 version, i.e., two-clock minimum for  $t_{WR}$ .
  - The A1 version requires one clock between  $\langle D_{IN} m+3 \rangle$  and the PRECHARGE command, provided  $t_{WR}$  is met.
  - Column-address A9 is a "Don't Care" on x8 version.
  - With AUTO PRECHARGE.

## ALTERNATING BANK WRITE ACCESSES <sup>1</sup>



## TIMING PARAMETERS

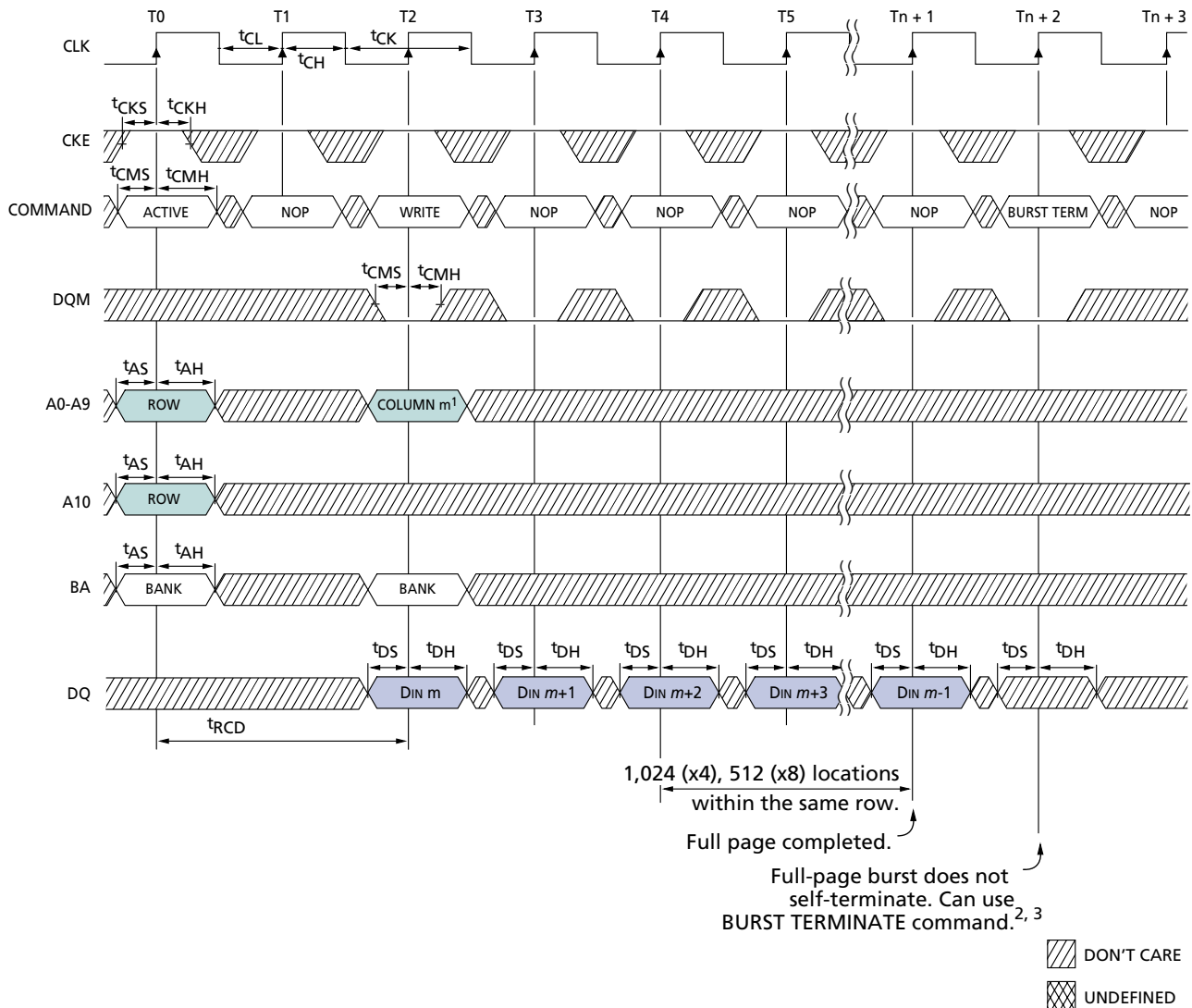
SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
$t_{AH}$	1		1		ns
$t_{AS}$	2		3		ns
$t_{CH}$	3		3.5		ns
$t_{CL}$	3		3.5		ns
$t_{CK}$ (3)	8		10		ns
$t_{CK}$ (2)	12		15		ns
$t_{CKH}$	1		1		ns
$t_{CKS}$	2		3		ns
$t_{CMH}$	1		1		ns
$t_{CMS}$	2		3		ns

SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
$t_{DH}$	1		1		ns
$t_{DS}$	2		3		ns
$t_{RAS}$	50	120,000	60	120,000	ns
$t_{RC}$	80		90		ns
$t_{RCD}$	20		30		ns
$t_{RP}$	24		30		ns
$t_{RRD}$	20		20		ns
$t_{WR}$ [A1]	Note 2		Note 2		—
$t_{WR}$ [A2]	Note 2		Note 2		—

\*CAS latency indicated in parentheses.

- NOTE:**
- For this example, the burst length = 4 with the A2 version, i.e., one-clock minimum for  $t_{WR}$ .
  - The A1 version requires one clock with AUTO PRECHARGE or 10ns with PRECHARGE between  $\langle D_{IN\ m+3} \rangle$  and the PRECHARGE command. The A2 version requires two clocks with AUTO PRECHARGE or 15ns with PRECHARGE.
  - Column-address A9 is a "Don't Care" on x8 version.

### WRITE – FULL-PAGE BURST



### TIMING PARAMETERS

SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
$t_{AH}$	1		1		ns
$t_{AS}$	2		3		ns
$t_{CH}$	3		3.5		ns
$t_{CL}$	3		3.5		ns
$t_{CK}$ (3)	8		10		ns
$t_{CK}$ (2)	12		15		ns
$t_{CKH}$	1		1		ns

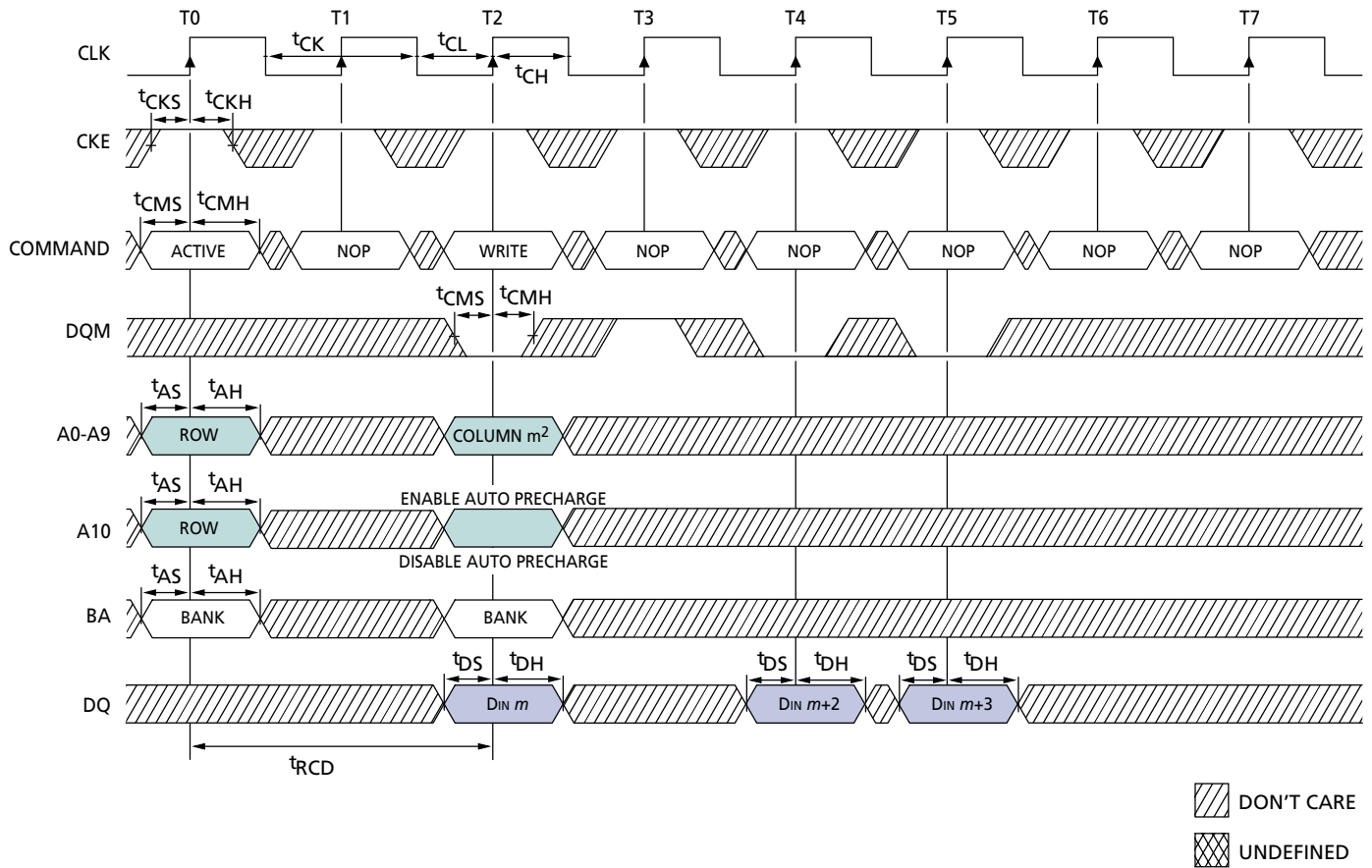
SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
$t_{CKS}$	2		3		ns
$t_{CMH}$	1		1		ns
$t_{CMS}$	2		3		ns
$t_{DH}$	1		1		ns
$t_{DS}$	2		3		ns
$t_{RCD}$	20		30		ns

\*CAS latency indicated in parentheses.

**NOTE:** 1. Column-address A9 is a "Don't Care" on x8 version.  
 2.  $t_{WR}$  must be satisfied prior to PRECHARGE command.  
 3. Page left open, no  $t_{RP}$ .



## WRITE – DQM OPERATION <sup>1</sup>



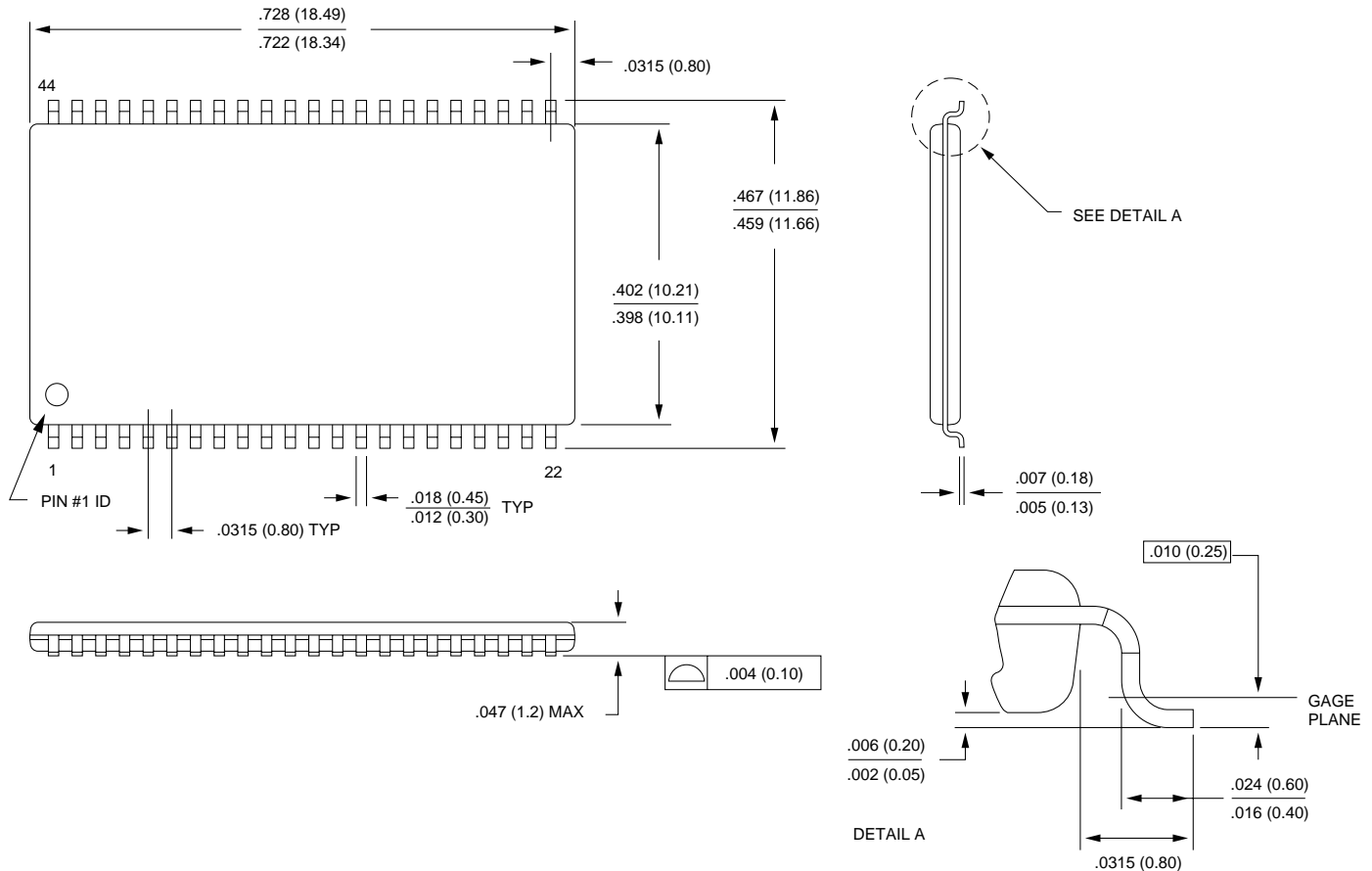
## TIMING PARAMETERS

SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
$t_{AH}$	1		1		ns
$t_{AS}$	2		3		ns
$t_{CH}$	3		3.5		ns
$t_{CL}$	3		3.5		ns
$t_{CK} (3)$	8		10		ns
$t_{CK} (2)$	12		15		ns
$t_{CKH}$	1		1		ns

SYMBOL*	-8B		-10		UNITS
	MIN	MAX	MIN	MAX	
$t_{CKS}$	2		3		ns
$t_{CMH}$	1		1		ns
$t_{CMS}$	2		3		ns
$t_{DH}$	1		1		ns
$t_{DS}$	2		3		ns
$t_{RCD}$	20		30		ns

\*CAS latency indicated in parentheses.

**NOTE:** 1. For this example, the burst length = 4.  
2. Column-address A9 is a "Don't Care" on x8 version.

**44-PIN PLASTIC TSOP (400 mil)**


- NOTE:** 1. All dimensions in inches (millimeters) MAX or typical where noted.  
MIN
2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.



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