X9401

Low Noise/Low Power/SPI Bus

Data Sheet | *October 12, 2006* | *FN8190.3*

Quad, 64 Tap, Digitally Controlled Potentiometer (XDCP™)

FEATURES

- **Quad–4 separate pots, 64 taps/pot**
- **Nonvolatile storage of wiper position**
- **Four Nonvolatile Data Registers for Each Pot**
- **16-bytes of EEPROM memory**
- **SPI serial interface**
- **R_{Total} = 10kΩ**
- **Wiper resistance = 150Ω typical**
- **Standby current < 1µA (total package)**
- **Operating current < 400µA max.**
- **V_{CC} = 2.7V to 5V**
- **Package–24 Ld SOIC**
- **100 year data retention**
- **Pb-free plus anneal available (RoHS compliant)**

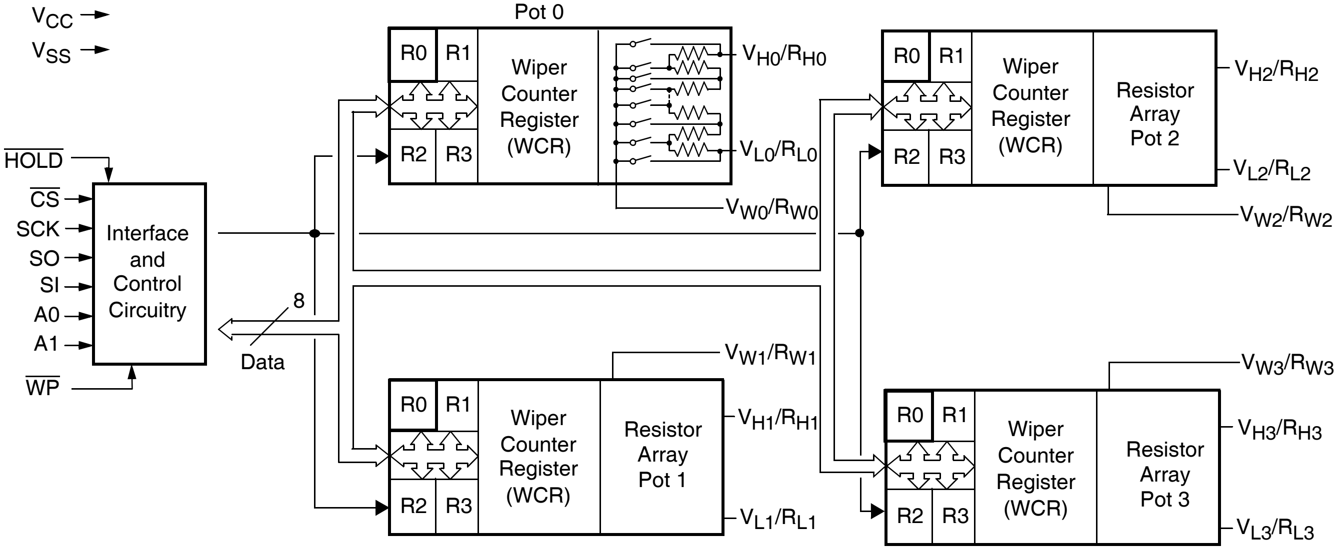
DESCRIPTION

The X9401 integrates 4 digitally controlled potentiometers (XDCP) on a monolithic CMOS integrated microcircuit.

The digitally controlled potentiometer is implemented using 64 resistive elements in a series array. Between each element are tap points connected to the wiper terminal through switches. The position of the wiper on the array is controlled by the user through the SPI bus interface. Each potentiometer has associated with it a volatile Wiper Counter Register (WCR) and 4 nonvolatile Data Registers (DR0:DR3) that can be directly written to and read by the user. The contents of the WCR controls the position of the wiper on the resistor array through the switches. Power-up recalls the contents of DR0 to the WCR.

The XDCP can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

BLOCK DIAGRAM



Ordering Information

PART NUMBER	PART MARKING	V_{CC} LIMITS (V)	POTENTIOMETER ORGANIZATION (kΩ)	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
X9401WS24IZ (Note)	X9401WS ZI	5 ±10%	10	-40 to 85	24 Ld SOIC (300 mil) (Pb-free)	MDP0027
X9401WS24I-2.7*	X9401WS G	2.7 to 5.5	10	-40 to 85	24 Ld SOIC (300 mil)	M24.3
X9401WS24IZ-2.7* (Note)	X9401WS ZG			-40 to 85	24 Ld SOIC (300 mil) (Pb-free)	MDP0027

*Add "T1" suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

PIN DESCRIPTIONS

Host Interface Pins

Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

Serial Input

SI is the serial data input pin. All opcodes, byte addresses and data to be written to the pots and pot registers are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Clock (SCK)

The SCK input is used to clock data into and out of the X9401.

Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X9401 is deselected and the SO pin is at high impedance, and (unless an internal write cycle is underway) the device will be in the standby state. $\overline{CS}$ LOW enables the X9401, placing it in the active power mode. It should be noted that after a power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

Hold ($\overline{HOLD}$)

$\overline{HOLD}$ is used in conjunction with the $\overline{CS}$ pin to select the device. Once the part is selected and a serial sequence is underway, $\overline{HOLD}$ may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, $\overline{HOLD}$ must be brought LOW while SCK is LOW. To resume communication, $\overline{HOLD}$ is brought HIGH, again while SCK is LOW. If the pause feature is not used, $\overline{HOLD}$ should be held HIGH at all times.

Device Address (A_0 - A_1)

The address inputs are used to set the least significant 2 bits of the 8-bit slave address. A match in the slave address serial data stream must be made with the address input in order to initiate communication with the X9401. A maximum of 4 devices may occupy the SPI serial bus.

Potentiometer Pins

V_H (V_{H0} - V_{H3}), V_L (V_{L0} - V_{L3}), R_H (R_{H0} - R_{H3}), R_L (R_{L0} - R_{L3})

The V_H/R_H and V_L/R_L inputs are equivalent to the terminal connections on either end of a mechanical potentiometer.

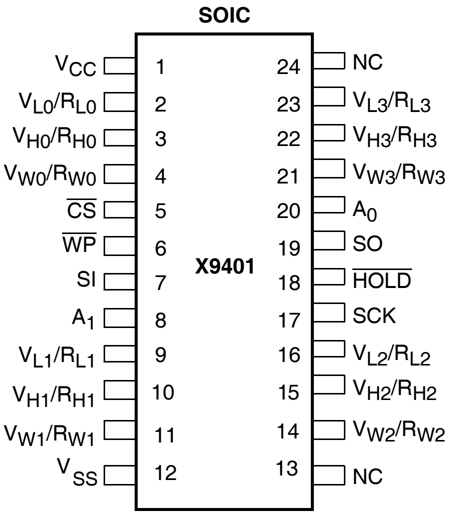
V_W (V_{W0} - V_{W3}), R_W (R_{W0} - R_{W3})

The wiper outputs are equivalent to the wiper output of a mechanical potentiometer.

Hardware Write Protect Input ($\overline{WP}$)

The $\overline{WP}$ pin when LOW prevents nonvolatile writes to the Wiper Counter Registers.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
SCK	Serial Clock
SI, SO	Serial Data
A_0 - A_1	Device Address
V_{H0}/R_{H0} - V_{H3}/R_{H3}, V_{L0}/R_{L0} - V_{L3}/R_{L3}	Potentiometers (terminal equivalent)
V_{W0}/R_{W0} - V_{W1}/R_{W1}	Potentiometers (wiper equivalent)
$\overline{WP}$	Hardware Write Protection
V_{CC}	System Supply Voltage
V_{SS}	System Ground
NC	No Connection

DEVICE DESCRIPTION

The X9401 is a highly integrated microcircuit incorporating four resistor arrays and their associated registers and counters and the serial interface logic providing direct communication between the host and the XDCP potentiometers.

Serial Interface

The X9401 supports the SPI interface hardware conventions. The device is accessed via the SI input with data clocked in on the rising SCK. $\overline{CS}$ must be LOW and the $\overline{HOLD}$ and $\overline{WP}$ pins must be HIGH during the entire operation.

The SO and SI pins can be connected together, since they have three state outputs. This can help to reduce system pin count.

Array Description

The X9401 is comprised of four resistor arrays. Each array contains 63 discrete resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (V_H/R_H and V_L/R_L inputs).

At both ends of each array and between each resistor segment is a CMOS switch connected to the wiper (V_W/R_W) output. Within each individual array only one switch may be turned on at a time.

These switches are controlled by a Wiper Counter Register (WCR). The six bits of the WCR are decoded to select, and enable, one of sixty-four switches.

Wiper Counter Register (WCR)

The X9401 contains four Wiper Counter Registers, one for each XDCP potentiometer. The WCR is equivalent to a serial-in, parallel-out register/counter with its outputs decoded to select one of sixty-four switches along its resistor array. The contents of the WCR can be altered in four ways: it may be written directly by the host via the Write Wiper Counter Register instruction (serial load); it may be written indirectly by transferring the contents of one of four associated data registers via the XFR Data Register or Global XFR Data Register instructions (parallel load); it can be modified one step at a time by the Increment/Decrement instruction. Finally, it is loaded with the contents of its data register zero (R0) upon power-up.

The Wiper Counter Register is a volatile register; that is, its contents are lost when the X9401 is powered-down. Although the register is automatically loaded with the value in R_0 upon power-up, this may be different from the value present at power-down. The wiper position must be stored in R_0 to insure restoring the wiper position after power-up.

Data Registers

Each potentiometer has four 6-bit nonvolatile data registers. These can be read or written directly by the host. Data can also be transferred between any of the four data registers and the associated Wiper Counter Register. All operations changing data in one of the data registers is a nonvolatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, the data registers can be used as memory locations for system parameters or user preference data.

Data Register Detail

(MSB) (LSB)

D5	D4	D3	D2	D1	D0
NV	NV	NV	NV	NV	NV

Write in Process

The contents of the Data Registers are saved to nonvolatile memory when the $\overline{CS}$ pin goes from LOW to HIGH after a complete write sequence is received by the device. The progress of this internal write operation can be monitored by a Write In Process bit (WIP). The WIP bit is read with a Read Status command.

INSTRUCTIONS

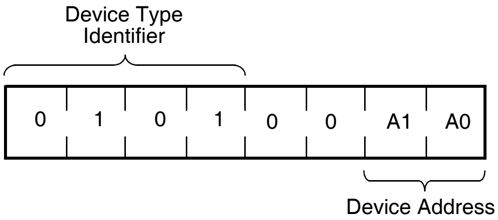
Identification (ID) Byte

The first byte sent to the X9401 from the host, following a $\overline{CS}$ going HIGH to LOW, is called the Identification byte. The most significant four bits of the slave address are a device type identifier, for the X9401 this is fixed as 0101[B] (refer to Figure 1).

The two least significant bits in the ID byte select one of four devices on the bus. The physical device address is defined by the state of the A_0 - A_1 input pins. The X9401 compares the serial data stream with the address input state; a successful compare of both address bits is required for the X9401 to successfully continue the command sequence. The A_0 - A_1 inputs can be actively driven by CMOS input signals or tied to V_{CC} or V_{SS}.

The remaining two bits in the slave byte must be set to 0.

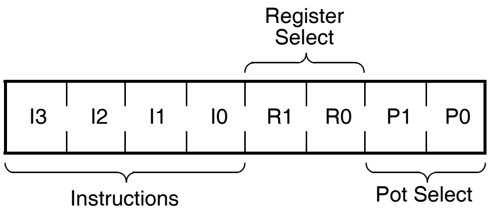
Figure 1. Identification Byte Format



Instruction Byte

The next byte sent to the X9401 contains the instruction and register pointer information. The four most significant bits are the instruction. The next four bits point to one of the four pots and, when applicable, they point to one of four associated registers. The format is shown below in Figure 2.

Figure 2. Instruction Byte Format



The four high order bits of the instruction byte specify the operation. The next two bits (R_1 and R_0) select one of the four registers that is to be acted upon when a register oriented instruction is issued. The last two bits (P1 and P_0) selects which one of the four potentiometers is to be affected by the instruction.

Four of the ten instructions are two bytes in length and end with the transmission of the instruction byte. These instructions are:

- – XFR Data Register to Wiper Counter Register—This transfers the contents of one specified Data Register to the associated Wiper Counter Register.
- – XFR Wiper Counter Register to Data Register—This transfers the contents of the specified Wiper Counter Register to the specified associated Data Register.
- – Global XFR Data Register to Wiper Counter Register —This transfers the contents of all specified Data Registers to the associated Wiper Counter Registers.
- – Global XFR Wiper Counter Register to Data Register—This transfers the contents of all Wiper Counter Registers to the specified associated Data Registers.

The basic sequence of the two byte instructions is illustrated in Figure 3. These two-byte instructions exchange data between the WCR and one of the data registers. A transfer from a data register to a WCR is essentially a write to a static RAM, with the static RAM controlling the wiper position. The response of the wiper to this action will be delayed by t_{WRL}. A transfer from the WCR (current wiper position), to a data register is a write to nonvolatile memory and takes a minimum of t_{WR} to complete. The transfer can occur between one of the four potentiometers and one of its associated registers; or it may occur globally, where the transfer occurs between all potentiometers and one associated register.

Five instructions require a three-byte sequence to complete. These instructions transfer data between the host and the X9401; either between the host and one of the data registers or directly between the host and the Wiper Counter Register. These instructions are:

- Read Wiper Counter Register— read the current wiper position of the selected pot,
- Write Wiper Counter Register—change current wiper position of the selected pot,
- Read Data Register—read the contents of the selected data register;
- Write Data Register—write a new value to the selected data register.
- Read Status—This command returns the contents of the WIP bit which indicates if the internal write cycle is in progress.

The sequence of these operations is shown in Figure 4 and Figure 5.

The final command is Increment/Decrement. It is different from the other commands, because it's length is indeterminate. Once the command is issued, the master can clock the selected wiper up and/or down in one resistor segment steps; thereby, providing a fine tuning capability to the host. For each SCK clock pulse (t_{HIGH}) while SI is HIGH, the selected wiper will move one resistor segment towards the V_H/R_H terminal. Similarly, for each SCK clock pulse while SI is LOW, the selected wiper will move one resistor segment towards the V_L/R_L terminal. A detailed illustration of the sequence and timing for this operation are shown in Figure 6 and Figure 7.

Detailed Potentiometer Block Diagram

(One of Four Arrays)

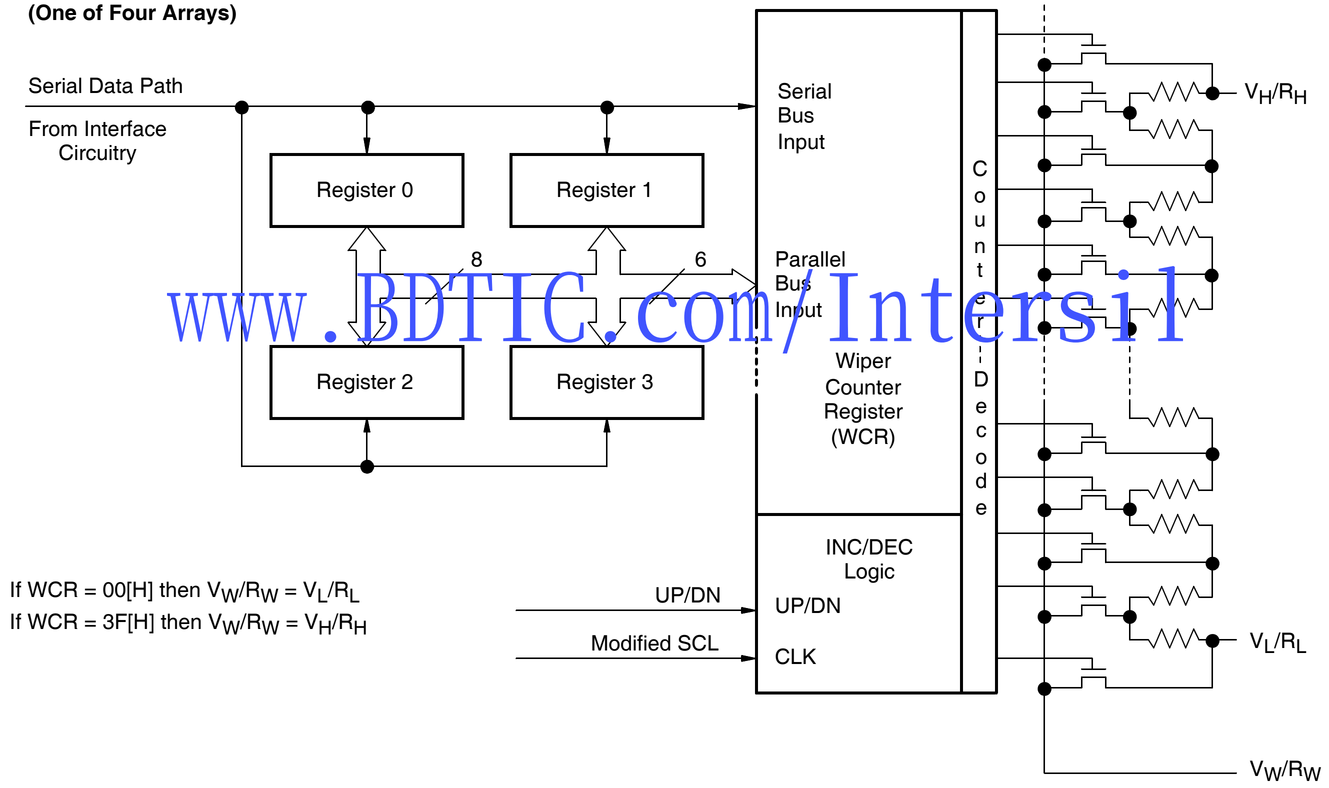


Figure 3. Two-Byte Command Sequence

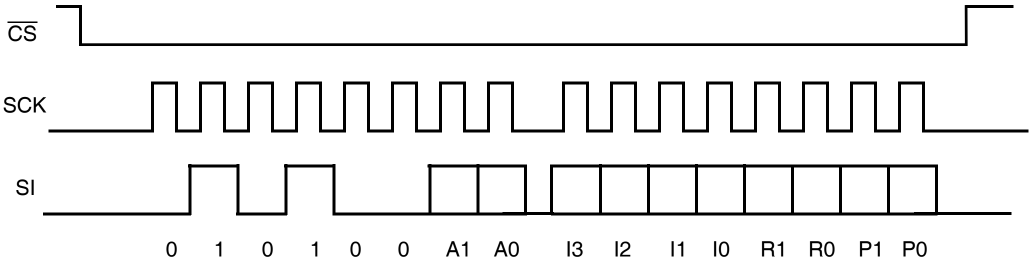


Figure 4. Three-Byte Command Sequence (Write)

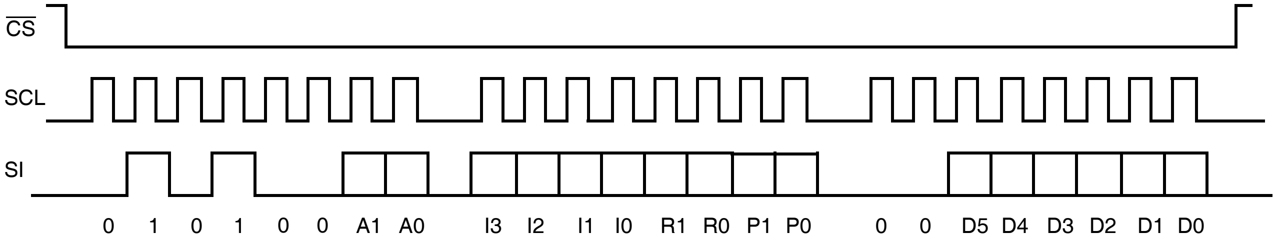


Figure 5. Three-Byte Command Sequence (Read)

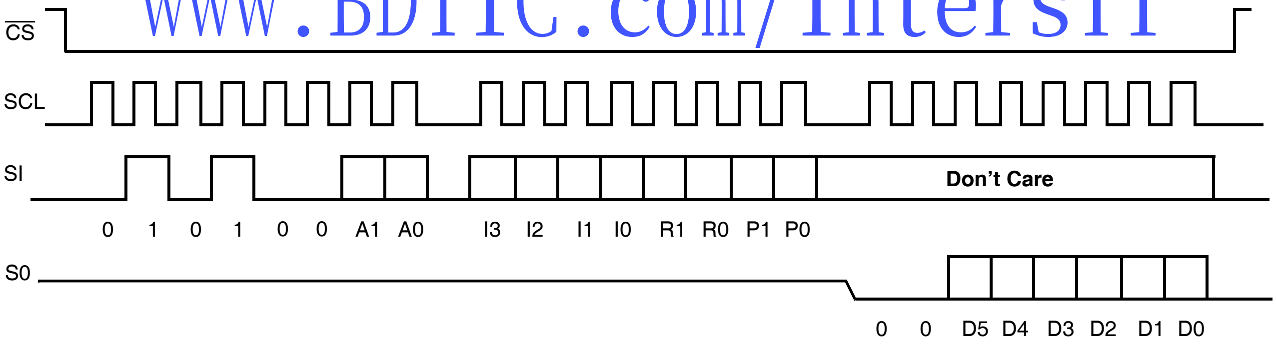


Figure 6. Increment/Decrement Command Sequence

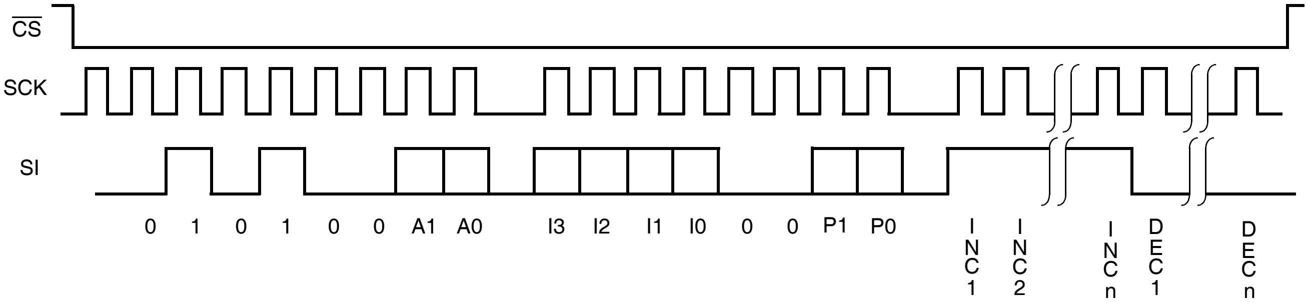


Figure 7. Increment/Decrement Timing Limits

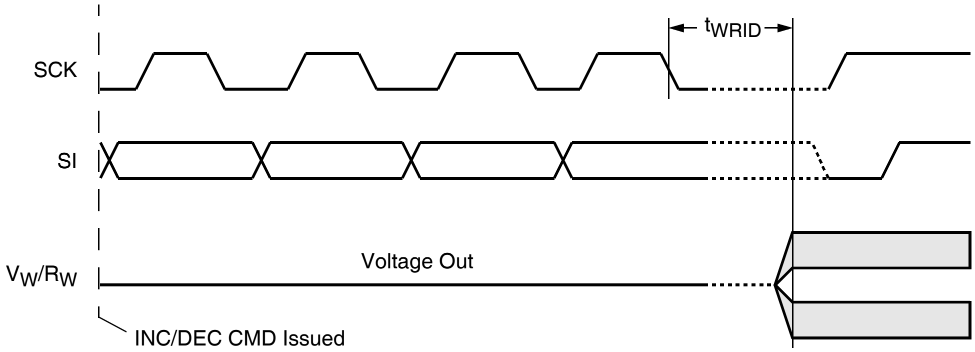


Table 1. Instruction Set

Instruction	Instruction Set								Operation
	I_3	I_2	I_1	I_0	R_1	R_0	P_1	P_0	
Read Wiper Counter Register	1	0	0	1	0	0	P_1	P_0	Read the contents of the Wiper Counter Register pointed to by P_1 - P_0
Write Wiper Counter Register	1	0	1	0	0	0	P_1	P_0	Write new value to the Wiper Counter Register pointed to by P_1 - P_0
Read Data Register	1	0	1	1	R_1	R_0	P_1	P_0	Read the contents of the Data Register pointed to by P_1 - P_0 and R_1 - R_0
Write Data Register	1	1	0	0	R_1	R_0	P_1	P_0	Write new value to the Data Register pointed to by P_1 - P_0 and R_1 - R_0
XFR Data Register to Wiper Counter Register	1	1	0	1	R_1	R_0	P_1	P_0	Transfer the contents of the Data Register pointed to by R_1 - R_0 to the Wiper Counter Register pointed to by P_1 - P_0
XFR Wiper Counter Register to Data Register	1	1	1	0	R_1	R_0	P_1	P_0	Transfer the contents of the Wiper Counter Register pointed to by P_1 - P_0 to the Register pointed to by R_1 - R_0
Global XFR Data Register to Wiper Counter Register	0	0	0	1	R_1	R_0	0	0	Transfer the contents of the Data Registers pointed to by R_1 - R_0 of all four pots to their respective Wiper Counter Register
Global XFR Wiper Counter Register to Data Register	1	0	0	0	R_1	R_0	0	0	Transfer the contents of all Wiper Counter Registers to their respective data Registers pointed to by R_1 - R_0 of all four pots
Increment/Decrement Wiper Counter Register	0	0	1	0	0	0	P_1	P_0	Enable Increment/decrement of the Wiper Counter Register pointed to by P_1 - P_0
Read Status (WIP bit)	0	1	0	1	0	0	0	1	Read the status of the internal write cycle, by checking the WIP bit.

Instruction Format

Notes: (1) "A1 ~ A0": stands for the device addresses sent by the master.
(2) WPx refers to wiper position data in the Counter Register
(3) "I": stands for the increment operation, SI held HIGH during active SCK phase (high).
(4) "D": stands for the decrement operation, SI held LOW during active SCK phase (high).

Read Wiper Counter Register (WCR)

CS Falling Edge	device type identifier				device addresses				instruction opcode				WCR addresses				wiper position (sent by X9401 on SO)								CS Rising Edge
	0	1	0	1	0	0	A1	A0	1	0	0	1	0	0	P1	P0	0	0	WP5	WP4	WP3	WP2	WP1	WP0	

Write Wiper Counter Register (WCR)

CS Falling Edge	device type identifier				device addresses				instruction opcode				WCR addresses				Data Byte (sent by Host on SI)								CS Rising Edge
	0	1	0	1	0	0	A1	A0	1	0	1	0	0	0	P1	P0	0	0	WP5	WP4	WP3	WP2	WP1	WP0	

Read Data Register (DR)

CS Falling Edge	device type identifier				device addresses				instruction opcode				DR and WCR addresses				Data Byte (sent by X9401 on SO)								CS Rising Edge
	0	1	0	1	0	0	A1	A0	1	0	1	1	R1	R0	P1	P0	0	0	WP5	WP4	WP3	WP2	WP1	WP0	

Write Data Register (DR)

CS Falling Edge	device type identifier				device addresses				instruction opcode				DR and WCR addresses				Data Byte (sent by host on SI)								CS Rising Edge	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	0	0	A1	A0	1	1	0	0	R1	R0	P1	P0	0	0	WP5	WP4	WP3	WP2	WP1	WP0		

Transfer Data Register (DR) to Wiper Counter Register (WCR)

CS Falling Edge	device type identifier				device addresses				instruction opcode				DR and WCR addresses				CS Rising Edge
	0	1	0	1	0	0	A1	A0	1	1	0	1	R1	R0	P1	P0	

Transfer Wiper Counter Register (WCR) to Data Register (DR)

$\overline{CS}$ Falling Edge	device type identifier				device addresses				instruction opcode				DR and WCR addresses				$\overline{CS}$ Rising Edge	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	0	0	A1	A0	1	1	1	0	R1	R0	P1	P0		

Increment/Decrement Wiper Counter Register (WCR)

$\overline{CS}$ Falling Edge	device type identifier				device addresses				instruction opcode				WCR addresses				increment/decrement (sent by master on SDA)					$\overline{CS}$ Rising Edge
	0	1	0	1	0	0	A1	A0	0	0	1	0	X	X	P1	P0	I/D	I/D	. . . .	I/D	I/D	

Global Transfer Data Register (DR) to Wiper Counter Register (WCR)

$\overline{CS}$ Falling Edge	device type identifier				device addresses				instruction opcode				DR addresses				$\overline{CS}$ Rising Edge
	0	1	0	1	0	0	A1	A0	0	0	0	1	R1	R0	0	0	

Global Transfer Wiper Counter Register (WCR) to Data Register (DR)

$\overline{CS}$ Falling Edge	device type identifier				device addresses				instruction opcode				DR addresses				$\overline{CS}$ Rising Edge	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	0	0	A1	A0	1	0	0	0	R1	R0	0	0		

Read Status

$\overline{CS}$ Falling Edge	device type identifier				device addresses				instruction opcode				wiper addresses				Data Byte (sent by X9401 on SO)								$\overline{CS}$ Rising Edge
	0	1	0	1	0	0	A1	A0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	WIP	

ABSOLUTE MAXIMUM RATINGS

Temperature under bias .... -65°C to +135°C
Storage temperature .... -65°C to +150°C
Voltage on SCK, SCL or any address
input with respect to V_{SS}......................... -1V to +7V
$\Delta V = |(V_H – V_L)|$..5.5V
Lead temperature (soldering, 10s) .... +300°C

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; the functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	+70°C
Industrial	-40°C	+85°C

Device	Supply Voltage (V_{CC}) Limits
X9401	5V ± 10%
X9401-2.7	2.7V to 5.5V

ANALOG CHARACTERISTICS (Over recommended operating conditions unless otherwise stated.)

Symbol	Parameter	Limits				Test Condition
		Min.	Typ.	Max.	Unit	
R_{TOTAL}	End to end resistance	–20		+20	%	
	Power rating			50	mW	+25°C, each pot
I_W	Wiper current	–6		+6	mA	
R_W	Wiper resistance		150	500	Ω	Wiper Current = ± 3mA
V_{TERM}	Voltage on any V_H or V_L Pin	V_{SS}		V_{CC}	V	V_{SS} = 0V
	Noise		-120		dBV	Ref: 1kHz
	Resolution		1.6		%	
	Absolute linearity (1)	-1		+1	MI(3)	$V_{w(n)(actual)} - V_{w(n)(expected)}$
	Relative linearity (2)	-0.2		+0.2	MI(3)	$V_{w(n+1)} - [V_{w(n)} + MI]$
	Temperature coefficient of R_{TOTAL}		±300		ppm/°C	
	Ratiometric temp. coefficient			±20	ppm/°C	
$C_H/C_L/C_W$	Potentiometer capacitances		10/10/25		pF	See Macro model
I_{AL}	R_H, R_L, R_W leakage current		0.1	10	µA	$V_{IN} = V_{SS}$ to V_{CC}. Device is in stand-by mode.

POWER-UP AND DOWN REQUIREMENTS

The are no restrictions on the power-up or power-down conditions of V_{CC} and the voltages applied to the potentiometer pins provided that V_{CC} is always more positive than or equal to V_H, V_L, and V_W, i.e., $V_{CC} \geq V_H, V_L, V_W$. The V_{CC} power-up spec is always in effect.

Notes: (1) Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
(2) Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
(3) MI = RTOT/63 or $(V_H - V_L)/63$, single pot

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.	Max.	Unit	
I_{CC1}	V_{CC} supply current (active)			400	µA	f_{SCK} = 2MHz, SO = Open, Other Inputs = V_{SS}
I_{CC2}	V_{CC} supply current (nonvolatile write)			1	mA	f_{SCK} = 2MHz, SO = Open, Other Inputs = V_{SS}
I_{SB}	V_{CC} current (standby)			1	µA	SCK = SI = V_{SS}, Addr. = V_{SS}, CS = V_{CC}
I_{LI}	Input leakage current			10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current			10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IH}	Input HIGH voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{IL}	Input LOW voltage	-0.5		V_{CC} x 0.1	V	
V_{OL}	Output LOW voltage			0.4	V	I_{OL} = 3mA

ENDURANCE AND DATA RETENTION

Parameter	Min.	Unit
Minimum endurance	100,000	Data changes per bit per register
Data retention	100	years

CAPACITANCE

Symbol	Test	Max.	Unit	Test Condition
C_{OUT}(4)	Output capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}(4)	Input capacitance (A0, A1, SI, and SCK)	6	pF	V_{IN} = 0V

POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Unit
t_r V_{CC}(6)	V_{CC} Power-up rate	0.2	50	V/ms
t_{PUR}(5)	Power-up to initiation of read operation		1	ms
t_{PUW}(5)	Power-up to initiation of write operation		5	ms

A.C. TEST CONDITIONS

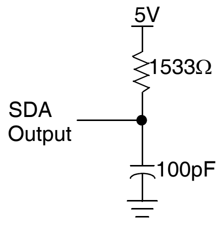
Input pulse levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10ns
Input and output timing level	V_{CC} x 0.5

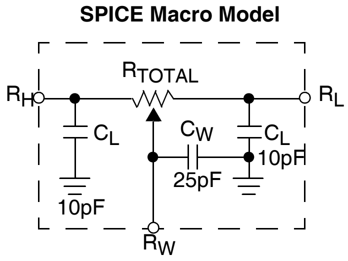
Notes: (4) This parameter is periodically sampled and not 100% tested

(5) t_{PUR} and t_{PUW} are the delays required from the time the (last) power supply (V_{CC}-) is stable until the specific instruction can be issued. These parameters are periodically sampled and not 100% tested.

(6) This is not a tested or guaranteed parameter and should be used only as a guideline.

EQUIVALENT A.C. LOAD CIRCUIT





AC TIMING

Symbol	Parameter	Min.	Max.	Unit
f_{SCK}	SSI/SPI clock frequency		2.0	MHz
t_{CYC}	SSI/SPI clock cycle rime	500		ns
t_{WH}	SSI/SPI clock high rime	200		ns
t_{WL}	SSI/SPI clock low time	200		ns
t_{LEAD}	Lead time	250		ns
t_{LAG}	Lag time	250		ns
t_{SU}	SI, SCK, $\overline{\text{HOLD}}$ and $\overline{\text{CS}}$ input setup time	50		ns
t_{H}	SI, SCK, $\overline{\text{HOLD}}$ and $\overline{\text{CS}}$ input hold time	50		ns
t_{RI}	SI, SCK, $\overline{\text{HOLD}}$ and $\overline{\text{CS}}$ input rise time		2	µs
t_{FI}	SI, SCK, $\overline{\text{HOLD}}$ and $\overline{\text{CS}}$ input fall time		2	µs
t_{DIS}	SO output disable time	0	500	ns
t_{V}	SO output valid time		100	ns
t_{HO}	SO output hold time	0		ns
t_{RO}	SO output rise time		50	ns
t_{FO}	SO output fall time		50	ns
t_{HOLD}	$\overline{\text{HOLD}}$ time	400		ns
t_{HSU}	$\overline{\text{HOLD}}$ setup time	100		ns
t_{HH}	$\overline{\text{HOLD}}$ hold time	100		ns
t_{HZ}	$\overline{\text{HOLD}}$ low to output in high Z		100	ns
t_{LZ}	$\overline{\text{HOLD}}$ high to output in low Z		100	ns
T_{I}	Noise suppression time constant at SI, SCK, $\overline{\text{HOLD}}$ and $\overline{\text{CS}}$ inputs		20	ns
t_{CS}	$\overline{\text{CS}}$ deselect time	2		µs
t_{WPASU}	$\overline{\text{WP}}$, A0 and A1 setup time	0		ns
t_{WPAH}	$\overline{\text{WP}}$, A0 and A1 hold time	0		ns

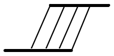
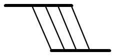
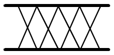
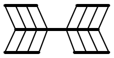
HIGH-VOLTAGE WRITE CYCLE TIMING

Symbol	Parameter	Typ.	Max.	Unit
t_{WR}	High-voltage write cycle time (store instructions)	5	10	ms

XDCP TIMING

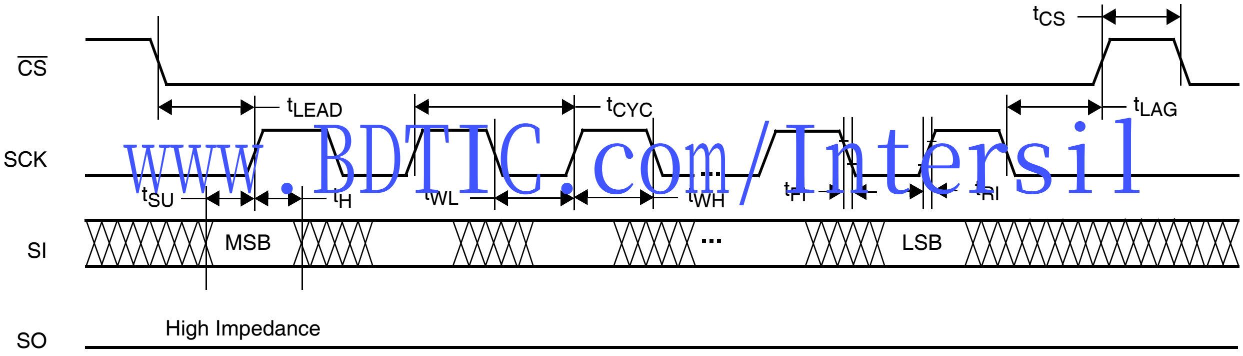
Symbol	Parameter	Min.	Max.	Unit
t_{WRPO}	Wiper response time after the third (last) power supply is stable		10	µs
t_{WRL}	Wiper response time after instruction issued (all load instructions)		10	µs
t_{WRID}	Wiper response time from an active SCL/SCK edge (increment/decrement instruction)		450	ns

SYMBOL TABLE

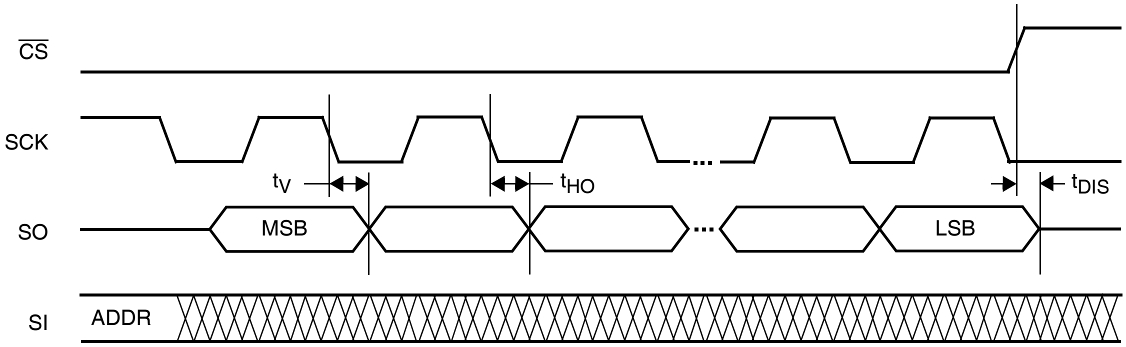
WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

TIMING DIAGRAMS

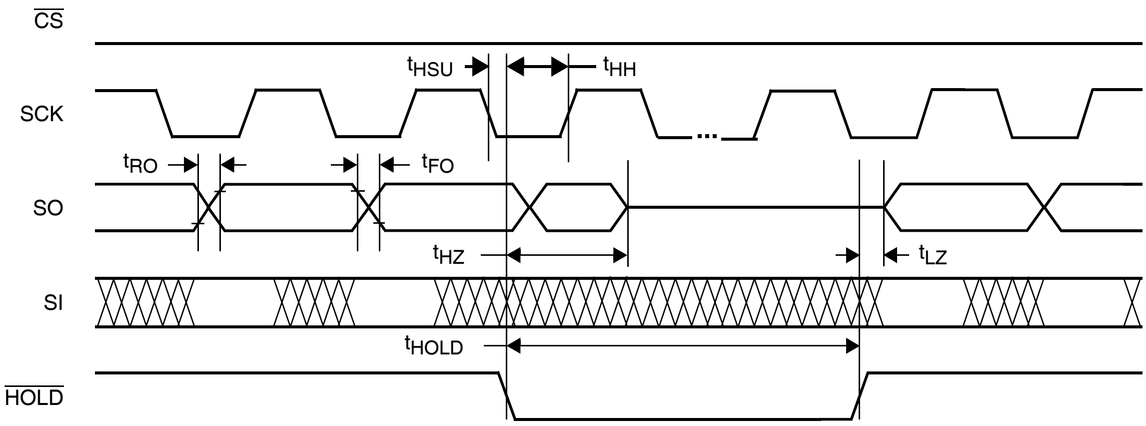
Input Timing



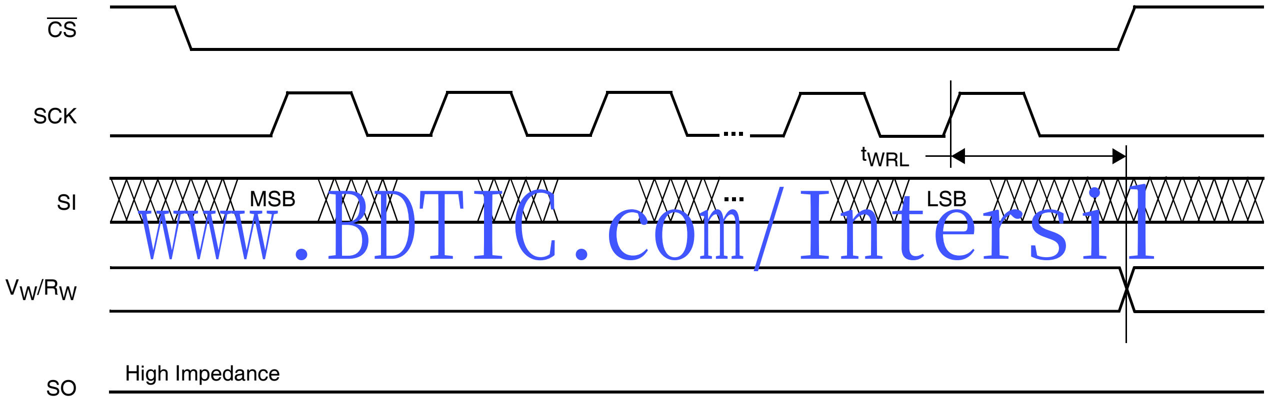
Output Timing



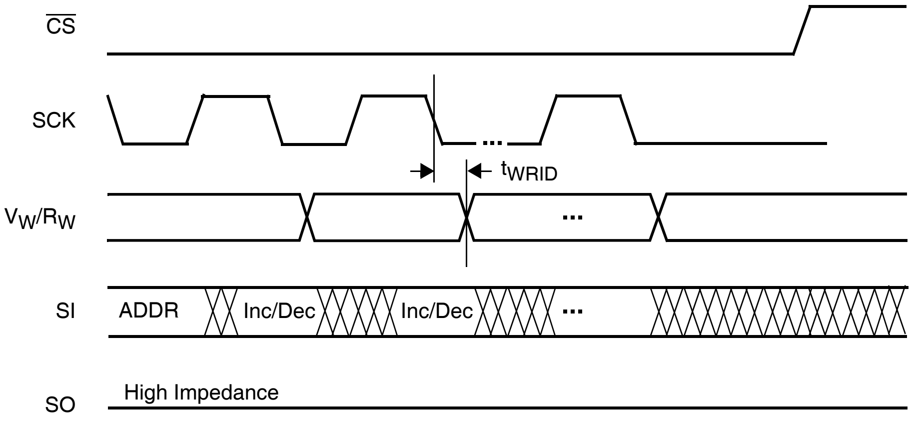
Hold Timing



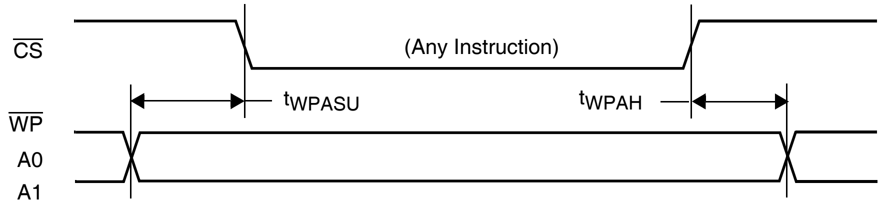
XDCP Timing (for All Load Instructions)



XDCP Timing (for Increment/Decrement Instruction)

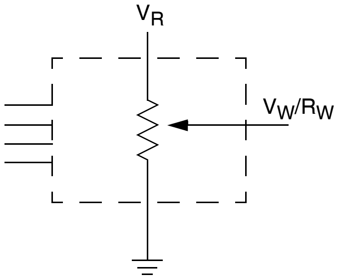


Write Protect and Device Address Pins Timing

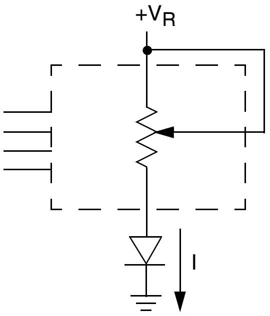


APPLICATIONS INFORMATION

Basic Configurations of Electronic Potentiometers



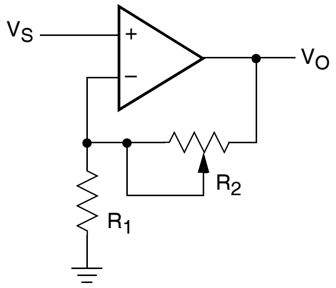
Three terminal Potentiometer;
Variable voltage divider



Two terminal Variable Resistor;
Variable current

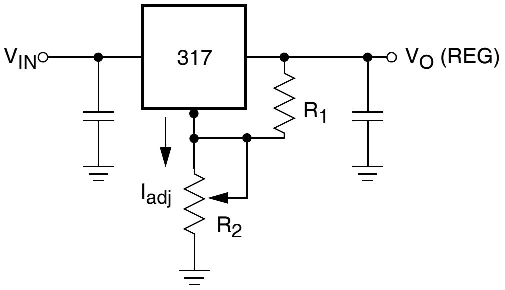
Application Circuits

NONINVERTING AMPLIFIER



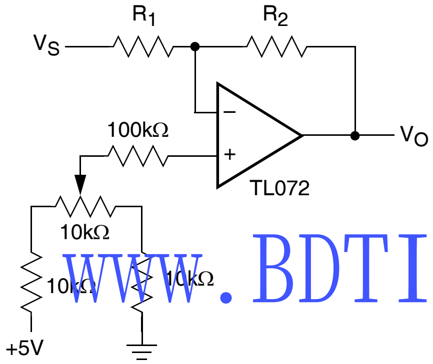
$V_O = (1+R_2/R_1)V_S$

VOLTAGE REGULATOR

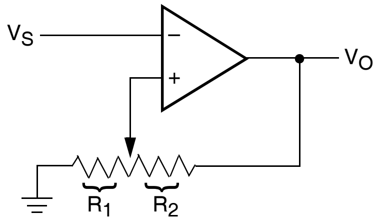


$V_O\ (REG) = 1.25V\ (1+R_2/R_1)+I_{adj}\ R_2$

OFFSET VOLTAGE ADJUSTMENT

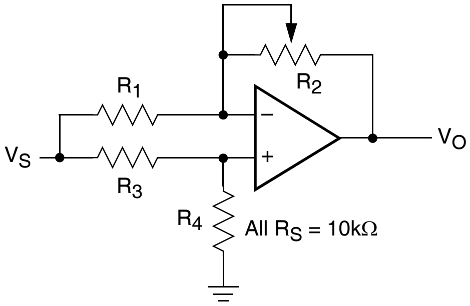


COMPARATOR WITH HYSTERESIS



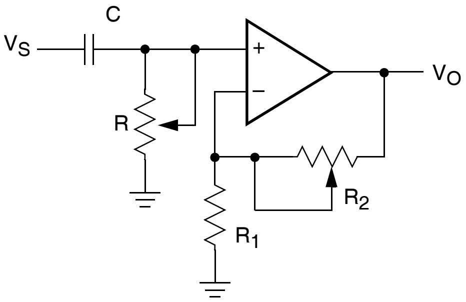
$V_{UL} = \{R_1/(R_1+R_2)\}\ V_O(max)$
$V_{LL} = \{R_1/(R_1+R_2)\}\ V_O(min)$

ATTENUATOR



$V_O = G\ V_S$
$-1/2 \leq G \leq +1/2$

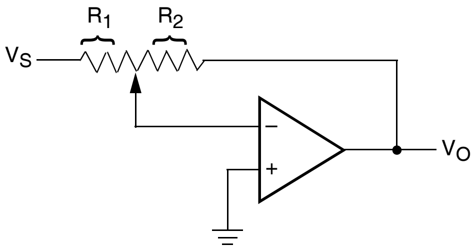
FILTER



$G_O = 1 + R_2/R_1$
$fc = 1/(2\pi RC)$

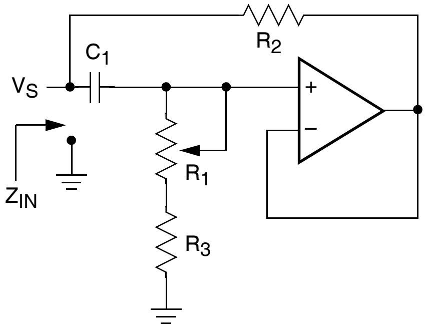
Application Circuits (continued)

INVERTING AMPLIFIER



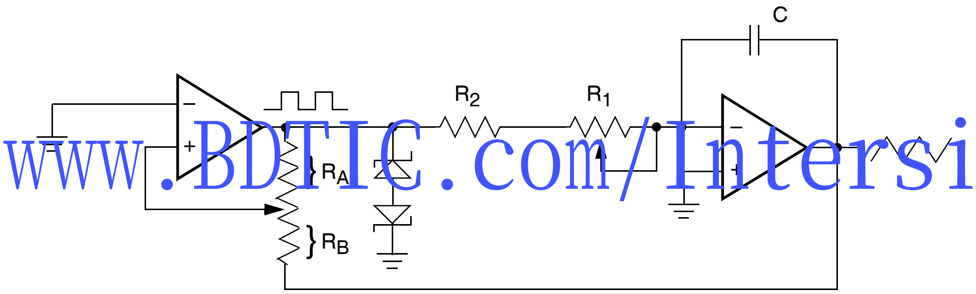
$V_O = G\ V_S$
$G = -\ R_2/R_1$

EQUIVALENT L-R CIRCUIT



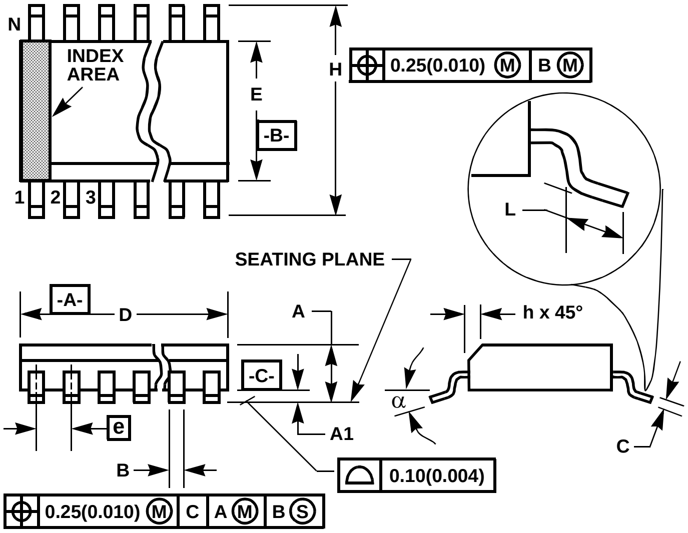
$Z_{IN} = R_2 + s\ R_2\ (R_1 + R_3)\ C_1 = R_2 + s\ Leq$
$(R_1 + R_3) >> R_2$

FUNCTION GENERATOR



frequency ∝ R_1, R_2, C
amplitude ∝ R_A, R_B

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M24.3 (JEDEC MS-013-AD ISSUE C)

24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.020	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.5985	0.6141	15.20	15.60	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0°	8°	0°	8°	-

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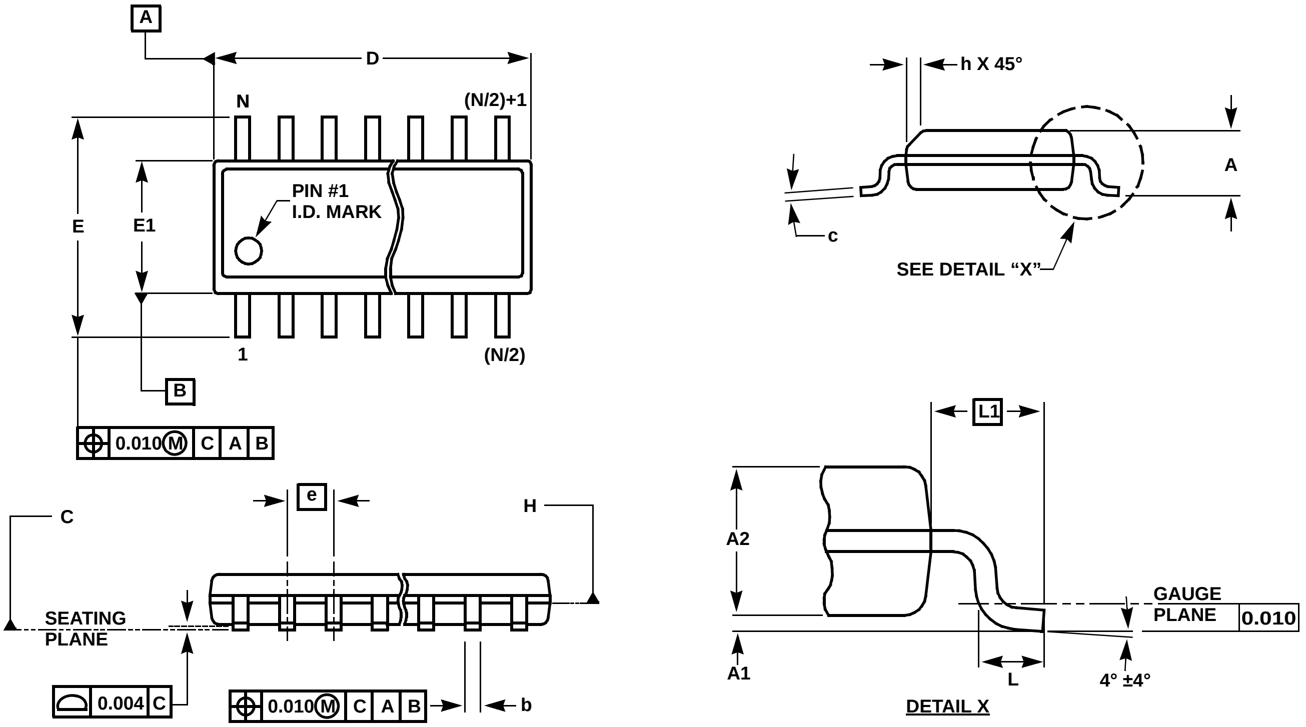
Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

SYMBOL	SO-8	SO-14	SO16 (0.150”)	SO16 (0.300”) (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)	TOLERANCE	NOTES
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

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NOTES:

1. Plastic or metal protrusions of 0.006” maximum per side are not included.
2. Plastic interlead protrusions of 0.010” maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994

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