## Quad Digitally Controlled Potentiometers (XDCP™)

### FEATURES

- **Four potentiometers in one package**
- **256 resistor taps/pot - 0.4% resolution**
- **SPI serial interface**
- **Wiper resistance, 40$\Omega$ typical @ $V_{CC}$ = 5V**
- **Four nonvolatile data registers for each pot**
- **Nonvolatile storage of wiper position**
- **Standby current < 5µA max (total package)**
- **Power supplies**
  - **—$V_{CC}$ = 2.7V to 5.5V**
  - **—V+ = 2.7V to 5.5V**
  - **—V− = -2.7V to -5.5V**
- **100k$\Omega$, 50k$\Omega$ total pot resistance**
- **High reliability**
  - **—Endurance – 100,000 data changes per bit per register**
  - **—Register data retention - 100 years**
- **24 Ld SOIC, 24 Ld TSSOP**
- **Dual supply version of X9251**
- **Pb-free plus anneal available (RoHS compliant)**

### DESCRIPTION

The X9250 integrates 4 digitally controlled potentiometers (XDCP) on a monolithic CMOS integrated circuit.

The digitally controlled potentiometer is implemented using 255 resistive elements in a series array. Between each element are tap points connected to the wiper terminal through switches. The position of the wiper on the array is controlled by the user through the SPI bus interface. Each potentiometer has associated with it a volatile Wiper Counter Register (WCR) and 4 nonvolatile Data Registers (DR0:DR3) that can be directly written to and read by the user. The contents of the WCR controls the position of the wiper on the resistor array though the switches. Power up recalls the contents of DR0 to the WCR.

The XDCP can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

### BLOCK DIAGRAM
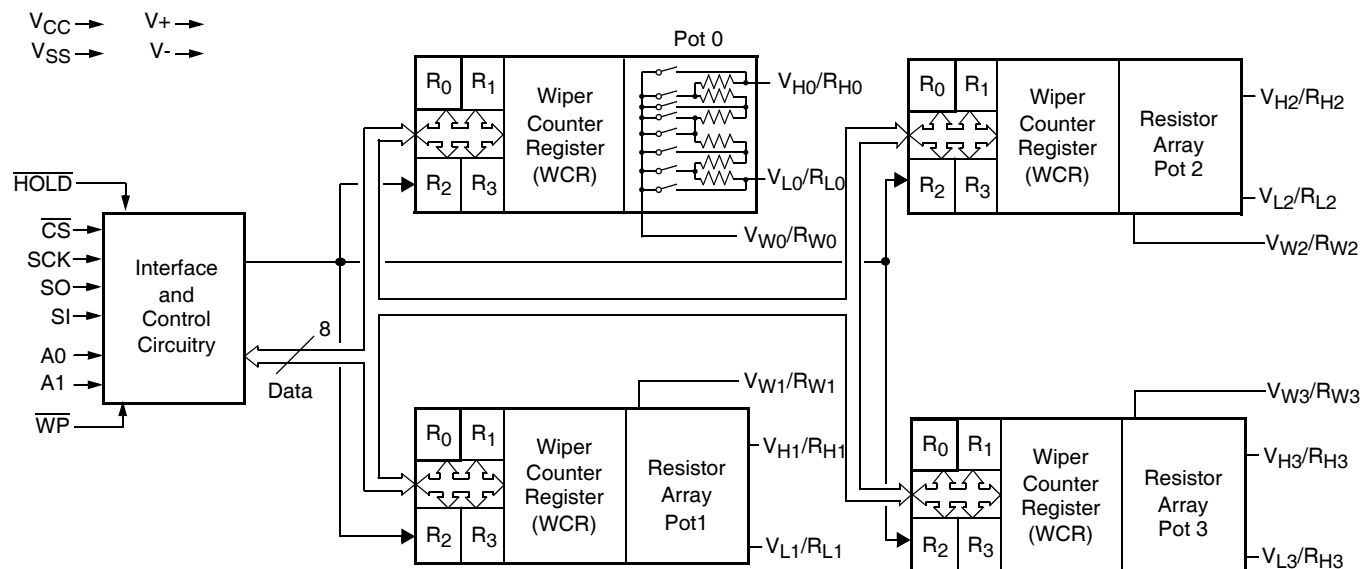
## Ordering Information

| PART NUMBER | PART MARKING | $V_{CC}$ LIMITS (V) | POTENTIOMETER ORGANIZATION (k$\Omega$) | TEMP. RANGE (°C) | PACKAGE | PKG. DWG. # |
|---|---|---|---|---|---|---|
| X9250TS24I | X9250TS I | 5 ±10% | 100 | -40 to +85 | 24 Ld SOIC (300 mil) | M24.3 |
| X9250TS24IZ (Note) | X9250TS ZI | | | -40 to +85 | 24 Ld SOIC (300 mil) (Pb-free) | M24.3 |
| X9250TV24I | X9250TV I | | | -40 to +85 | 24 Ld TSSOP (4.4mm) | MDP0044 |
| X9250TV24IZ (Note) | X9250TV ZI | | | -40 to +85 | 24 Ld TSSOP (4.4mm) (Pb-free) | MDP0044 |
| X9250US24 | X9250US | | 50 | 0 to +70 | 24 Ld SOIC (300 mil) | M24.3 |
| X9250US24Z (Note) | X9250US Z | | | 0 to +70 | 24 Ld SOIC (300 mil) (Pb-free) | M24.3 |
| X9250US24I | X9250US I | | | -40 to +85 | 24 Ld SOIC (300 mil) | M24.3 |
| X9250US24IZ (Note) | X9250US ZI | | | -40 to +85 | 24 Ld SOIC (300 mil) (Pb-free) | M24.3 |
| X9250UV24I | X9250UV I | | | -40 to +85 | 24 Ld TSSOP (4.4mm) | MDP0044 |
| X9250UV24IZ (Note) | X9250UV ZI | | | -40 to +85 | 24 Ld TSSOP (4.4mm) (Pb-free) | MDP0044 |
| X9250TS24-2.7 | X9250TS F | -2.7 to 5.5 | 100 | 0 to +70 | 24 Ld SOIC (300 mil) | M24.3 |
| X9250TS24Z-2.7 (Note) | X9250TS ZF | | | 0 to +70 | 24 Ld SOIC (300 mil) (Pb-free) | M24.3 |
| X9250TS24I-2.7* | X9250TS G | | | -40 to +85 | 24 Ld SOIC (300 mil) | M24.3 |
| X9250TS24IZ-2.7* (Note) | X9250TS ZG | | | -40 to +85 | 24 Ld SOIC (300 mil) (Pb-free) | M24.3 |
| X9250TV24I-2.7 | X9250TV G | | | -40 to +85 | 24 Ld TSSOP (4.4mm) | MDP0044 |
| X9250TV24IZ-2.7 (Note) | X9250TV ZG | | | -40 to +85 | 24 Ld TSSOP (4.4mm) (Pb-free) | MDP0044 |
| X9250US24-2.7* | X9250US F | | 50 | 0 to +70 | 24 Ld SOIC (300 mil) | M24.3 |
| X9250US24Z-2.7* (Note) | X9250US ZF | | | 0 to +70 | 24 Ld SOIC (300 mil) (Pb-free) | M24.3 |
| X9250US24I-2.7 | X9250US G | | | -40 to +85 | 24 Ld SOIC (300 mil) | M24.3 |
| X9250US24IZ-2.7 (Note) | X9250US ZG | | | -40 to +85 | 24 Ld SOIC (300 mil) (Pb-free) | M24.3 |
| X9250UV24-2.7 | X9250UV F | | | 0 to +70 | 24 Ld TSSOP (4.4mm) | MDP0044 |
| X9250UV24Z-2.7 (Note) | X9250UV ZF | | | 0 to +70 | 24 Ld TSSOP (4.4mm) (Pb-free) | MDP0044 |
| X9250UV24I-2.7 | X9250UV G | | | -40 to +85 | 24 Ld TSSOP (4.4mm) | MDP0044 |
| X9250UV24IZ-2.7 (Note) | X9250UV ZG | | | -40 to +85 | 24 Ld TSSOP (4.4mm) (Pb-free) | MDP0044 |

*Add "T1" suffix for tape and reel.

NOTE:  Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## PIN DESCRIPTIONS

### Serial Output (SO)

SO is a serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

### Serial Input

SI is the serial data input pin. All opcodes, byte addresses and data to be written to the pots and pot registers are input on this pin. Data is latched by the rising edge of the serial clock.

### Serial Clock (SCK)

The SCK input is used to clock data into and out of the X9250.

### Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X9250 is deselected and the SO pin is at high impedance, and (unless an internal write cycle is underway) the device will be in the standby state. $\overline{CS}$ LOW enables the X9250, placing it in the active power mode. It should be noted that after a power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

### Hold ($\overline{HOLD}$)

$\overline{HOLD}$ is used in conjunction with the $\overline{CS}$ pin to select the device. Once the part is selected and a serial sequence is underway, $\overline{HOLD}$ may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, $\overline{HOLD}$ must be brought LOW while SCK is LOW. To resume communication, $\overline{HOLD}$ is brought HIGH, again while SCK is LOW. If the pause feature is not used, $\overline{HOLD}$ should be held HIGH at all times.

### Device Address ($A_0$ - $A_1$)

The address inputs are used to set the least significant 2 bits of the 8-bit slave address. A match in the slave address serial data stream must be made with the address input in order to initiate communication with the X9250. A maximum of 4 devices may occupy the SPI serial bus.

### Potentiometer Pins

### $V_H/R_H$ ($V_{H0}/R_{H0}$ - $V_{H3}/R_{H3}$), $V_L/R_L$ ($V_{L0}/R_{L0}$ - $V_{L3}/R_{L3}$)

The $R_H$ and $R_L$ pins are equivalent to the terminal connections on a mechanical potentiometer.

### $V_W/R_W$ ($V_{W0}/R_{W0}$ - $V_{W3}/R_{W3}$)

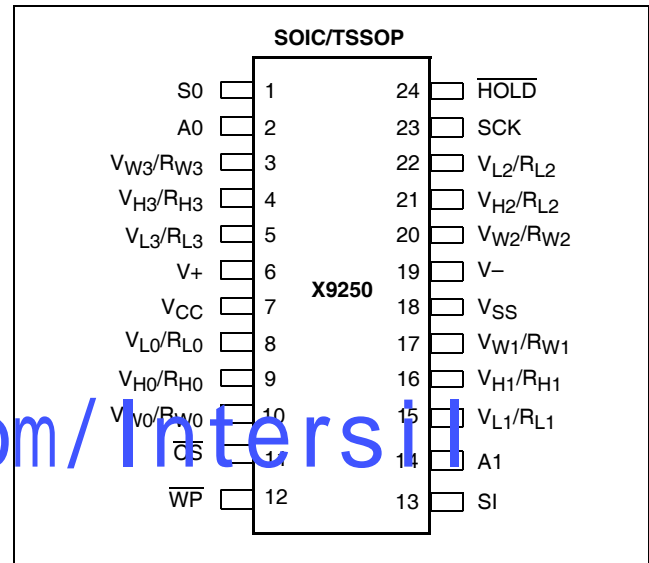The wiper pins are equivalent to the wiper terminal of a mechanical potentiometer.

### Hardware Write Protect Input ($\overline{WP}$)

The $\overline{WP}$ pin when LOW prevents nonvolatile writes to the Data Registers.

### Analog Supplies (V+, V-)

The analog supplies V+, V- are the supply voltages for the XDCP analog section.

## PIN CONFIGURATION



**SOIC/TSSOP**

| Left Pin | # | | # | Right Pin |
|---|---|---|---|---|
| S0 | 1 | | 24 | $\overline{HOLD}$ |
| A0 | 2 | | 23 | SCK |
| $V_{W3}/R_{W3}$ | 3 | | 22 | $V_{L2}/R_{L2}$ |
| $V_{H3}/R_{H3}$ | 4 | | 21 | $V_{H2}/R_{L2}$ |
| $V_{L3}/R_{L3}$ | 5 | | 20 | $V_{W2}/R_{W2}$ |
| V+ | 6 | X9250 | 19 | V− |
| $V_{CC}$ | 7 | | 18 | $V_{SS}$ |
| $V_{L0}/R_{L0}$ | 8 | | 17 | $V_{W1}/R_{W1}$ |
| $V_{H0}/R_{H0}$ | 9 | | 16 | $V_{H1}/R_{H1}$ |
| $V_{W0}/R_{W0}$ | 10 | | 15 | $V_{L1}/R_{L1}$ |
| $\overline{CS}$ | 11 | | 14 | A1 |
| $\overline{WP}$ | 12 | | 13 | SI |

## PIN NAMES

| Symbol | Description |
|---|---|
| SCK | Serial Clock |
| SI, SO | Serial Data |
| $A_0$-$A_1$ | Device Address |
| $V_{H0}/R_{H0}$–$V_{H3}/R_{H3}$, $V_{L0}/R_{L0}$–$V_{L3}/R_{L3}$ | Potentiometer Pins (terminal equivalent) |
| $V_{W0}/R_{W0}$–$V_{W3}/R_{W3}$ | Potentiometer Pins (wiper equivalent) |
| $\overline{WP}$ | Hardware Write Protection |
| V+,V- | Analog Supplies |
| $V_{CC}$ | System Supply Voltage |
| $V_{SS}$ | System Ground |
| NC | No Connection |

# DEVICE DESCRIPTION

## Serial Interface

The X9250 supports the SPI interface hardware conventions. The device is accessed via the SI input with data clocked in on the rising SCK. $\overline{CS}$ must be LOW and the $\overline{HOLD}$ and $\overline{WP}$ pins must be HIGH during the entire operation.

The SO and SI pins can be connected together, since they have three state outputs. This can help to reduce system pin count.

## Array Description

The X9250 is comprised of four resistor arrays. Each array contains 255 discrete resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer ($V_H/R_H$ and $V_L/R_L$ inputs).

At both ends of each array and between each resistor segment is a CMOS switch connected to the wiper ($V_W/R_W$) output. Within each individual array only one switch may be turned on at a time.

These switches are controlled by a Wiper Counter Register (WCR). The 8 bits of the WCR are decoded to select, and enable, one of 256 switches.

## Wiper Counter Register (WCR)

The X9250 contains four Wiper Counter Registers, one for each XDCP potentiometer. The WCR is equivalent to a serial-in, parallel-out register/counter with its outputs decoded to select one of 256 switches along its resistor array. The contents of the WCR can be altered in four ways: it may be written directly by the host via the write Wiper Counter Register instruction (serial load); it may be written indirectly by transferring the contents of one of four associated Data Registers via the XFR Data Register or Global XFR Data Register instructions (parallel load); it can be modified one step at a time by the increment/decrement instruction. Finally, it is loaded with the contents of its Data Register zero (DR0) upon power-up.

The Wiper Counter Register is a volatile register; that is, its contents are lost when the X9250 is powered-down. Although the register is automatically loaded with the value in R0 upon power-up, this may be different from the value present at power-down.
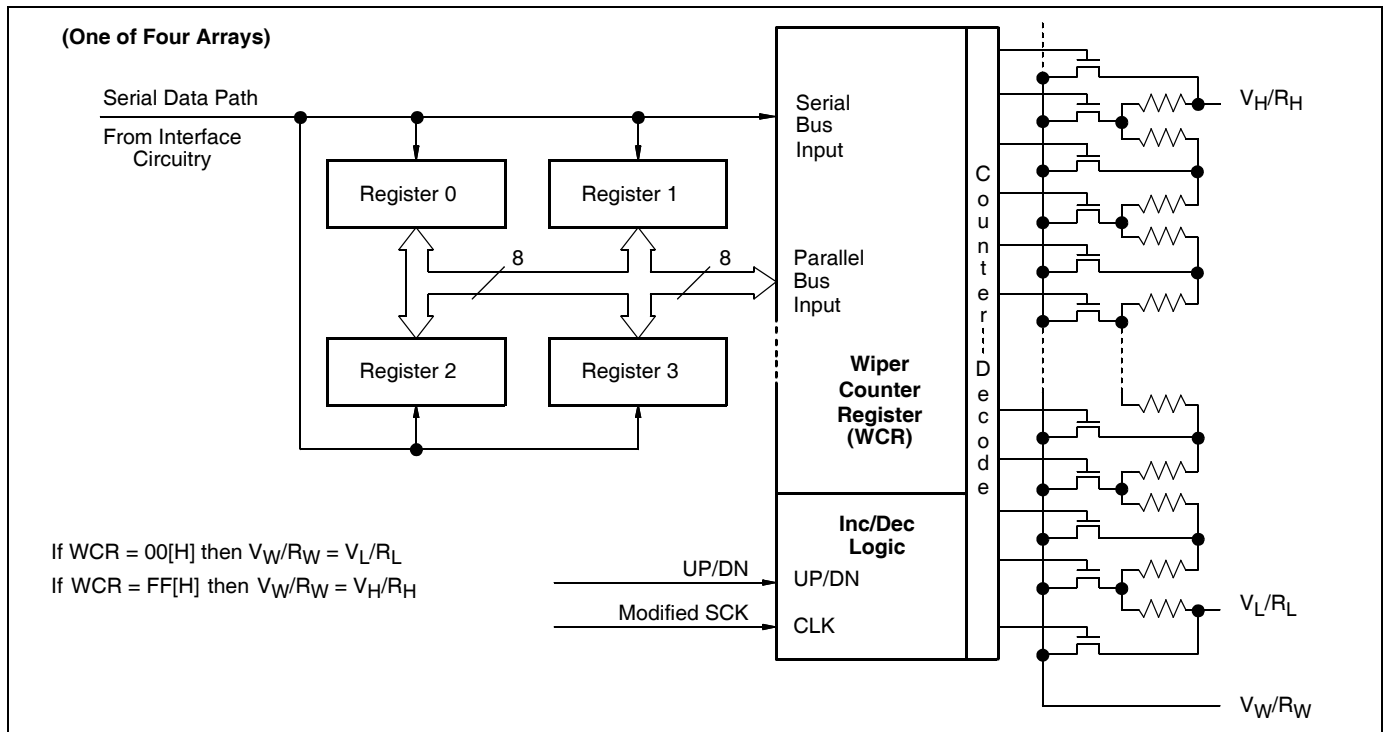
## Data Registers

Each potentiometer has four 8-bit nonvolatile Data Registers. These can be read or written directly by the host. Data can also be transferred between any of the four Data Registers and the associated Wiper Counter Register. All operations changing data in one of the Data Registers is a nonvolatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, the Data Registers can be used as regular memory locations for system parameters or user preference data.

## Data Register Detail

(MSB)                                                (LSB)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
| NV | NV | NV | NV | NV | NV | NV | NV |

**Figure 1. Detailed Potentiometer Block Diagram**



**Write in Process**

The contents of the Data Registers are saved to nonvolatile memory when the $\overline{CS}$ pin goes from LOW to HIGH after a complete write sequence is received by the device. The progress of this internal write operation can be monitored by a write in process bit (WIP). The WIP bit is read with a read status command.
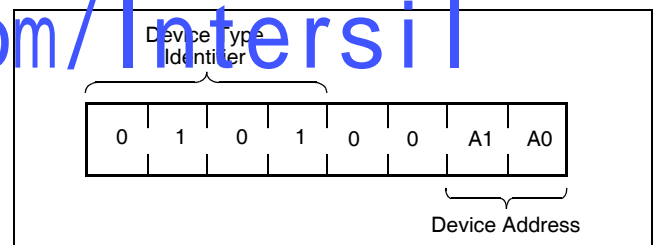
**INSTRUCTIONS**

**Identification (ID) Byte**

The first byte sent to the X9250 from the host, following a $\overline{CS}$ going HIGH to LOW, is called the Identification byte. The most significant four bits of the slave address are a device type identifier, for the X9250 this is fixed as 0101[B] (refer to Figure 2).

The two least significant bits in the ID byte select one of four devices on the bus. The physical device address is defined by the state of the $A_0$ - $A_1$ input pins. The X9250 compares the serial data stream with the address input state; a successful compare of both address bits is required for the X9250 to successfully continue the command sequence. The $A_0$ - $A_1$ inputs can be actively driven by CMOS input signals or tied to $V_{CC}$ or $V_{SS}$.

The remaining two bits in the slave byte must be set to 0.

**Figure 2. Identification Byte Format**



**Instruction Byte**

The next byte sent to the X9250 contains the instruction and register pointer information. The four most significant bits are the instruction. The next four bits point to one of the four pots and, when applicable, they point to one of four associated registers. The format is shown below in Figure 3.

**Figure 3. Instruction Byte Format**
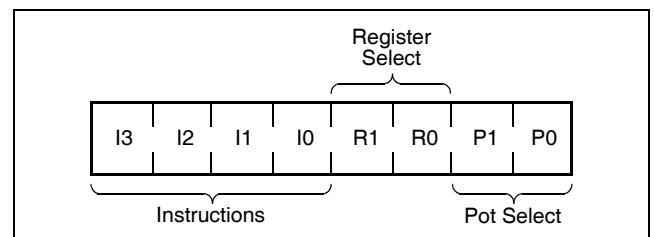
The four high order bits of the instruction byte specify the operation. The next two bits ($R_1$ and $R_0$) select one of the four registers that is to be acted upon when a register oriented instruction is issued. The last two bits (P1 and $P_0$) selects which one of the four potentiometers is to be affected by the instruction.

Four of the ten instructions are two bytes in length and end with the transmission of the instruction byte. These instructions are:

– <u>XFR Data Register to Wiper Counter Register</u>—This transfers the contents of one specified Data Register to the associated Wiper Counter Register.

– <u>XFR Wiper Counter Register to Data Register</u>—This transfers the contents of the specified Wiper Counter Register to the specified associated Data Register.

– <u>Global XFR Data Register to Wiper Counter Regiter</u>—This transfers the contents of all specified Data Registers to the associated Wiper Counter Registers.

– <u>Global XFR Wiper Counter Register to Data Regiter</u>—This transfers the contents of all Wiper Counter Registers to the specified associated Data Registers.

The basic sequence of the two byte instructions is illustrated in Figure 4. These two-byte instructions exchange data between the WCR and one of the Data Registers. A transfer from a Data Register to a WCR is essentially a write to a static RAM, with the static RAM controlling the wiper position. The response of the wiper to this action will be delayed by $t_{WRL}$. A transfer from the WCR (current wiper position), to a Data Register is a write to nonvolatile memory and takes a minimum of $t_{WR}$ to complete. The transfer can occur between one of the four potentiometers and one of its associated registers; or it may occur globally, where the transfer occurs between all potentiometers and one associated register.

Five instructions require a three-byte sequence to complete. These instructions transfer data between the host and the X9250; either between the host and one of the data registers or directly between the host and the Wiper Counter Register. These instructions are:

– <u>Read Wiper Counter Register</u>—read the current wiper position of the selected pot,

– <u>Write Wiper Counter Register</u>—change current wiper position of the selected pot,

– <u>Read Data Register</u>—read the contents of the selected data register;

– <u>Write Data Register</u>—write a new value to the selected data register.

– <u>Read Status</u>—This command returns the contents of the WIP bit which indicates if the internal write cycle is in progress.

The sequence of these operations is shown in Figure 5 and Figure 6.

The final command is Increment/Decrement. It is different from the other commands, because it's length is indeterminate. Once the command is issued, the master can clock the selected wiper up and/or down in one resistor segment steps; thereby, providing a fine tuning capability to the host. For each SCK clock pulse (HIGH) while SI is HIGH, the selected wiper will move one resistor segment towards the $V_H/R_H$ terminal. Similarly, for each SCK clock pulse while SI is LOW, the selected wiper will move one resistor segment towards the $V_L/R_L$ terminal. A detailed illustration of the sequence and timing for this operation are shown in Figure 7 and Figure 8.
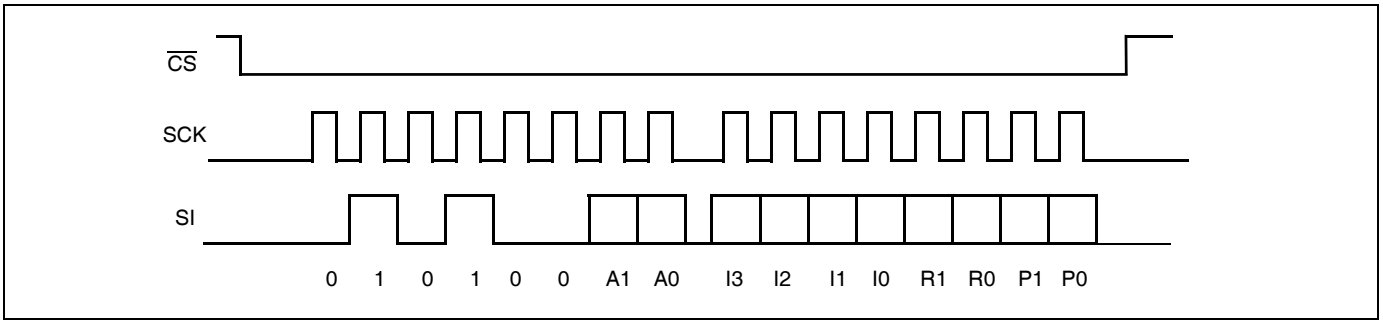
**Figure 4. Two-Byte Instruction Sequence**

CS

SCK

SI

0 1 0 1 0 0 A1 A0 I3 I2 I1 I0 R1 R0 P1 P0

**Figure 5. Three-Byte Instruction Sequence (Write)**

CS

SCL

SI

0 1 0 1 0 0 A1 A0 I3 I2 I1 I0 R1 R0 P1 P0 D7 D6 D5 D4 D3 D2 D1 D0
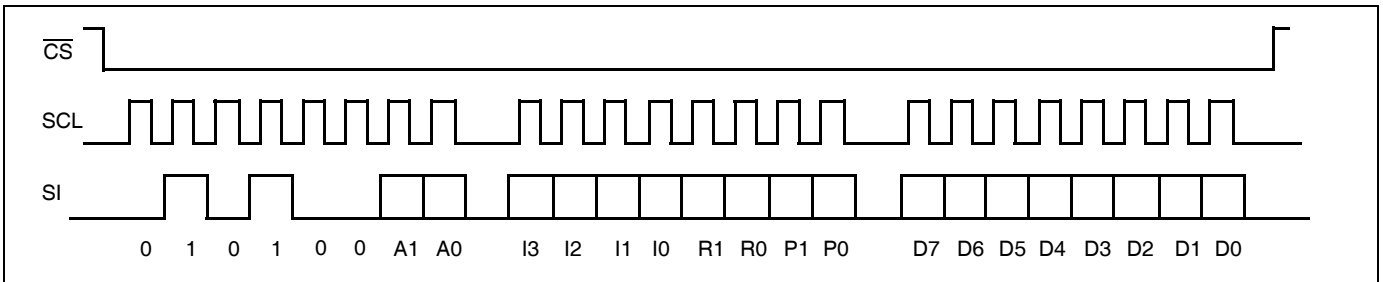
**Figure 6. Three-Byte Instruction Sequence (Read)**

CS

SCL

SI

Don't Care

0 1 0 1 0 0 A1 A0 I3 I2 I1 I0 R1 R0 P1 P0

S0

D7 D6 D5 D4 D3 D2 D1 D0
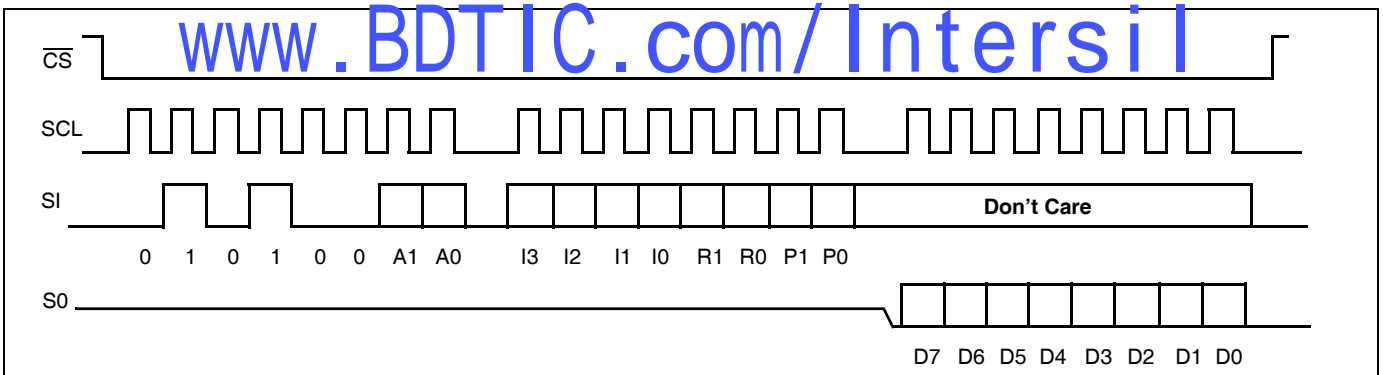
**Figure 7. Increment/Decrement Instruction Sequence**

CS

SCK

SI

0 1 0 1 0 0 A1 A0 I3 I2 I1 I0 0 0 P1 P0 INC1 INC2 INCn DEC1 DECn
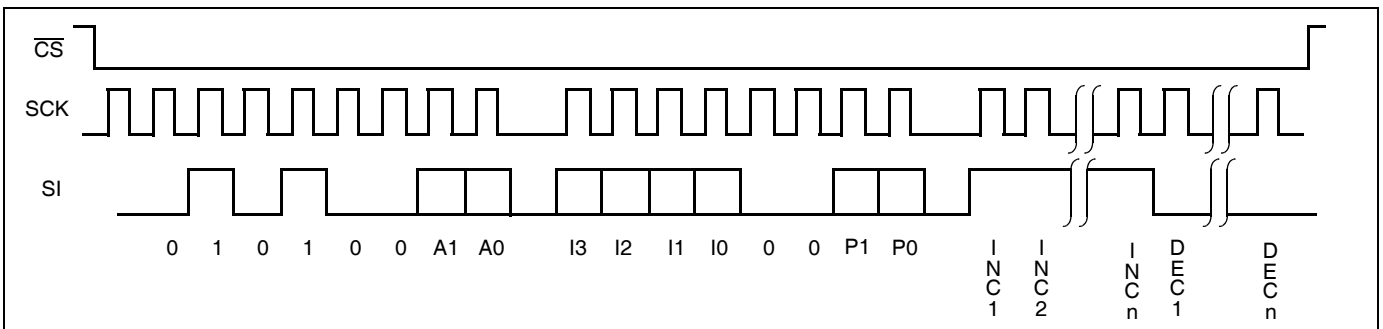
**Figure 8. Increment/Decrement Timing Limits**
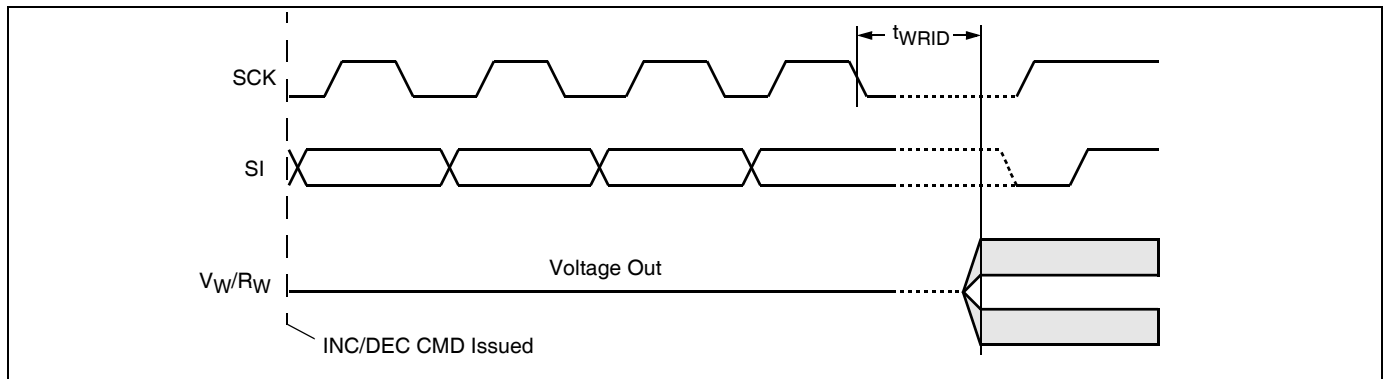


**Table 1. Instruction Set**

| Instruction | Instruction Set | | | | | | | | Operation |
|---|---|---|---|---|---|---|---|---|---|
| | $I_3$ | $I_2$ | $I_1$ | $I_0$ | $R_1$ | $R_0$ | $P_1$ | $P_0$ | |
| Read Wiper Counter Register | 1 | 0 | 0 | 1 | 0 | 0 | $P_1$ | $P_0$ | Read the contents of the Wiper Counter Register pointed to by $P_1$- $P_0$ |
| Write Wiper Counter Register | 1 | 0 | 1 | 0 | 0 | 0 | $P_1$ | $P_0$ | Write new value to the Wiper Counter Register pointed to by $P_1$- $P_0$ |
| Read Data Register | 1 | 0 | 1 | 1 | $R_1$ | $R_0$ | $P_1$ | $P_0$ | Read the contents of the Data Register pointed to by $P_1$- $P_0$ and $R_1$- $R_0$ |
| Write Data Register | 1 | 1 | 0 | 0 | $R_1$ | $R_0$ | $P_1$ | $P_0$ | Write new value to the Data Register pointed to by $P_1$- $P_0$ and $R_1$- $R_0$ |
| XFR Data Register to Wiper Counter Register | 1 | 1 | 0 | 1 | $R_1$ | $R_0$ | $P_1$ | $P_0$ | Transfer the contents of the Data Register pointed to by $R_1$- $R_0$ to the Wiper Counter Register pointed to by $P_1$-$P_0$ |
| XFR Wiper Counter Register to Data Register | 1 | 1 | 1 | 0 | $R_1$ | $R_0$ | $P_1$ | $P_0$ | Transfer the contents of the Wiper Counter Register pointed to by $P_1$- $P_0$ to the Register pointed to by $R_1$- $R_0$ |
| Global XFR Data Register to Wiper Counter Register | 0 | 0 | 0 | 1 | $R_1$ | $R_0$ | 0 | 0 | Transfer the contents of the Data Registers pointed to by $R_1$- $R_0$ of all four pots to their respective Wiper Counter Register |
| Global XFR Wiper Counter Register to Data Register | 1 | 0 | 0 | 0 | $R_1$ | $R_0$ | 0 | 0 | Transfer the contents of all Wiper Counter Registers to their respective data Registers pointed to by $R_1$- $R_0$ of all four pots |
| Increment/Decrement Wiper Counter Register | 0 | 0 | 1 | 0 | 0 | 0 | $P_1$ | $P_0$ | Enable Increment/decrement of the Wiper Counter Register pointed to by $P_1$- $P_0$ |
| Read Status (WIP bit) | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | Read the status of the internal write cycle, by checking the WIP bit. |

## Instruction Format

**Notes:** (1) "A1 ~ A0": stands for the device addresses sent by the master.
(2) WPx refers to wiper position data in the Counter Register
(2) "I": stands for the increment operation, SI held HIGH during active SCK phase (high).
(3) "D": stands for the decrement operation, SI held LOW during active SCK phase (high).

### Read Wiper Counter Register(WCR)

| $\overline{CS}$ Falling Edge | device type identifier | | | | device addresses | | | instruction opcode | | | | WCR addresses | | | | wiper position (sent by X9250 on SO) | | | | | | | | $\overline{CS}$ Rising Edge |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 1 | 0 | 0 | 1 | 0 | 0 | P1 | P0 | WP7 | WP6 | WP5 | WP4 | WP3 | WP2 | WP1 | WP0 | |

### Write Wiper Counter Register (WCR)

| $\overline{CS}$ Falling Edge | device type identifier | | | | device addresses | | | instruction opcode | | | | WCR addresses | | | | Data Byte (sent by Host on SI) | | | | | | | | $\overline{CS}$ Rising Edge |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 1 | 0 | 1 | 0 | 0 | 0 | P1 | P0 | WP7 | WP6 | WP5 | WP4 | WP3 | WP2 | WP1 | WP0 | |

### Read Data Register (DR)

| $\overline{CS}$ Falling Edge | device type identifier | | | | device addresses | | | instruction opcode | | | | DR and WCR addresses | | | | Data Byte (sent by X9250 on SO) | | | | | | | | $\overline{CS}$ Rising Edge |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 1 | 1 | 1 | 1 | R1 | R0 | P1 | P0 | WP7 | WP6 | WP5 | WP4 | WP3 | WP2 | WP1 | WP0 | |

### Write Data Register (DR)

| $\overline{CS}$ Falling Edge | device type identifier | | | | device addresses | | | instruction opcode | | | | DR and WCR addresses | | | | Data Byte (sent by host on SI) | | | | | | | | $\overline{CS}$ Rising Edge | HIGH-VOLTAGE WRITE CYCLE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 1 | 1 | 0 | 0 | R1 | R0 | P1 | P0 | WP7 | WP6 | WP5 | WP4 | WP3 | WP2 | WP1 | WP0 | | |

### Transfer Data Register (DR) to Wiper Counter Register (WCR)

| $\overline{CS}$ Falling Edge | device type identifier | | | | device addresses | | | instruction opcode | | | | DR and WCR addresses | | | | $\overline{CS}$ Rising Edge |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 1 | 1 | 0 | 1 | R1 | R0 | P1 | P0 | |

**Transfer Wiper Counter Register (WCR) to Data Register (DR)**

| $\overline{CS}$ Falling Edge | device type identifier | | | device addresses | | | | instruction opcode | | | | DR and WCR addresses | | | | $\overline{CS}$ Rising Edge | HIGH-VOLTAGE WRITE CYCLE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 1 | 1 | 1 | 0 | R1 | R0 | P1 | P0 | | |

**Increment/Decrement Wiper Counter Register (WCR)**

| $\overline{CS}$ Falling Edge | device type identifier | | | device addresses | | | | instruction opcode | | | | WCR addresses | | | | increment/decrement (sent by master on SI) | | | | | | $\overline{CS}$ Rising Edge |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 0 | 0 | 1 | 0 | X | X | P1 | P0 | I/D | I/D | . . . . | I/D | I/D | |

**Global Transfer Data Register (DR) to Wiper Counter Register (WCR)**

| $\overline{CS}$ Falling Edge | device type identifier | | | device addresses | | | | instruction opcode | | | | DR addresses | | | | $\overline{CS}$ Rising Edge |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 0 | 0 | 0 | 1 | R1 | R0 | 0 | 0 | |

**Global Transfer Wiper Counter Register (WCR) to Data Register (DR)**

| $\overline{CS}$ Falling Edge | device type identifier | | | device addresses | | | | instruction opcode | | | | DR addresses | | | | $\overline{CS}$ Rising Edge | HIGH-VOLTAGE WRITE CYCLE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 1 | 0 | 0 | 0 | R1 | R0 | 0 | 0 | | |

**Read Status**

| $\overline{CS}$ Falling Edge | device type identifier | | | device addresses | | | | instruction opcode | | | | | | | | Data Byte (sent by X9250 on SO) | | | | | | | | $\overline{CS}$ Rising Edge |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 0 | 1 | 0 | 0 | A1 | A0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | WIP | |

## ABSOLUTE MAXIMUM RATINGS

Temperature under bias ......................... -65 to +135°C
Storage temperature ............................ -65 to +150°C
Voltage on SCK, SCL or any address input
  with respect to $V_{SS}$ ................................ -1V to +7V
Voltage on V+ (referenced to $V_{SS}$) ....................... 10V
Voltage on V- (referenced to $V_{SS}$) ....................... -10V
(V+) - (V-) .............................................. 12V
Any $V_H/R_H$ ............................................. V+
Any $V_L/R_L$ ............................................. V-
Lead temperature (soldering, 10s) .................. +300°C
$I_W$ (10s) ........................................... ±15mA

## COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### RECOMMENDED OPERATING CONDITIONS

| Temp | Min. | Max. |
|---|---|---|
| Commercial | 0°C | +70°C |
| Industrial | -40°C | +85°C |

| Device | Supply Voltage ($V_{CC}$) Limits[4] |
|---|---|
| X9250 | 5V ±10% |
| X9250-2.7 | 2.7V to 5.5V |

### POTENTIOMETER CHARACTERISTICS (Over recommended operating conditions unless otherwise stated.)

| Symbol | Parameter | | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | End to end resistance tolerance | | | | ±20 | % | |
| | Power rating | | | | 50 | mW | +25°C, each pot |
| $I_W$ | Wiper current | | | | ±15 | mA | |
| $R_W$ | Wiper resistance | | | 150 | 250 | Ω | Wiper current = ± 1mA |
| $V_{V+}$ | Voltage on V+ pin | X9250 | +4.5 | | +5.5 | V | |
| | | X9250-2.7 | +2.7 | | +5.5 | | |
| $V_{V-}$ | Voltage on V- pin | X9250 | -5.5 | | -4.5 | V | |
| | | X9250-2.7 | -5.5 | | -2.7 | | |
| $V_{TERM}$ | Voltage on any $V_H/R_H$ or $V_L/R_L$ pin | | V- | | V+ | V | |
| | Noise | | | -120 | | dBV | Ref: 1kHz |
| | Resolution [4] | | | 0.6 | | % | |
| | Absolute linearity [1] | | | | ±1 | MI[3] | $V_{w(n)(actual)}$ - $V_{w(n)(expected)}$ |
| | Relative linearity [2] | | | | ±0.6 | MI[3] | $V_{w(n + 1} - [V_{w(n)} + MI]$ |
| | Temperature coefficient of $R_{TOTAL}$ | | | ±300 | | ppm/°C | |
| | Ratiometric Temperature Coefficient | | | | ±20 | ppm/°C | |
| $C_H/C_L/C_W$ | Potentiometer Capacitances | | | 10/10/25 | | pF | See Circuit #3 |

**Notes:** (1) Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.

(2) Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.

(3) MI = RTOT/255 or ($V_H/R_H$ - $V_L/R_L$)/255, single pot

(4) Individual array resolutions.

## D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

| Symbol | Parameter | Limits | | | | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Unit | |
| $I_{CC1}$ | $V_{CC}$ supply current (active) | | | 400 | µA | $f_{SCK}$ = 2MHz, SO = Open, Other Inputs = $V_{SS}$ |
| $I_{CC2}$ | $V_{CC}$ supply current (nonvolatile write) | | | 1 | mA | $f_{SCK}$ = 2MHz, SO = Open, Other Inputs = $V_{SS}$ |
| $I_{SB}$ | $V_{CC}$ current (standby) | | | 5 | µA | SCK = SI = $V_{SS}$, Addr. = $V_{SS}$ |
| $I_{LI}$ | Input leakage current | | | 10 | µA | $V_{IN}$ = $V_{SS}$ to $V_{CC}$ |
| $I_{LO}$ | Output leakage current | | | 10 | µA | $V_{OUT}$ = $V_{SS}$ to $V_{CC}$ |
| $V_{IH}$ | Input HIGH voltage | $V_{CC}$ x 0.7 | | $V_{CC}$ + 0.1 | V | |
| $V_{IL}$ | Input LOW voltage | -0.5 | | $V_{CC}$ x 0.3 | V | |
| $V_{OL}$ | Output LOW voltage | | | 0.4 | V | $I_{OL}$ = 3mA |

## ENDURANCE AND DATA RETENTION

| Parameter | Min. | Unit |
|---|---|---|
| Minimum endurance | 100,000 | Data changes per bit per register |
| Data retention | 100 | Years |

## CAPACITANCE

| Symbol | Test | Max. | Unit | Test Conditions |
|---|---|---|---|---|
| $C_{OUT}$[5] | Output capacitance (SO) | 8 | pF | $V_{OUT}$ = 0V |
| $C_{IN}$[5] | Input capacitance (A0, A1, SI and SCK, CS) | 6 | pF | $V_{IN}$ = 0V |

## POWER-UP TIMING

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{PUR}$[6] | Power-up to initiation of read operation | | 1 | ms |
| $t_{PUW}$[6] | Power-up to initiation of write operation | | 5 | ms |
| $t_R V_{CC}$[7] | $V_{CC}$ power up ramp rate | 0.2 | 50 | V/msec |

## POWER UP AND DOWN REQUIREMENT

The are no restrictions on the sequencing of the bias supplies $V_{CC}$, V+, and V- provided that all three supplies reach their final values within 1msec of each other. At all times, the voltages on the potentiometer pins must be less than V+ and more than V-. The recall of the wiper position from nonvolatile memory is not in effect until all supplies reach their final value. The $V_{CC}$ ramp rate spec is always in effect.

**Notes:** (5) This parameter is periodically sampled and not 100% tested
      (6) $t_{PUR}$ and $t_{PUW}$ are the delays required from the time the third (last) power supply ($V_{CC}$, V+ or V-) is stable until the specific instruction can be issued. These parameters are periodically sampled and not 100% tested.
      (7) Sample tested only.

## A.C. TEST CONDITIONS

| | |
|---|---|
| Input pulse levels | $V_{CC}$ x 0.1 to $V_{CC}$ x 0.9 |
| Input rise and fall times | 10ns |
| Input and output timing level | $V_{CC}$ x 0.5 |

**Circuit #3 SPICE Macro Model**
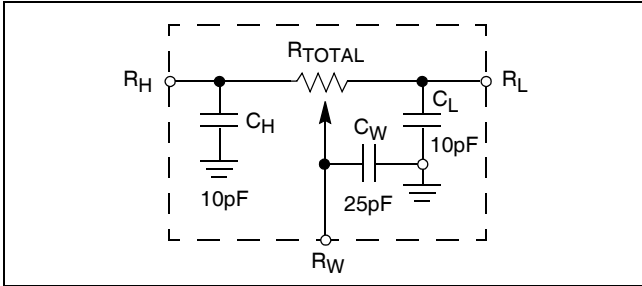


**EQUIVALENT A.C. LOAD CIRCUIT**
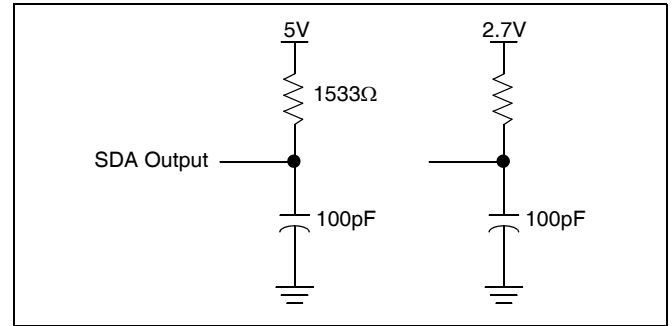


**AC TIMING**

| Symbol | Parameter | Min. | Max. | Unit |
|--------|-----------|------|------|------|
| $f_{SCK}$ | SSI/SPI clock frequency | | 2.0 | MHz |
| $t_{CYC}$ | SSI/SPI clock cycle time | 500 | | ns |
| $t_{WH}$ | SSI/SPI clock high time | 200 | | ns |
| $t_{WL}$ | SSI/SPI clock low time | 200 | | ns |
| $t_{LEAD}$ | Lead time | 250 | | ns |
| $t_{LAG}$ | Lag time | 250 | | ns |
| $t_{SU}$ | SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input setup time | 50 | | ns |
| $t_H$ | SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input hold time | 75 | | ns |
| $t_{RI}$ | SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input rise time | | 2 | µs |
| $t_{FI}$ | SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input fall time | | 2 | µs |
| $t_{DIS}$ | SO output disable Time | 0 | 500 | ns |
| $t_V$ | SO output valid time | | 100 | ns |
| $t_{HO}$ | SO output hold time | 0 | | ns |
| $t_{RO}$ | SO output rise time | | 50 | ns |
| $t_{FO}$ | SO output fall time | | 50 | ns |
| $t_{HOLD}$ | $\overline{HOLD}$ time | 400 | | ns |
| $t_{HSU}$ | $\overline{HOLD}$ setup time | 100 | | ns |
| $t_{HH}$ | $\overline{HOLD}$ hold time | 100 | | ns |
| $t_{HZ}$ | $\overline{HOLD}$ low to output in high Z | | 100 | ns |
| $t_{LZ}$ | $\overline{HOLD}$ high to output in low Z | | 100 | ns |
| $T_I$ | Noise suppression time constant at SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ inputs | | TBD | ns |
| $t_{CS}$ | $\overline{CS}$ deselect time | 2 | | µs |
| $t_{WPASU}$ | $\overline{WP}$, A0 and A1 setup time | 0 | | ns |
| $t_{WPAH}$ | $\overline{WP}$, A0 and A1 hold time | 0 | | ns |
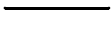
## HIGH-VOLTAGE WRITE CYCLE TIMING

| Symbol | Parameter | Typ. | Max. | Unit |
|---|---|---|---|---|
| $t_{WR}$ | High-voltage write cycle time (store instructions) | 5 | 10 | ms |

## XDCP TIMING

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{WRPO}$ | Wiper response time after the third (last) power supply is stable | | 10 | µs |
| $t_{WRL}$ | Wiper response time after instruction issued (all load instructions) | | 10 | µs |
| $t_{WRID}$ | Wiper response time from an active SCL/SCK edge (increment/decrement instruction) | | 40 | µs |

## SYMBOL TABLE

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| | Must be steady | Will be steady |
| | May change from Low to High | Will change from Low to High |
| | May change from High to Low | Will change from High to Low |
| | Don't Care: Changes Allowed | Changing: State Not Known |
| | N/A | Center Line is High Impedance |

## TIMING DIAGRAMS

### Input Timing
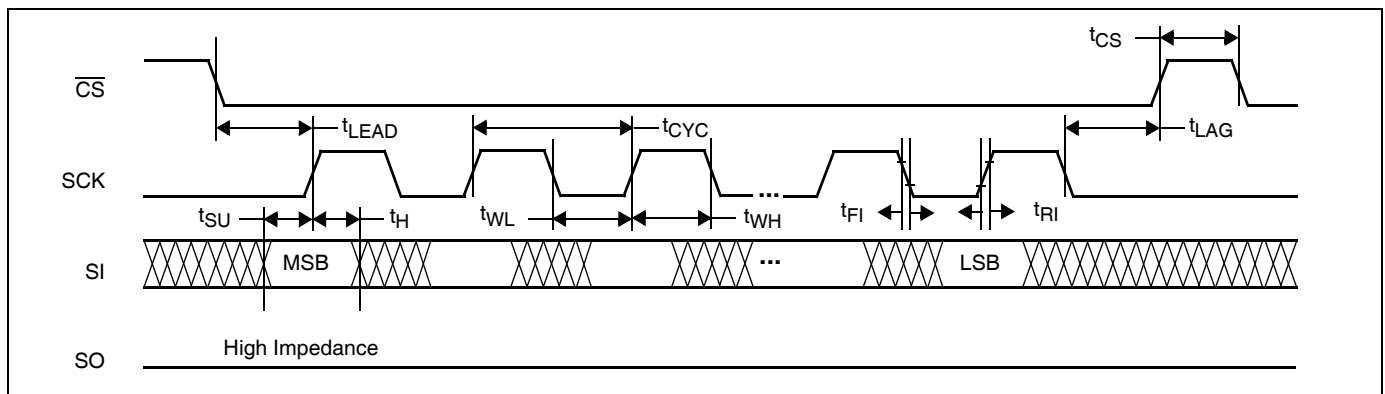
**Output Timing**
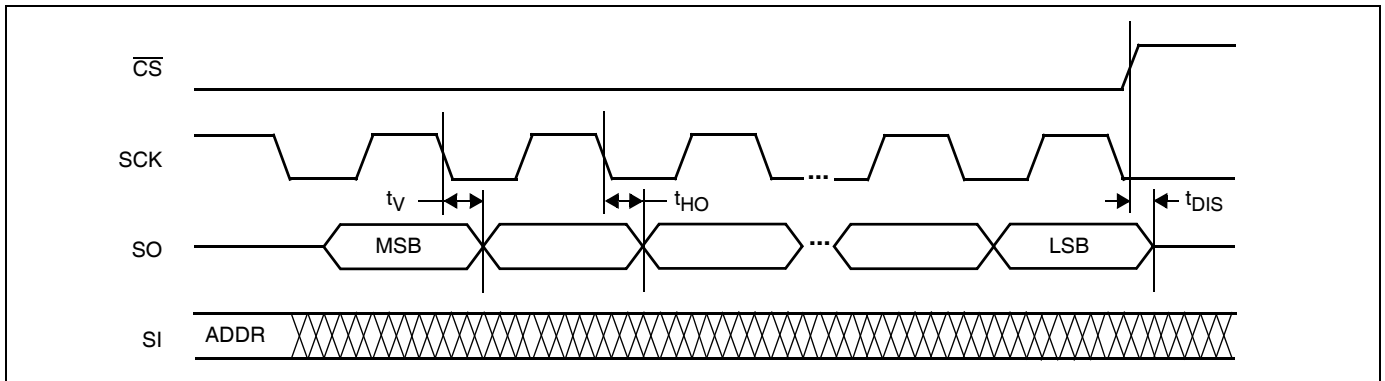


**Hold Timing**
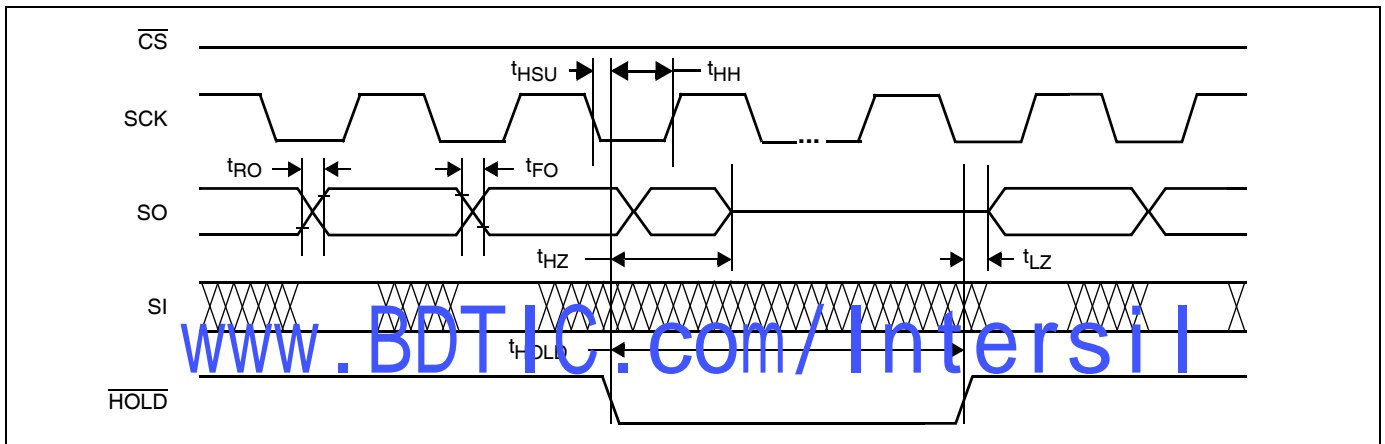


**XDCP Timing (for all Load Instructions)**
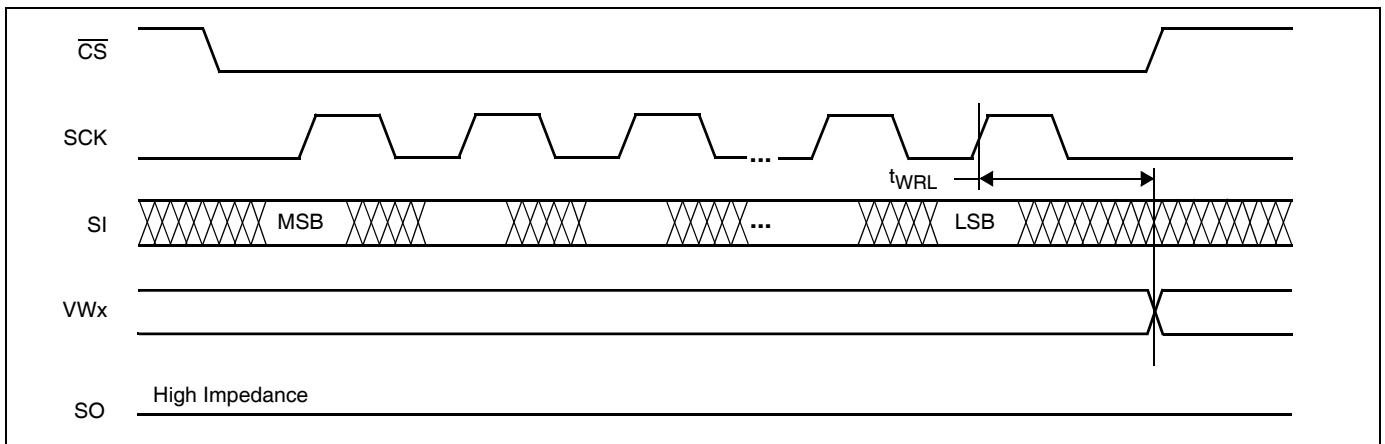
**XDCP Timing (for Increment/Decrement Instruction)**
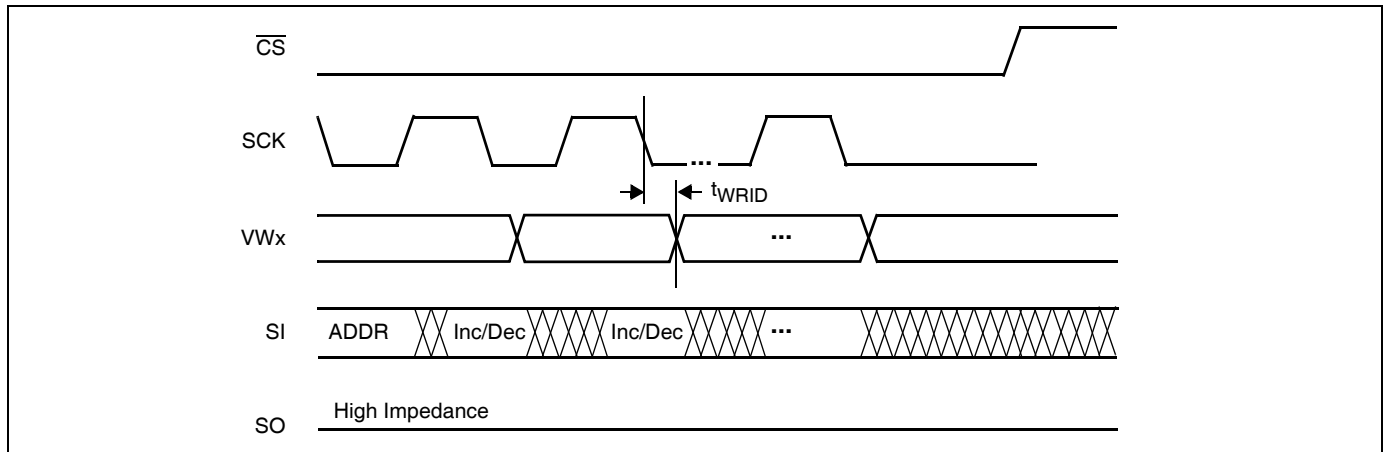


**Write Protect and Device Address Pins Timing**
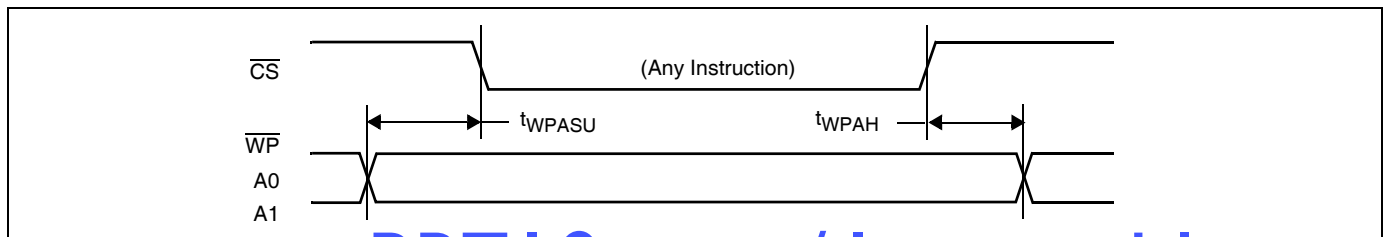
## APPLICATIONS INFORMATION

### Basic Configurations of Electronic Potentiometers
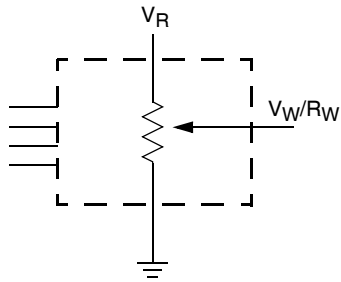
Three terminal Potentiometer;
Variable voltage divider
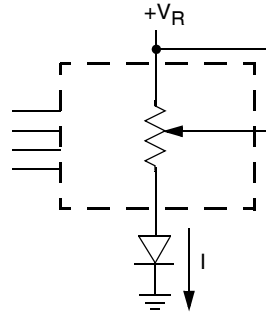
Two terminal Variable Resistor;
Variable current

### Application Circuits

**Noninverting Amplifier**
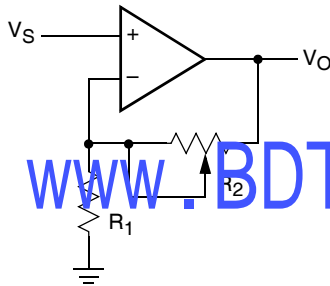
$V_O = (1+R_2/R_1)V_S$

**Voltage Regulator**
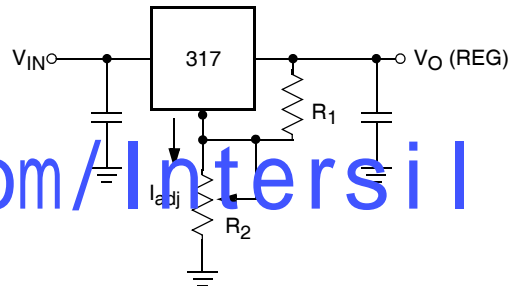
$V_O \text{ (REG)} = 1.25V \ (1+R_2/R_1)+I_{adj} R_2$

**Offset Voltage Adjustment**
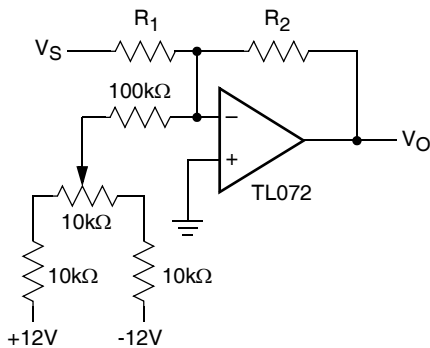
**Comparator with Hysterisis**
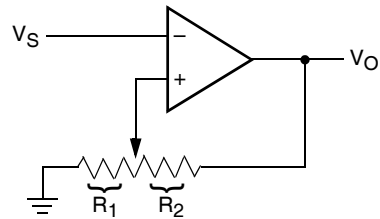
$V_{UL} = \{R_1/(R_1+R_2) \ V_O(max)$
$V_{LL} = \{R_1/(R_1+R_2) \ V_O(min)$

## Application Circuits (continued)

**Attenuator**



$R_1 = R_2 = R_3 = R_4 = 10k\Omega$
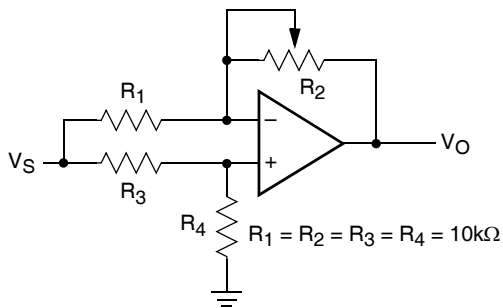
$V_O = G\ V_S$

$-1/2 \leq G \leq +1/2$

**Filter**
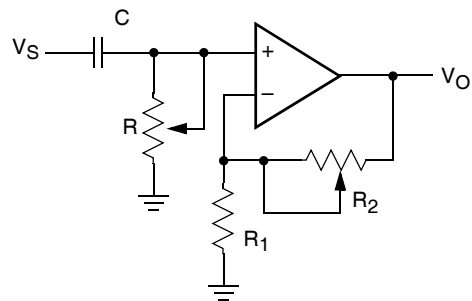


$G_O = 1 + R_2/R_1$

$fc = 1/(2\pi RC)$

**Inverting Amplifier**
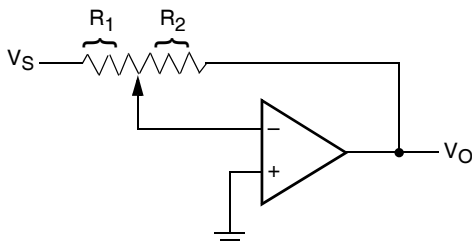


$V_O = G\ V_S$

$G = -R_2/R_1$

**Equivalent L-R Circuit**
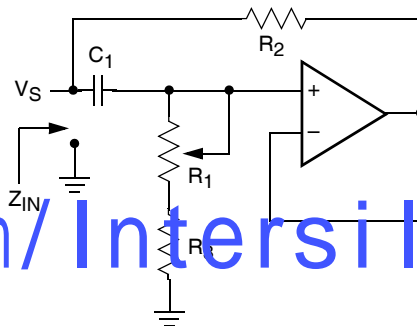


$Z_{IN} = R_2 + s\ R_2\ (R_1 + R_3)\ C_1 = R_2 + s\ Leq$

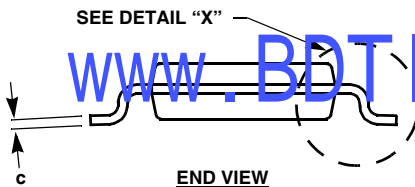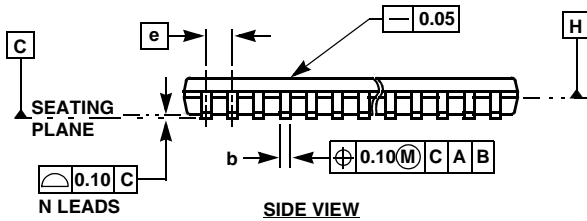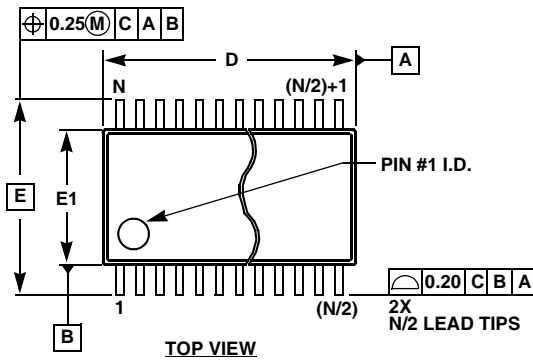$(R_1 + R_3) >> R_2$
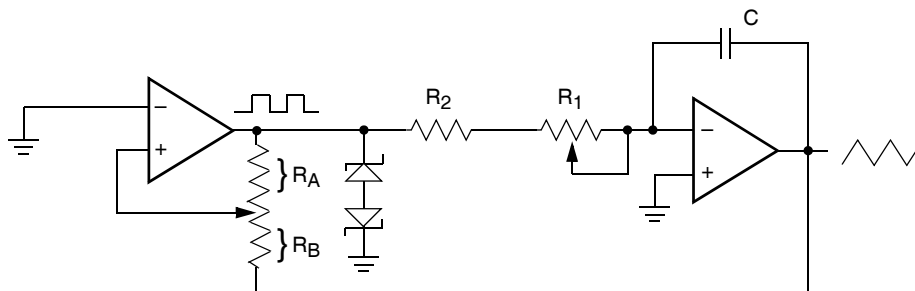


frequency $\propto R_1, R_2, C$

amplitude $\propto R_A, R_B$

## Thin Shrink Small Outline Package Family (TSSOP)
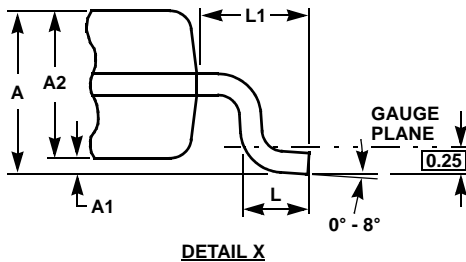
### MDP0044
**THIN SHRINK SMALL OUTLINE PACKAGE FAMILY**

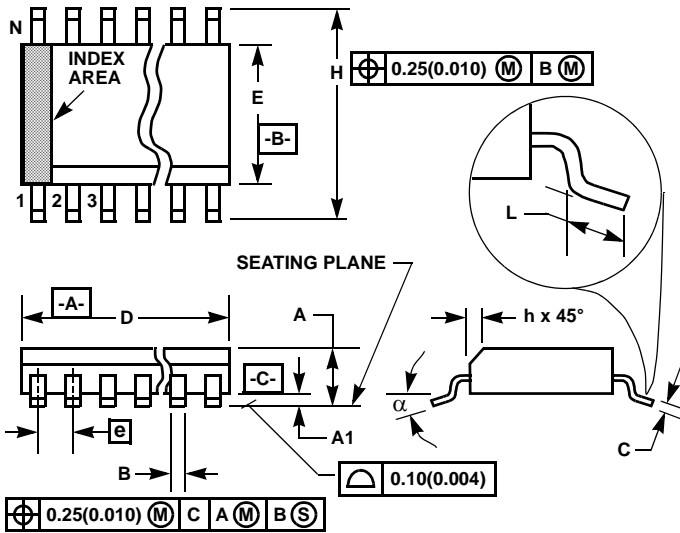| SYMBOL | 14 LD | 16 LD | 20 LD | 24 LD | 28 LD | TOLERANCE |
|--------|-------|-------|-------|-------|-------|-----------|
| A | 1.20 | 1.20 | 1.20 | 1.20 | 1.20 | Max |
| A1 | 0.10 | 0.10 | 0.10 | 0.10 | 0.10 | ±0.05 |
| A2 | 0.90 | 0.90 | 0.90 | 0.90 | 0.90 | ±0.05 |
| b | 0.25 | 0.25 | 0.25 | 0.25 | 0.25 | +0.05/-0.06 |
| c | 0.15 | 0.15 | 0.15 | 0.15 | 0.15 | +0.05/-0.06 |
| D | 5.00 | 5.00 | 6.50 | 7.80 | 9.70 | ±0.10 |
| E | 6.40 | 6.40 | 6.40 | 6.40 | 6.40 | Basic |
| E1 | 4.40 | 4.40 | 4.40 | 4.40 | 4.40 | ±0.10 |
| e | 0.65 | 0.65 | 0.65 | 0.65 | 0.65 | Basic |
| L | 0.60 | 0.60 | 0.60 | 0.60 | 0.60 | ±0.15 |
| L1 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | Reference |

Rev. E  12/02

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.

2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.

3. Dimensions "D" and "E1" are measured at dAtum Plane H.

4. Dimensioning and tolerancing per ASME Y14.5M-1994.

## Small Outline Plastic Packages (SOIC)



**M24.3** (JEDEC MS-013-AD ISSUE C)
**24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|--------|--------|--------|-------------|--------|-------|
| | MIN | MAX | MIN | MAX | |
| A | 0.0926 | 0.1043 | 2.35 | 2.65 | - |
| A1 | 0.0040 | 0.0118 | 0.10 | 0.30 | - |
| B | 0.013 | 0.020 | 0.33 | 0.51 | 9 |
| C | 0.0091 | 0.0125 | 0.23 | 0.32 | - |
| D | 0.5985 | 0.6141 | 15.20 | 15.60 | 3 |
| E | 0.2914 | 0.2992 | 7.40 | 7.60 | 4 |
| e | 0.05 BSC | | 1.27 BSC | | - |
| H | 0.394 | 0.419 | 10.00 | 10.65 | - |
| h | 0.010 | 0.029 | 0.25 | 0.75 | 5 |
| L | 0.016 | 0.050 | 0.40 | 1.27 | 6 |
| N | 24 | | 24 | | 7 |
| $\alpha$ | 0° | 8° | 0° | 8° | - |

Rev. 1 4/06

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.

2. Dimensioning and tolerancing per ANSI Y14.5M-1982.

3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.

4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.

5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.

6. "L" is the length of terminal for soldering to a substrate.

7. "N" is the number of terminal positions.

8. Terminal numbers are shown for reference only.

9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)

10. Controlling dimension:  MILLIMETER. Converted inch dimensions are not necessarily exact.

---

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.

Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

---

For information regarding Intersil Corporation and its products, see www.intersil.com

FN8165.3
August 29, 2006