Low Noise, Low Power, I^2C® Bus, 256 Taps

The ISL90843 integrates four digitally controlled potentiometers (XDCP) on a monolithic CMOS integrated circuit.

The digitally controlled potentiometers are implemented with a combination of resistor elements and CMOS switches. The position of the wipers are controlled by the user through the I^2C bus interface. Each potentiometer has an associated Wiper Register (WR) that can be directly written to and read by the user. The contents of the WR controls the position of the wiper.

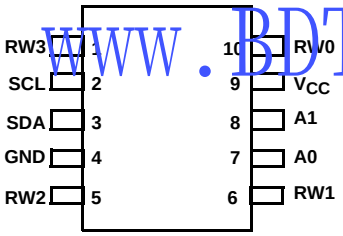
The DCPs can be used as a voltage divider in a wide variety of applications including control, AC measurement, and signal processing.

Features

- Four potentiometers in one package
- 256 resistor taps–0.4% resolution
- I^2C serial interface
  - Two address pins allow up to four devices/bus
- Wiper resistance: 70Ω typical @ 3.3V
- Standby current <5µA max
- Power supply: 2.7V to 5.5V
- 10kΩ or 50kΩ total resistance
- 10 Ld MSOP package
- Pb-free plus anneal product (RoHS compliant)

Pinout

ISL90843
(10 LD MSOP)
TOP VIEW



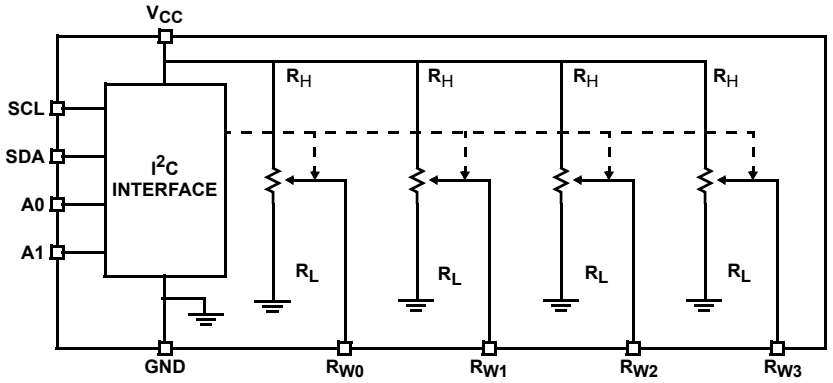
Ordering Information

PART NUMBER (Note)	PART MARKING	RESISTANCE OPTION (kΩ)	TEMP RANGE (°C)	PACKAGE (Pb-Free)
ISL90843WIU1027Z*	DET	10	-40 to +85	10 Ld MSOP
ISL90843UIU1027Z*	DES	50	-40 to +85	10 Ld MSOP

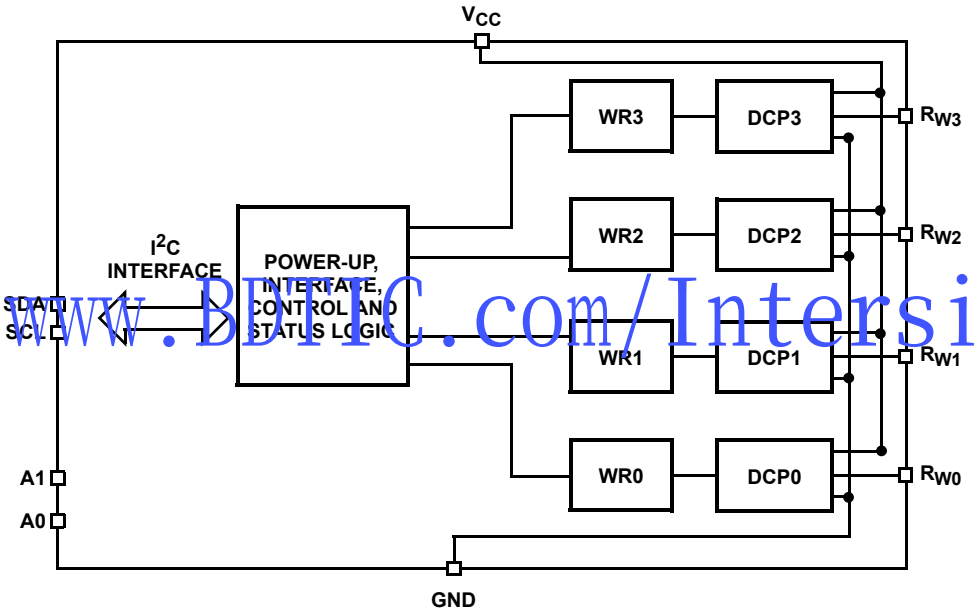
*Add "-TK" suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Functional Diagram



Block Diagram



Pin Descriptions

MSOP PIN	SYMBOL	DESCRIPTION
1	RW3	“Wiper” terminal of DCP3
2	SCL	I^2C interface clock
3	SDA	Serial data I/O for the I^2C interface
4	GND	Device ground pin
5	RW2	“Wiper” terminal of DCP2
6	RW1	“Wiper” terminal of DCP1
7	A0	Device address for the I^2C interface
8	A1	Device address for the I^2C interface
9	V_{CC}	Power supply pin
10	RW0	“Wiper” terminal of DCP0

Absolute Maximum Ratings

Storage Temperature . . . . . -65°C to +150°C
Voltage at any Digital Interface Pin with Respect to GND . . . . . -0.3V to V_{CC}+0.3
V_{CC} . . . . . -0.3V to +6V
Voltage at any DCP Pin with Respect to GND . . . . . -0.3V to V_{CC}
Lead Temperature (Soldering, 10s) . . . . . 300°C
I_W (10s) . . . . . ±6mA

Recommended Operating Conditions

Industrial . . . . . -40°C to +85°C
V_{CC} . . . . . 2.7V to 5.5V
Power Rating of each DCP 5mW
Wiper Current of each DCP . . . . . ±3.0mA

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Analog Specifications

Over recommended operating conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 1)	MAX	UNITS
R_{TOTAL}	R_H to R_L Resistance	W, U versions respectively		10, 50		kΩ
	R_H to R_L Resistance Tolerance		-20		+20	%
R_W	Wiper Resistance	V_{CC} = 3.3V @ 25°C		70		Ω
C_W	Potentiometer Capacitance (Note 15)			25		pF
VOLTAGE DIVIDER MODE (0V @ RL_i; V_{CC} @ RH_i; measured at RW_i, unloaded; i = 0, 1, 2, or 3)						
INL (Note 6)	Integral Non-Linearity		-1		1	LSB (Note 2)
DNL (Note 5)	Differential Non-Linearity	Monotonic over all tap positions	-0.5		0.5	LSB (Note 2)
ZSerror (Note 3)	Zero-Scale Error	W option	0	1	7	LSB (Note 2)
		U option	0	0.5	2	
FSerror (Note 4)	Full-Scale Error	W option	-7	-1	0	LSB (Note 2)
		U option	-2	-1	0	
V_{MATCH} (Note 7)	DCP to DCP Matching	Any two DCPs at same tap position, same voltage at all RH terminals, and same voltage at all RL terminals	-2		2	LSB (Note 2)
TC_V (Note 8)	Ratiometric Temperature Coefficient	DCP register set to 80 hex		±4		ppm/°C

Operating Specifications

Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 1)	MAX	UNITS
I_{CC1}	V_{CC} Supply Current (Volatile write/read)	10k DCPs, f_{SCL} = 400kHz; SDA = Open; (for I^2C, Active, Read and Write States)			3.8	mA
I_{CC2}	V_{CC} Supply Current (Volatile write/read)	50k DCPs, f_{SCL} = 400kHz; SDA = Open; (for I^2C, Active, Read and Write States)			2.9	mA
I_{SB}	V_{CC} current (standby)	V_{CC} = +5.5V, 10k DCPs, I^2C Interface in Standby State			2.8	mA
		V_{CC} = +5.5V, 50k DCPs, I^2C Interface in Standby State			0.6	mA
		V_{CC} = +3.6V, 10k DCPs, I^2C Interface in Standby State			1.9	mA
		V_{CC} = +3.6V, 50k DCPs, I^2C Interface in Standby State			0.4	mA
I_{LkgDig}	Leakage Current, at Pins A0, A1, SDA and SCL Pins	Voltage at pin from GND to V_{CC}	-10		10	µA
t_{DCP} (Note 15)	DCP Wiper Response Time	SCL falling edge of last bit of DCP Data Byte to wiper change			1	µs
Vpor	Power-On Recall Voltage	Minimum V_{CC} at which memory recall occurs	1.8		2.6	V

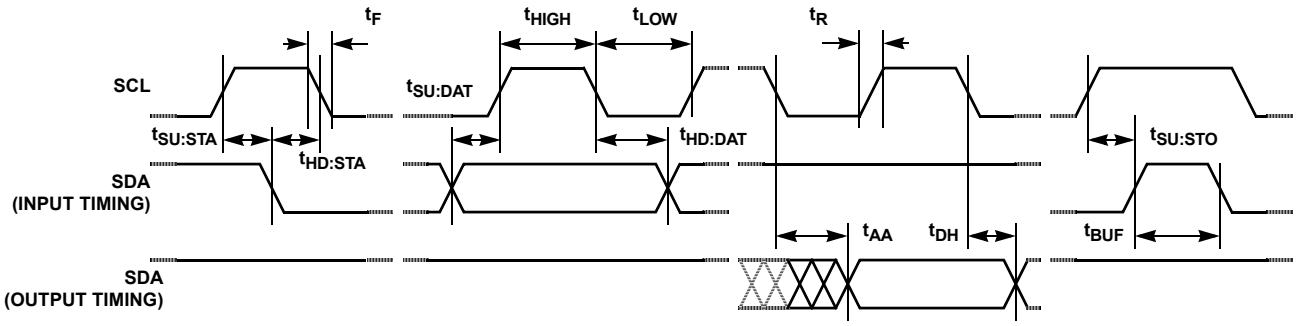
Operating Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 1)	MAX	UNITS
VccRamp	V_{CC} Ramp Rate		0.2			V/ms
t_D (Note 15)	Power-Up Delay	V_{CC} above Vpor, to DCP Initial Value Register recall completed, and I^2C Interface in Standby State.			3	ms
SERIAL INTERFACE SPECS						
V_{IL}	A1, A0, SDA, and SCL Input Buffer LOW Voltage		-0.3		0.3*V_{CC}	V
V_{IH}	A1, A0, SDA, and SCL Input Buffer HIGH Voltage		0.7*V_{CC}		V_{CC}+0.3	V
Hysteresis (Note 15)	SDA and SCL Input Buffer Hysteresis		0.05* V_{CC}			V
V_{OL} (Note 15)	SDA Output Buffer LOW Voltage, Sinking 4mA		0		0.4	V
Cpin (Note 15)	A1, A0, SDA, and SCL Pin Capacitance				10	pF
f_{SCL}	SCL Frequency				400	kHz
t_{IN} (Note 15)	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed.			50	ns
t_{AA} (Note 15)	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{CC}, until SDA exits the 30% to 70% of V_{CC} window.			900	ns
t_{BUF} (Note 15)	Time the Bus Must be Free Before the Start of a New Transmission	SDA crossing 70% of V_{CC} during a STOP condition, to SDA crossing 70% of V_{CC} during the following START condition.	1300			ns
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{CC} crossing.	1300			ns
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{CC} crossing.	600			ns
$t_{SU:STA}$	START Condition Setup Time	SCL rising edge to SDA falling edge. Both crossing 70% of V_{CC}.	600			ns
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{CC} to SCL falling edge crossing 70% of V_{CC}.	600			ns
$t_{SU:DAT}$	Input Data Setup Time	From SDA exiting the 30% to 70% of V_{CC} window, to SCL rising edge crossing 30% of V_{CC}.	100			ns
$t_{HD:DAT}$	Input Data Hold Time	From SCL rising edge crossing 70% of V_{CC} to SDA entering the 30% to 70% of V_{CC} window.	0			ns
$t_{SU:STO}$	STOP Condition Setup Time	From SCL rising edge crossing 70% of V_{CC}, to SDA rising edge crossing 30% of V_{CC}.	600			ns
$t_{HD:STO}$	STOP Condition Hold Time for Read, or Volatile Only Write	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{CC}.	600			ns
t_{DH} (Note 15)	Output Data Hold Time	From SCL falling edge crossing 30% of V_{CC}, until SDA enters the 30% to 70% of V_{CC} window.	0			ns
t_R (Note 15)	SDA and SCL Rise Time	From 30% to 70% of V_{CC}	20 + 0.1 * Cb		250	ns
t_F (Note 15)	SDA and SCL Fall Time	From 70% to 30% of V_{CC}	20 + 0.1 * Cb		250	ns
Cb (Note 15)	Capacitive Loading of SDA or SCL	Total on-chip and off-chip	10		400	pF
Rpu (Note 15)	SDA and SCL Bus Pull-Up Resistor Off-Chip	Maximum is determined by t_R and t_F. For Cb = 400pF, max is about 2~2.5kΩ. For Cb = 40pF, max is about 15~20kΩ	1			kΩ

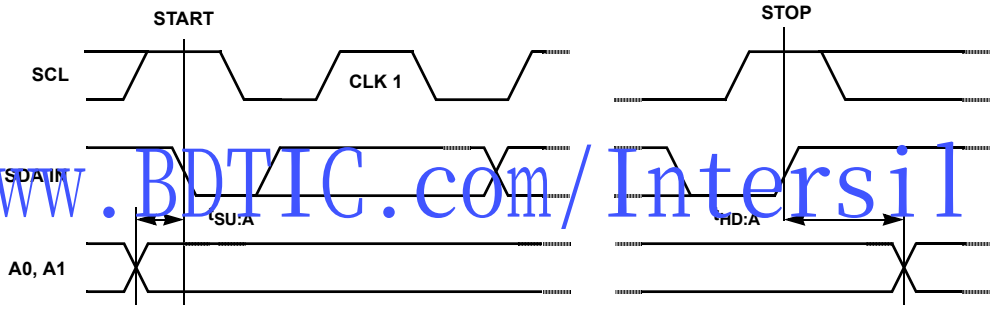
Operating Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (NOTE 1)	MAX	UNITS
$t_{SU:A}$	A1 and A0 Setup Time	Before START condition	600			ns
$t_{HD:A}$	A1 and A0 Hold Time	After STOP condition	600			ns

SDA vs SCL Timing



A0 and A1 Pin Timing



NOTES:

1. Typical values are for T_A = 25°C and 3.3V supply voltage.
2. LSB: $[V(RW)_{255} – V(RW)_0]/255$. $V(RW)_{255}$ and $V(RW)_0$ are V(RW) for the DCP register set to FF hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
3. ZS error = $V(RW)_0$/LSB.
4. FS error = $[V(RW)_{255} – V_{CC}]$/LSB.
5. DNL = $[V(RW)_i – V(RW)_{i-1}]$/LSB-1, for i = 1 to 255. i is the DCP register setting.
6. INL = $[V(RW)_i – i • LSB – V(RW)_0]$/LSB for i = 1 to 255.
7. $V_{MATCH} = [V(RWx)_i – V(RWy)_i]$/LSB, for i = 0 to 255, x = 0 to 3 and y = 0 to 3.
8. $TC_V = \frac{Max(V(RW)_i) - Min(V(RW)_i)}{[Max(V(RW)_i) + Min(V(RW)_i)]/2} \times \frac{10^6}{125°C}$ for i = 16 to 240 decimal, T = -40°C to 85°C. Max( ) is the maximum value of the wiper voltage and Min ( ) is the minimum value of the wiper voltage over the temperature range.
9. MI = $|R_{255} – R_0|/255$. R_{255} and R_0 are the measured resistances for the DCP register set to FF hex and 00 hex respectively.
10. Roffset = R_0/MI, when measuring between RW and RL.
    Roffset = R_{255}/MI, when measuring between RW and RH.
11. RDNL = $(R_i – R_{i-1})$/MI-1, for i = 32 to 255.
12. RINL = $[R_i – (MI • i) – R_0]$/MI, for i = 32 to 255.
13. $R_{MATCH} = (R_{i,x} – R_{i,y})$/MI, for i = 0 to 255, x = 0 to 3 and y = 0 to 3.
14. $TC_R = \frac{[Max(Ri) - Min(Ri)]}{[Max(Ri) + Min(Ri)]/2} \times \frac{10^6}{125°C}$ for i = 32 to 255, T = -40°C to 85°C. Max( ) is the maximum value of the resistance and Min ( ) is the minimum value of the resistance over the temperature range.
15. This parameter is not 100% tested.

Typical Performance Curves

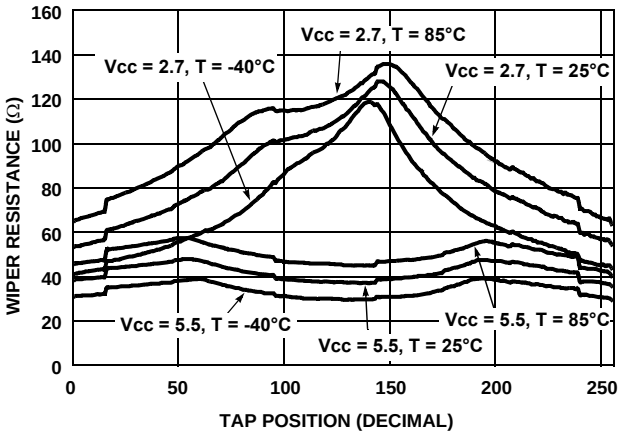


FIGURE 1. WIPER RESISTANCE vs TAP POSITION [I(RW) = Vcc/R_{TOTAL}] FOR 50kΩ (U)

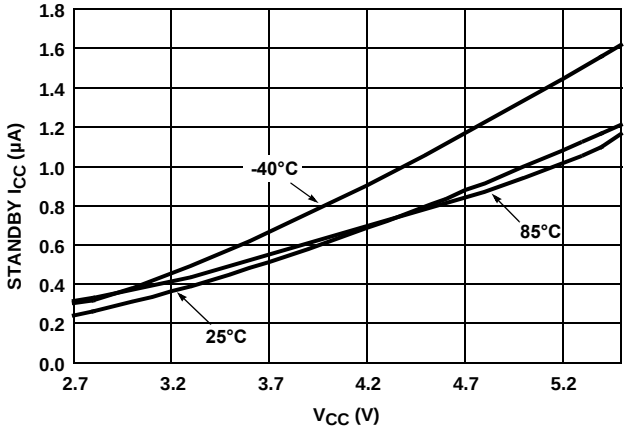


FIGURE 2. STANDBY Icc vs Vcc

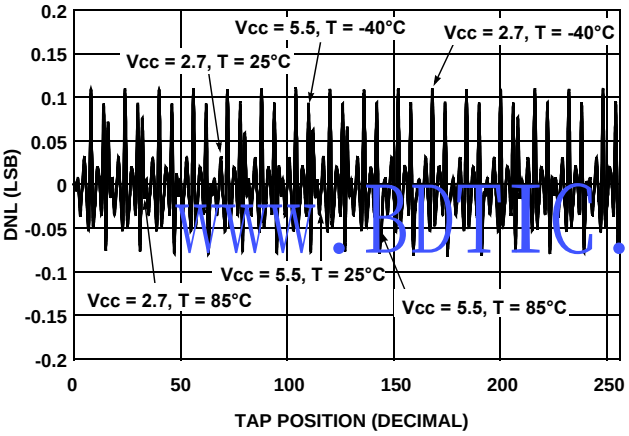


FIGURE 3. DNL vs TAP POSITION FOR 10kΩ (W)

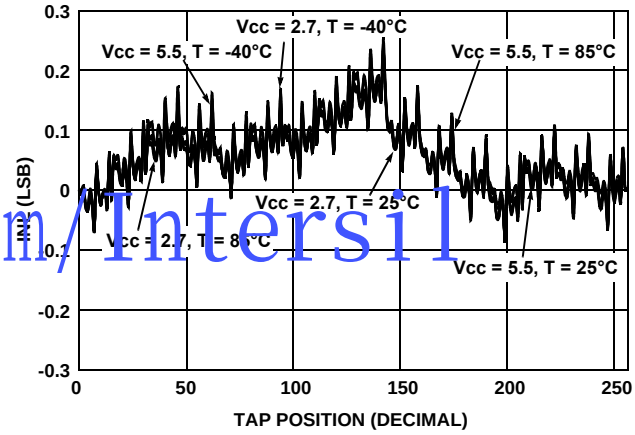


FIGURE 4. INL vs TAP POSITION FOR 10kΩ (W)

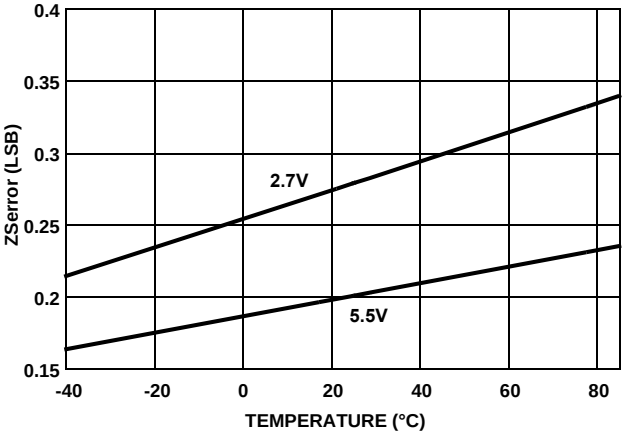


FIGURE 5. ZSerror vs TEMPERATURE

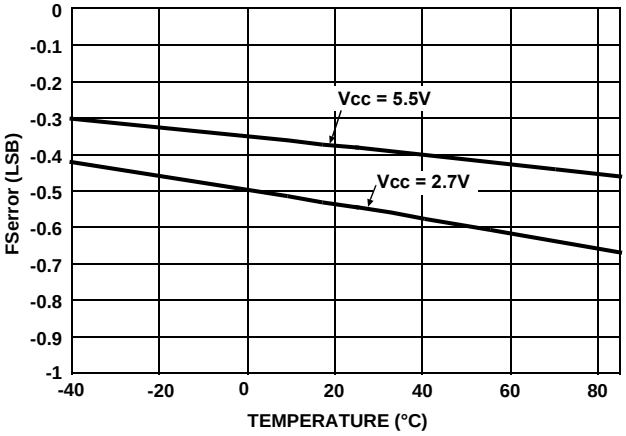


FIGURE 6. FSerror vs TEMPERATURE

Typical Performance Curves (Continued)

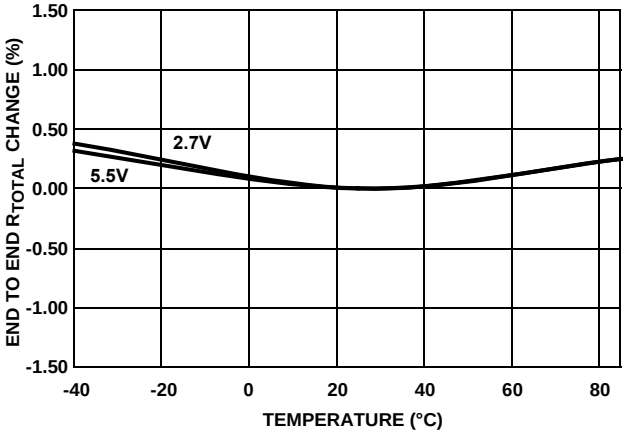


FIGURE 7. END TO END R_{TOTAL} % CHANGE vs TEMPERATURE

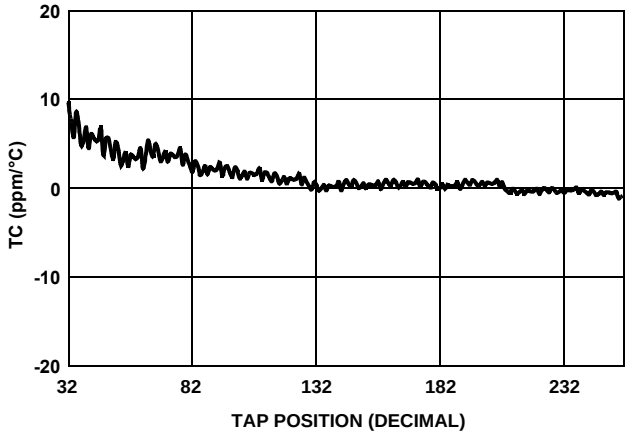


FIGURE 8. TC FOR VOLTAGE DIVIDER MODE IN ppm

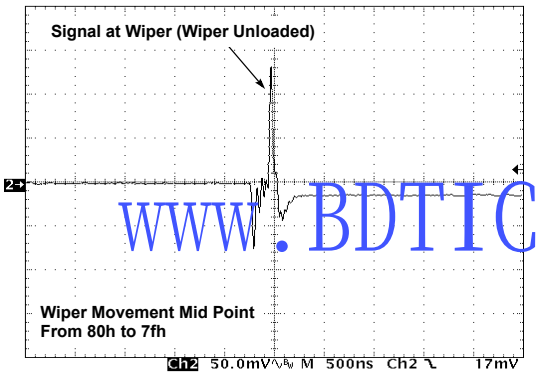


FIGURE 9. MIDSCALE GLITCH, CODE 80h TO 7Fh (WIPER 0)

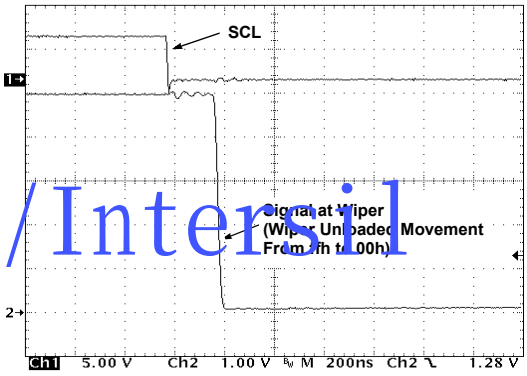


FIGURE 10. LARGE SIGNAL SETTLING TIME

Principles of Operation

The ISL90843 is an integrated circuit incorporating four DCPs with their associated registers, and an I^2C serial interface providing direct communication between a host and the potentiometers.

DCP Description

Each DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer (RH and RL pins). The RW pin of each DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by an 8-bit volatile Wiper Register (WR). Each DCP has its own WR. When the WR of a DCP contains all zeroes (WR<7:0>: 00h), its wiper terminal (RW) is closest to its “Low” terminal (RL). When the WR of a DCP contains all ones (WR<7:0>: FFh), its wiper terminal (RH) is closest to its “High” terminal (RH).

As the value of the WR increases from all zeroes (00h) to all ones (255 decimal), the wiper moves monotonically from the position closest to RL to the closest to RH. At the same time, the resistance between RW and RL increases monotonically, while the resistance between RH and RW decreases monotonically.

While the ISL90843 is being powered up, all four WRs are reset to 80h (128 decimal), which locates RW roughly at the center between RL and RH.

The WRs can be read or written directly using the I^2C serial interface as described in the following sections. The I^2C interface Address Byte has to be set to 00hex, 01hex, 02hex, and 03hex to access the WR of DCP0, DCP1, DCP2, and DCP3 respectively.

I^2C Serial Interface

The ISL90843 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the

bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL90843 operates as a slave device in all applications.

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (See Figure 11). On power-up of the ISL90843 the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL90843 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (See Figure 11). A START condition is ignored during the power-up of the device.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (See Figure 11). A STOP condition at the end of a read operation, or at the end of a write operation places the device in its standby mode.

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (See Figure 12).

The ISL90843 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL90843 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation

A valid Identification Byte contains 01010 as the five MSBs, and the following two bits matching the logic values present at pins A1 and A0. The LSB is in the Read/$\overline{\text{Write}}$ bit. Its value is “1” for a Read operation, and “0” for a Write operation (See Table 1).

TABLE 1. IDENTIFICATION BYTE FORMAT

					Logic values at pins A1, and A0 respectively		
0	1	0	1	0	A1	A0	R/$\overline{\text{W}}$
(MSB)							(LSB)

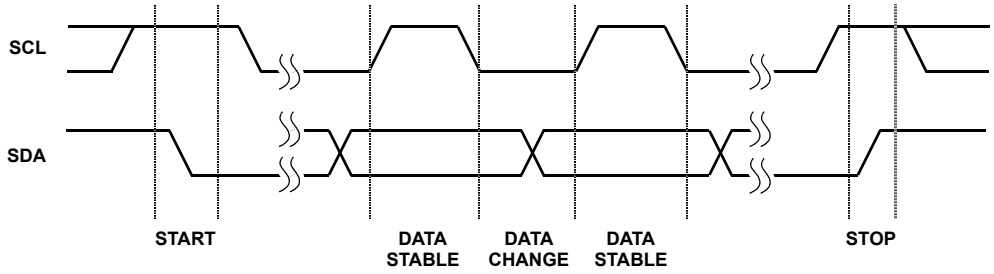


FIGURE 11. VALID DATA CHANGES, START, AND STOP CONDITIONS

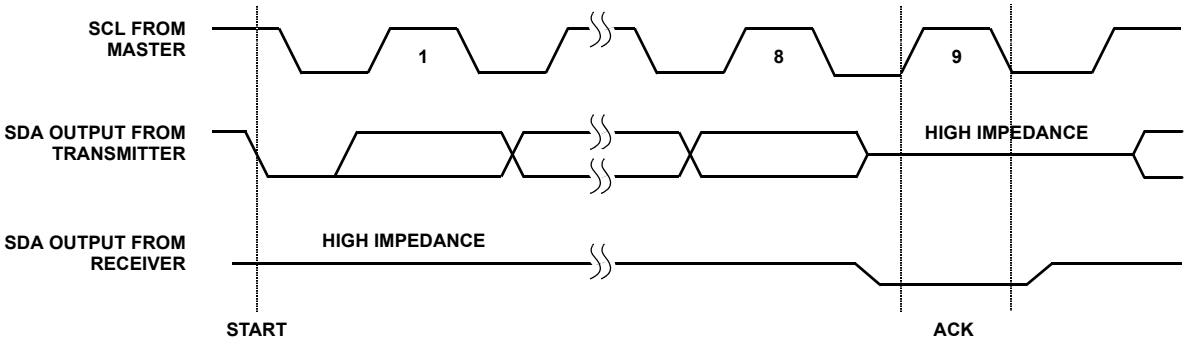


FIGURE 12. ACKNOWLEDGE RESPONSE FROM RECEIVER

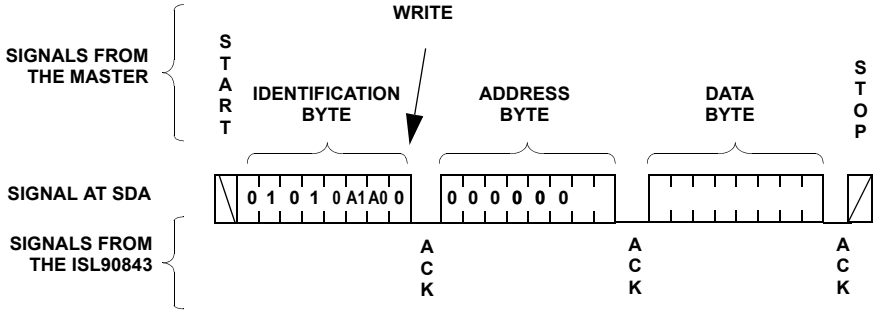


FIGURE 13. BYTE WRITE SEQUENCE

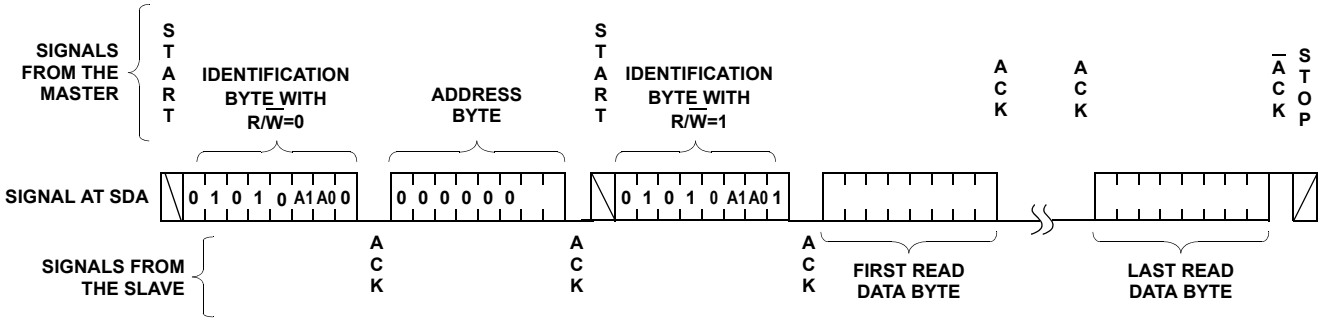


FIGURE 14. READ SEQUENCE

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL90843 responds with an ACK. At this time, the device enters its standby state (See Figure 13).

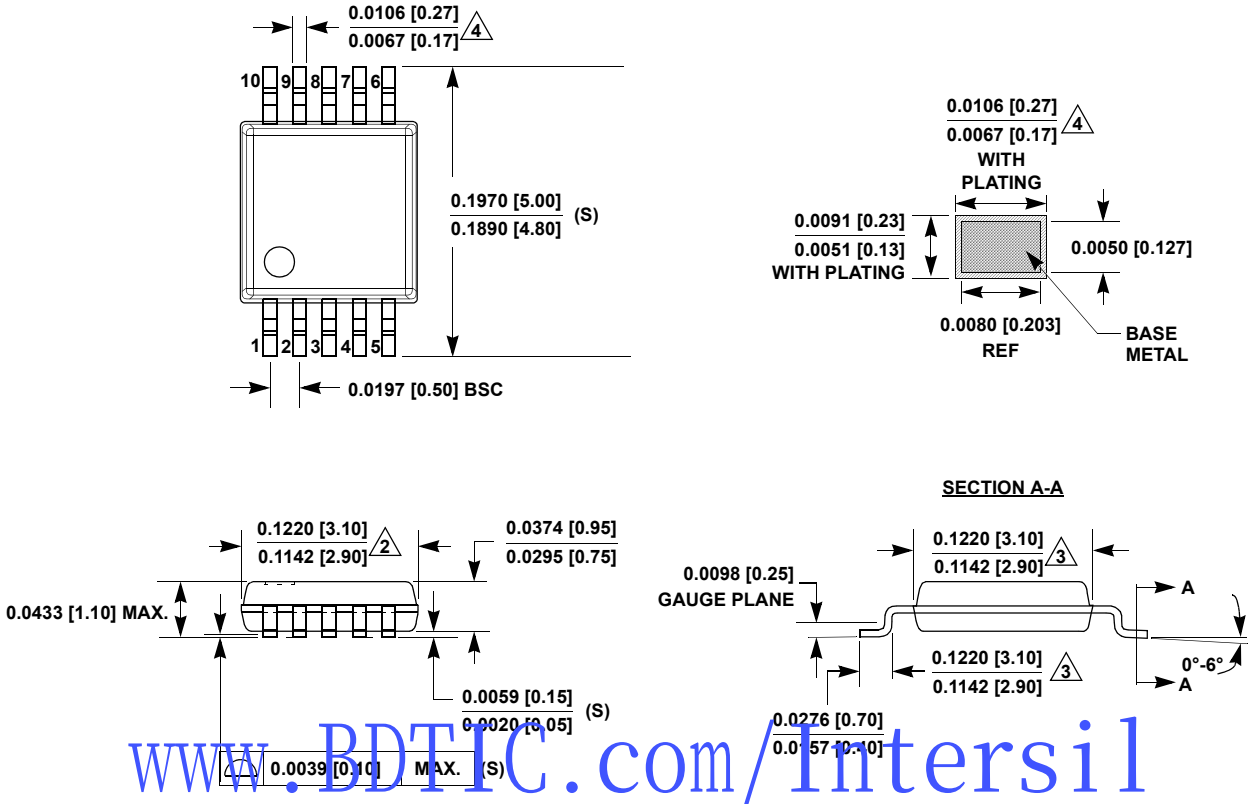
Read Operation

A Read operation consist of a three byte instruction followed by one or more Data Bytes (See Figure 14). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{W}$ bit set to “0”, an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to “1”. After each of the three bytes, the ISL90843 responds with an ACK. Then the ISL90843 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the read operation (issuing a NACK and a STOP condition) following the last bit of the last Data Byte (See Figure 14).

The Data Bytes are from the registers indicated by an internal pointer. This pointer initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. After reaching the memory location 03h the pointer “rolls over” to 00h, and the device continues to output data for each ACK received.

MSOP Packaging Information

10 Lead MSOP, Package Code



NOTES:

1. Package dimensions conform to JEDEC specification MO-187BA.
2. 2 Does not include mold flash, protrusion or gate burrs, mold flash protrusions or gate burrs shall not exceed 0.15 mm per side.
3. 3 Does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.15 mm per side.
4. 4 Does not include dambar protrusion. Allowable dambar protrusion shall be 0.8 mm.
5. Lead span/stand-off height/coplanarity are considered as special characteristics.
6. Controlling dimensions in inches [mm].