intersil®

Data Sheet | March 11, 2008 | FN6299.3

Low Noise LDO with Low I_Q and High PSRR

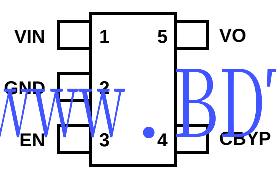
ISL9003A is a high performance single low noise, high PSRR LDO that delivers a continuous 150mA of load current. It has a low standby current and is stable with 1µF of MLCC output capacitance with an ESR of up to 200mΩ.

The ISL9003A has a very high PSRR of 90dB and output noise is 20µV_{RMS} (typical). When coupled with a no load quiescent current of 31µA (typical), and 0.5µA shutdown current, the ISL9003A is an ideal choice for portable wireless equipment.

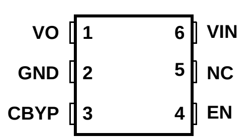
The ISL9003A comes in many fixed voltage options with ±1.8% output voltage accuracy over temperature, line and load. Other output voltage options are available on request.

Pinouts

ISL9003A
(5 LD SC-70)
TOP VIEW



ISL9003A
(6 LD 1.6x1.6 µTDFN)
TOP VIEW



Features

- High performance LDO with 150mA continuous output
- Excellent transient response to large current steps
- Excellent load regulation:
  <0.1% voltage change across full range of load current
- Very high PSRR: >90dB @ 1kHz
- Wide input voltage capability: 2.3V to 6.5V
- Extremely low quiescent current: 31µA
- Low dropout voltage: typically 200mV @ 150mA
- Low output noise: typically 20µV_{RMS} @ 100µA (1.5V)
- Stable with 1µF to 4.7µF ceramic capacitors
- Shutdown pin turns off LDO with 1µA (max) standby current
- Soft-start limits input current surge during enable
- Current limit and overheat protection
- ±1.8% accuracy over all operating conditions
- 5 Ld SC-70 package or 6 Ld µTDFN package
- -40°C to +85°C operating temperature range
- Pb-free (RoHS compliant)

Applications

- PDAs, cell phones and smart phones
- Portable instruments, MP3 players
- Handheld devices including medical handhelds

Ordering Information

PART NUMBER (Note 1)	PART MARKING	V_O VOLTAGE (V) (Note 2)	TEMP. RANGE (°C)	PACKAGE Tape and Reel (Pb-Free)	PKG. DWG. NUMBER
ISL9003AIENZ-T (Note 3)	CBK	3.30	-40 to +85	5 Ld SC-70	P5.049
ISL9003AIEMZ-T (Note 3)	CBJ	3.00	-40 to +85	5 Ld SC-70	P5.049
ISL9003AIEKZ-T (Note 3)	CCE	2.85	-40 to +85	5 Ld SC-70	P5.049
ISL9003AIEJZ-T (Note 3)	CCD	2.80	-40 to +85	5 Ld SC-70	P5.049
ISL9003AIEHZ-T (Note 3)	CCC	2.75	-40 to +85	5 Ld SC-70	P5.049
ISL9003AIEFZ-T (Note 3)	CCB	2.50	-40 to +85	5 Ld SC-70	P5.049
ISL9003AIECZ-T (Note 3)	CBY	1.80	-40 to +85	5 Ld SC-70	P5.049
ISL9003AIEBZ-T (Note 3)	CBW	1.50	-40 to +85	5 Ld SC-70	P5.049
ISL9003AIRUBZ-T (Note 3)	L	1.50	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9003AIRUCZ-T (Note 4)	G	1.80	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9003AIRUFZ-T (Note 4)	F	2.50	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9003AIRURZ-T (Note 4)	M2	2.60	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9003AIRUHZ-T (Note 4)	H	2.75	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9003AIRUJZ-T (Note 4)	J	2.80	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9003AIRUKZ-T (Note 4)	K	2.85	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9003AIRUMZ-T (Note 4)	M	3.00	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A
ISL9003AIRUNZ-T (Note 4)	N	3.30	-40 to +85	6 Ld µTDFN	L6.1.6x1.6A

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. For other output voltages, contact Intersil Marketing.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020..

Absolute Maximum Ratings

Supply Voltage (VIN) . . . . +7.1V
V_O Pin . . . . +3.6V
All Other Pins . . . . -0.3V to (VIN + 0.3V)

Recommended Operating Conditions

Ambient Temperature Range (T_A) . . . . -40°C to +85°C
Supply Voltage (VIN) . . . . 2.3V to 6.5V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)
5 Ld SC-70 Package (Note 5)	231
6 Ld µTDFN Package (Note 6)	125

Junction Temperature Range . . . . -40°C to +125°C
Operating Temperature Range . . . . -40°C to +85°C
Storage Temperature Range . . . . -65°C to +150°C
Pb-free reflow profile . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
6. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

Electrical Specifications

Unless otherwise noted, all parameters are guaranteed over the operational supply voltage and temperature range of the device as follows: T_A = -40°C to +85°C; V_{IN} = (V_O + 0.5V) to 6.5V with a minimum V_{IN} of 2.3V; C_{IN} = 1µF; C_O = 1µF; C_{BYP} = 0.01µF

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
DC CHARACTERISTICS						
Supply Voltage	V_{IN}		2.3		6.5	V
Ground Current	I_{DD}	Output Enabled; I_O = 0µA; V_{IN} < 4.2V		31	40	µA
		Output Enabled; I_O = 0µA; Full voltage range			57	µA
Shutdown Current	I_{DDS}			0.5	1.2	µA
UVLO Threshold	V_{UV+}		1.9	2.1	2.3	V
	V_{UV-}		1.6	1.8	2.0	V
Regulation Voltage Accuracy		Initial accuracy at V_{IN} = V_O + 0.5V, I_O = 10mA, T_J = +25°C	-0.7		+0.7	%
		V_{IN} = V_O + 0.5V to 6.5V, I_O = 10µA to150mA, T_J = +25°C	-0.8		+0.8	%
		V_{IN} = V_O + 0.5V to 6.5V, I_O = 10µA to 150mA, T_J = -40°C to +125°C	-1.8		+1.8	%
Maximum Output Current	I_{MAX}	Continuous	150			mA
Internal Current Limit	I_{LIM}		175	265	355	mA
Drop-out Voltage (Note 8)	V_{DO1}	I_O = 150mA; V_O < 2.5V		300	500	mV
	V_{DO2}	I_O = 150mA; 2.5V ≤ V_O ≤ 2.8V		250	400	mV
	V_{DO3}	I_O = 150mA; 2.8V < V_O		200	325	mV
Thermal Shutdown Temperature	T_{SD+}			140		°C
	T_{SD-}			110		°C
AC CHARACTERISTICS						
Ripple Rejection (Note 7)		I_O = 10mA, V_{IN} = 2.8V(min), V_O = 1.8V, C_{BYP} = 0.1µF				
		@ 1kHz		90		dB
		@ 10kHz		70		dB
		@ 100kHz		50		dB
Output Noise Voltage (Note 7)		V_O = 1.5V, T_A = +25°C, C_{BYP} = 0.1µF				
		BW = 10Hz to 100kHz, I_O = 100µA		20		μV_{RMS}
		BW = 10Hz to 100kHz, I_O = 10mA		30		μV_{RMS}

Electrical Specifications Unless otherwise noted, all parameters are guaranteed over the operational supply voltage and temperature range of the device as follows: T_A = -40°C to +85°C; V_{IN} = (V_O + 0.5V) to 6.5V with a minimum V_{IN} of 2.3V; C_{IN} = 1µF; C_O = 1µF; C_{BYP} = 0.01µF **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
DEVICE START-UP CHARACTERISTICS						
Device Enable tIme	t_{EN}	Time from assertion of the EN pin to when the output voltage reaches 95% of the V_O(nom).		250	500	µs
LDO Soft-start Ramp Rate	t_{SSR}	Slope of linear portion of LDO output voltage ramp during start-up		30	60	µs/V
EN PIN CHARACTERISTICS						
Input Low Voltage	V_{IL}		-0.3		0.4	V
Input High Voltage	V_{IH}		1.4		V_{IN} + 0.3	V
Input Leakage Current	I_{IL}, I_{IH}				0.1	µA
Pin Capacitance	C_{PIN}	Informative		5		pF

NOTES:

7. Limits established by characterization and are not production tested.
8. V_O = 0.98 * V_O(NOM); Valid for V_O greater than 1.85V.
9. Parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested

Typical Performance Curves

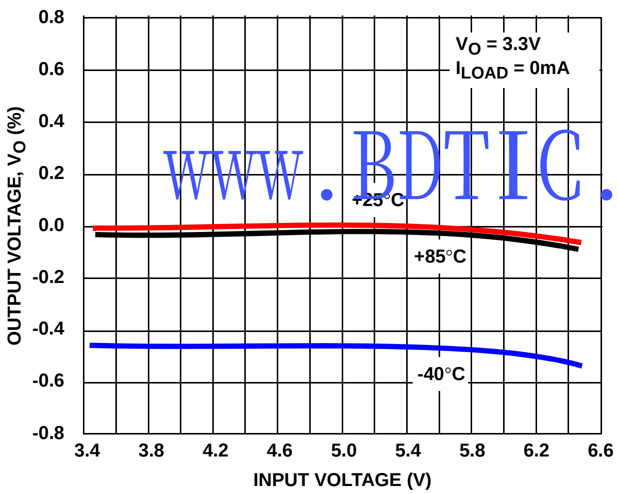


FIGURE 1. OUTPUT VOLTAGE vs INPUT VOLTAGE (3.3V OUTPUT)

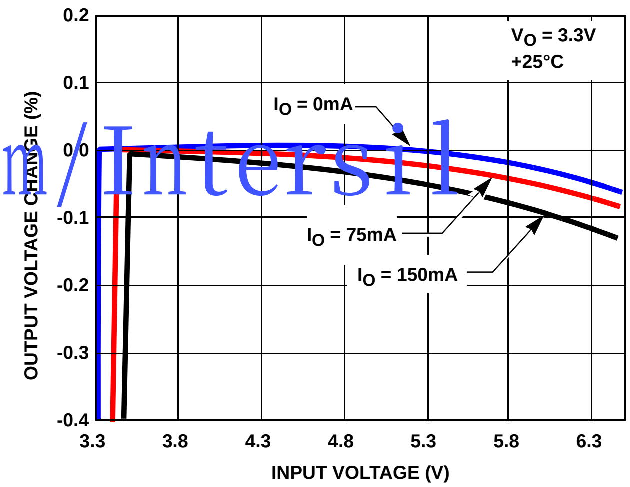


FIGURE 2. OUTPUT VOLTAGECHANGE (%) vs INPUT VOLTAGE (3.3V OUTPUT)

Typical Performance Curves (Continued)

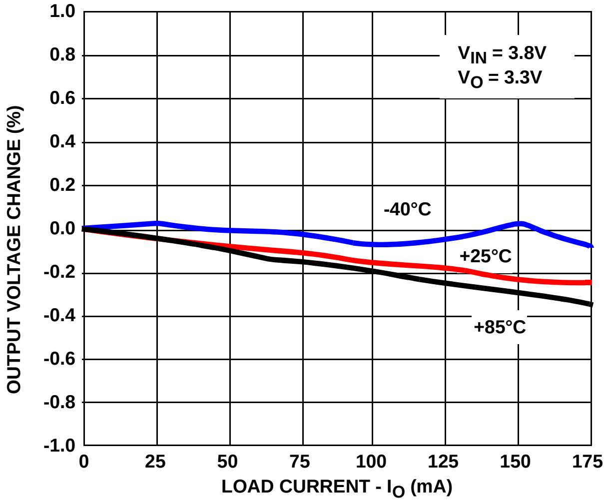


FIGURE 3. OUTPUT VOLTAGE vs LOAD CURRENT

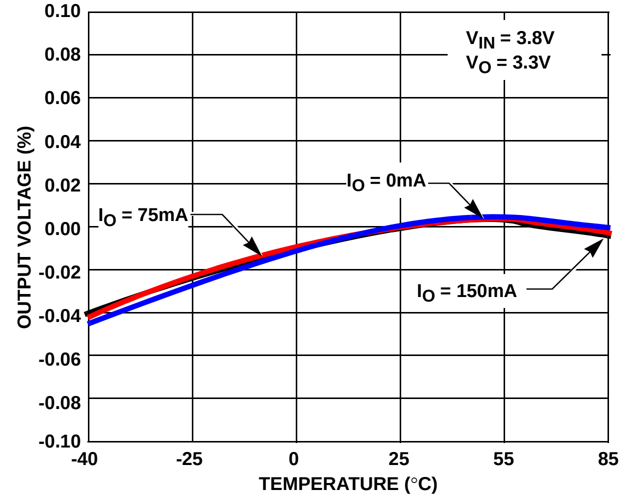


FIGURE 4. OUTPUT VOLTAGE vs TEMPERATURE

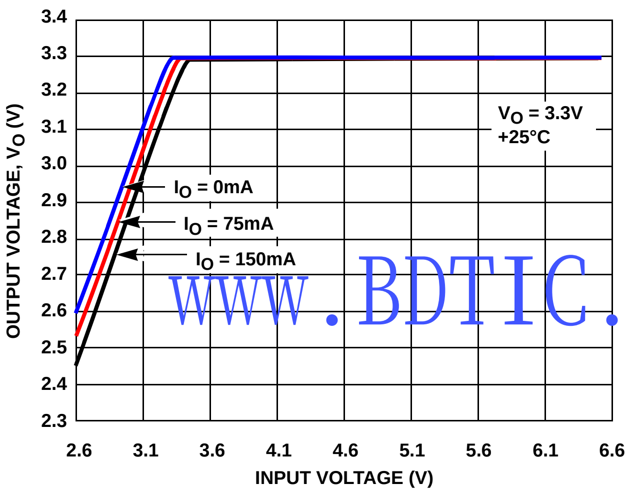


FIGURE 5. DROPOUT VOLTAGE vs INPUT VOLTAGE (3.3V OUTPUT)

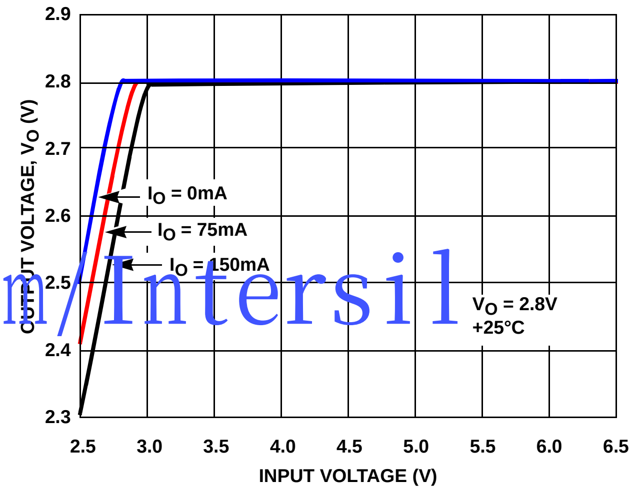


FIGURE 6. DROPOUT VOLTAGE vs INPUT VOLTAGE (2.8V OUTPUT)

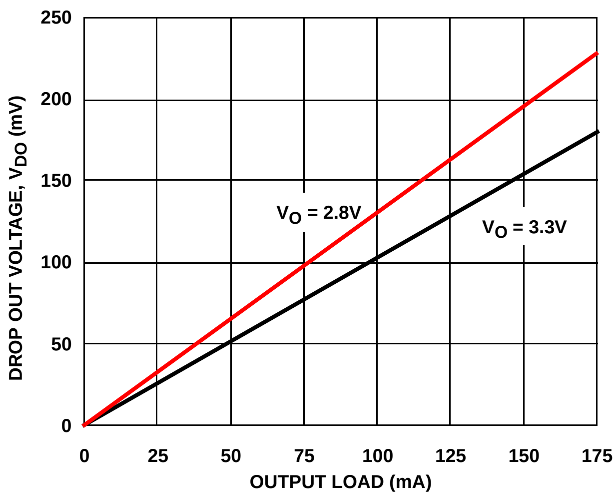


FIGURE 7. DROPOUT VOLTAGE vs LOAD CURRENT

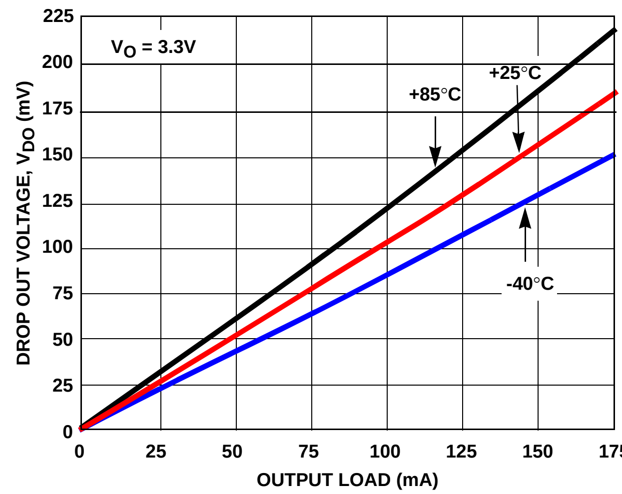


FIGURE 8. DROPOUT VOLTAGE vs LOAD CURRENT

Typical Performance Curves (Continued)

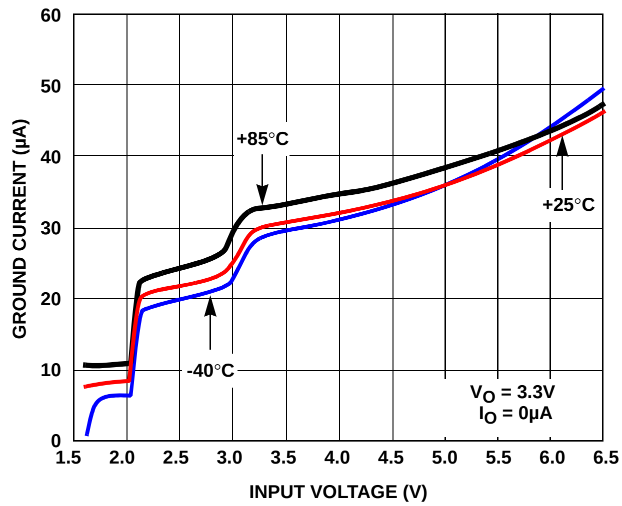


FIGURE 9. GROUND CURRENT vs INPUT VOLTAGE

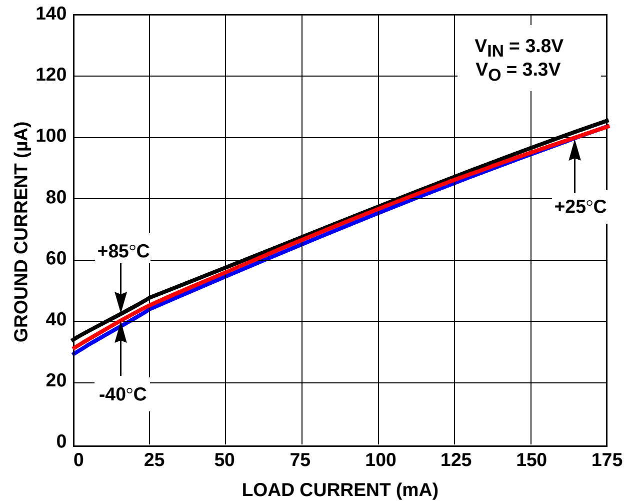


FIGURE 10. GROUND CURRENT vs LOAD

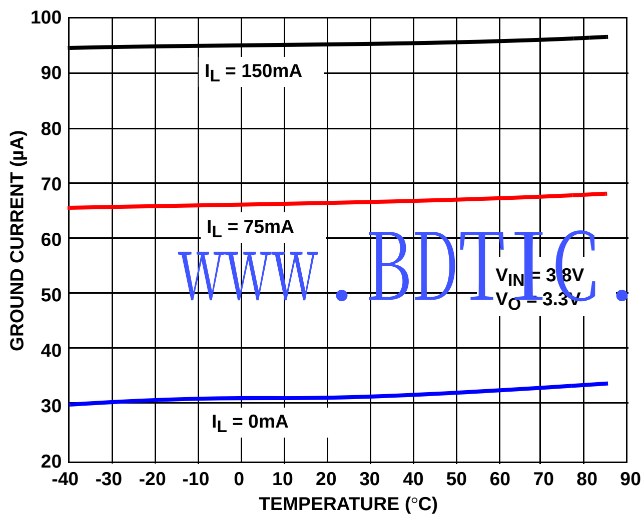


FIGURE 11. GROUND CURRENT vs TEMPERATURE

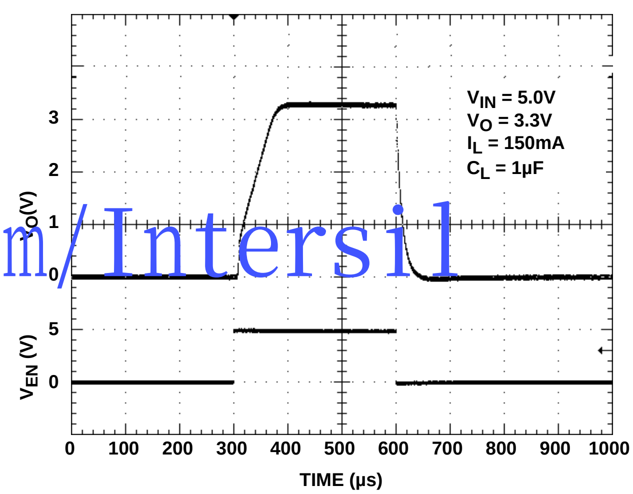


FIGURE 12. TURN ON/TURN OFF RESPONSE

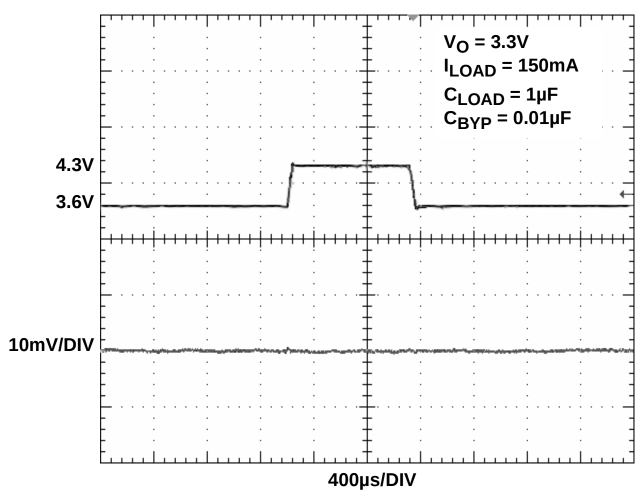


FIGURE 13. LINE TRANSIENT RESPONSE, 3.3V OUTPUT

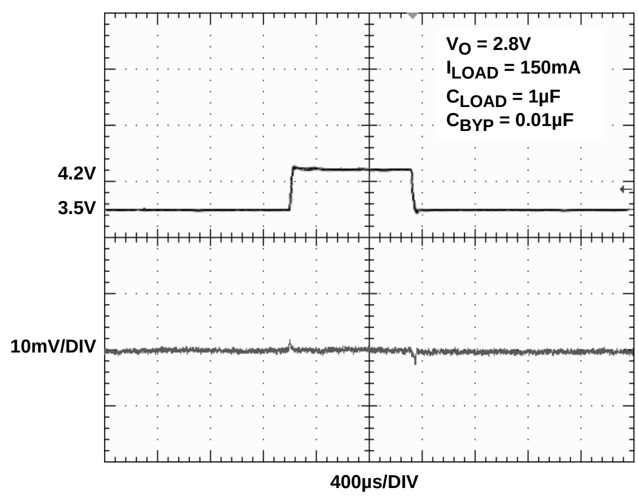


FIGURE 14. LINE TRANSIENT RESPONSE, 2.8V OUTPUT

Typical Performance Curves (Continued)

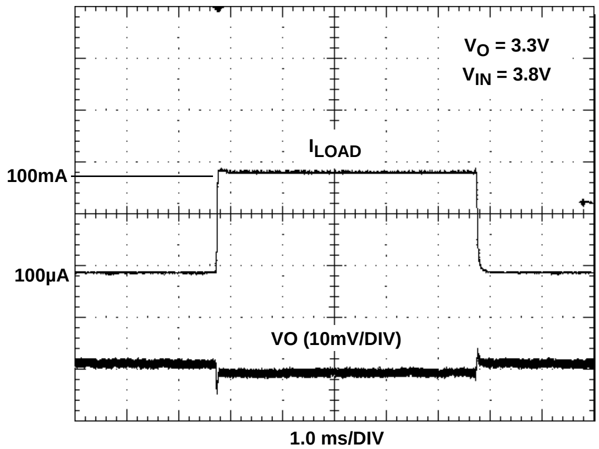


FIGURE 15. LOAD TRANSIENT RESPONSE

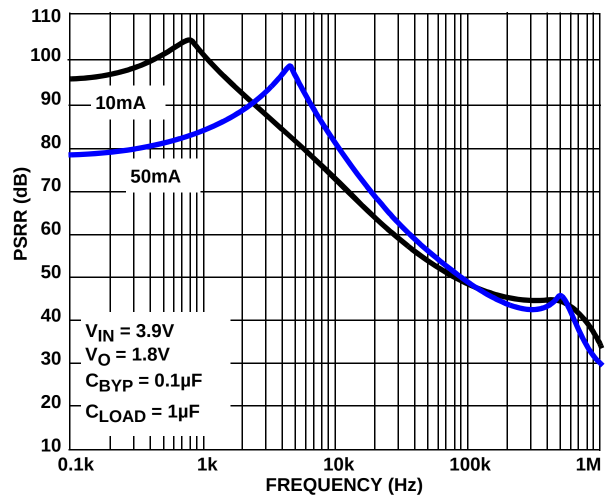


FIGURE 16. PSRR vs FREQUENCY

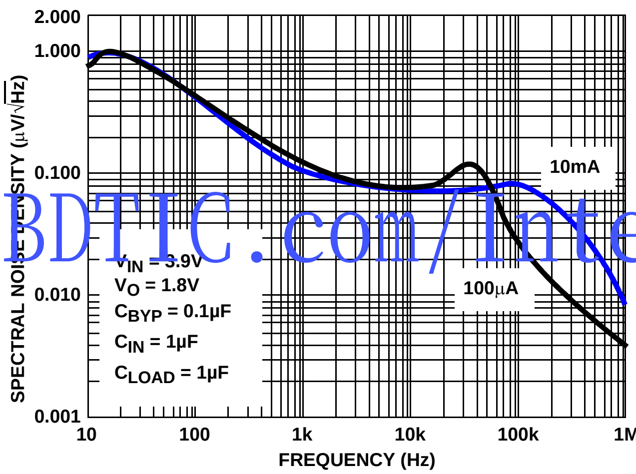
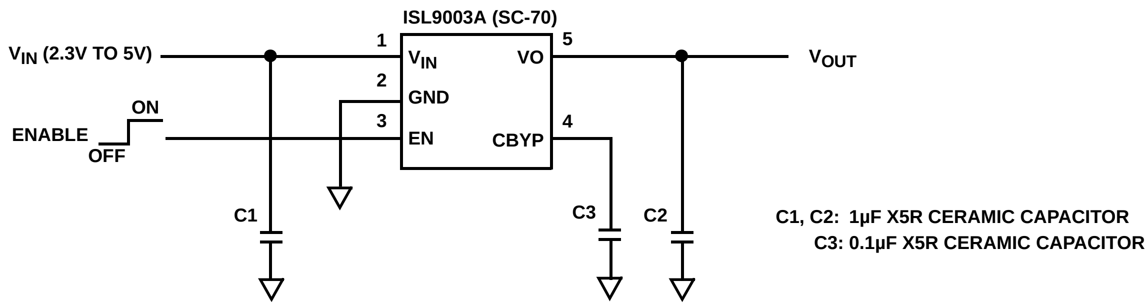


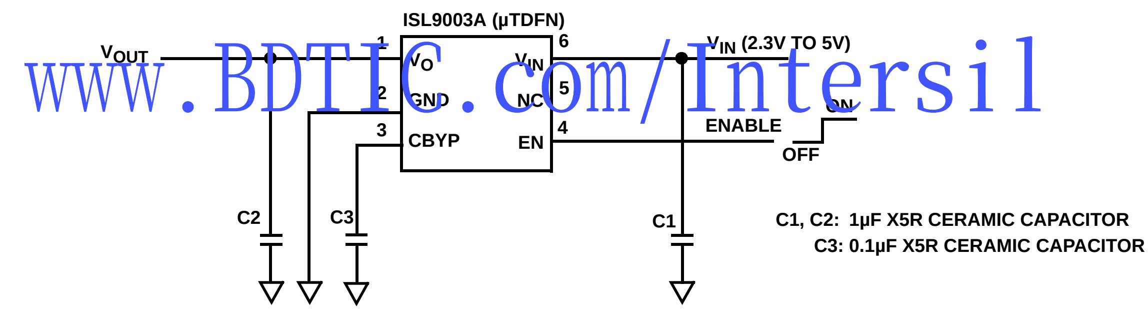
FIGURE 17. SPECTRAL NOISE DENSITY vs FREQUENCY

Pin Description

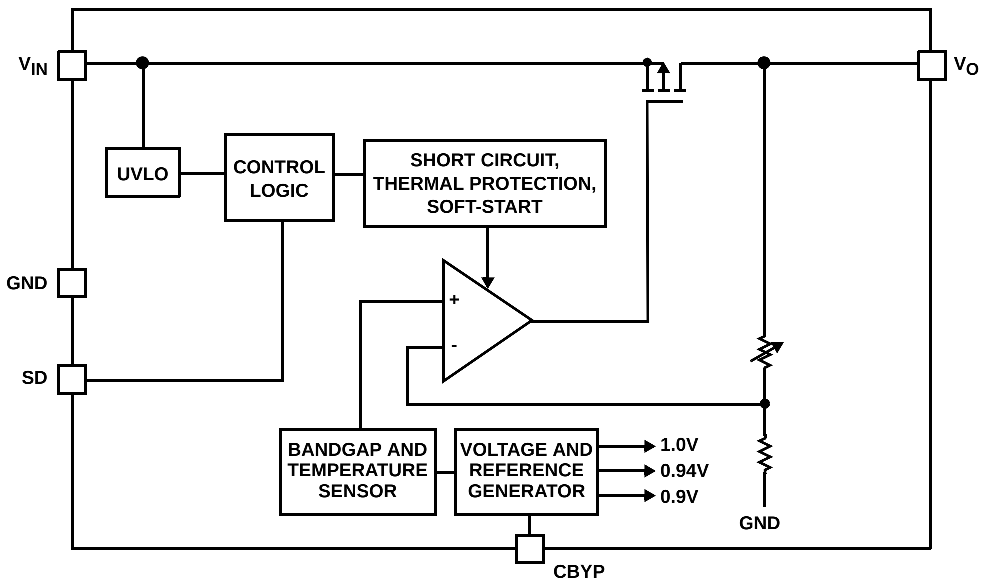
5 LD SC-70 PIN NUMBER	6 LD µTDFN PIN NUMTBER	PIN NAME	DESCRIPTION
1	6	V_{IN}	Supply Voltage/LDO Input. Connect a 1µF capacitor to GND.
2	2	GND	GND is the connection to system ground. Connect to PCB Ground plane.
3	4	EN	Output Enable. When this signal goes high, the LDO is turned on.
4	3	CBYP	Reference Bypass Capacitor Pin. Optionally connect capacitor of value 0.01µF to 1µF between this pin and GND to tune in the desired noise and PSRR performance.
5	1	V_O	LDO Output. Connect a 1µF capacitor of value to GND.
-	5	NC	No Connect.

Typical Application





Block Diagram



Functional Description

The ISL9003A contains all circuitry required to implement a high performance LDO. High performance is achieved through a circuit that delivers fast transient response to varying load conditions. In a quiescent condition, the ISL9003A adjusts its biasing to achieve the lowest standby current consumption.

The device also integrates current limit protection, smart thermal shutdown protection, and soft-start. Smart Thermal shutdown protects the device against overheating. Soft-start minimizes start-up input current surges without causing excessive device turn-on time.

Power Control

The ISL9003A has an enable pin, (EN), to control power to the LDO output. When EN is low, the device is in shutdown mode. In this condition, all on-chip circuits are off, and the device draws minimum current, typically less than 0.3µA. When the EN pin goes high, the device first polls the output of the UVLO detector to ensure that VIN voltage is at least 2.1V (typical). Once verified, the device initiates a start-up sequence. During the start-up sequence, trim settings are first read and latched. Then, sequentially, the bandgap, reference voltage and current generation circuitry turn-on. Once the references are stable, the LDO powers-up.

During operation, whenever the VIN voltage drops below about 1.84V, the ISL9003A immediately disables the LDO output. When VIN rises back above 2.1V (assuming the EN pin is high), the device re-initiates its start-up sequence and LDO operation resumes automatically.

Reference Generation

The reference generation circuitry includes a trimmed bandgap, a trimmed voltage reference divider, a trimmed current reference generator, and an RC noise filter. The filter includes the external capacitor connected to the CBYP pin. A 0.01µF capacitor connected CBYP implements a 100Hz lowpass filter, and is recommended for most high performance applications. For the lowest noise application, a 0.1µF or greater CBYP capacitor should be used. This filters the reference noise to below the 10Hz to 1kHz frequency band, which is crucial in many noise-sensitive applications.

The bandgap generates a zero temperature coefficient (TC) voltage for the regulator reference and other voltage references required for current generation and over-temperature detection.

A current generator provides references required for adaptive biasing as well as references for LDO output current limit and thermal shutdown determination.

LDO Regulation and Programmable Output Divider

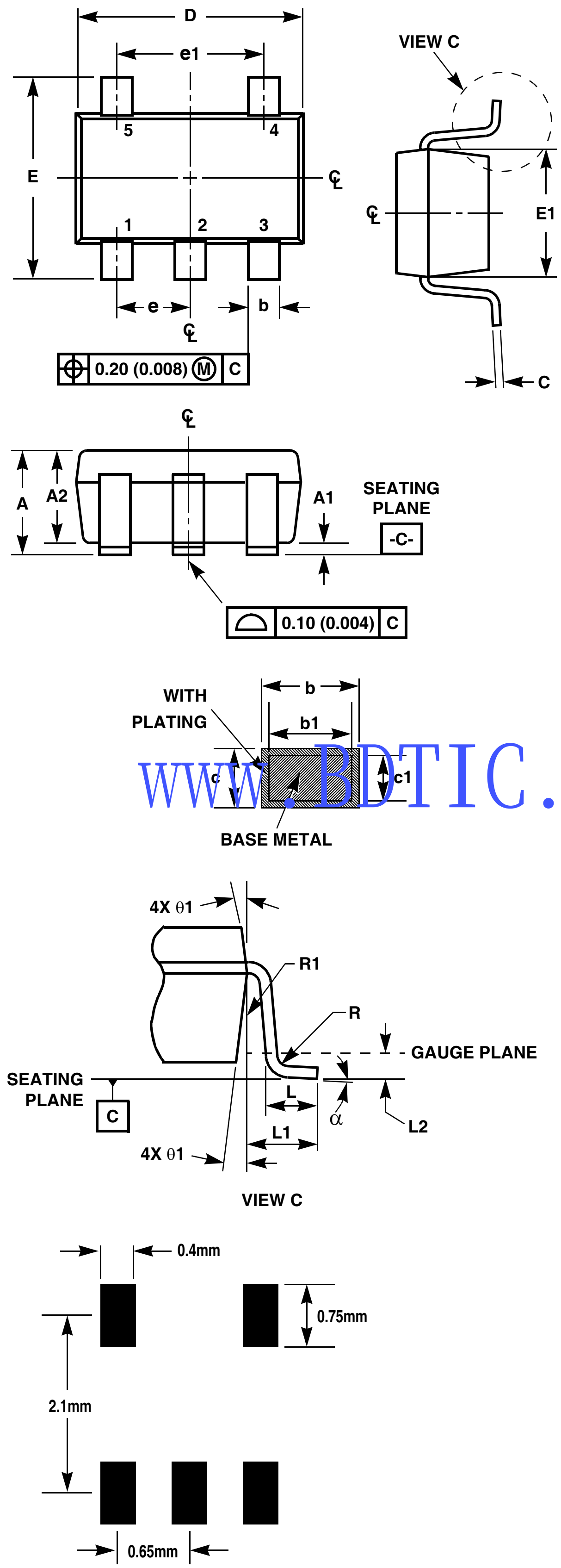
The LDO Regulator is implemented with a high-gain operational amplifier driving a PMOS pass transistor. The design of the ISL9003A provides a regulator that has low quiescent current, fast transient response, and overall stability across all operating and load current conditions. LDO stability is guaranteed for a 1µF to 4.7µF output capacitor that has a tolerance better than 20% and ESR less than 200mΩ. The design is performance-optimized for a 1µF capacitor. Unless limited by the application, use of an output capacitor value above 4.7µF is not recommended as LDO performance improvement is minimal. Soft-start circuitry integrated into each LDO limits the initial ramp-up rate to about 30µs/V to minimize current surge. The ISL9003A provides short-circuit protection by limiting the output current to about 265mA (typ).

The LDO uses an independently trimmed 1V reference as its input. An internal resistor divider drops the LDO output voltage down to 1V. This is compared to the 1V reference for regulation. The resistor division ratio is programmed in the factory.

Overheat Detection

The bandgap outputs a proportional-to-temperature current that is indicative of the temperature of the silicon. This current is compared with references to determine if the device is in danger of damage due to overheating. When the die temperature reaches about +140°C, the LDO momentarily shuts down until the die cools sufficiently. In the overheat condition, if the LDO sources more than 50mA it will be shut off. Once the die temperature falls back below about +110°C, the disabled LDO is re-enabled and soft-start automatically takes place.

Small Outline Transistor Plastic Packages (SC70-5)



TYPICAL RECOMMENDED LAND PATTERN

P5.049

5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.031	0.043	0.80	1.10	-
A1	0.000	0.004	0.00	0.10	-
A2	0.031	0.039	0.80	1.00	-
b	0.006	0.012	0.15	0.30	-
b1	0.006	0.010	0.15	0.25	
c	0.003	0.009	0.08	0.22	6
c1	0.003	0.009	0.08	0.20	6
D	0.073	0.085	1.85	2.15	3
E	0.071	0.094	1.80	2.40	-
E1	0.045	0.053	1.15	1.35	3
e	0.0256 Ref		0.65 Ref		-
e1	0.0512 Ref		1.30 Ref		-
L	0.010	0.018	0.26	0.46	4
L1	0.017 Ref.		0.420 Ref.		-
L2	0.006 BSC		0.15 BSC		
α	0^{o}	8^{o}	0^{o}	8^{o}	-
N	5		5		5
R	0.004	-	0.10	-	
R1	0.004	0.010	0.15	0.25	

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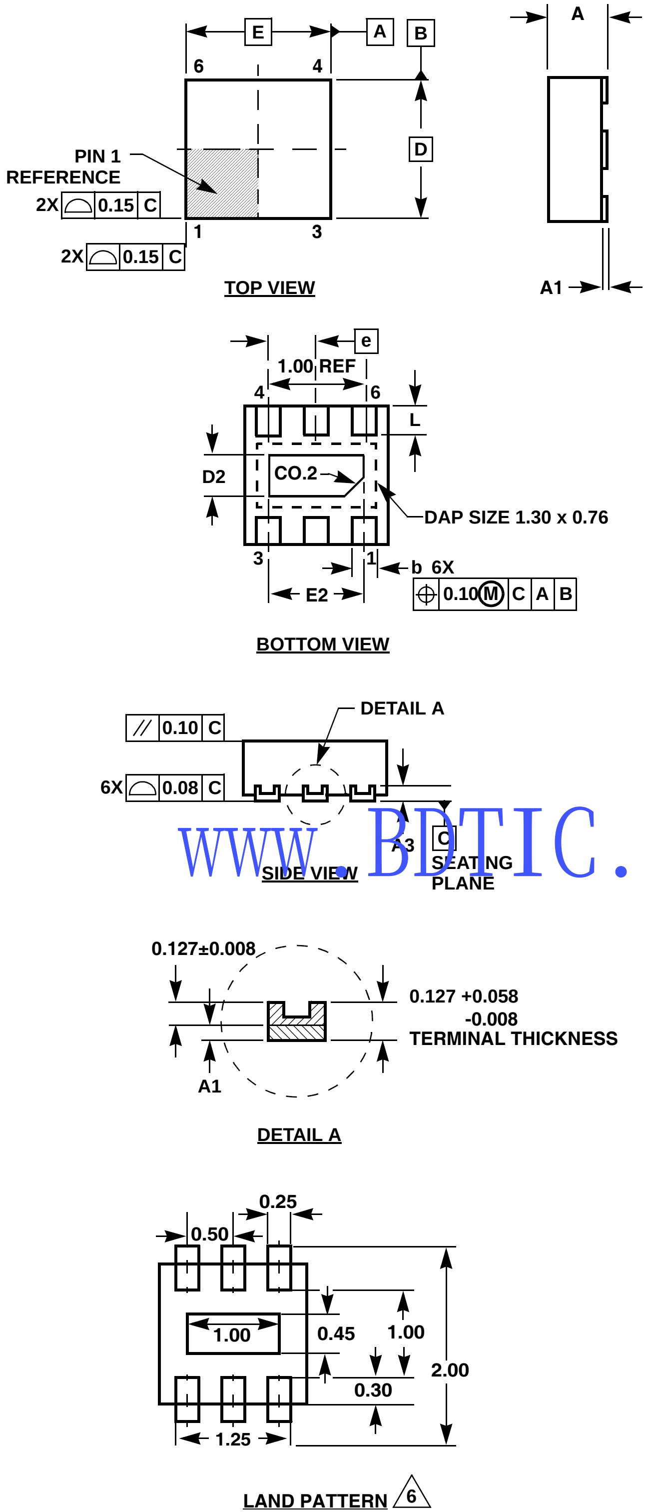
NOTES:

1. Dimensioning and tolerances per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC70 and JEDEC MO-203AA.
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to gauge plane.
5. “N” is the number of terminal positions.
6. These Dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

Ultra Thin Dual Flat No-Lead Plastic Package (UTDFN)



L6.1.6x1.6A

6 LEAD ULTRA THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS MIN	NOMINAL	MAX	NOTES
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3	0.127 REF			-
b	0.15	0.20	0.25	-
D	1.55	1.60	1.65	4
D2	0.40	0.45	0.50	-
E	1.55	1.60	1.65	4
E2	0.95	1.00	1.05	-
e	0.50 BSC			-
L	0.25	0.30	0.35	-

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NOTES:

1. Dimensions are in mm. Angles in degrees.
2. Coplanarity applies to the exposed pad as well as the terminals. Coplanarity shall not exceed 0.08mm.
3. Warpage shall not exceed 0.10mm.
4. Package length/package width are considered as special characteristics.
5. JEDEC Reference MO-229.
6. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.