Data Sheet | October 29, 2007 | FN6575.0

Enhanced Product (EP) 6.0A Dual Synchronous Buck Regulator with Integrated MOSFETs

The ISL65426MREP is a high efficiency dual output monolithic synchronous buck converter operating over an input voltage range of 2.5V to 5.5V. This single chip power solution provides two output voltages which are selectable or externally adjustable from 1.2V to 80% of the supply voltage while delivering up to 6.0A of total combined output current when used at T_J of +125°C or less. The two PWMs are synchronized 180° out of phase reducing the RMS input current and ripple voltage.

The ISL65426MREP switches at a fixed frequency of 1MHz and utilizes current-mode control with integrated compensation to minimize the size and number of external components. The internal synchronous power switches are optimized for good thermal performance, high efficiency, and eliminate the need for an external Schottky diode.

A unique power block architecture allows partitioning to support one of four configuration options. One master power block is associated with each synchronous converter channel. Four floating slave power blocks allow the user to assign them to either channel. Proper external configuration of the power blocks is verified internally prior to soft-start initialization.

Independent enable inputs allow for synchronization or sequencing soft-start intervals of the two converter channels. A third enable input allows additional sequencing for multi-input bias supply designs. Individual power good indicators (PG1, PG2) signal when output voltage is within regulation window.

The ISL65426MREP integrates protection for both synchronous buck regulator channels. The fault conditions include overcurrent, undervoltage, and IC thermal monitor.

High integration contained in a thin Quad Flat No-lead (QFN) package makes the ISL65426MREP an ideal choice to power many of today's small form factor applications. A single chip solution for large scale digital ICs, like field programmable gate arrays (FPGA), requiring separate core and I/O voltages.

Device Information

The specifications for an Enhanced Product (EP) device are defined in a Vendor Item Drawing (VID), which is controlled by the Defense Supply Center in Columbus (DSCC). "Hot-links" to the applicable VID and other supporting application information are provided on our website.

Features

- Specifications per DSCC VID V62/07639
- Full Mil-Temp Electrical Performance from -55°C to +125°C
- Controlled Baseline with One Wafer Fabrication Site and One Assembly/Test Site
- Full Homogeneous Lot Processing in Wafer Fab
- Current Density Validated per MIL-PRF-38535
- Full Traceability Through Assembly and Test by Date/Trace Code Assignment
- Enhanced Process Change Notification
- Enhanced Obsolescence Management
- Eliminates Need for Up-Screening a COTS Component
- High Efficiency of up to 90%
- Fixed Frequency: 1MHz
- Operates From 2.5V to 5.5V Supply
- ±2.0% Reference
- Flexible Output Voltage Options
  - Programmable 2-Bit VID Input
  - Adjustable Output From 1.2V to 4.0V
- Power Blocks are Rated at:
  - 1A typ for T_J < +125°C and VIN Range 4.0V to 5.5V
  - 0.7A typ for T_J < +125°C and VIN Range 2.5V to 5.5V
- Ultra-Compact DC/DC Converter Design
- PWMs Synchronized 180° Out of Phase
- Independent Enable Inputs and System Enable
- Independent Output Digital Soft-Start
- Power Good Output Voltage Monitor
- Short-Circuit and Thermal-Overload Protection
- Overcurrent and Undervoltage Protection

Applications

- FPGA, CPLD, DSP, and CPU Core and I/O Voltages
- Point-of-Load Regulation in Distributed Power Systems

Ordering Information

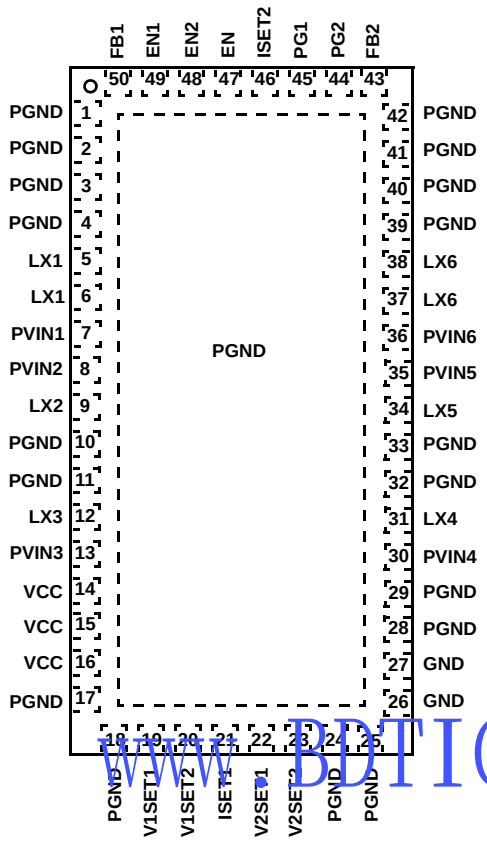
VENDOR PART NUMBER (Notes 1, 2)	VENDOR ITEM DRAWING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL65426MREP	V62/07639-01XB	-55 to +125	50 Ld 5x10 QFN	L50.5x10

NOTES:

1. Add -TK suffix for 1000 piece tape and reel. Please refer to TB347 for details on reel specifications.
2. Devices must be procured to the VENDOR PART NUMBER.

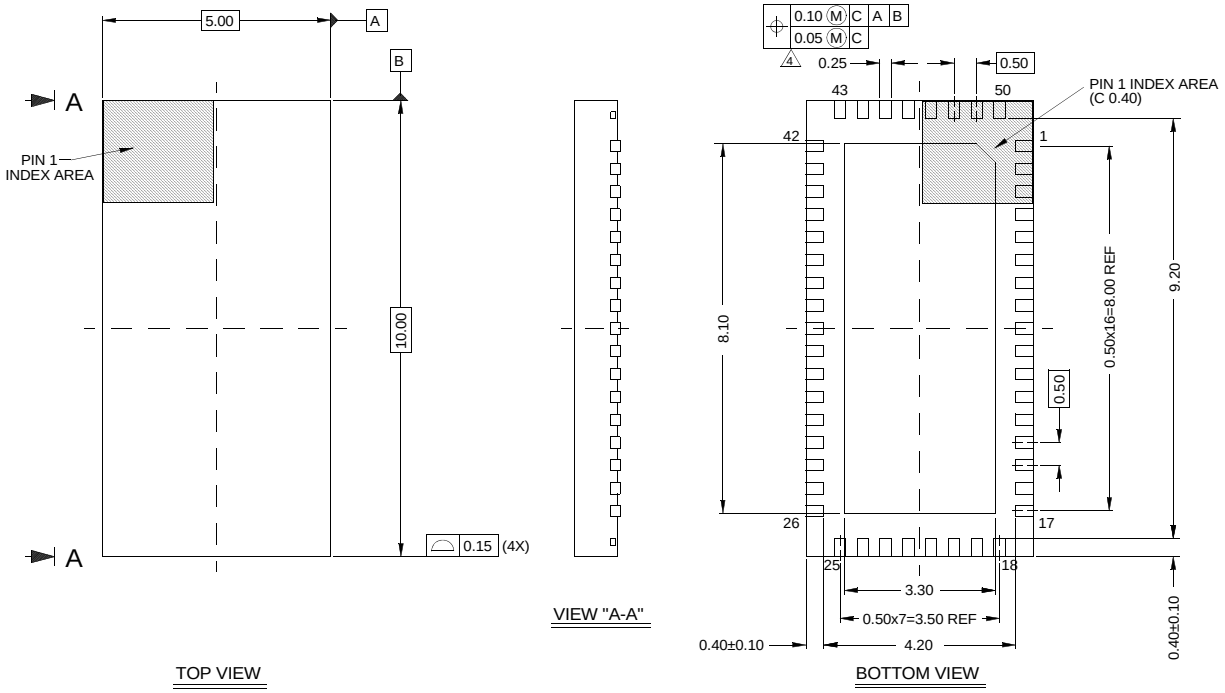
Pinout

ISL65426MREP
(50 LD QFN)
TOP VIEW



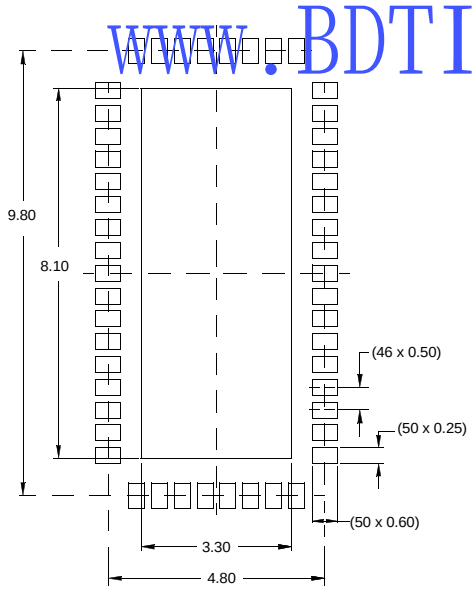
L50.5x10

50 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 7/06

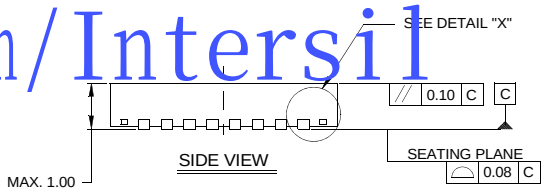


TOP VIEW

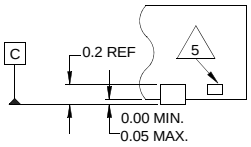
BOTTOM VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MM.
2. UNLESS OTHERWISE SPECIFIED TOLERANCE : DECIMAL ±0.05
   ANGULAR ±2×
3. DIMENSIONING AND TOLERANCE PER ASME Y 14.5M-1994.
4. DIMENSION LEAD WIDTH APPLIES TO THE PLATED TERMINAL AND IS MEASURED BETWEEN 0.23MM AND 0.28MM FROM THE TERMINAL TIP.
5. TIEBAR SHOWN (if present) IS A NON-FUNCTIONAL FEATURE