Data Sheet | August 10, 2007 | FN9190.2

Dual Output LNB Supply and Control Voltage Regulator with I²C Interface for Advanced Satellite Set-Top Box Designs

The ISL6422 is a highly integrated voltage regulator and interface IC, specifically designed for supplying power and control signals from advanced satellite set-top box (STB) modules to the low noise blocks (LNBs) of two antenna ports. The device is consists of two independent current-mode boost PWMs and two low-noise linear regulators along with the circuitry required for 22kHz tone generation, modulation and I²C device interface. The device makes the total LNB supply design simple, efficient and compact with low external component count.

Two independent current-mode boost converters provide the linear regulators with input voltages that are set to the final output voltages, plus typically 0.8V to insure minimum power dissipation across each linear regulator. This maintains constant voltage drops across each linear pass element while permitting adequate voltage range for tone injection.

The final regulated output voltages are available at two output terminals to support simultaneous operation of two antenna ports for dual tuners. The outputs for each PWM can be controlled in two ways:

- Full control from I²C using the VTOP1, VTOP2, VBOT1, and VBOT12 bits, or
- Set the I²C to the lower range (13V/14V) and switch to the higher range (18V/19V) with the SELVTOP1 or SELVTOP2 pin.

All the functions on this IC are controlled via the I²C bus by writing 8-bit words onto the System Registers (SR). The same register can be read back, and 4-bits per output will report the diagnostic status. Separate enable commands sent on the I²C bus provide independent standby mode control for each PWM and linear combination, disabling the output into shutdown mode. Each output channel is capable of providing 750mA of continuous current. The overcurrent limit can be digitally programmed.

The External modulation input EXTM1, EXTM2 can accept a modulated Diseqc command and transfer it symmetrically to the output. Alternatively, the EXTM1 or EXTM2 pin can be used to modulate the continuous internal tone.

The $\overline{FLT}$ pin serves as an interrupt for the processor when an over temperature, overcurrent or backwards overcurrent fault conditions is detected by the LNB controller or when both channels are disabled by the I²C EN bits set low. The nature of the fault can be read of the I²C registers.

Features

- Single Chip Power Solution
  - True Dual Operation for 2-Tuner/2-Dish Applications
  - Both Outputs May be Enabled Simultaneously at Maximum Power
  - Integrated DC/DC Converter and I²C Interface
- Switch-Mode Power Converter for Lowest Dissipation
  - Boost PWMs with >92% Efficiency
  - Selectable 13.3V or 18.3V Outputs
  - Digital Cable Length Compensation (1V)
  - I²C and Pin controllable output
- Output Back Bias Capability of 28V
- I²C Compatible Interface for Remote Device Control
- Four level Slave Address 0001 00XX
- 2.5V, 3.3V, 5V Logic Compatible
- External Pins to Toggle Between V and H Polarization.
- Supports DiSEqC 2.0 Protocol
- Built-In Tone Oscillator Factory Trimmed to 22kHz
  - Facilitates DiSEqC (EUTELSAT) Encoding
  - External Modulation Input
- Internal Over-Temperature Protection and Diagnostics
- Internal OV, UV, Overload and Over-Temperature Flags (Visible on I²C)
- $\overline{FLT}$ Signal
- LNB Short-Circuit Protection and Diagnostics
- QFN, EPTSSOP Packages
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- LNB Power Supply and Control for Satellite Set-Top Box

Ordering Information

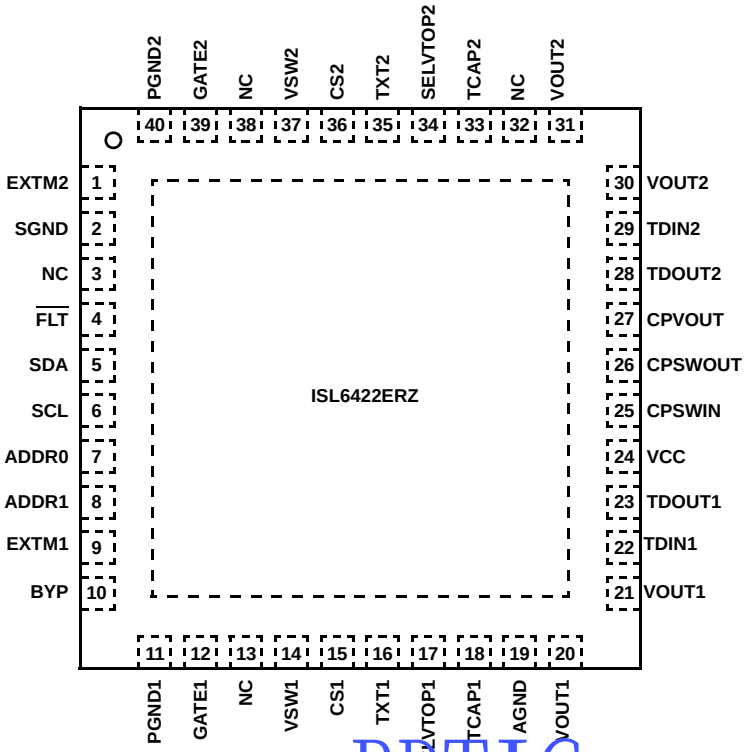
PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL6422ERZ*	ISL6422 ERZ	-20 to +85	40 Ld 6x6 QFN	L40.6x6
ISL6422EVEZ*	ISL6422 EVEZ	-20 to+ 85	38 Ld EPTSSOP	M38.173B

*Add “-T” suffix for tape and reel.

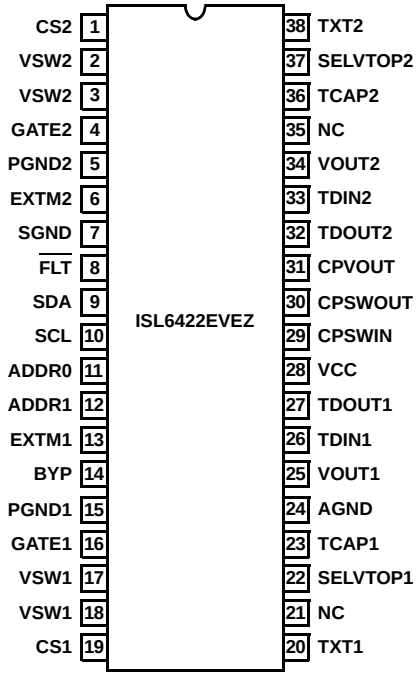
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinouts

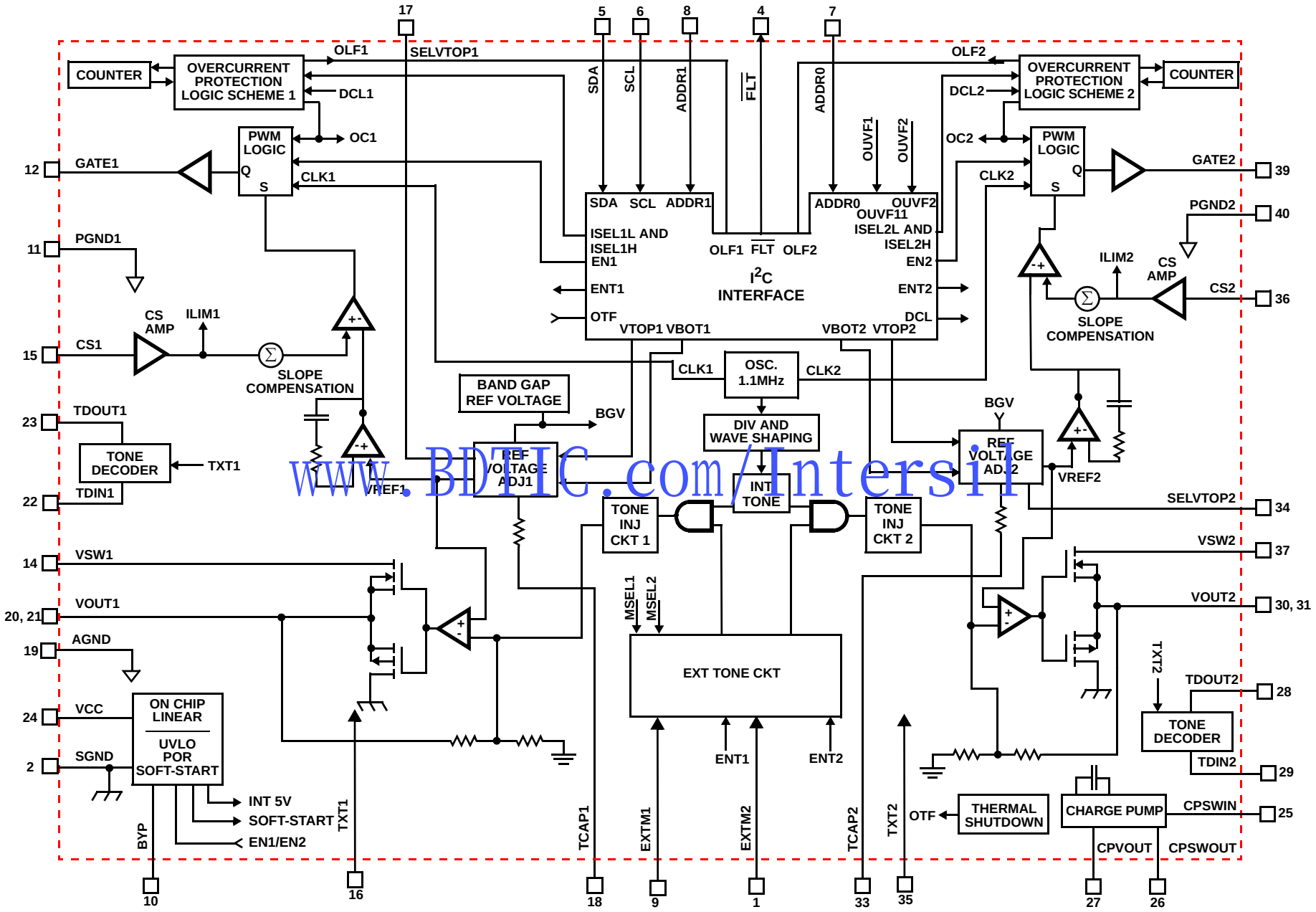
ISL6422
(40 LD QFN)
TOP VIEW



ISL6422
(38 LD EPTSSOP)
TOP VIEW



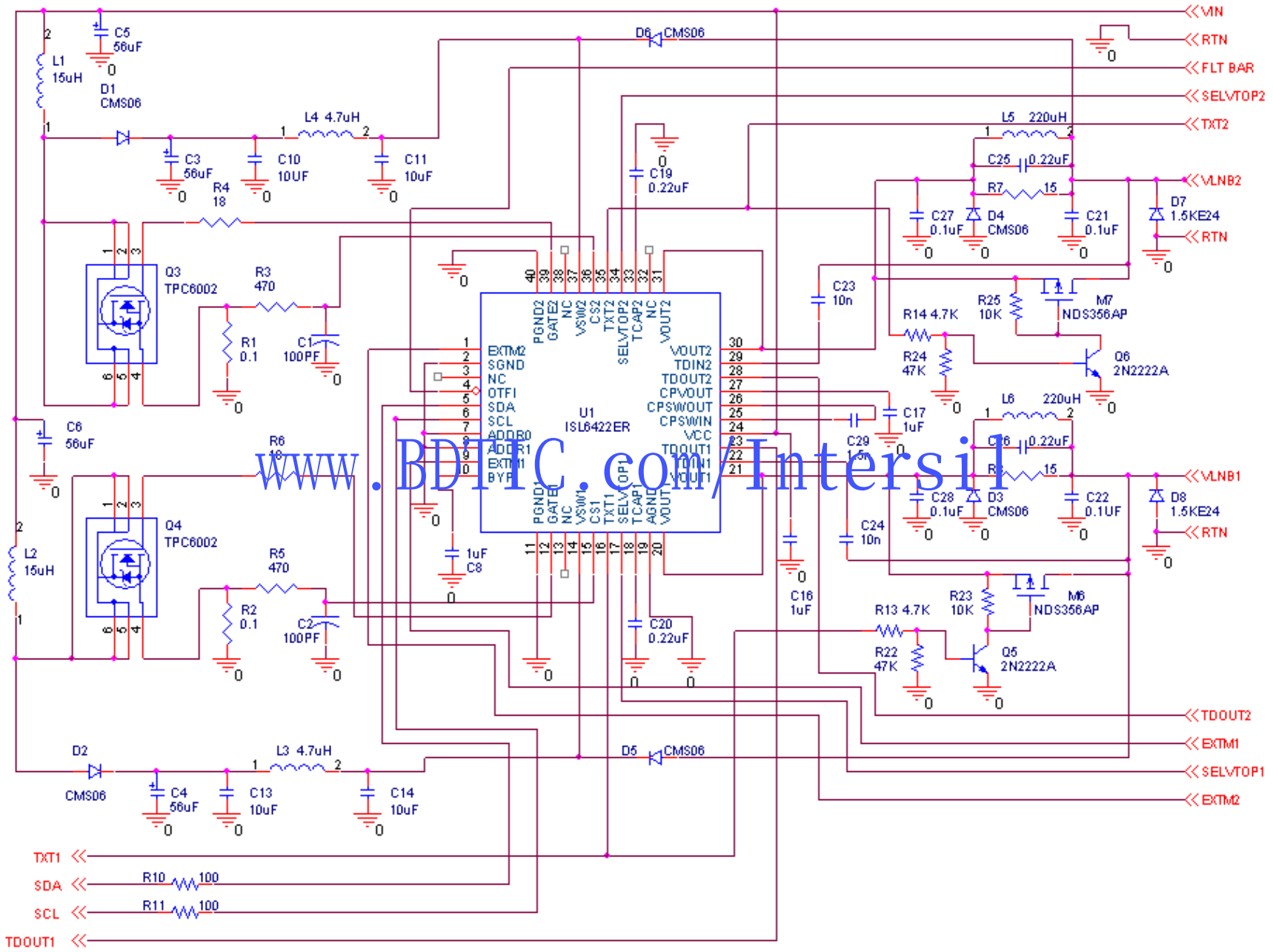
Block Diagram



NOTE:

1. Pinouts shown are for the QFN package.

Typical Application Schematic QFN



Absolute Maximum Ratings

Supply Voltage, V_{CC} . . . . . 8.0V to 18.0V
Logic Input Voltage Range
(SDA, SCL, ENT, DSQIN1 and DSQIN2,
SEL18V1 and SEL18V2) . . . . . -0.5V to 7V

Thermal Information

Thermal Resistance (Typical, Notes 2, 3)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
EPTSSOP Package	29	4
QFN Package.	34	6

Maximum Junction Temperature (Note 4) . . . . . +150°C
Maximum Storage Temperature Range. . . . . -40°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.aspOperating
Temperature Range. . . . . -20°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
3. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
4. The device junction temperature should be kept below +150°C. Thermal shut-down circuitry turns off the device if junction temperature exceeds +150°C typically.

Electrical Specifications

V_{CC} = 12V, T_A = -20°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. EN1 = EN2 = H, VTOP1 = VTOP2 = L, ENT1 = ENT2 = L, DCL = L, DSQIN1 = DSQIN2 = L, I_{OUT} = 12mA, unless otherwise noted. See “ISL6422 Software Description” on page 12 for I^2C access to the system.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage Range			8	12	14	V
Standby Supply Current		EN1 = EN2 = L		1.5	3.0	mA
Supply Current	I_{IN}	EN1 = EN2 = VTOP1 = VTOP2 = VBOT1 = VBOT2 = ENT1 = ENT2 = H, No Load		4.0	8.0	mA
UNDERVOLTAGE LOCKOUT						
Start Threshold			7.5		7.95	V
Stop Threshold			7.0		7.55	V
Start to Stop Hysteresis			350	400	500	mV
SOFT-START						
COMP Rise Time (Note 5)		(Note 5)		8196		Cycles
Output Voltage (Note 5)	V_{OUT1}	(Refer to Table 11)	13.04	13.3	13.56	V
	V_{OUT1}	(Refer to Table 11)	14.02	14.3	14.58	V
	V_{OUT1}	(Refer to Table 11)	17.94	18.3	18.66	V
	V_{OUT1}	(Refer to Table 11)	19.00	19.3	19.68	V
	V_{OUT2}	(Refer to Table 15)	13.04	13.3	13.56	V
	V_{OUT2}	(Refer to Table 15)	14.02	14.3	14.58	V
	V_{OUT2}	(Refer to Table 15)	17.94	18.3	18.66	V
	V_{OUT2}	(Refer to Table 15)	19.00	19.3	19.68	V
Line Regulation	DV_{OUT1}, DV_{OUT2}	V_{IN} = 8V to 14V; V_{OUT1}, V_{OUT2} = 13V		4.0	40.0	mV
		V_{IN} = 8V to 14V; V_{OUT1}, V_{OUT2} = 18V		4.0	60.0	mV
Load Regulation	DV_{OUT1}, DV_{OUT2}	I_O = 12mA to 350mA		50	80	mV
		I_O = 12mA to 750mA		100	200	mV

Electrical Specifications V_{CC} = 12V, T_A = -20°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. EN1 = EN2 = H, VTOP1 = VTOP2 = L, ENT1 = ENT2 = L, DCL = L, DSQIN1 = DSQIN2 = L, I_{OUT} = 12mA, unless otherwise noted. See "ISL6422 Software Description" on page 12 for I^2C access to the system. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Dynamic Output Current Limiting (Note 8)	I_{MAX}	DCL = 0, ISEL1H and ISEL2H = 0, ISEL1L and ISEL2L = 0, ISEL1R and ISEL2R = 0	270	305	345	mA
		DCL = 0, ISEL1H and ISEL2H = 0, ISEL1L and ISEL2L = 0, ISEL1R and ISEL2R = 1	350	388	422	mA
		DCL = 0, ISEL1H and ISEL2H = 0, ISEL1L and ISEL2L = 1, ISEL1R and ISEL2R = 1	515	570	630	mA
		DCL = 0, ISEL1H and ISEL2H = 1, ISEL1L and ISEL2L = 0, ISEL1R and ISEL2R = 1	635	705	775	mA
		DCL = 0, ISEL1H and ISEL2H = 1, ISEL1L and ISEL2L = 1, ISEL1R and ISEL2R = 1	800	890	980	mA
Dynamic Overload Protection Off Time	t_{OFF}	DCL = L, Output Shorted (Note 8)		900		ms
Dynamic Overload Protection On Time	t_{ON}			20		ms
Static Output Current Limiting	I_{MAX}	DCL = 1 (Note 8)		990		mA
Cable Fault CABF Asserted High	I_{CAB}	EN1 and EN2 = 1;	2	10	20	mA
TONE OSCILLATOR						
Tone Frequency	f_{tone}	ENT1 and ENT2 = H	20.0	22.0	24.0	kHz
Tone Amplitude	V_{tone}	ENT1 and ENT2 = H, I_{OUT} = 5mA	500	680	800	mV
Tone Duty Cycle	dc_{tone}	ENT1 and ENT2 = H	40	50	60	%
Tone Rise or Fall Time	t_r, t_f	ENT1 and ENT2 = H	5	10	14	µs
TONE DECODER						
Input Amplitude	Vtdin		200		1000	mV
Frequency Capture Range	Ftdin		17.5		26.5	kHz
Input Impedance	Z_{DET}			8.6		kΩ
Detector Output Voltage	V_{TDOUT_L}	Tone Present, I_{LOAD} = 3mA			0.4	V
Detector Output Leakage	I_{TDOUT_H}	Tone absent, V_O = 6V			10	µA
Tone Decoder Rx Threshold	V_{RXth}	TXT1 and TXT2 = L	100	150	200	mV
Tone Decoder Tx Threshold	V_{TXth}	TXT1 and TXT2 = H	400	450	500	mV
LINEAR REGULATOR						
Drop-out Voltage		I_{OUT} = 750mA		0.8	1.0	V
Output Backward Leakage Current	I_{OBK}	EN1 and EN2 = 0; V_{OBK} = 27V		2.0	3.0	mA
Output Backward Leakage Current	I_{OBK}	EN1 and EN2 = 0; V_{OBK} = 28V		15.0	17.0	mA
Output Backward Current Threshold	I_{OBKTH}	EN1 and EN2 = 1; V_{OFAULT} = 19V (Note 7)		125		mA
Output Backward Voltage	I_{OBK}	EN1 and EN2 = 0			27	V
Output Undervoltage (Asserted high during soft-start)		OUVF1, OUVF2 bit is asserted high, measured from the typ output set value	-6		2	%
Output Overvoltage (Asserted high during soft-start)		OUVF1, OUVF2 bit is asserted high, measured from the typ output set value	+2		+6	%

Electrical Specifications V_{CC} = 12V, T_A = -20°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. EN1 = EN2 = H, VTOP1 = VTOP2 = L, ENT1 = ENT2 = L, DCL = L, DSQIN1 = DSQIN2 = L, I_{OUT} = 12mA, unless otherwise noted. See "ISL6422 Software Description" on page 12 for I^2C access to the system. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TXT1 AND TXT2, EXTM1 AND EXTM2, SELVTOP1 AND SELVTOP2, ADDR0 AND ADDR1 INPUT PINs (Note 8)						
Asserted LOW					0.8	V
Asserted HIGH			1.7			V
Input Current				25		µA
CURRENT SENSE (CS pin)						
Input Bias Current	I_{BIAS}			700		nA
Overcurrent Threshold	V_{CS}	Static current mode, DCL = H	325	450	500	mV
ERROR AMPLIFIER						
Open Loop Voltage Gain	A_{OL}			88		dB
Gain Bandwidth Product	GBP			14		MHz
PWM						
Maximum Duty Cycle			90	93		%
Minimum Pulse Width				20		ns
OSCILLATOR						
Oscillator Frequency	f_o	Fixed at (20) (f_{tone})	396	440	484	kHz
Thermal Shutdown						
Temperature Shutdown Threshold				150		°C
Temperature Shutdown Hysteresis				20		°C
$\overline{FLT}$						
$\overline{FLT}$ (released)		V_O = 6V			10	µA
$\overline{FLT}$ (asserted)		I_{SINK} = 3.2mA (1.5k pull-up resistor to 5V)			0.4	V

NOTES:

5. Internal digital soft-start.
6. The EXTM1 and EXTM2, SELVTOP1 and SELVTOP2, TXT1 and TXT2, and ADDR0 and ADDR1 pins have 200k internal pull-downs.
7. On exceeding this dynamic back current limit threshold for a period of 100µs, the device enters the dynamic current limit mode, and the BCF I^2C bit is set. The dynamic back current limit duty during a BCF is ON = 100µs or OFF = 5ms.
8. In the dynamic back current limit mode, the output is ON for 20ms and OFF for 900ms, but remains continuously ON in the Static mode. When tone is ON, the minimum current limit is 50mA lower than the values indicated in the table. While in the dynamic mode of current limit, the trip level is momentarily increased to 990mA during the 20ms ON time to facilitate recovery from overload conditions.

Tone Waveform

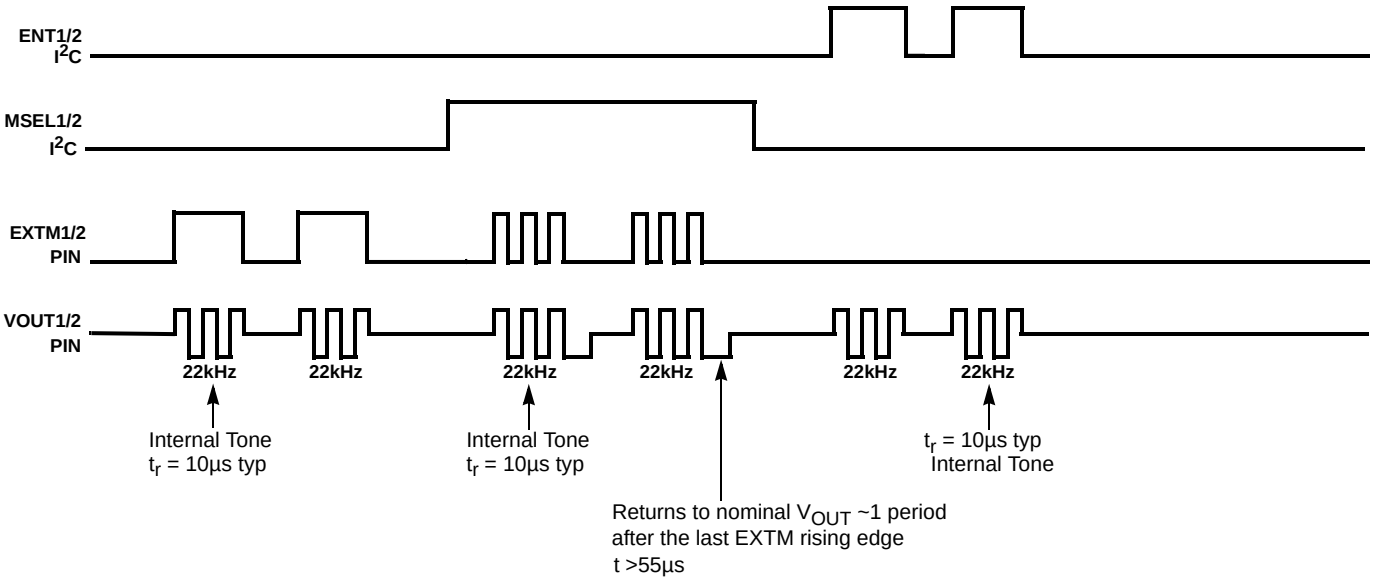


FIGURE 1. TONE WAVEFORM

NOTES:

9. The logic presented to the signal pins TXT1 and TXT2 changes the decoder threshold during tone Transmit and Receive. TTH1 and TTH2 allow threshold control through the I^2C provided that TXT1 and TXT2 = 0.
10. The tone rise and fall times are not shown due to resolution of graphics. It is 10µs typ for 22kHz.
11. The EXTM1 and EXTM2 pins have input thresholds of $V_{IL(max)}$ = 0.8V and $V_{IH(min)}$ = 1.7V

Typical Performance Curves

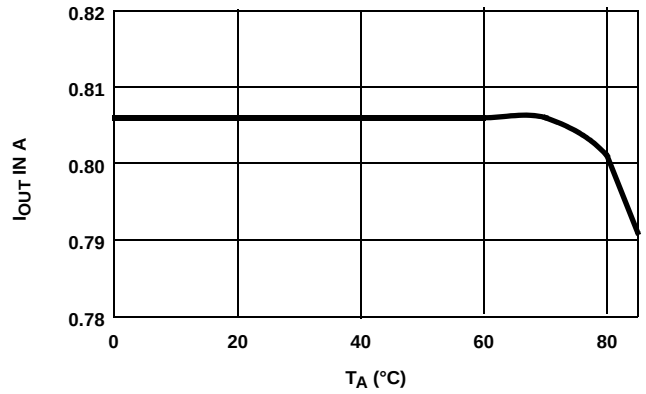


FIGURE 2. OUTPUT CURRENT DERATING 38 LD HTSSOP: I_{OUT}_max vs T_A

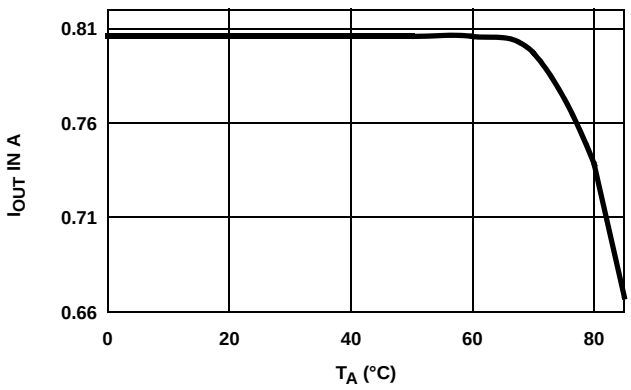


FIGURE 3. OUTPUT CURRENT DERATING 40 LD 6x6 QFN: I_{OUT}_max vs T_A

NOTE: With both channels in simultaneous operation at rated output.

Functional Pin Descriptions

SYMBOL	FUNCTION
SDA	Bidirectional data from/to I^2C bus.
SCL	Clock from I^2C bus.
VSW1 and VSW2	Input of the linear post-regulator.
PGND1 and PGND2	Dedicated ground for the output gate driver of respective PWM.
CS1 and CS2	Current sense input; connect the sense resistor Rsc at this pin for desired overcurrent value for respective PWM.
SGND	Small signal ground for the IC.
TCAP1 and TCAP2	Capacitor for setting rise and fall time of the output of LNB A and LNB B respectively. Typical value is 0.22µF.
BYP	Bypass capacitor for internal 5V.
TXT1 and TXT2	TXT1 and TXT2 are the Tone Transmit signal inputs used to change the tone decoder threshold. The threshold is 200mV max for the Rx mode when the TXT1 and TXT2 are set low. The threshold is 400mV min in the Tx mode when TXT1 and TXT2 are set high. If Tx/Rx mode is set by I^2C bit TTH(1 ,2), when TTH(1, 2) = 1, then TXT(1, 2) will be driven high (5V) by an on-chip driver.
VCC	Main power supply to the chip.
GATE1 and GATE2	These are the device outputs of PWM A and PWM B respectively. These high current driver outputs are capable of driving the gate of a power FET. These outputs are actively held low when V_{CC} is below the UVLO threshold.
VOUT1 and VOUT2	Output voltage for LNB A and LNB B respectively.
ADDR0 and ADDR1	Address pins select four different device addresses per Table 19.
EXTM1 and EXTM2	These pins can be used in two ways: 1. As an input for externally modulated DiSEqC tone signal that is transferred symmetrically onto V_{OUT}. 2. Alternatively apply a DiSEqC modulation envelope that modulates an internal tone and then transfers it symmetrically onto V_{OUT}.
$\overline{FLT}$	This is an open drain output from the controller. When the $\overline{FLT}$ goes low, it indicates that an Over-Temperature has occurred. The processor should then look at the I^2C register to get the actual cause of the error. A high on the $\overline{FLT}$ indicates that the device is functioning normally.
CPVOUT, CPSWIN, CPSWOUT	A 47nF charge pump cap is connected to CPVOUT. Connect a 1.5nF capacitor between CPSWIN and CPSWOUT.
SELVTOP1 and SELVTOP2	The following description applies to both pins and both bits. When this pin is low, the V_{OUT} is in the 13V/14V range selected by the I^2C bit VBOT1 and VBOT2. When this pin is high, the 18V/19V range is selected by the I^2C bit VTOP1 and VTOP2. The voltage select pin voltage VSPEN1 and VSPEN2 I^2C bit must be set low for the SELVTOP1 and SELVTOP2 pins to be active. Setting VSPEN1 and VSPEN2 high disables these pins and voltage selection will be done using the I^2C bits VBOT1 and VBOT2 and VTOP1 and VTOP2 only.
TDIN1 and TDIN2 TDOUT1 and TDOUT2	TDIN1 and TDIN2 are the tone decoder inputs for Channels 1 and 2. TDOUT1 and TDOUT2 are the tone detector outputs for Channels 1 and 2. TDOUT1 and TDOUT2 are open drain outputs.
AGND	Analog ground for the IC.

Functional Description

The ISL6422 dual output voltage regulator makes an ideal choice for advanced satellite set-top box and personal video recorder applications. Both supply and control voltage outputs for two low-noise blocks (LNBs) are available simultaneously in any output configuration. The device utilizes built-in DC/DC step up converters that, from a single supply source ranging from 8V to 14V, generate the voltages that enable the linear post-regulators to work with a minimum of dissipated power. An undervoltage lockout circuit disables the device when VCC drops below a fixed threshold (7.5V typical).

DiSEqC Encoding

The internal oscillator is factory-trimmed to provide a tone of 22kHz in accordance with DiSEqC (EUTELSAT) standards. No further adjustment is required. The tone oscillator can be controlled either by the I^2C interface (ENT1 or ENT2 bit) or by a dedicated pin (EXTM1 or EXTM2) that allows immediate DiSEqC data encoding separately for each LNB. All the functions of this IC are controlled via the I^2C bus by writing to the system registers. The same registers can be read back, and four bits will report the diagnostic status. The internal oscillator operates the converters at twenty times the 22k tone frequency. The device offers full I^2C compatibility and supports 2.5V, 3.3V or 5V logic, and up to 400kHz operation.

If the Tone Enable bits (ENT1 and ENT2) are set LOW and the MSEL1 and MSEL2 bits set LOW through I^2C, then the EXTM1 and EXTM2 terminal activates the internal tone signal, modulating the DC output with a $680mV_{P-P}$ typ symmetrical tone waveform. The presence of this signal usually provides the LNB with information about the band to be received.

Burst coding of the tone can be accomplished due to the fast response of the EXTM1 and EXTM2 input and rapid tone response. This allows implementation of the DiSEqC (EUTELSAT) protocols.

When the ENT1 or ENT2 bit is set HIGH, a continuous 22kHz tone is generated regardless of the EXTM1 and EXTM2 pin logic status for the corresponding regulator channel (LNB-A or LNB-B). The ENT1 or ENT2 bit must be set LOW when the EXTM1 and/or EXTM2 pin is used for DiSEqC encoding.

The EXTM1 and EXTM2 pins also accept an externally modulated tone command when the MSEL1 or MSEL2 I^2C bit is set high.

DiSEqC Decoder

TDIN1 and TDIN2 are the inputs to the tone decoders of Channels 1 and 2 respectively. They accept the tone signal derived from the V_{OUT} through the 10nF decoupling capacitor. The detector threshold can be set to 200mV maximum in the Receive mode and to 400mV minimum in the Transmit mode by means of the logic presented to the TXT1 or TXT2 pin. If tone is detected, the open drain pin TDOUT1 or TDOUT2 is asserted low. This also enables the tone diagnostics to be performed, apart from the normal tone detection function.

Linear Regulator

The output linear regulator will sink and source current. This feature allows full modulation capability into capacitive loads as high as 0.75µF. In order to minimize the power dissipation, the output voltage of the internal step-up converter is adjusted to allow the linear regulator to work at minimum dropout.

When the device is put in the shutdown mode (EN1 and EN2 = LOW), both PWM power blocks are disabled (that is, when EN1 = 0, PWM1 is disabled, and when EN2 = 0, PWM2 is disabled).

When the regulator blocks are active (EN1 and EN2 = HIGH, and VSPEN1 and VSPEN2 = LOW), the output can be controlled via I^2C logic to be between 13V and 14V or between 18V and 19V (typical) by means of the Voltage Select bits (VTOP1, VTOP2, VBOT1, and VBOT2) for remote controlling of non-DiSEqC LNBs.

When the regulator blocks are active (EN1 and EN2 = HIGH, and VSPEN1 and VSPEN2 = HIGH), the VBOT1 and VBOT2 bits and the SELVTOP1 and SELVTOP2 pins will control the output between 13V and 14V and the VTOP1 and VTOP2 and the SELVTOP1 and SELVTOP2 pins will control the output between 18V and 19V.

Output Timing

The output voltage rise and fall times can be set by an the external capacitor on the TCAP1 and TCAP2 pins. The output rise and fall times is given by Equation 1:

$$C = \frac{(270)t}{\Delta V} \quad \text{(EQ. 1)}$$

where:

- C is the TCAP value in nF
- t is the required slew rate in ms, and
- ΔV is the differential transition voltage from low output voltage range to the high output range in Volts.

Rise and fall time will typically be the same.

The maximum recommended value for TCAP1 and TCAP2 would be the base on the maximum transition time allowed in the system application. Too small a value of TCAP1 and TCAP2 can cause high peak currents in the boost circuit. For example, a 10V/ms slew on a 80µF VSW capacitor with an inductor of 15µH can cause a peak inductor current of approximately 2.3A.

Current Limiting

The dynamic back current limit block has five thresholds that can be selected by the following bits of the SR.

- ISEL1H and ISEL2H
- ISEL1L and ISEL2L
- ISEL1R and ISEL2R

See Table 8 and Table 9 for threshold selection using these bits. The DCL1 and DCL2 bits have to be set to low for this mode of operation. In this mode, the overcurrent protection circuit works dynamically 23µs after an overload is detected, and the output is shutdown for a time t_{OFF}, typically 900ms. Simultaneously, the OLF1 or OLF2 bit of the System Register is set to HIGH. After this time has elapsed, the output is resumed for a time t_{ON} = 20ms. During t_{ON}, the device output will be current limited to a 990mA typ level. If the overload is still detected, the protection circuit will cycle again through t_{OFF} and t_{ON}. At the end of a full t_{ON}, in which no overload is detected, normal operation is resumed and the OLF1 or OLF2 bit is reset to LOW. Typical t_{ON} + t_{OFF} time is 920ms as determined by an internal timer. This dynamic operation can greatly reduce the power dissipation in a short circuit condition, still ensuring excellent power-on start-up in most conditions.

However, there could be some cases in which a highly capacitive load on the output may cause a difficult start-up when the dynamic protection is chosen. This can be solved by initiating any power start-up in static mode (DCL = HIGH) and then switching to the dynamic mode (DCL = LOW) after a chosen amount of time. When in static mode, the OLF1 or OLF2 bit goes HIGH when the peak current sense threshold is reached and returns LOW when the overload condition is cleared. The OLF1, OLF2, BCF1, and BCF2 bits will be LOW at the end of initial power-on soft-start. In the static mode the output current through the linears is limited to 990mA typ.

When a 19.3V line is connected onto a VOUT1 or VOUT2 pin that has been set to 13.3V, the linear will then enter a dynamic back current limit state. When a dynamic back current limit of greater that 125mA typ is sensed at the lower FET of the linear for a period greater that 100µs, the output is disabled for a period of 5ms and the BCF1 and BCF2 bits are set. If the 19.3V remains connected, the output will cycle through the ON = 100µs/OFF = 5ms. The output will recover when the fault is removed.

Thermal Protection

This IC is protected against overheating. When the junction temperature exceeds +150°C (typical), the step-up converter and the linear regulator are shut off and the OTF bit of the SR is set HIGH. Normal operation is resumed and the OTF bit is reset LOW when the junction is cooled down to +130°C (typical).

The $\overline{FLT}$ pin serves as an interrupt for the processor when an over temperature, overcurrent or backwards overcurrent fault is detected by the LNB controller or when both channels are disabled by the I^2C EN1 and EN2 bits being set low. Should the I^2C lose power (for example by shorting BYP pin to ground), it is designed to power up with all control bits set to 0 (particularly the EN1 and EN2 bits). This prevents the device from coming back up in a state not desired by the host controller. If the host controller sees a $\overline{FLT}$ low, it should read the I^2C bits and find both EN1 and EN2 bits low. When it desires one or both to be high, it should re-write the I^2C to the desired state.

External Output Voltage Selection

The output voltage can be selected by the I^2C bus. Additionally, the package offers two pins (SELVTOP1 and SELVTOP2) for independent 13 through 19V output voltage selection.

TABLE 1.

VSPEN1, VSPEN2	VTOP1, VTOP2	VBOT1, VBOT2	SELVTOP1, SELVTOP2	VOUT1, VOUT12
0	X	0	0	13.3V
0	X	1	0	14.3V
0	0	X	1	18.3V
0	1	X	1	19.3V
1	0	0	X	13.3V
1	0	1	X	14.3V
1	1	0	X	18.3V
1	1	1	X	19.3V

I^2C Bus Interface for ISL6422

(Refer to Phillips I^2C Specification, Rev. 2.1)

Data transmission from the main microprocessor to the ISL6422 and vice versa takes place through the two-wire I^2C bus interface, consisting of the two lines SDA and SCL. Both SDA and SCL are bidirectional lines. They are connected to a positive supply voltage via a pull-up resistor. (Pull-up resistors to positive supply voltage must be externally connected). When the bus is free, both lines are HIGH. The output stages of ISL6422 will have an open drain/open collector in order to perform the wired-AND function. Data on the I^2C bus can be transferred up to 100kbps in the standard mode or up to 400kbps in the fast mode. The level of logic “0” and logic “1” depends on the value of V_{DD} as per the “Electrical Specifications” table on page 5. One clock pulse is generated for each data bit transferred.

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can change only when the clock signal on the SCL line is LOW. Refer to Figure 4.

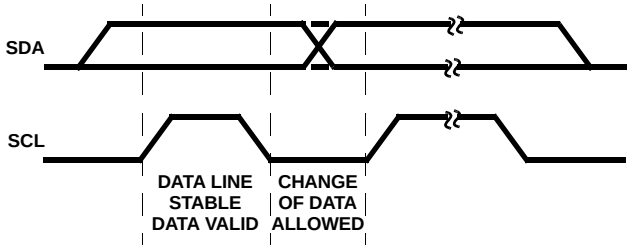


FIGURE 4. DATA VALIDITY

START and STOP Conditions

As shown in Figure 5, the START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH.

The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

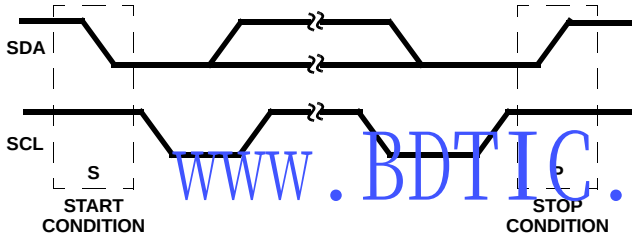


FIGURE 5. START AND STOP WAVEFORMS

Byte Format

Every byte put on the SDA line must be eight bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit first (MSB).

Acknowledge

The master (microprocessor) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see Figure 6). The peripheral that acknowledges has to pull down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse. (Set-up and hold times must also be taken into account).

The peripheral which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case, the master transmitter can generate the STOP information in order to abort the transfer.

The ISL6422 will not generate the acknowledge if the POWER OK signal from the UVLO is LOW.

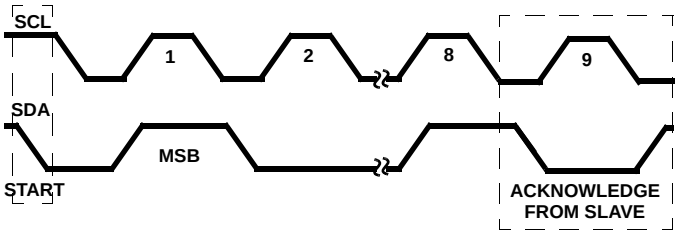


FIGURE 6. ACKNOWLEDGE ON THE I^2C BUS

Transmission Without Acknowledge

Avoiding detection of the acknowledgement, the microprocessor can use a simpler transmission; it waits one clock pulse without checking the slave acknowledging and sends the new data. Although, this approach is less protected from error and decreases the noise immunity.

ISL6422 Software Description

Interface Protocol

The interface protocol is comprised of the following, as shown in Table 2:

- Start condition (S)
- Chip address byte (MSB on left; the LSB bit determines read (1) or write (0) transmission) (the assigned I^2C slave address for the ISL6422 is 0001 00XX)
- Sequence of data (1 byte + Acknowledge)
- Stop condition (P)

TABLE 2. INTERFACE PROTOCOL

S	0	0	0	1	0	0	0	R/W	ACK	Data (8 bits)	ACK	P

System Register Format

- R, W = Read and Write bit
- R = Read-only bit
- X = Unused

All bits reset to 0 at Power-On

TABLE 3. STATUS REGISTER 1 (SR1)

R, W	R, W	R, W	R	R	R	R	R
SR1H	SR1M	SR1L	OTF	CABF1	OUVF1	OLF1	BCF1

TABLE 4. TONE REGISTER 2 (SR2)

R, W	R, W	R, W	R, W	R, W	R, W	R, W	R, W
SR2H	SR2M	SR2L	ENT1	MSEL1	TTH1	X	X

TABLE 5. COMMAND REGISTER 3 (SR3)

R, W	R, W	R, W	R, W	R, W	R, W	R, W	R, W
SR3H	SR3M	SR3L	DCL1	VSPEN1	ISEL1R X	ISEL1H	ISEL1L

TABLE 6. CONTROL REGISTER 4 (SR4)

R, W	R, W	R, W	R, W	R, W	R, W	R, W	R, W
SR4H	SR4M	SR4L	EN1	X	X	VTOP1	VBOT1

TABLE 7. STATUS REGISTER 5 (SR5)

R, W	R, W	R, W	X	R	R	R	R
SR5H	SR5M	SR5L	X	CABF2	OUVF2	OLF2	BCF2

TABLE 8. TONE REGISTER 6 (SR6)

R, W	R, W	R, W	R, W	R, W	R, W	R, W	R, W
SR6H	SR6M	SR6L	ENT2	MSEL2	TTH2	X	X

TABLE 9. COMMAND REGISTER 7 (SR7)

R, W	R, W	R, W	R, W	R, W	R, W	R, W	R, W
SR7H	SR7M	SR7L	DCL2	VSPEN2	ISEL2R	ISEL2H	ISEL2L

TABLE 10. CONTROL REGISTER 8 (SR8)

R, W	R, W	R, W	R, W	R, W	R, W	R, W	R, W
SR8H	SR8M	SR8L	EN2	X	X	VTOP2	VBOT2

Transmitted Data (I^2C bus WRITE mode)

When the R/W bit in the chip is set to 0, the main microprocessor can write on the system registers (SR1 through SR8) of the ISL6422 via I^2C bus. These will be written by the microprocessor as shown in the following. The spare bits of registers can be used for other functions.

TABLE 11. STATUS REGISTER SR1 CONFIGURATION

SR1H	SR1M	SR1L	OTF	CABF1	OUVF1	OLF1	BCF1	FUNCTION
0	0	0	X	X	X	X	X	SR1 is selected
0	0	0	X	X	X	0	X	I_{OUT} ≤set limit, Normal Operation
0	0	0	X	X	X	1	X	I_{OUT} >Static/Dynamic Limiting Mode/Power blocks disabled
0	0	0	X	X	X	X	0	I_{OBCK} ≤set limit, Normal Operation
0	0	0	X	X	X	X	1	I_{OBCK} >Dynamic Limiting Mode/Power blocks disabled
0	0	0	X	X	0	X	X	V_{IN}/V_{OUT} within specified range
0	0	0	X	X	1	X	X	V_{IN}/V_{OUT} is not within specified range
0	0	0	X	0	X	X	X	Cable is connected, I_{OUT} is >20mA
0	0	0	X	1	X	X	X	Cable is open, I_{OUT} <2mA
0	0	0	0	X	X	X	X	T_J ≤+130°C, Normal operation
0	0	0	1	X	X	X	X	T_J >+150°C, Power blocks disabled

NOTE: X indicates “Read Only” and is a “Don’t Care” for the Write mode.

TABLE 12. TONE REGISTER SR2 CONFIGURATION

SR2H	SR2M	SR2L	ENT1	MSEL1	TTH1	X	X	FUNCTION
0	0	1	X	X	X	X	X	SR2 is selected
0	0	1	0	0	X	X	X	Internal Tone = 22kHz, modulated by EXTM1, t_r, t_f = 10µs typ
0	0	1	0	1	X	X	X	Ext 22k modulated input, t_r, t_f = 10µs typ
0	0	1	1	0	X	X	X	Internal Tone = 22kHz, modulated by the ENT1 bit, t_r, t_f = 10µs typ
0	0	1	X	X	0	X	X	TXT = 0; Decoder Rx threshold is set at 200mV max
0	0	1	X	X	1	X	X	TXT = 0; Decoder Tx threshold is set at 400mV min

NOTE: X is a “Don’t Care” for the Write mode.

TABLE 13. COMMAND REGISTER SR3 CONFIGURATION

SR3H	SR3M	SR3L	DCL1	VSPEN1	ISEL1R	ISEL1H	ISEL1L	FUNCTION
0	1	0	X	X	X	X	X	SR3 is selected
0	1	0	0	X	0	X	X	I_{OUT1} = 275mA maximum
0	1	0	0	X	1	0	0	I_{OUT1} = 350mA maximum
0	1	0	0	X	1	0	1	I_{OUT1} = 515mA maximum
0	1	0	0	X	1	1	0	I_{OUT1} = 635mA maximum
0	1	0	0	X	1	1	1	I_{OUT1} = 800mA maximum
0	1	0	1	X	X	X	X	Dynamic current limit NOT selected
0	1	0	0	X	X	X		Dynamic current limit selected
0	1	0	X	0	X	X	X	SELVTOP H/W pin Enabled
0	1	0	X	1	X	X	X	SELVTOP H/W pin Disabled

NOTE: X is a “Don’t Care” for the Write mode.

TABLE 14. CONTROL REGISTER SR4 CONFIGURATION

SR4H	SR4M	SR4L	EN1	X	X	VTOP1	VBOT1	FUNCTION
0	1	1	1	X	X	0	0	SR4 is selected
0	1	1	1	X	X	0	0	VSPEN1 = SELVTOP1 = 0, V_{OUT1} = 13V, V_{BOOST1} = 13V + V_{DROP}
0	1	1	1	X	X	0	1	VSPEN1 = SELVTOP1 = 0, V_{OUT1} = 14V, V_{BOOST1} = 14V + V_{DROP}
0	1	1	1	X	X	1	0	VSPEN1 = SELVTOP1 = 0, V_{OUT1} = 13V, V_{BOOST1} = 13V + V_{DROP}
0	1	1	1	X	X	1	1	VSPEN1 = SELVTOP1 = 0, V_{OUT1} = 14V, V_{BOOST1} = 14V + V_{DROP}
0	1	1	1	X	X	0	0	VSPEN1 = 0, SELVTOP1 = 1, V_{OUT1} = 18V, V_{BOOST1} = 18V + V_{DROP}
0	1	1	1	X	X	0	1	VSPEN1 = 0, SELVTOP1 = 1, V_{OUT1} = 18V, V_{BOOST1} = 18V + V_{DROP}
0	1	1	1	X	X	1	0	VSPEN1 = 0, SELVTOP1 = 1, V_{OUT1} = 19V, V_{BOOST1} = 19V + V_{DROP}
0	1	1	1	X	X	1	1	VSPEN1 = 0, SELVTOP1 = 1, V_{OUT1} = 19V, V_{BOOST1} = 19V + V_{DROP}
0	1	1	1	X	X	0	0	VSPEN1 = 1, SELVTOP1 = X, V_{OUT1} = 13V, V_{BOOST1} = 13V + V_{DROP}
0	1	1	1	X	X	0	1	VSPEN1 = 1, SELVTOP1 = X, V_{OUT1} = 14V, V_{BOOST1} = 14V + V_{DROP}
0	1	1	1	X	X	1	0	VSPEN1 = 1, SELVTOP1 = X, V_{OUT1} = 18V, V_{BOOST1} = 18V + V_{DROP}
0	1	1	1	X	X	1	1	VSPEN1 = 1, SELVTOP1 = X, V_{OUT1} = 19V, V_{BOOST1} = 19V + V_{DROP}
0	1	1	0	X	X	X	X	PWM and Linear for Channel 1 disabled

NOTE: X is a “Don’t Care” for the Write mode.

TABLE 15. STATUS REGISTER SR5 CONFIGURATION

SR5H	SR5M	SR5L		CABF2	OUVF2	OLF2	BCF2	FUNCTION
1	0	0	X	X	X	X	X	SR5 is selected
1	0	0	X	X	X	0	X	I_{OUT} ≤ set limit, Normal Operation
1	0	0	X	X	X	1	X	I_{OUT} > Static/Dynamic Limiting Mode/Power blocks disabled
1	0	0	X	X	X	X	0	I_{OBCK} ≤ set limit, Normal Operation
1	0	0	X	X	X	X	1	I_{OBCK} > Dynamic Limiting Mode/Power blocks disabled
1	0	0	X	X	0	X	X	V_{IN}/V_{OUT} within specified range
1	0	0	X	X	1	X	X	V_{IN}/V_{OUT} is not within specified range
1	0	0	X	0	X	X	X	Cable is connected, I_{OUT} is >20mA
1	0	0	X	1	X	X	X	Cable is open, I_{OUT} <2mA

NOTE: X indicates “Read Only” state.

TABLE 16. TONE REGISTER SR6 CONFIGURATION

SR6H	SR6M	SR6L	ENT2	MSEL2	TTH2	X	X	FUNCTION
1	0	1	X	X	X	X	X	SR2 is selected
1	0	1	0	0	X	X	X	Int Tone = 22kHz, modulated by EXTM2, T_r, T_f = 10µs typ
1	0	1	0	1	X	X	X	Ext 22k modulated input, T_r, T_f = 10µs typ
1	0	1	1	0	X	X	X	Int Tone = 22kHz, modulated by ENT2 bit, T_r, T_f = 10µs typ
1	0	1	X	X	0	X	X	TXT2 = 0; Decoder Rx threshold is set at 200mV max
1	0	1	X	X	1	X	X	TXT2 = 0; Decoder Tx threshold is set at 400mV min

NOTE: X is a “Don’t Care” for the Write mode.

TABLE 17. COMMAND REGISTER SR7 CONFIGURATION

SR7H	SR7M	SR7L	DCL2	VSPEN2	ISEL2R	ISEL2H	ISEL2L	FUNCTION
1	1	0	X	X	X	X	X	SR7 is selected
1	1	0	0	X	0	X	X	$I_{OUT}1$ = 275mA max.
1	1	0	0	X	1	0	0	$I_{OUT}1$ = 350mA max.
1	1	0	0	X	1	0	1	$I_{OUT}1$ = 515mA max.
1	1	0	0	X	1	1	0	$I_{OUT}1$ = 635mA max.
1	1	0	0	X	1	1	1	$I_{OUT}1$ = 800mA max.
1	1	0	1	X	X	X	X	Dynamic current limit NOT selected
1	1	0	0	X	X	X	X	Dynamic current limit selected
1	1	0	X	0	X	X	X	SELVTOP H/W pin Enabled
1	1	0	X	1	X	X	X	SELVTOP H/W pin Disabled

NOTE: X is a “Don’t Care” for the Write mode.

TABLE 18. CONTROL REGISTER SR8 CONFIGURATION

SR8H	SR8M	SR8L	EN2	X	X	VTOP2	VBOT2	FUNCTION
1	1	1	1	X	X	0	0	SR4 is selected
1	1	1	1	X	X	0	0	VSPEN2 = SELVTOP2 = 0, V_{OUT1} = 13V, V_{BOOST1} = 13V + V_{DROP}
1	1	1	1	X	X	0	1	VSPEN2 = SELVTOP2 = 0, V_{OUT1} = 14V, V_{BOOST1} = 14V + V_{DROP}
1	1	1	1	X	X	1	0	VSPEN2 = SELVTOP2 = 0, V_{OUT1} = 13V, V_{BOOST1} = 13V + V_{DROP}
1	1	1	1	X	X	1	1	VSPEN2 = SELVTOP2 = 0, V_{OUT1} = 14V, V_{BOOST1} = 14V + V_{DROP}
1	1	1	1	X	X	0	0	VSPEN2 = 0,SELVTOP2 = 1, V_{OUT1} = 18V, V_{BOOST1} = 18V + V_{DROP}
1	1	1	1	X	X	0	1	VSPEN2 = 0, SELVTOP2 = 1, V_{OUT1} = 18V, V_{BOOST1} = 18V + V_{DROP}
1	1	1	1	X	X	1	0	VSPEN2 = 0, SELVTOP2 = 1, V_{OUT1} = 19V, V_{BOOST1} = 19V + V_{DROP}
1	1	1	1	X	X	1	1	VSPEN2 = 0, SELVTOP2 = 1, V_{OUT1} = 19V, V_{BOOST1} = 19V + V_{DROP}
1	1	1	1	X	X	0	0	VSPEN2 = 1, SELVTOP2 = X, V_{OUT1} = 13V, V_{BOOST1} = 13V + V_{DROP}
1	1	1	1	X	X	0	1	VSPEN2 = 1, SELVTOP2 = X, V_{OUT1} = 14V, V_{BOOST1} = 14V + V_{DROP}
1	1	1	1	X	X	1	0	VSPEN2 = 1, SELVTOP2 = X, V_{OUT1} = 18V, V_{BOOST1} = 18V + V_{DROP}
1	1	1	1	X	X	1	1	VSPEN2 = 1, SELVTOP2 = X, V_{OUT1} = 19V, V_{BOOST1} = 19V + V_{DROP}
1	1	1	0	X	X	X	X	PWM and Linear for channel 1 disabled

NOTE: X is a “Don’t Care” for the Write mode.

Received Data (I²C bus READ MODE)

The ISL6422 can provide to the master a copy of the system register information via the I²C bus in read mode. The read mode is master-activated by sending the chip address with the R/W bit set to 1. At the following master-generated clock bits, the ISL6422 issues a byte on the SDA data bus line (MSB transmitted first).

At the ninth clock bit, the MCU master can:

- Acknowledge the reception, thus starting the transmission of another byte from the ISL6422.
- Not acknowledge, thus stopping the read mode communication.

While the whole register is read back by the microprocessor, the following read-only bits convey diagnostic information about the ISL6422.

- OUC1 and OUC2 (Over or Undercurrent bits)
- UV1 and UV2 (Over or Undervoltage bits)
- TPR1 and TPR2 (Tone present bits)
- OTF (Over-temperature fault bit).

Power–On I²C Interface Reset

The I²C interface built into the ISL6422 is automatically reset at power-on. The I²C interface block will receive a Power OK logic signal from the UVLO circuit. This signal will go HIGH when chip power is OK. As long as this signal is LOW, the interface will not respond to any I²C commands and the system register SR1 and SR2 are initialized to all zeros, thus keeping the power blocks disabled. Once the V_{CC} rises above UVLO, the POWER OK signal given to the I²C interface block will be HIGH, the I²C interface becomes operative and the SRs can be configured by the main microprocessor. About 400mV of hysteresis is provided in the UVLO threshold to avoid false triggering of the power-on reset circuit. (I²C comes up with EN = 0; EN goes HIGH at the same time as (or later than) all other I²C data for that PWM becomes valid).

ADDR0 and ADDR1 Pins

Connecting either ADDR0 or ADDR1 to GND, the chip I^2C interface address is 0001000, but it is possible to choose between four different addresses simply by setting the logic as indicated in Table 19.

TABLE 19. ADDRESS PIN CHARACTERISTICS

V_{ADDR}	ADDR1	ADDR0
V_{ADDR}-1 “0001000”	0	0
V_{ADDR}-2 “0001001”	0	1
V_{ADDR}-3 “0001010”	1	0
V_{ADDR}-4 “0001011”	1	1

I^2C Electrical Characteristics

TABLE 20. I^2C SPECIFICATIONS

PARAMETER	TEST CONDITION	MIN	TYP	MAX
Input Logic High, VIH	SDA, SCL	2.0V		
Input Logic Low, VIL	SDA, SCL			0.8V
Input Logic Current, IIL	SDA, SCL; 0.4V < V_{DD} < 3.3V			10µA
Input Hysterisis	SDA, SCL	165mV	200mV	235mV
SCL Clock Frequency		0	100kHz	400kHz

I^2C Bit Description

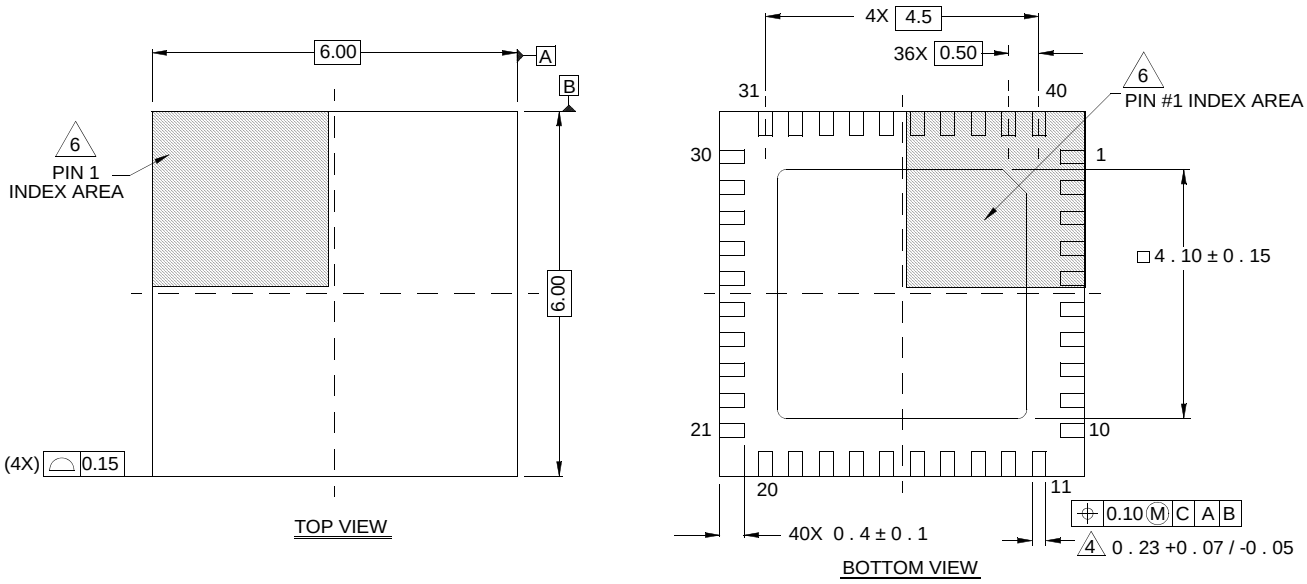
TABLE 21.

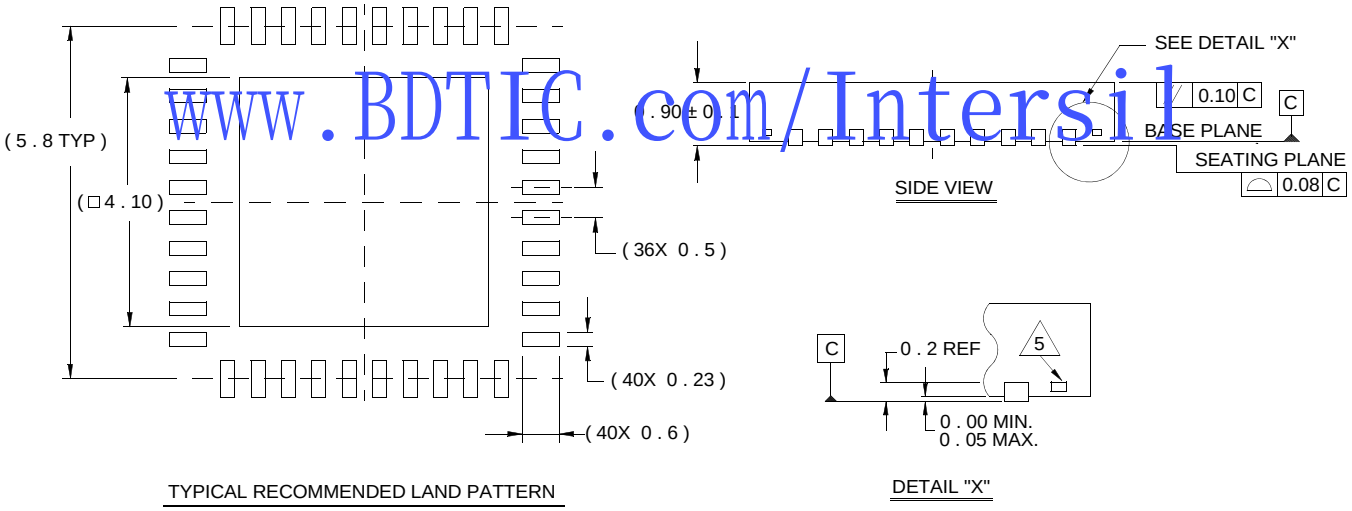
BIT NAME	DESCRIPTION
EN1 and EN2	ENable Output for Channels 1 and 2
VTOP1 and VTOP2	Voltage TOP Select (that is, 18V/19V for Channels 1 and 2)
VBOT1 and VTOP2	Voltage BOTtom Select (that is, 13V/14V for Channels 1 and 2)
ENT1 and ENT2	ENable Tone for Channels 1 and 2
MSEL1 and MSEL2	Modulation SELect for Channels 1 and 2
TFR1 and TFR2	Tone Frequency and Rise time select for Channels 1 and 2
DCL1 and DCL2	Dynamic Current Limit select for Channels 1 and 2
VSPEN1 and VSPEN2	Voltage Select Pin ENable for Channels 1 and 2
ISEL1H and ISEL2H, ISEL1L and ISEL2L, ISEL1R and ISEL2R	Current limit “I” SELect high and low bits for Channels 1 and 2
OTF	Over-Temperature Fault bit
CABF1, CABF2	CABle Fault or open status bit for Channels 1 and 2
OUVF1, OUVF2	Over and Undervoltage Fault status bit for Channels 1 and 2
OLF1, OLF2	Over Load Fault status bit for Channels 1 and 2
BCF1, BCF2	Backward Current Fault Bit for Channels 1 and 2
TTH1, TTH2	Tone THreshold is the OR of the signal pin TXT1 or TXT2

Package Outline Drawing

L40.6x6

40 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 3, 10/06

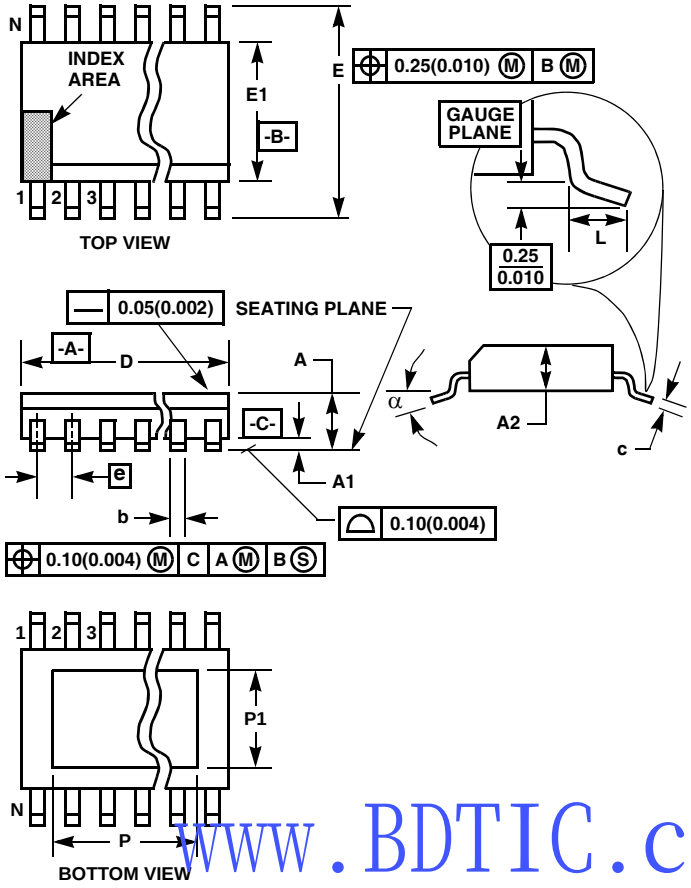




NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

Thin Shrink Small Outline Exposed Pad Plastic Packages (EPTSSOP)



M38.173B

38 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.051	0.80	1.05	-
b	0.0075	0.0106	0.17	0.27	9
c	0.0035	0.0079	0.09	0.20	-
D	0.378	0.386	9.60	9.80	3
E1	0.169	0.177	4.30	4.50	4
e	0.0197 BSC		0.500 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	38		38		7
α	0^o	8^o	0^o	8^o	-
P	-	0.256	-	6.5	11
P1	-	0.126	-	3.2	11

Rev. 0 9/06

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-BD-1, Issue F.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)
11. Dimensions "P" and "P1" are thermal and/or electrical enhanced variations. Values shown are maximum size of exposed pad within lead count and body size.