Data Sheet | July 2004 | FN9026.2

Dual Output LNB Supply and Control Voltage Regulator with I²C Interface for Advanced Satellite Set-Top Box Designs

The ISL6405 is a highly integrated voltage regulator and interface IC, specifically designed for supplying power and control signals from advanced satellite set-top box (STB) modules to the low noise blocks (LNBs) of two antenna ports. The device is comprised of two independent current-mode boost PWMs and two low-noise linear regulators along with the circuitry required for 22kHz tone generation, modulation and I²C device interface. The device makes the total LNB supply design simple, efficient and compact with low external component count.

Two independent current-mode boost converters provide the linear regulators with input voltages that are set to the final output voltages, plus typically 1.2V to insure minimum power dissipation across each linear regulator. This maintains constant voltage drops across each linear pass element while permitting adequate voltage range for tone injection.

The final regulated output voltages are available at two output terminals to support simultaneous operation of two antenna ports for dual tuners. The outputs for each PWM are set to 13V or 18V by independent voltage select commands (VSEL1, VSEL2) through the I²C bus. Additionally, to compensate for the voltage drop in the coaxial cable, the selected voltage may be increased by 1V with the line length compensation (LLC) feature. All the functions on this IC are controlled via the I²C bus by writing 8 bits on System Register (SR, 8 bits). The same register can be read back, and two bits will report the diagnostic status. Separate enable commands sent on the I²C bus provide independent standby mode control for each PWM and linear combination, disabling the output into shutdown mode.

Each output channel is capable of providing 750mA of continuous current. The overcurrent limit can be digitally programmed. The SEL18V pin with QFN package allows the 13V to 18V transition with an external pin, over-riding the I²C input.

Features

- Single Chip Power solution
  - True Dual Operation for 2-Tuner/2-Dish Applications
  - Both Outputs May be Enabled Simultaneously at Maximum Power
  - Integrated DC-DC Converter and I²C Interface
- Switch-Mode Power Converter for Lowest Dissipation
  - Boost PWMs with > 92% Efficiency
  - Selectable 13V or 18V Outputs
  - Digital Cable Length Compensation (1V)
- I²C Compatible Interface for Remote Device Control
  - Registered Slave Address 0001 00XX
  - Full 3.3V/5V Operation up to 400kHz
- External Pins to Select 13V/18V Options
  - Available with QFN Package Only
- Built-In Tone Oscillator Factory Trimmed to 22kHz
  - Facilitates DiSEqC$_{TM}$ (EUTELSAT) Encoding
- Internal Over-Temperature Protection and Diagnostics
- Internal Overload and Overtemp Flags (Visible on I²C)
- LNB Short-Circuit Protection and Diagnostics
- QFN Package
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Product Outline
  - Near Chip-Scale Package Footprint
- Pb-free Packaging Available
  - Designated with “Z” Suffix (Refer to Note Below)

Applications

- LNB Power Supply and Control for Satellite Set-Top Box

References

- Tech Brief 389 (TB389) - “PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages”; Available on the Intersil website, www.intersil.com

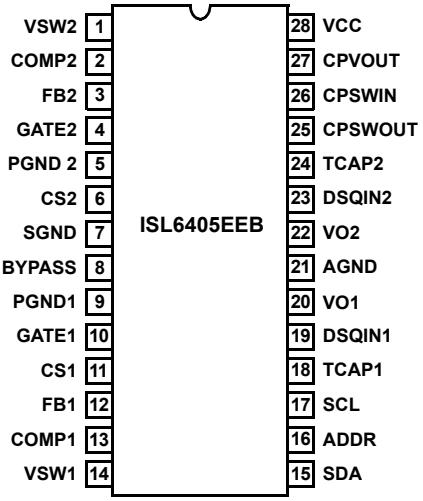
Ordering Information

PART #	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6405EEB	-20 to 85	28 Ld EPSOIC	M28.3B
ISL6405EEBZ (Note 1)	-20 to 85	28 Ld EPSOIC (Pb-free)	M28.3B
ISL6405ER	-20 to 85	32 Ld 5x5 QFN	L32.5x5
ISL6405ERZ (Note 1)	-20 to 85	32 Ld 5x5 QFN (Pb-free)	L32.5x5

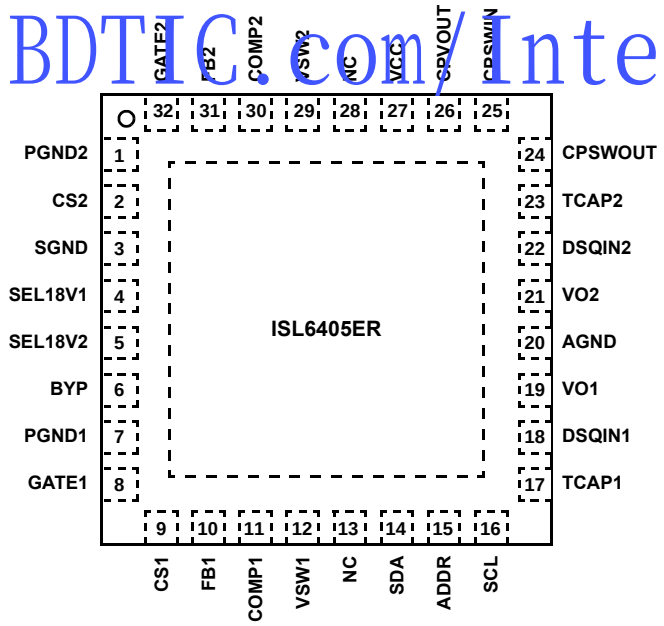
NOTES:

1. Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.
2. Tape and Reel available. Add “-T” suffix for Tape and Reel Packing Option.

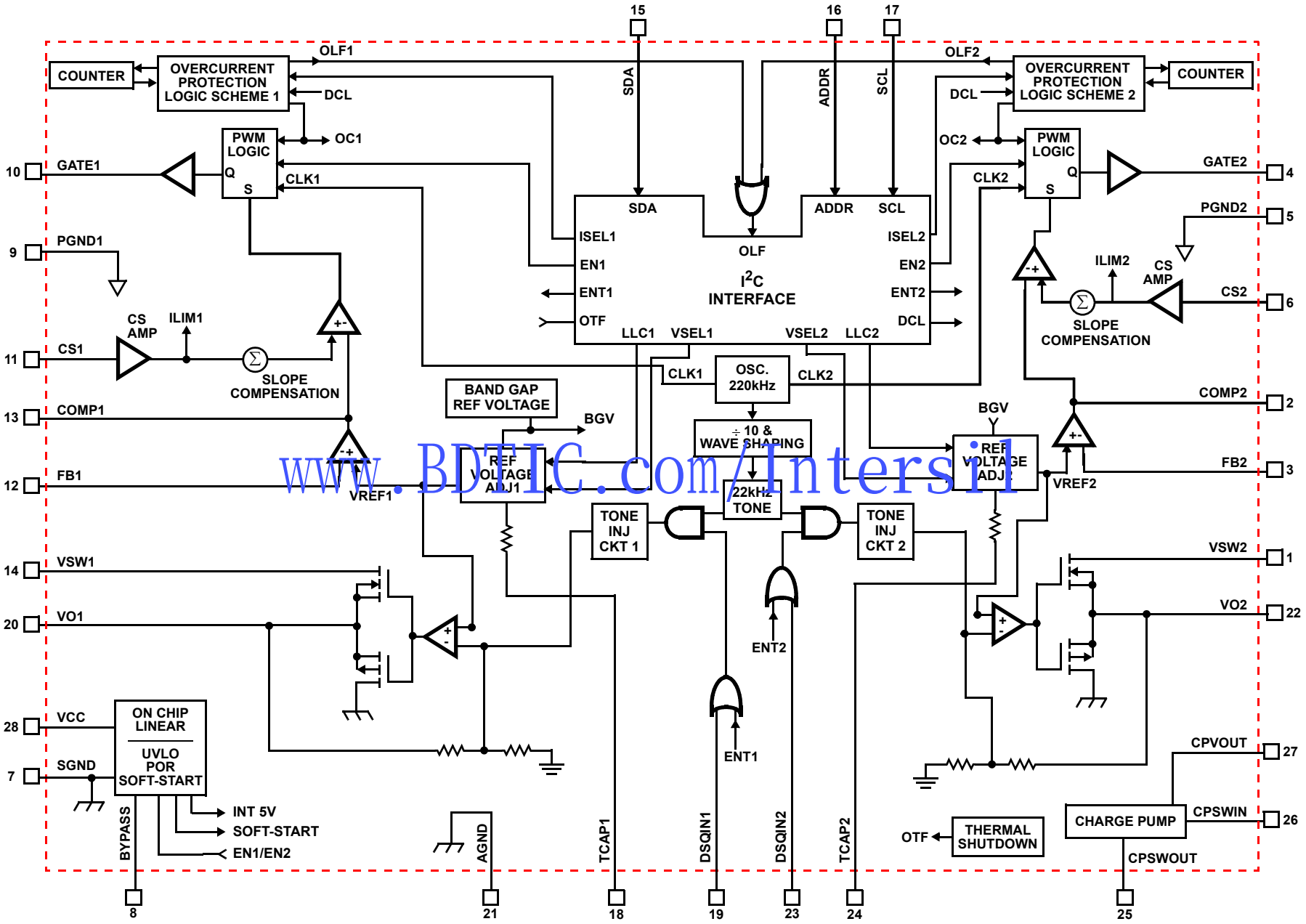
ISL6405 (EPSOIC)
TOP VIEW



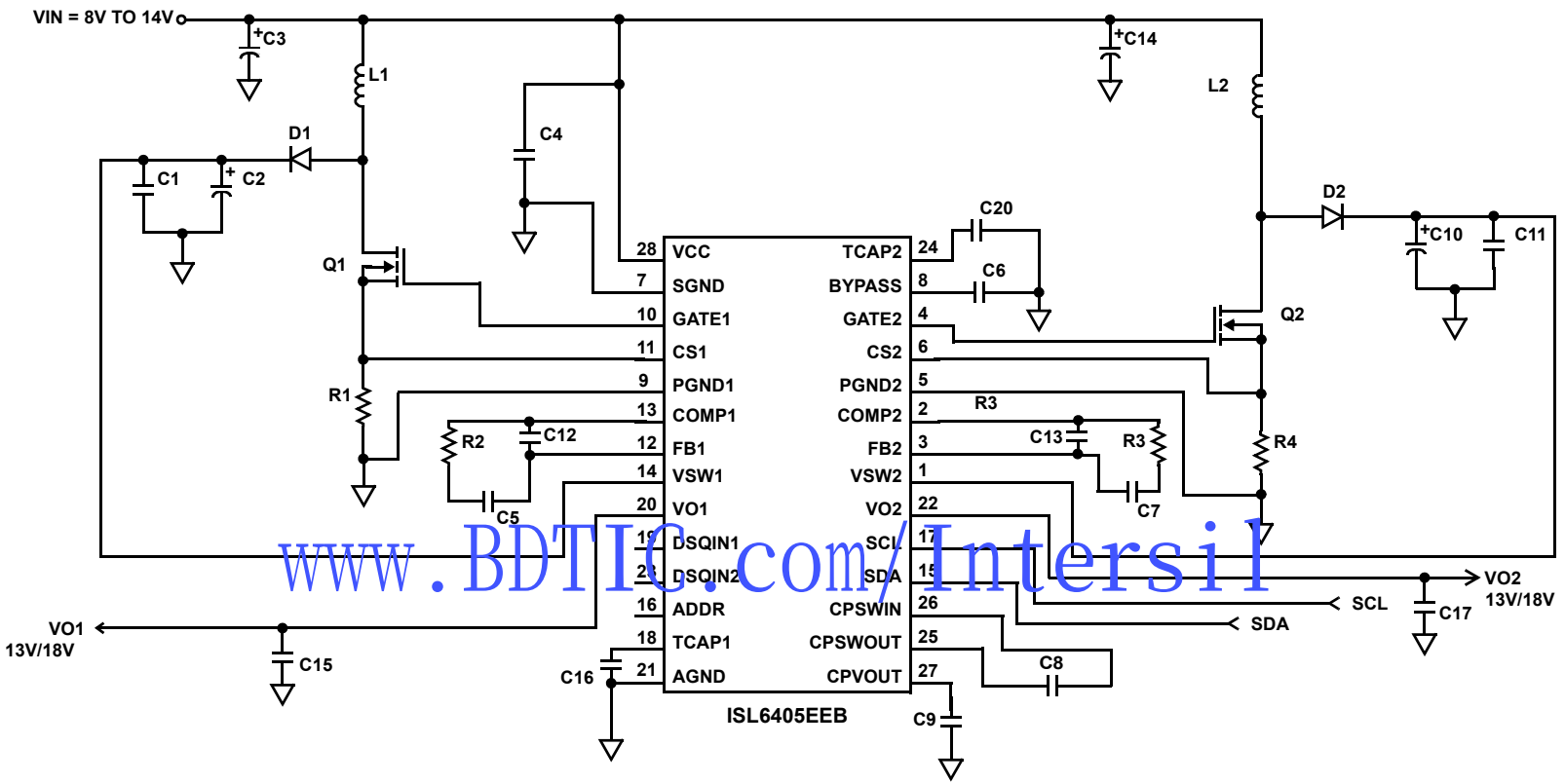
ISL6405 (QFN)
TOP VIEW



Block Diagram



Typical Application Schematic



Absolute Maximum Ratings

Supply Voltage, V_{CC} . . . . . 8.0V to 18.0V
Logic Input Voltage Range (SDA, SCL, ENT) . . . . . -0.5V to 7V

Thermal Information

Thermal Resistance (Typical, Notes 3, 4)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
EPSOIC Package (Notes 3, 4)	29	4
QFN Package (Notes 3, 4)	34	6

Maximum Junction Temperature (Note 5) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -40^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)
Operating Temperature Range . . . . . -20^oC to 85^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
4. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
5. The device junction temperature should be kept below 150^oC. Thermal shut-down circuitry turns off the device if junction temperature exceeds $+150^oC$ typically.

Electrical Specifications

V_{CC} = 12V, T_A = -20^oC to $+85^oC$, unless otherwise noted. Typical values are at T_A = 25^oC. EN1 = EN2 = H, LLC1 = LLC2 = L, ENT1 = ENT2 = L, DCL = L, DSQIN1 = DSQIN2 = L, Iout = 12mA, unless otherwise noted. See software description section for I^2C access to the system.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage Range			8	12	14	V
Standby Supply Current		EN1 = EN2 = L	-	1.5	3.0	mA
Supply Current	I_{IN}	EN1 = EN2 = LLC1 = LLC2 = VSEL1 = VSEL2 = ENT1 = ENT2 = H, No Load	-	4.0	8.0	mA
UNDER VOLTAGE LOCKOUT						
Start Threshold			7.5	-	7.95	V
Stop Threshold			7.0	-	7.55	V
Start to Stop Hysteresis			350	400	500	mV
SOFT START						
COMP Rise Time (Note 6)		(Note 7)	-	512	-	Cycles
Output Voltage (Note 7)	V_{O1}	VSEL1 = L, LLC1 = L	12.74	13.0	13.26	V
	V_{O1}	VSEL1 = L, LLC1 = H	13.72	14.0	14.28	V
	V_{O1}	VSEL1 = H, LLC1 = L	17.64	18.0	18.36	V
	V_{O1}	VSEL1 = H, LLC1 = H	18.62	19.0	19.38	V
	V_{O2}	VSEL2 = L, LLC2 = L	12.74	13.0	13.26	V
	V_{O2}	VSEL2 = L, LLC2 = H	13.72	14.0	14.28	V
	V_{O2}	VSEL2 = H, LLC2 = L	17.64	18.0	18.36	V
	V_{O2}	VSEL2 = H, LLC2 = H	18.62	19.0	19.38	V
Line Regulation	DV_{O1}, DV_{O2}	V_{IN} = 8V to 14V; V_{O1}, V_{O2} = 13V	-	4.0	40.0	mV
		V_{IN} = 8V to 14V; V_{O1}, V_{O2} = 18V	-	4.0	60.0	mV
Load Regulation	DV_{O1}, DV_{O2}	I_O = 12mA to 350mA	-	50	80	mV
		I_O = 12mA to 750mA (Note 8)	-	100	200	mV
Dynamic Output Current Limiting	I_{MAX}	DCL = L, ISEL1/2 = L	425	-	550	mA
		DCL = L, ISEL1/2 = H (Note 8)	775	850	950	mA
Dynamic Overload Protection Off Time	TOFF	DCL = L, Output Shorted (Note 8)	-	900	-	ms
Dynamic Overload Protection On Time	TON		-	20	-	ms

Electrical Specifications V_{CC} = 12V, T_A = -20°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C. EN1 = EN2 = H, LLC1 = LLC2 = L, ENT1 = ENT2 = L, DCL = L, DSQIN1 = DSQIN2 = L, Iout = 12mA, unless otherwise noted. See software description section for I^2C access to the system. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
22kHz TONE SECTION						
Tone Frequency	f_{tone}	ENT1/2 = H	20.0	22.0	24.0	kHz
Tone Amplitude	V_{tone}	ENT1/2 = H	500	680	800	mV
Tone Duty Cycle	dc_{tone}	ENT1/2 = H	40	50	60	%
Tone Rise or Fall Time	T_r, T_f	ENT1/2 = H	5	8	14	µs
LINEAR REGULATOR						
Drop-out Voltage		Iout = 750mA (Note 8)	-	1.2	-	V
DSQIN PIN						
DSQIN pin logic Low			-	-	1.5V	V
DSQIN pin Logic HIGH			3.0	-	-	V
DSQIN pin Input Current			-	1	-	µA
CURRENT SENSE						
Pulse by Pulse Current Limit (max Vin)			150	200	250	mV
Input Bias Current	I_{BIAS}		-	700	-	nA
Over Current Threshold		Static current mode, DCL = H	325	400	500	mV
ERROR AMPLIFIER						
Open Loop Voltage Gain	A_{OL}	(Note 8)	70	88	-	dB
Gain Bandwidth Product	GBP	(Note 8)	10	-	-	MHz
PWM						
Maximum Duty Cycle			90	93	-	%
Minimum Pulse Width		(Note 8)	-	20	-	ns
OSCILLATOR						
Oscillator Frequency	f_o	Fixed at (10)(f_{tone})	200	220	240	kHz
Thermal Shutdown						
Temperature Shutdown Threshold		(Note 8)	-	150	-	
Temperature Shutdown Hysteresis		(Note 8)	-	20	-	

NOTES:

6. Internal Digital Soft-start
7. VO1 for LNB1, VO2 for LNB2. Voltage programming signals VSEL1, VSEL2, LLC1, and LLC2 are implemented via the I^2C bus. IO1 = IO2 = 350mA/750mA.
8. Guaranteed by Design

Functional Pin Description

SYMBOL	FUNCTION
SDA	Bidirectional data from/to I^2C bus.
SCL	Clock from I^2C bus.
VSW1, 2	Input of the linear post-regulator.
PGND1, 2	Dedicated ground for the output gate driver of respective PWM.
CS1, 2	Current sense input; connect Rsc at this pin for desired over current value for respective PWM.
SGND	Small signal ground for the IC.
AGND	Analog ground for the IC.
TCAP1, 2	Capacitor for setting rise and fall time of the output of LNB A and LNB B respectively. Use this capacitor value 1µF or higher.
BYPASS	Bypass capacitor for internal 5V.
DSQIN1, 2	When HIGH enables internal 22kHz modulation for LNB A and LNA B respectively, Use this pin for tone enable function for LNB A and LNB B.
VCC	Main power supply to the chip.
GATE1, 2	These are the device outputs of PWM A and PWM B respectively. These high current driver outputs are capable of driving the gate of a power FET. These outputs are actively held low when Vcc is below the UVLO threshold.
VO1, 2	Output voltage of LNB A and LNB B respectively.
ADDR	Address pin to select two different addresses per voltage level at this pin.
COMP1, 2	Error amp outputs used for compensation.
FB1, 2	Feedback pins for respective PWMs
CPVOUT, CPSWIN, CPSWOUT	Charge pump connections.
SEL18V1, 2	When connected HIGH, this pin will change the output of the respective PWM to 18V. Only available on the QFN package option.

Functional Description

The ISL6405 dual output voltage regulator makes an ideal choice for advanced satellite set-top box and personal video recorder applications. Both supply and control voltage outputs for two low-noise blocks (LNBs) are available simultaneously in any output configuration. The device utilizes built-in DC/DC step-converters that, from a single supply source ranging from 8V to 14V, generate the voltages that enable the linear post-regulators to work with a minimum of dissipated power. An undervoltage lockout circuit disables the circuit when VCC drops below a fixed threshold (7.5V typ).

DiSEqC Encoding

The internal oscillator is factory-trimmed to provide a tone of 22kHz in accordance with DiSEqC (EUTELSAT) standards. No further adjustment is required. The 22kHz oscillator can be controlled either by the I^2C interface (ENT1/2 bit) or by a dedicated pin (DSQIN1/2) that allows immediate DiSEqC data encoding separately for each LNB. (Please see Note 1 at the end of this section.) All the functions of this IC are controlled via the I^2C bus by writing to the system registers (SR1, SR2). The same registers can be read back, and two bits will report the diagnostic status. The internal oscillator operates the converters at ten times the tone frequency. The device offers full I^2C compatible functionality, 3.3V or 5V, and up to 400kHz operation.

If the Tone Enable (ENT1/2) bit is set LOW through I^2C, then the DSQIN1/2 terminal activates the internal tone signal, modulating the dc output with a 0.3V, 22kHz, symmetrical waveform. The presence of this signal usually gives the LNB information about the band to be received.

Burst coding of the 22kHz tone can be accomplished due to the fast response of the DSQIN1/2 input and rapid tone response. This allows implementation of the DiSEqC (EUTELSAT) protocols.

When the ENT1/2 bit is set HIGH, a continuous 22kHz tone is generated regardless of the DSQIN1/2 pin logic status for the corresponding regulator channel (LNB-A or LNB-B). The ENT1/2 bit must be set LOW when the DSQIN1 and/or DSQIN2 pin is used for DiSEqC encoding.

Linear Regulator

The output linear regulator will sink and source current. This feature allows full modulation capability into capacitive loads as high as 0.25µF. In order to minimize the power dissipation, the output voltage of the internal step-up converter is adjusted to allow the linear regulator to work at minimum dropout.

When the device is put in the shutdown mode (EN1, EN2 = LOW), both PWM power blocks are disabled. (i.e. when EN1 = 0, PWM1 is disabled, and when EN2 = 0, PWM2 is disabled).

When the regulator blocks are active (EN1, EN2 = HIGH), the output can be logic controlled to be 13V or 18V (typical) by mean of the VSEL bit (Voltage Select) for remote controlling of non-DiSEqC LNBs. Additionally, it is possible to increment by 1V (typical) the selected voltage value to compensate for the excess voltage drop along the coaxial cable (LLC1/2 bit HIGH).

Output Timing

The programmed output voltage rise and fall times can be set by an external capacitor. The output rise and fall times will be approximately 3400 times the TCAP value. For the recommended range of 0.47µF to 2.2µF, the rise and fall time would be 1.6ms to 7.6ms. Using a 0.47µF capacitor insures the PWM stays below its overcurrent threshold when charging a 120µF VSW filter cap during the worst case 13V to 19V transition. A typical value of 1.0µF is recommended.

This feature only affects the turn-on and programmed voltage rise and fall times.

Current Limiting

The current limiting block has two thresholds that can be selected by the ISEL bit of the SR and can work either statically (simple current clamp) or dynamically. The lower threshold is between 425mA and 530mA (ISEL = L), while the higher threshold is between 775mA and 925mA (ISEL = H). When the DCL (Dynamic Current Limiting) bit is set to LOW, the over current protection circuit works dynamically: as soon as an overload is detected, the output is shutdown for a time t_{OFF}, typically 900ms. Simultaneously the OLF bit of the System Register is set to HIGH. After this time has elapsed, the output is resumed for a time t_{ON} = 20ms. During t_{ON}, the device output will be current limited to 425mA or 775mA, depending on the ISEL bits. At the end of t_{ON}, if the overload is still detected, the protection circuit will cycle again through t_{OFF} and t_{ON}. At the end of a full t_{ON} in which no overload is detected, normal operation is resumed and the OLF bit is reset to LOW. Typical t_{ON} + t_{OFF} time is 920ms as determined by an internal timer. This dynamic operation can greatly reduce the power dissipation in a short circuit condition, still ensuring excellent power-on start-up in most conditions.

However, there could be some cases in which a highly capacitive load on the output may cause a difficult start-up when the dynamic protection is chosen. This can be solved by initiating any power start-up in static mode (DCL = HIGH) and then switching to the dynamic mode (DCL = LOW) after a chosen amount of time. When in static mode, the OLF1/2 bit goes HIGH when the current clamp limit is reached and returns LOW when the overload condition is cleared. The OLF1/2 bit will be LOW at the end of initial power-on soft-start.

Thermal Protection

This IC is protected against overheating. When the junction temperature exceeds 150°C (typical), the step-up converter and the linear regulator are shut off and the OTF bit of the SR is set HIGH. Normal operation is resumed and the OTF bit is reset LOW when the junction is cooled down to 135°C (typical).

In over temperature conditions, the OTF Flag goes HIGH and the I^2C data will be cleared. The user may need to monitor the I^2C enable bits and OTF flag continuously and enable the chip, if I^2C data is cleared. OTF conditions may also make the OLF flags go HIGH, when high capacitive loads are present or self-heating conditions occur at higher loads.

External Output Voltage Selection

The output voltage can be selected by the I^2C bus. Additionally, the QFN package offers two pins (SEL18V1, SEL18V2) for independent 13V/18V output voltage selection. When using these pins, the I^2C bits should be initialized to 13V status.

TABLE 1.

I^2C BITS	SEL18V (1, 2)	O/P VOLTAGE
13V	Low	13V
14V	Low	14V
13V	High	18V
14V	High	19V

I^2C Bus Interface for ISL6405

(Refer to Philips I^2C Specification, Rev. 2.1)

Data transmission from main microprocessor to the ISL6405 and vice versa takes place through the two wire I^2C bus interface, consisting of the two lines SDA and SCL. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull up resistor. (Pull up resistors to positive supply voltage must be externally connected). When the bus is free, both lines are HIGH. The output stages of ISL6405 will have an open drain/open collector in order to perform the wired-AND function. Data on the I^2C bus can be transferred up to 100Kbps in the standard-mode or up to 400Kbps in the fast-mode. The level of logic “0” and logic “1” is dependent of associated value of V_{DD} as per electrical specification table. One clock pulse is generated for each data bit transferred.

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. Refer to Figure 1.

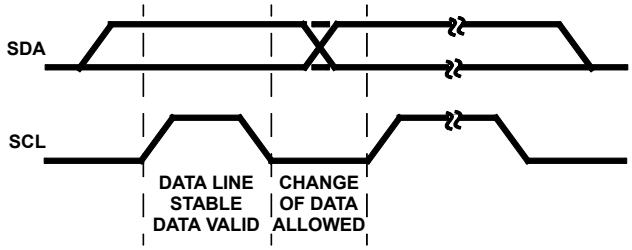


FIGURE 1. DATA VALIDITY

START and STOP Conditions

As shown in Figure 2, START condition is a HIGH to LOW transition of the SDA line while SCL is HIGH.

The STOP condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

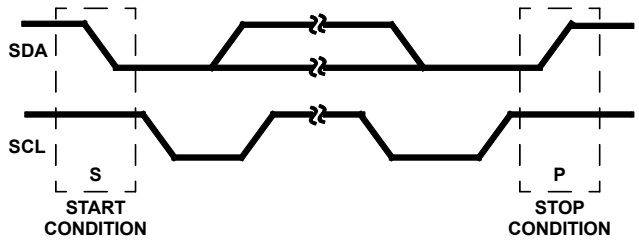


FIGURE 2. START AND STOP WAVEFORMS

Byte Format

Every byte put on the SDA line must be eight bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit first (MSB).

Acknowledge

The master (microprocessor) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (Figure 3). The peripheral that acknowledges has to pull down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse. (Of course, set-up and hold times must also be taken into account.)

The peripheral which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case, the master transmitter can generate the STOP information in order to abort the transfer. The ISL6405 will not generate the acknowledge if the POWER OK signal from the UVLO is LOW.

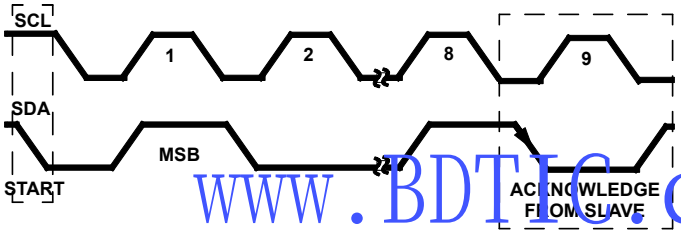


FIGURE 3. ACKNOWLEDGE ON THE I^2C BUS

Transmission Without Acknowledge

Avoiding detection of the acknowledgement, the microprocessor can use a simpler transmission; it waits one clock without checking the slave acknowledging, and sends the new data.

This approach, though, is less protected from error and decreases the noise immunity.

ISL6405 Software Description

Interface Protocol

The interface protocol is comprised of the following, as shown below in Table 2:

- A start condition (S)
- A chip address byte (MSB on left; the LSB bit determines read (1) or write (0) transmission) (the assigned I^2C slave address for the ISL6405 is 0001 00XX)
- A sequence of data (1 byte + Acknowledge)
- A stop condition (P)

TABLE 2. INTERFACE PROTOCOL

S	0	0	0	1	0	0	0	R/W	ACK	Data (8 bits)	ACK	P

System Register Format

- R, W = Read and Write bit
- R = Read-only bit
- All bits reset to 0 at Power-On

TABLE 3. SYSTEM REGISTER 1 (SR1)

R, W	R, W	R, W	R, W	R, W	R, W	R, W	R
SR1	DCL	ISEL1	ENT1	LLC1	VSEL1	EN1	OLF1

TABLE 4. SYSTEM REGISTER 2 (SR2)

R, W	R, W	R, W	R, W	R, W	R, W	R	R
SR2	ISEL2	ENT2	LLC2	VSEL2	EN2	OTF	OLF2

Transmitted Data (I^2C bus WRITE mode)

When the R/W bit in the chip is set to 0, the main microprocessor can write on the system registers (SR1/SR2) of the ISL6405 via I^2C bus. These will be written by the microprocessor as shown below. The spare bits of SR1/SR2 can be used for other functions.

TABLE 5. SYSTEM REGISTER (SR1 AND SR2) CONFIGURATION

SR	DCL	ISEL1	ENT1	LLC1	VSEL1	EN1	OLF1	FUNCTION
0				0	0	1		SR1 is selected
0				0	0	1		Vout1 = 13V, Vboost1 = 13V + Vdrop
0				0	1	1		Vout1 = 18V, Vboost1 = 18V + Vdrop
0				1	0	1		Vout1 = 14V, Vboost1 = 14V + Vdrop
0				1	1	1		Vout1 = 19V, Vboost1 = 19V + Vdrop
0			0			1		22kHz tone is controlled by DSQIN1 pin
0			1			1		22kHz tone is ON, DSQIN1 is disabled
0		0				1		Iout1 = 425mA max.
0		1				1		Iout1 = 775mA max.
0	1					1		Dynamic current limit NOT selected
0	0					1		Dynamic current limit selected
0	X	X	X	X	X	0		PWM and Linear for channel 1 disabled
SR	**ISEL2**	**ENT2**	**LLC2**	**VSEL2**	**EN2**	**OTF**	**OLF2**	**FUNCTION**
1						X	X	SR2 is selected
1			0	0	1	X	X	Vout2 = 13V, Vboost2 = 13V + Vdrop
1			0	1	1	X	X	Vout2 = 18V, Vboost2 = 18V + Vdrop
1			1	0	1	X	X	Vout2 = 14V, Vboost2 = 14V + Vdrop
1			1	1	1	X	X	Vout2 = 19V, Vboost2 = 19V + Vdrop
1		0				X	X	22kHz tone is controlled by DSQIN2 pin
1		1				X	X	22kHz tone is ON, DSQIN2 is disabled
1	0					X	X	Iout2 = 425mA max.
1	1					X	X	Iout2 = 775mA max.
1	X	X	X	X	0	X	X	PWM and Linear for channel 2 disabled

Received Data (I²C bus READ MODE)

The ISL6405 can provide to the master a copy of the system register information via the I²C bus in read mode. The read mode is Master activated by sending the chip address with R/W bit set to 1. At the following Master generated clock bits, the ISL6405 issues a byte on the SDA data bus line (MSB transmitted first).

At the ninth clock bit the MCU master can:

- Acknowledge the reception, starting in this way the transmission of another byte from the ISL6405.
- Not acknowledge, stopping the read mode communication.

While the whole register is read back by the microprocessor, only the two read-only bits, OLF and OTF, convey diagnostic information about the ISL6405.

After selection of SR1/SR2 ?

Power–On I²C Interface Reset

The I²C interface built into the ISL6405 is automatically reset at power-on. The I²C interface block will receive a Power OK logic signal from the UVLO circuit. This signal will go HIGH when chip power is OK. As long as this signal is LOW, the interface will not respond to any I²C commands and the system register SR1 and SR2 are initialized to all zeros, thus keeping the power blocks disabled. Once the Vcc rises above UVLO, the POWER OK signal given to the I²C interface block will be HIGH, the I²C interface becomes operative and the SRs can be configured by the main microprocessor. About 400mV of hysteresis is provided in the UVLO threshold to avoid false triggering of the Power-On reset circuit. (I²C comes up with EN = 0; EN goes HIGH at the same time as (or later than) all other I²C data for that PWM becomes valid).

ADDRESS Pin

Connecting this pin to GND the chip I²C interface address is 0001000, but, it is possible to choose between two different addresses simply by setting this pin at one of the two fixed voltage levels as shown in Table 8.

TABLE 6. ADDRESS PIN CHARACTERISTICS

V_{ADDR}	MINIMUM	TYPICAL	MAXIMUM
V_{ADDR}-1 “0001000”	0V	-	2V
V_{ADDR}-2 “0001001”	2.7V	-	5V

TABLE 7. READING SYSTEM REGISTERS

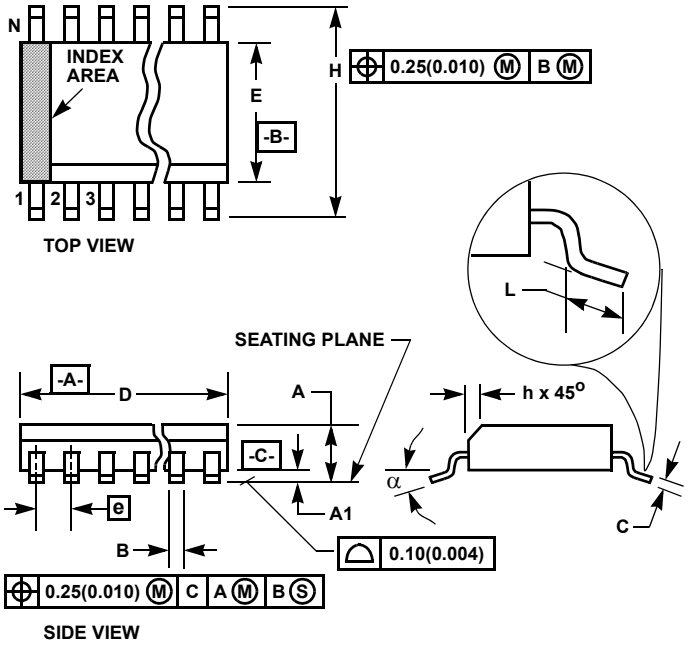
DCL	ISEL1/2	EN1/2	LLC1/2	VSEL1/1	EN1/2	OTF2	OLF1/2	FUNCTION
These bits are read as they were after the last write operation.						0		$T_J \leq 130°C$, normal operation
						1		$T_J > 150°C$, power blocks disabled
							0	$I_{OUT} < I_{MAX}$, normal operation
							1	$I_{OUT} > I_{MAX}$, overload protection triggered

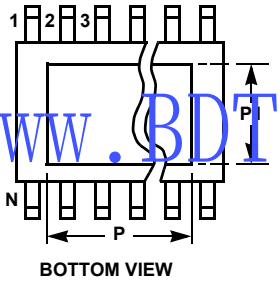
I²C Electrical Characteristics

TABLE 8. I²C SPECIFICATIONS

PARAMETER	TEST CONDITION	MINIMUM	TYPICAL	MAXIMUM
Input Logic High, VIH	SDA, SCL		0.7 x V_{DD}	
Input Logic Low, VIL	SDA, SCL		0.3 x V_{DD}	
Input Logic Current, IIL	SDA, SCL; 0.4V < V_{IN} < 4.5V			10µA
SCL Clock Frequency		0	100kHz	400kHz

Small Outline Exposed Pad Plastic Packages (EPSOIC)





M28.3B

28 LEAD WIDE BODY SMALL OUTLINE EXPOSED PAD PLASTIC PACKAGE

SYMBOL	INCHES			NOTES
	MIN	NOMINAL	MAX	
A	0.091	-	0.099	-
A1	0.001	-	0.005	-
B	0.014	-	0.019	9
C	0.0091	-	0.0125	-
D	0.701	-	0.711	3
E	0.292	-	0.299	4
e	0.050 BSC			-
H	0.400	-	0.410	-
h	0.010	-	0.016	5
L	0.024	-	0.040	6
N	28			7
α	0°	5°	8°	-
P	0.180	0.214	0.218	11
P1	0.156	0.190	0.194	11

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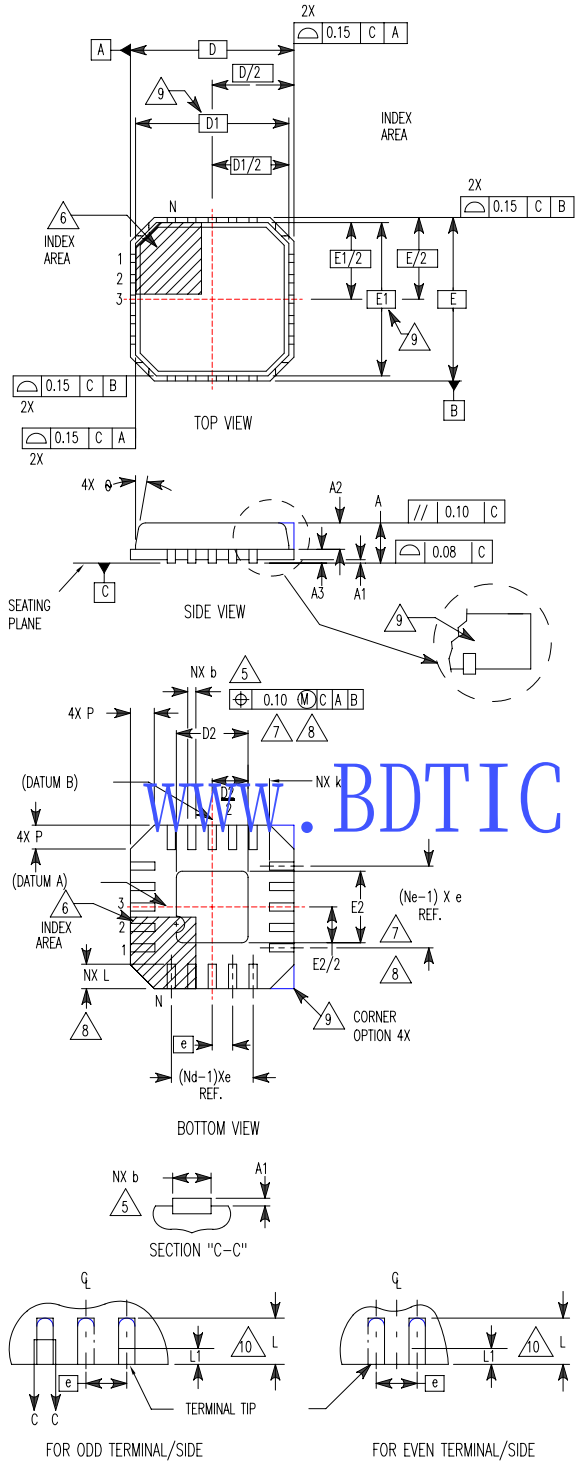
NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: INCH.
11. Dimensions “P” and “P1” are thermal and/or electrical enhanced variations. Values shown are maximum size of exposed pad within lead count body size.

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L32.5x5

32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VHHD-2 ISSUE C

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.23	0.30	5,8
D		5.00 BSC		-
D1		4.75 BSC		9
D2	2.95	3.10	3.25	7,8
E		5.00 BSC		-
E1		4.75 BSC		9
E2	2.95	3.10	3.25	7,8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
L1	-	-	0.15	10
N		32		2
Nd		8		3
Ne	8	8		3
P	-	-	0.60	9
θ	-	-	12	9

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.