intersil

ISL6112

Data Sheet **September 28, 2007** **FN6456.0**

Dual Slot PCI-Express Power Controller

The ISL6112 targets the PCI-Express add-in card hot plug application. Together with two each of N-Channel and P-Channel MOSFETs, four current sense resistors and several external passive components the ISL6112 provides a compliant hot plug power control solution to any combination of two PCI-Express X1, X4, X8 or X16 slots.

The ISL6112 features the ability to program a maximum current regulated level for each of the MAIN outputs for a common programmable duration so that both fault isolation protection and imperviousness to electrical transients (OC and soft-start protection) are provided to each system supply. For each 12VMAIN supply, the current regulated (CR) level is set by a resistor value dependant on the size of the PCI-Express connector (X1, X4/X8 or X16) to be powered. This resistor is a sub ohm standard value current sense resistor one each for each of the 3VMAIN and 12VMAIN supplies. The voltage across this resistor is compared to a 50mV reference providing a nominal CR protection level which would be set above the maximum specified slot limits. The 3.3V supply can use a 15mΩ sense resistor compared to a 50mV reference to provide a nominal regulated current limit of 3.3A to all connector sizes. A shutdown without a CR duration delay is invoked if R_{SENSE} voltage is >100mV. The VAUX is internally monitored and controlled to provide nominal limiting to 1A of load current.

The ISL6112 is System Management Interface (SMI) capable with an integrated SMBus link for communication, control, monitoring and reporting of IC and slot conditions. Information such as UV, OC, STATUS, power level etc. are available. Additionally the IC has a minimum of I/O for implementations where Hot-Plug Hardware Interface (HPI) is implemented.

Features

- Supports Two Independent PCI Express Slots
- Highest Available Accuracy External RSENSE Current Monitoring on Main Supplies
- Programmable Current Regulation Protection Function for X1, X4, X8, X16 Connectors
- 12V, 3.3V, and 3.3VAUX Supplies Supported per PCI Express Specification V1.0A
- Voltage Tolerant I/O SMBus Interface for Slot Power Control and Status, compatible with SMBus 2.0 Systems
- Programmable Current Regulation Duration
- Programmable In-rush Current Limiting
- Dual Level Fault Detection for Quick Fault Response without Nuisance Tripping
- Slot to Slot Electrical and Thermal Isolation
- Two General Purpose Input Pins Suitable for Interface to Logic and Switches.
- TQFP or QFN Pb-Free Package Options
    - TQFP is pin for pin equivalent to MIC2592B-2YTQ and is compatible with the TPS2363 pinout
    - The QFN package is 40% smaller and has lower die to case thermal impedance than the TQFP
- Pb-Free (RoHS Compliant)

Applications

- PCI Express V1.0A hot-plug power control
- PCI-Express Servers
- Power Supply Distribution and Control

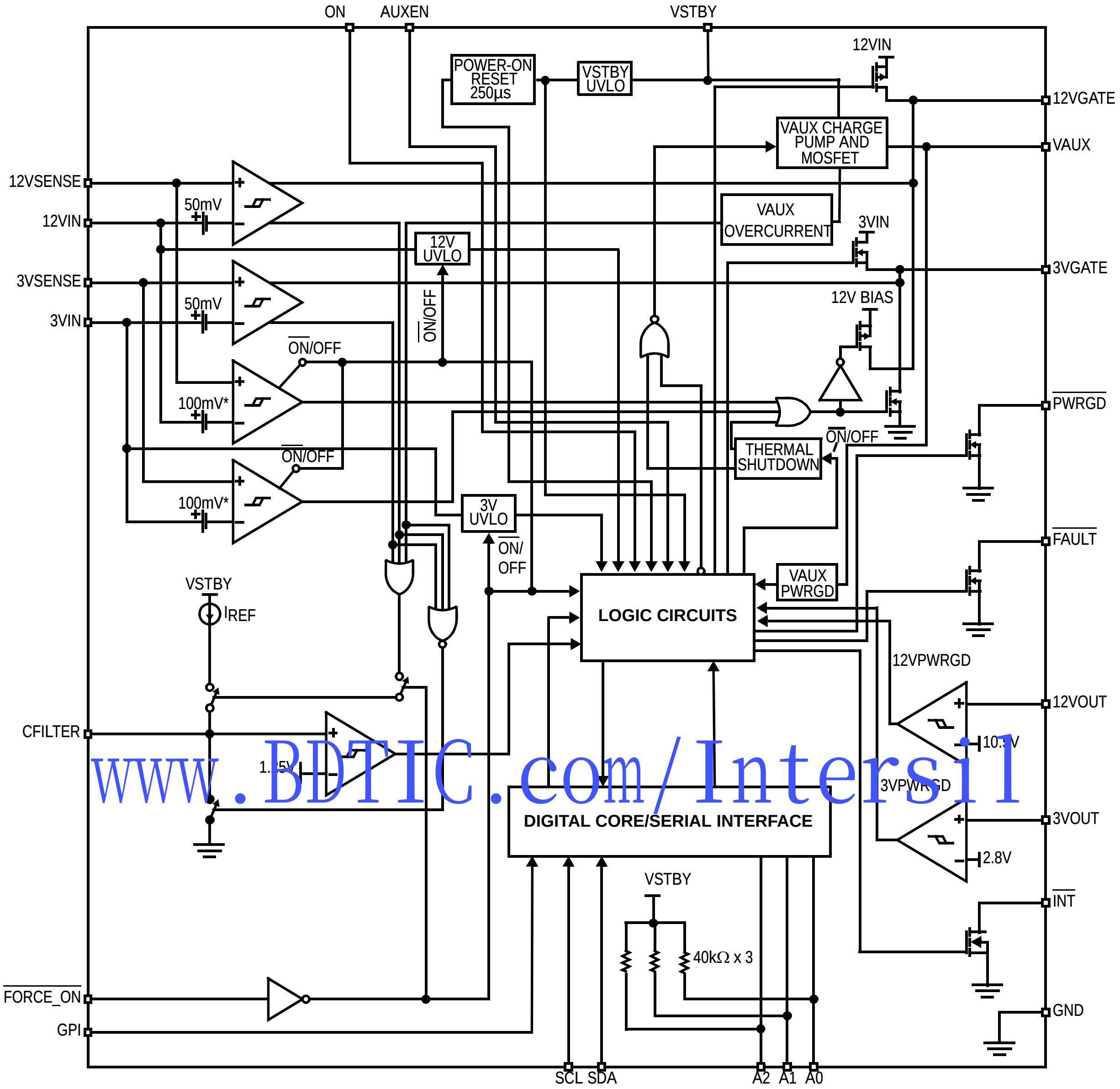
Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL6112IRZA	ISL6112 IRZ	-40 to +85	48 Ld 7x7 QFN	L48.7x7
ISL6112IRZA-T*	ISL6112 IRZ	-40 to +85	48 Ld 7x7 QFN Tape and Reel	L48.7x7
ISL6112INZA	ISL6112 INZ	-40 to +85	48 Ld 7x7 TQFP	Q48.7x7
ISL6112INZA-T*	ISL6112 INZ	-40 to +85	48 Ld 7x7 TQFP Tape and Reel	Q48.7x7
ISL6112EVAL1Z	Evaluation Platform			

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

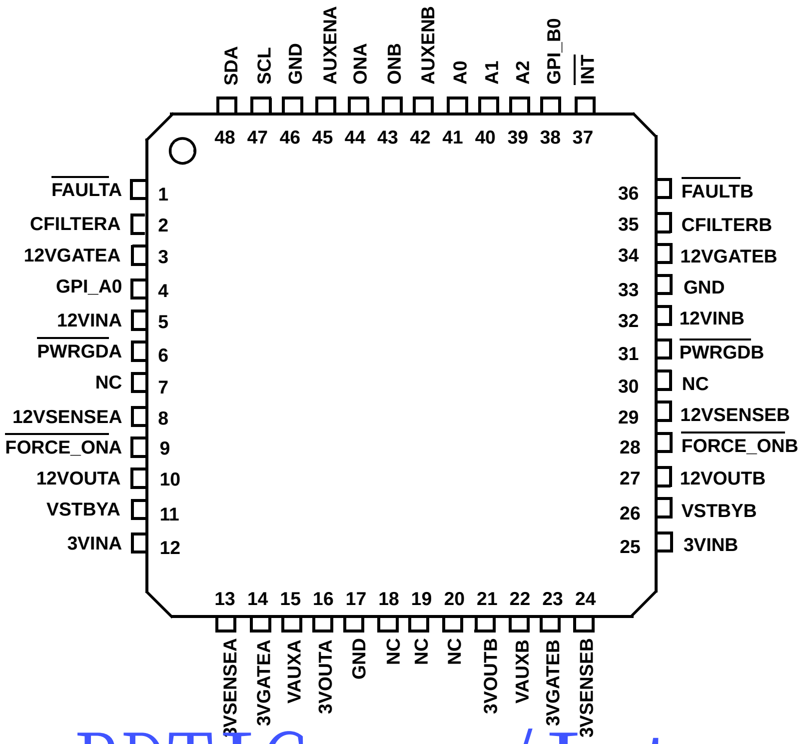
Functional Block Diagram (1 Channel)



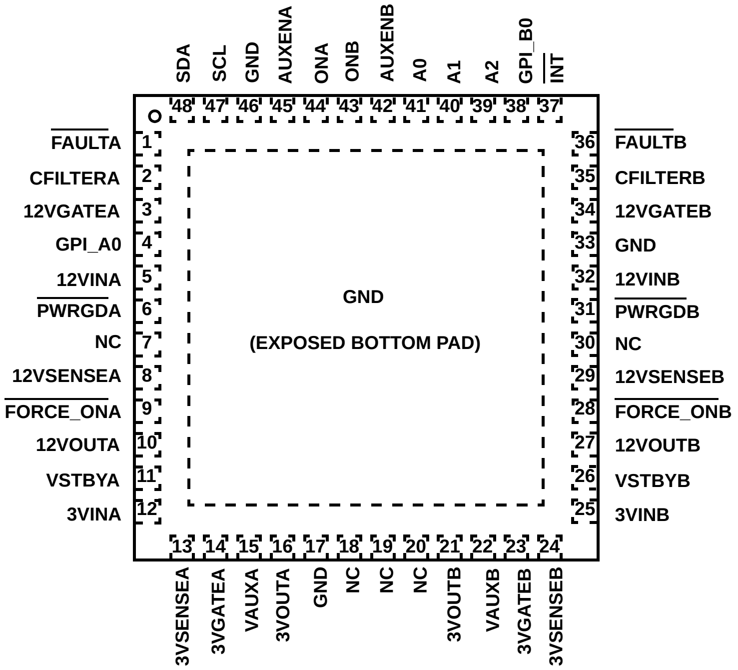
BOTH A AND B SLOTS SHARE THE SCL, SDA, A0, A1, A2, INT PINS.

Pinouts

ISL6112
(48 LD 7X7 TQFP)
TOP VIEW



ISL6112
(48 LD 7X7 QFN)
TOP VIEW



Pin Descriptions (Pin Numbers and Names are Related)

PIN NUMBER	PIN NAME	PIN FUNCTION
5, 32	12VINA, 12VINB	Provides 12VMAIN power supply and the high side of the sense resistor inputs. This must be a Kelvin connection between IC and sense resistor. An undervoltage lockout circuit (UVLO) prevents the switches from turning on while this input is less than its lockout threshold.
12, 25	3VINA, 3VINB	Provides 3.3VMAIN power supply and the high side of the sense resistor inputs. This must be a Kelvin connection between IC and sense resistor. An undervoltage lockout circuit (UVLO) prevents the switches from turning on while this input is less than its lockout threshold.
16, 21	3VOUTA, 3VOUTB	3.3VOUT. Connected to 3.3V FET source. These are used to monitor the 3.3V output voltages for Power Good status.
10, 27	12VOUTA, 12VOUTB	12VOUT. Connected to 12V FET drain. These are used to monitor the 3.3V output voltages for Power Good status.
8, 29	12VSENSEA, 12VSENSEB	12VMAIN low side of sense resistor connection. When either current limit threshold of the load current across the sense resistor = 50mV is reached, the related 12VGATE pin is modulated to maintain a constant voltage across the sense resistor and thus a constant current into the load. If the 50mV threshold is exceeded for tFLT, the isolation protection is tripped and the GATE pin for the affected supply's external MOSFET is immediately pulled high. This must be a Kelvin connection between IC and sense resistor.
13, 24	3VSENSEA, 3VSENSEB	3.3VMAIN low side of sense resistor connection. When either current limit threshold of the load current across the sense resistor = 50mV is reached, the related 3V GATE pin is modulated to maintain a constant voltage across the sense resistor and thus a constant current into the load. If the 50mV threshold is exceeded for tFLT, the isolation protection is tripped and the GATE pin for the affected supply's external MOSFET is immediately pulled low. This must be a Kelvin connection between IC and sense resistor.
3, 34	12VGATEA 12VGATEB	12V Gate Drive Outputs: Each pin connects to the gate of an external P-Channel MOSFET. During power-up, the CGATE and the CGS of the MOSFETs are connected to a 25µA current sink. This controls the value of dv/dt seen at the source of the MOSFETs. During current limit events, the voltage at this pin is adjusted to maintain constant current through the switch for a period of tFLT. Whenever an overcurrent, thermal shutdown, or input undervoltage fault condition occurs, the GATE pin for the affected slot is immediately brought high. These pins are charged by an internal current source during power-down.
14, 23	3VGATEA 3VGATEB	3V Gate Drive Outputs: Each pin connects to the gate of an external N-Channel MOSFET. During power-up, the CGATE and the CGS of the MOSFETs are connected to a 25µA current source. This controls the value of dv/dt seen at the source of the MOSFETs, and hence the current flowing into the load capacitance. During current limit events, the voltage at this pin is adjusted to maintain constant current through the switch for a period of tFLT. Whenever an overcurrent, thermal shutdown, or input undervoltage fault condition occurs, the GATE pin for the affected slot is immediately brought low. During power-down, these pins are discharged by an internal current source.
11, 26	VSTBYA, VSTBYB	3.3V Standby Input Voltage: Required to support PCI Express VAUX output. Additionally, the SMBus logic and internal registers run off of VSTBY to ensure that the chip is accessible during standby modes. A UVLO circuit prevents turn-on of this supply until VSTBY rises above its UVLO threshold. Both pins must be externally connected together at the ISL6112 controller.
15, 22	VAUXA, VAUXB	3.3VAUX Outputs to PCI Express Card Slots: These outputs connect the 3.3AUX pin of the PCI Express connectors to VSTBY via internal 400mΩ MOSFETs. These outputs are 1A current limited and protected against short-circuit faults.
44, 43	ONA, ONB	Enable Inputs: Rising-edge triggered. Used to enable or disable the MAINA and MAINB (+3.3V and +12V) outputs. Taking ON low after a fault resets the +12V and/or +3.3V fault latches for the affected slot. Tie these pins to GND if using SMI power control. Also, see pin description for $\overline{\text{FAULTA}}$ and $\overline{\text{FAULTB}}$.
45, 42	AUXENA, AUXENB	Level sensitive auxiliary enable Inputs. Used to enable or disable the VAUX outputs. Taking AUXEN low after a fault resets the respective slot's Aux Output Fault Latch. Tie these pins to GND if using SMI power control. Also, see pin description for $\overline{\text{FAULTA}}$ and $\overline{\text{FAULTB}}$.
2, 35	CFILTERA, CFILTERB	Overcurrent Timers: Capacitors connected between these pins and GND set the duration of CR_{TIM}. CR_{TIM} is the amount of time for which a slot remains in current limit before its isolation protection is invoked.
6, 31	$\overline{\text{PWRGDA}}$ $\overline{\text{PWRGDB}}$	Power-is-Good Outputs: Open-drain, active-low. Asserted when a slot has been commanded to turn on and has successfully begun delivering power to its respective +12V, +3.3V, and VAUX outputs. Each pin requires an external pull-up resistor to V_{STBY}.

Pin Descriptions (Pin Numbers and Names are Related) (Continued)

PIN NUMBER	PIN NAME	PIN FUNCTION
1, 36	$\overline{\text{FAULTA}}$, $\overline{\text{FAULTB}}$	Fault Outputs: Open-drain, active-low. Asserted whenever the isolation protection trips due to a fault condition (overcurrent, input undervoltage, over-temperature). Each pin requires an external pull-up resistor to V_{STBY}. Bringing the slot's ON pin low resets $\overline{\text{FAULT}}$ if $\overline{\text{FAULT}}$ was asserted in response to a fault condition on one of the slot's MAIN outputs (+12V or +3.3V). $\overline{\text{FAULT}}$ is reset by bringing the slot's AUXEN pin low if $\overline{\text{FAULT}}$ was asserted in response to a fault condition on the slot's VAUX output. If a fault condition occurred on both the MAIN and VAUX outputs of the same slot, then both ON and AUXEN must be brought low to de-assert the $\overline{\text{FAULT}}$ output.
9, 28	$\overline{\text{FORCE\_ONA}}$ $\overline{\text{FORCE\_ONB}}$	Enable Inputs: Active-low, level-sensitive. Asserting a $\overline{\text{FORCE\_ON}}$ input will turn on all three of the respective slot's outputs (+12V, +3.3V, and VAUX), while specifically defeating all protections on those supplies. This explicitly includes all overcurrent and short circuit protections, and on-chip thermal protection for the VAUX supplies. Additionally included are the UVLO protections for the +3.3V and +12VMAIN supplies. The $\overline{\text{FORCE\_ON}}$ pins do not disable UVLO protection for the VAUX supplies. These input pins are intended for diagnostic purposes only. Asserting $\overline{\text{FORCE\_ON}}$ will cause the respective slot's $\overline{\text{PWRGD}}$ and $\overline{\text{FAULT}}$ pins to enter their open-drain state. Note that the SMBus register set will continue to reflect the actual state of each slot's supplies. There is a pair of register bits, accessible via the SMBus, which can be set to disable (unconditionally de-assert) either or both of the $\overline{\text{FORCE\_ON}}$ pins -- See CNTRL Register Bit D[2].
4, 38	GPI_A0, GPI_B0	General Purpose Inputs: The states of these two inputs are available by reading the Common Status Register, Bits [4:5]. If not used, connect each pin to GND.
39, 40, 41	A2, A1, A0	SMBus Address Select Pins. Connect to ground or leave open in order to program device SMBus base address. These inputs have internal pull-up resistors to VSTBY. Address programmed on rising VSTBY.
48	SDA	Bidirectional SMBus data line.
47	SCL	SMBus Clock Input.
37	$\overline{\text{INT}}$	Interrupt Output. Open-drain, active-low. output. Asserted whenever a power fault is detected if the INTMSK bit (CS Register Bit D[3]) is a logical "0". This output is cleared by performing an "echo reset" to the appropriate fault bit(s) in the STAT and/or CS registers. This pin requires an external pull-up resistor to VSTBY.
17, 33, 46	GND	IC Reference pins. Connect together and tie directly to the system's analog GND plane directly at the device.
7, 18, 19, 20, 30	NC	Reserved: Make no external connections to these pins.

Absolute Maximum Ratings (Note 4)

12VIN, 12VSENSE, 12VOUT	+14.5V
VSTBY, 3VIN, 3VSENSE, 3VOUT	+7V
12VGATE	-0.3V to 12VI
3VGATE	-0.3V to 12VI
Logic I/O	-0.5V to +5.5V
VAUX Output Current	Short Circuit Protected
ESD Rating	
Human Body Model	2kV
Machine Model	200V
Charged Device Model	1kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
48 Ld 7x7 TQFP Package (Note 1)	57	N/A
48 Ld 7x7 QFN Package (Notes 2, 3)	27	3

Maximum Junction Temperature	+150°C
Maximum Storage Temperature Range	-65°C to +150°C
Pb-free reflow profile	see link below

http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

12VMAIN Supply Voltage Range	+12V ± -10%
3.3VMAIN Supply Voltage Range	+3.3V ± -10%
AUXI Supply Voltage Range	+3.3V ± -10%
Temperature Range (T_A)	-40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
3. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
4. All voltages are relative to GND, unless otherwise specified.

Electrical Specifications

12VIN = 12V, 3VIN = 3.3V, VSTBY = 3.3V, $T_A = T_J$ = -40°C to +85°C, Unless Otherwise Noted.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
POWER CONTROL AND LOGIC SECTIONS						
Supply Current	ICC12	HPI Enabled or SMI enabled with no load		0.9	1.5	mA
	ICC3.3			0.1	0.2	mA
	ICCSTBY			5	6	mA
Undervoltage Lockout Thresholds	VUVLO(12V)	12VIN increasing	8	9	10	V
	VUVLO(3V)	3VIN increasing	2.1	2.5	2.75	V
	VUVLO(STBY)	VSTBY increasing	2.8	2.9	2.96	V
Undervoltage Lockout Hysteresis 12VIN, 3VIN	VHYSUV			180		mV
Undervoltage Lockout Hysteresis VSTBY	VHYSSTBY			50		mV
Power-Good Undervoltage Thresholds	VUVTH(12V)	12VOUT decreasing	10.15	10.5	10.75	V
	VUVTH(3V)	3VOUT decreasing	2.7	2.8	2.9	V
	VUVTH(VAUX)	VAUX decreasing	2.55	2.8	3	V
Power-Good Detect Hysteresis	VHYSPG			30		mV
12VGATE Voltage	VGATE (12V)	Max. Gate Voltage when Enabled	0	0.4	0.55	V
12VGATE Sink Current	IGATE(12VSINK)	Start Cycle	17	25	35	µA
12VGATE Pull-up Current (Fault Off)	IGATE (12VPULL-UP)	Any fault condition (VDD – VGATE) = 2.5V	35	72	-	mA
3VGATE Voltage	VGATE(3V)	Minimum Gate Voltage when Enabled	12VIN – 0.3	12VIN – 0.2	12VIN	V
3VGATE Charge Current	IGATE (3VCHARGE)	Start Cycle	17	25	35	µA
3VGATE Sink Current (Fault Off)	IGATE(3VSINK)	Any fault condition VGATE = 2.5V	80	105		mA

Electrical Specifications

12VIN = 12V, 3VIN = 3.3V, VSTBY = 3.3V, $T_A = T_J$ = -40°C to +85°C, Unless Otherwise Noted. **(Continued)**

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
CFILTER OVERCURRENT DELAY TIME PINS 2 AND 35 FLOATING						
CFILTER Threshold Voltage	VFILTER		1.20	1.25	1.30	V
CFILTER Charging Current Nominal Current Limit Duration = $C_{CFILTER}$ x 550k	IFILTER	VXVIN – VXSENSE > VTHILIMIT	2	2.5	3	µA
	tFILTER	CFILTER Open		10		µs
Current Limit Threshold Voltages	VTHILIMIT	VXIN – VXVSENSE	47.5	50	52.5	mV
Fast-Trip Threshold Voltages	VTHFAST	VXVIN – VXVSENSE	85	100	115	mV
XVSENSE Input Current	ISENSE			0.1		µA
LOW-Level Input Voltage ON, AUXEN, GPI, FORCE_ON, PRSNT	VIL				0.8	V
Output LOW Voltage FAULT, PWRGD	VOL	IOL = 3mA			0.4	V
HIGH-Level Input Voltage ON, AUXEN, GPI, FORCE_ON	VIH		2.1.		5	V
Internal Pull-ups to VSTBY (Note 5)	RPULL-UP			40	50	kΩ
12VIN, 3VIN Input Leakage Current	ILKG,OFF XVIN	VSTBY = +3.3V, 12VIN = OFF; 3VIN = OFF		0.5	1	µA
Input Leakage Current, ON, AUXEN, FORCE_ON	IIL		-2		2	µA
Off-State Leakage Current FAULT, PWRGD, GPI	ILKG(OFF)	GPI ILKG for these two pins measured with VAUX OFF	-2		2	µA
Over-temperature Shutdown and Reset Thresholds, with Overcurrent On Slot	TOV	T_J increasing, each slot (Note 5)		140		°C
		T_J decreasing, each slot (Note 5)		130		°C
Over-temperature Shutdown and Reset Thresholds, All Other Conditions (All Outputs Will Latch Off)		T_J increasing, each slot (Note 5)		160		°C
		T_J decreasing, each slot (Note 5)		150		°C
Output MOSFET Resistance VAUX MOSFET	r_{DS}(AUX)	IDS = 375mA			350	mΩ
Off-State Output Offset Voltage VAUX	VOFF(VAUX)	VAUX = Off		25	40	mV
Regulated Current Level	ILIM(AUX)		0.8	1	1.2	A
Output Discharge Resistance	RDIS(12V)	12VOUT = 6.0V		1400	1850	Ω
	RDIS(3V)	3VOUT = 1.65V		140	180	Ω
	RDIS(VAUX)	3VAUX = 1.65V		350	400	Ω
12V Current Limit Response Time (See “Typical Application Diagram” on page 9).	tOFF(12V)	CGATE = 25pF VIN – VSENSE = 140mV		1	2.1	µs
3.3V Current Limit Response Time (See “Typical Application Diagram” on page 9).	tOFF(3V)	CGATE = 25pF VIN – VSENSE = 140mV		0.3	1	µs
VAUX Current Limit Response Time (See “Typical Application Diagram” on page 9).	tSC	VAUX = 0V, VSTBY = +3.3V		2.5		µs
Delay from MAIN Overcurrent to FAULT Output	tPROP (12V FAULT or 3V FAULT)	CFILTER = 0 VIN – VSENSE = 140mV		1		µs
Delay from VAUX Overcurrent to FAULT Output	tPROP (VAUXFAULT)	$I_{LIM(AUX)}$ to FAULT output CFILTER = 0 VAUX Output Grounded		1		µs
ON, AUXEN, PRSNT Minimum Pulse Width	tW	(Note 5)		100		ns
Power-On Reset Time after VSTBY Becomes Valid	tPOR	(Note 5)		250		µs

Electrical Specifications

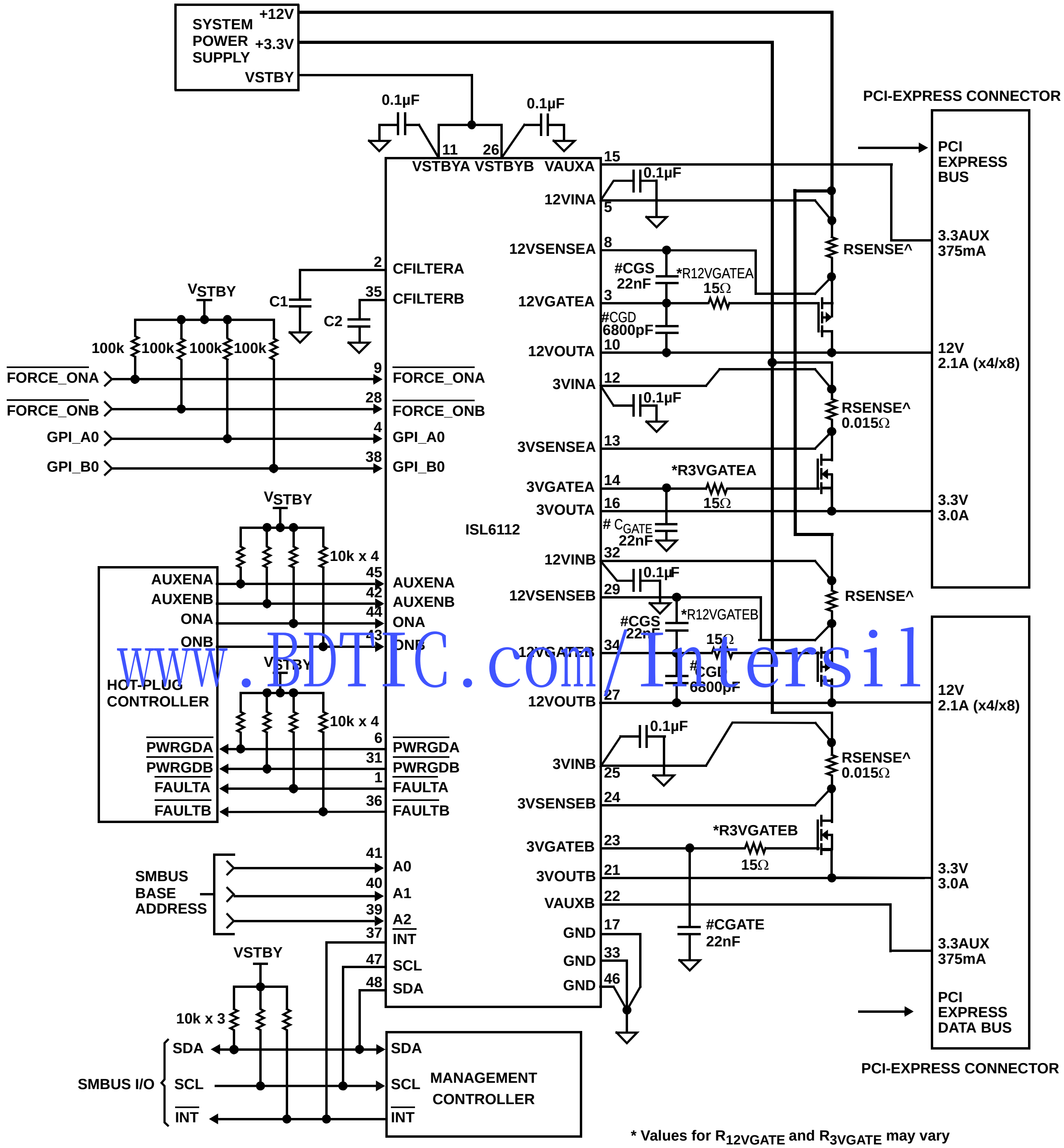
12VIN = 12V, 3VIN = 3.3V, VSTBY = 3.3V, $T_A = T_J$ = -40°C to +85°C, Unless Otherwise Noted. **(Continued)**

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
SMBUS TIMING						
SCL (clock) period	t1	(Note 5)	2.5			µs
Data In setup time to SCL HIGH	t2	(Note 5)	100			ns
Data Out stable after SCL LOW	t3	(Note 5)	300			ns
Data LOW setup time to SCL LOW	t4	(Note 5)	100			ns
Data HIGH hold time after SCL HIGH	t5	(Note 5)	100			ns

NOTE:

5. Limits established by design and are not production tested.

Typical Application Diagram



* Values for $R_{12VGATE}$ and R_{3VGATE} may vary depending upon the C_{GS} of the external MOSFETs.

\# These components are not required for ISL6112 operation but can be implemented for GATE output slew rate control (application specific)

- Bold lines indicate high current paths

^ R_{SENSE} value is application specific

Functional Description

The ISL6112 protects the power supplies in PCI-Express systems that utilize hot-pluggable add-in cards. This IC together with two each of N-Channel and P-Channel MOSFETs, four current sense resistors and a few external passive components, provide a compliant hot plug power control solution to any combination of two PCI-Express X1, X4, X8 or X16 slots.

The ISL6112 primarily features start-up in-rush current protection, maximum current regulated (CR) levels for each of the MAIN and AUX outputs, programmable CR duration so that both fault isolation protection and imperviousness to electrical transients are provided. The ISL6112 also offers input and output voltage supervisory functions and two operational system interfaces for implementation flexibility.

In-Rush Current Protection

When any electronic circuitry is powered up, there is an in-rush of current due to the charging of bulk capacitance that resides across the circuit board's supply pins. This transient in-rush current may cause the systems supply voltages to temporarily droop out of regulation, causing data loss or system lock-up. The ISL6112 addresses these issues by limiting the in-rush currents to the PCI-Express add-in cards, and thereby controlling the rate at which the loads circuits turn-on. See Figures 2, 3, 4, 5, 6 and 7 for AUX and MAIN turn-on examples illustrating the current limiting capabilities across a variety of compensation component values.

MAIN Supply Overcurrent Protection

For each of the 3VMAIN and 12VMAIN supplies, the current regulated (CR) levels are set by a sub ohm value sense resistor. The value for the 12VMAIN is dependant on the size of the PCI-Express connector (X1, X4/X8 or X16) to be powered. The voltage across this resistor is compared to a 50mV internal reference providing a nominal CR protection level which would be set above the maximum specified slot limits. The 3.3VMAIN supply can use a 15mΩ sense resistor compared to a 50mV reference to provide a nominal regulated current limit of 3.3A, as this supply has a common 3A maximum across all slot sizes. For both MAIN supplies, there is a Way Overcurrent (WOC) shutdown protocol that is without a CR duration. WOC is invoked if the load current causes the RSENSE voltage to be >100mV. See Figures 10 and 11.

VAUX Supply Overcurrent Protection

The VAUX load current is internally monitored and controlled via an internal power FET. This FET has a typical $r_{DS(ON)}$ of 320mW at a VAUX current of 375mA to minimize distribution losses to typically <100mV through the IC. Using active monitoring and control, the ISL6112 provides nominal limiting to ~1000mA of load current across the temperature range and for various loading conditions. See Figures 2, 12 and 13 for examples of this performance.

Current Regulation (CR) Duration

The CR duration for each slot is set by an external capacitor between the associated CFILTER pin and ground. This feature masks current transients and overcurrents prior to supply turn-off. Once the CR duration has expired, the IC then quickly turns-off the associated MAIN outputs via its external FETs or the failed AUX output, unloading the faulted load card from the supply voltage rails.

UVLO, Power Good and FAULT

The ISL6112 incorporates undervoltage lock out (UVLO) protections on each of the four MAIN VIN and two VSTBY supplies to prevent operation during a 'brown out' condition. Likewise on the outputs are minimum voltage compliances that must be satisfied for the Power Good output, PWRGD to be asserted. There is some hysteresis on the UVLO levels as the voltage on VIN decreases to ensure IC operation below the minimum operating supply standards. The $\overline{\text{FAULT}}$ output is asserted (low) whenever there is an OC, OT or UV condition. The $\overline{\text{FAULT}}$ is cleared once the appropriate enable is deasserted.

Operational System Interfaces

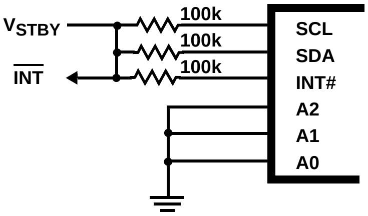
The ISL6112 employs two system interfaces: the hardware Hot-Plug Interface (HPI) and the System Management Interface (SMI). The HPI I/O includes ON, AUXEN, $\overline{\text{FAULT}}$ and $\overline{\text{PWRGD}}$]; the SMI I/O consists of SDA, SCL, and $\overline{\text{INT}}$, whose signals conform to the levels and timing of the SMBus specification; see "SMI only Control Applications" on page 17 The ISL6112 can be operated exclusively from either the SMI or HPI, or can employ the HPI for power control while continuing to use the SMI for access to all but the power control registers.

In addition to the basic power control features of the ISL6112 accessible by the HPI, the SMI also gives the host access to the following information from the part:

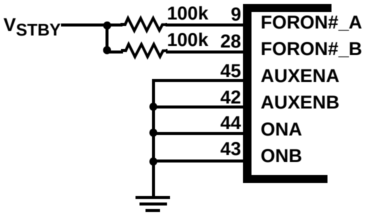
- Fault conditions occurring on each supply. These faults include Overcurrent, Over-Temperature and undervoltage
- GPI pin status when using the System

When using the System Management Interface for power control, do not use the Hot-Plug Interface. Conversely, when using the Hot-Plug Interface for power control, do not execute power control commands over the System Management Interface bus (all other register accesses via the SMI bus remain permissible while in the HPI control mode). When utilizing the SMI exclusively, the HPI input pins (ON, AUXEN, and $\overline{\text{FORCE\_ON}}$) should be configured, as shown in Figure 1 (disabling HPI when SMI control is used). This configuration safeguards the power slots in the event that the SMBus communication link is disconnected for any reason.

Additionally, when utilizing the HPI exclusively, the SMBus (or SMI) will be inactive if the input pins (SDA, SCL, A0, A1, and A2) are configured as shown in Figure 1.



DISABLING SMI WHEN HPI CONTROL IS USED



DISABLING HPI WHEN SMI CONTROL IS USED

FIGURE 1. I/O CONFIGURATION FOR DISABLING HPI/SMI CONTROL

ISL6112 Bias, Power-On Reset and Power Cycling

The ISL6112 utilizes VSTBY as the only supply source. VSTBY is required for proper operation of the ISL6112's SMBus and registers and must be applied at all times. A Power-On Reset (POR) cycle is initiated after VSTBY rises above its UVLO threshold and remains satisfied for 250µs. All internal registers are cleared after POR. If VSTBY is recycled, the ISL6112 enters a new power-on-reset cycle. VSTBY must be the first supply voltage applied followed by the MAIN supply inputs of 12VIN and 3VIN. The SMBus is ready for access at the end of the POR cycle (250µs after VSTBY is valid). During t_{POR}, all outputs remain off.

Enabling the VAUX Outputs

Upon asserting an AUXEN input, the related internal power switch turns on connecting the nominally 3.3V VSTBY supply to its VAUX load. The turn-on is slew rate limited and invokes the ICs current regulation feature so as to not droop the supply due to in-rush current load. Figure 2 illustrates the VAUX turn-on performance into a 10Ω, 100µF load.

Standby Mode

Standby mode is entered when one or more of the MAIN supply inputs (12VIN and/or 3VIN) is absent, below its respective UVLO threshold or OFF. The ISL6112 also has 3.3V auxiliary outputs (VAUXA and VAUXB), satisfying an optional PCI Express requirement. These outputs are fed from the VSTBY input pins, they are independent of the MAIN outputs and are controlled by the AUXEN input pins or via their respective bits in the control registers. Should the MAIN supply inputs fall below their respective UVLO thresholds, VAUX will still function as long as VSTBY is compliant. Prior to standby mode, ONA and ONB (or the control registers' MAINA and MAINB bits) inputs must be deasserted or else the ISL6112 will assert its $\overline{\text{FAULT}}$ outputs. If an undervoltage condition on either of the MAIN supply inputs is detected, the $\overline{\text{INT}}$ will also assert if interrupts are enabled.

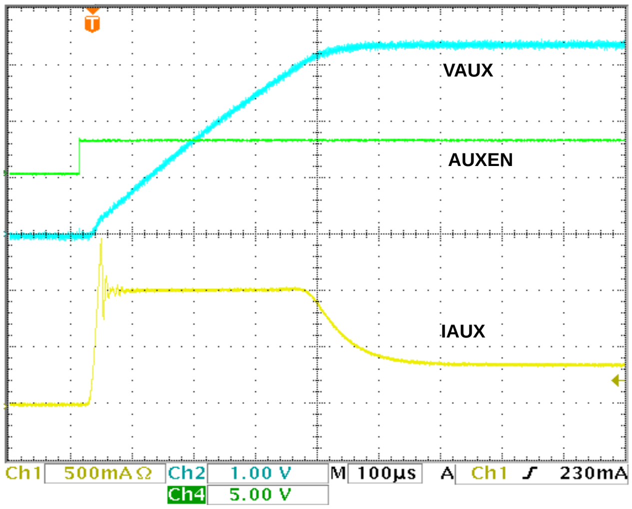


FIGURE 2. VAUX TURN-ON R_{LOAD} = 10Ω, C_{LOAD} = 100µF

Enabling the MAIN GATE outputs

When a slot's MAIN supplies are off, the 12VGATE pin is held high with an internal pull-up to the 12VIN voltage. Similarly, the 3VGATE pin is internally held low to GND. When the MAIN supplies of the ISL6112 are enabled by asserting ON, the related 3VGATE and 12VGATE pins are each connected to a constant current supply. For the 3VGATE pin, this is nominally a 25µA current source and for the 12VGATE pin, this is nominally a -25µA current sink. The 3VGATE will be charged up to the 12VIN voltage whereas the 12GATE will be pulled down to GND for maximum enhancement of the N-Channel and P-Channel FETs, respectively.

Estimating In-Rush Current and V_{OUT} Slew Rate at Start-up

The expected in-rush current can be estimated by using Equation 1:

$$I_{IN-RUSH}\,\text{NOMINALLY} = 25\mu A\left(\frac{C_{LOAD}}{C_{GATE}}\right) \quad \text{(EQ. 1)}$$

with 25µA being the GATE pin charge current, C_{LOAD} is the load capacitance, and C_{GATE} is the total GATE capacitance including C_{ISS} of the external MOSFET and any external capacitance connected from the GATE output pin to the GATE reference, GND or source.

An estimate for the output slew rate of 3.3V outputs and 12V outputs where there is little or no external 12VGATE output capacitors, can be had from Equation 2:

$$dv/dt\ \text{VOUT}\ \ \text{NOMINALLY} = \frac{I_{LIM}}{C_{LOAD}} \quad \text{(EQ. 2)}$$

where I_{LIM} = 50mV/R_{SENSE} and C_{LOAD} is the load capacitance. As a consequence, the CR duration, t_{FILTER}, must be programmed to exceed the time it will take to fully charge the output load to the input rail voltage level.

MAIN Outputs (Start-up Delay and Slew-Rate Control)

The 3.3V outputs act as source followers. In this mode of operation, $V_{SOURCE} = [V_{GATE} - V_{TH(ON)}]$ until the associated output reaches 3.3V. The voltage on the gate of the MOSFET will then continue to rise until it reaches 12V, which ensures minimum $r_{DS(ON)}$. For the 12V outputs, when the MOSFET is optionally configured as a Miller integrator to adjust the V_{OUT} ramp time by having a C_{GD} capacitor, which is connected between the MOSFET's gate and drain. In this configuration, the feedback action from drain to gate of the MOSFET causes the voltage at the drain of the MOSFET to slew in a linear fashion at a rate estimated by Equation 3:

$$\text{dv/dt VOUT NOMINALLY} = \frac{25\mu A}{C_{GD}} \qquad \text{(EQ. 3)}$$

Table 1 approximates the output slew-rate for various values of C_{GATE} when start-up is dominated by GATE capacitance (external C_{GATE} from GATE pin to ground plus C_{GS} of the external MOSFET for the 3.3V rail; C_{GD} for the 12V rail).

TABLE 1. 3.3V AND 12V OUTPUT SLEW-RATE SELECTION FOR GATE CAPACITANCE DOMINATED START-UP

| IGATE | = 25µA	
CGATE or C_{GD}	dv/dt (load)
0.01µF*	2.5V/ms
0.022µF*	1.136V/ms
0.047µF	0.532 V/ms
0.1µF	0.250V/ms

*Values in this range will be affected by the internal parasitic capacitances of the MOSFETs used, and should be verified experimentally.

Note that all of these performance estimates are useful only for first order time and loading expectations as they do not look at other significant loading factors. Figures 3, 4, 5, 6 and 7 illustrate empirically the discussed turn-on performance with the noted loading and compensation conditions.

Notice the degree of control over the in-rush current and the GATE ramp rate as the and values are changed thus providing for highly customizable turn-on characteristics.

In some scope shots although the C_{FILTER} shows a ramping in the absence of excessive displayed loading current the C_{FILTER} is responding to the other MAIN supply current that is not displayed.

All scope shots were taken from the ISL6112EVAL1Z with any component changes noted.

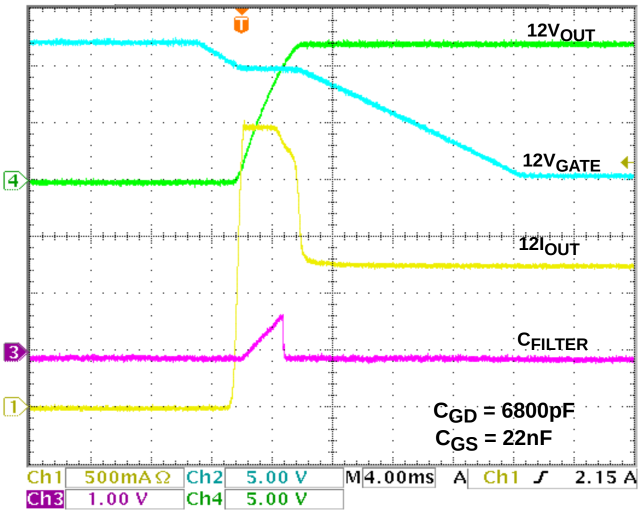


FIGURE 3. 12VMAIN START-UP R_{LOAD} = 10Ω, C_{LOAD} = 470µF

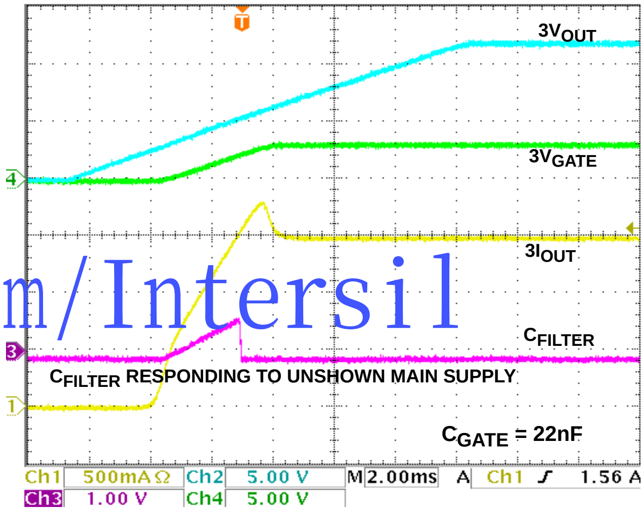


FIGURE 4. 3VMAIN START-UP R_{LOAD} = 2Ω, C_{LOAD} = 470µF

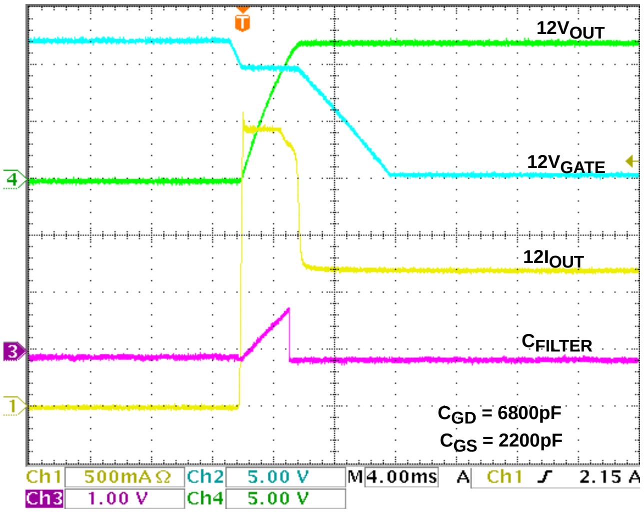


FIGURE 5. 12VMAIN START-UP RLOAD = 10Ω, C_{LOAD} = 470µF

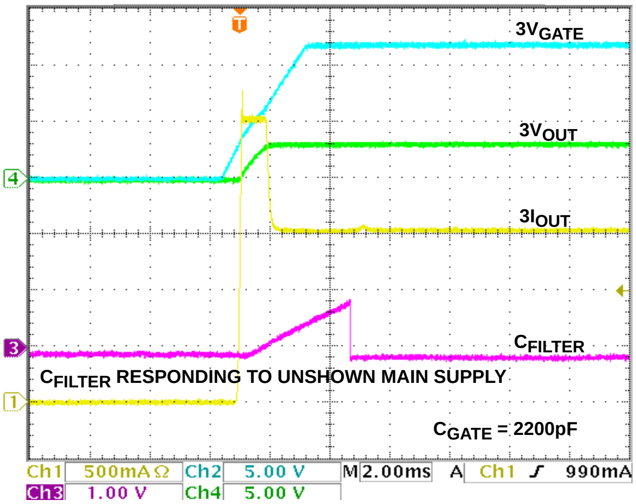


FIGURE 6. 3VMAIN START-UP $R_{LOAD} = 2\Omega$, $C_{LOAD} = 470\mu F$

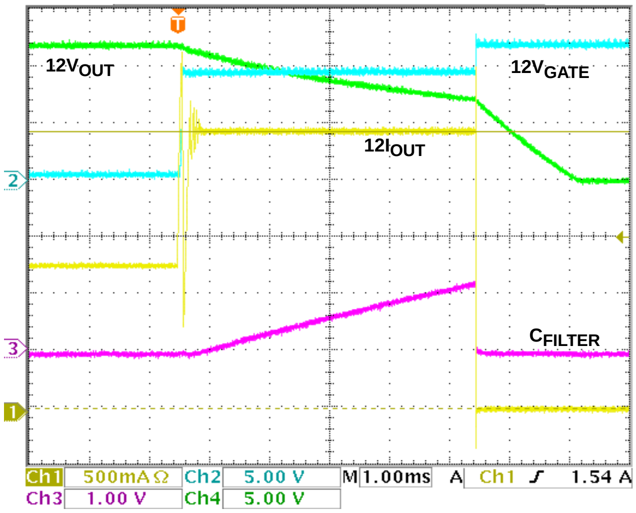


FIGURE 8. 12VMAIN CR AND SHUT-DOWN

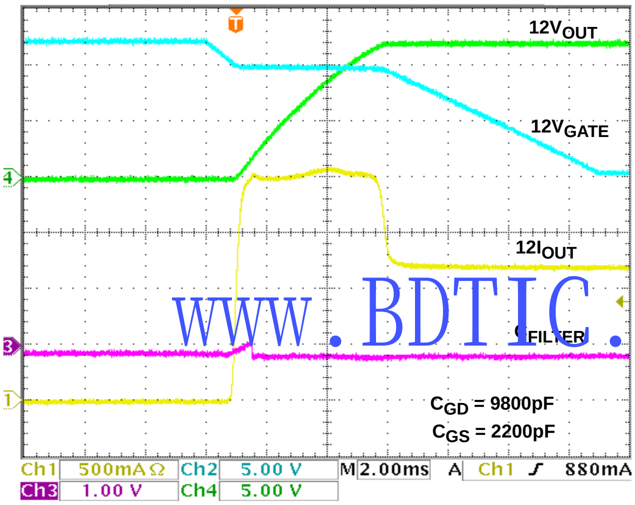


FIGURE 7. 12VMAIN START-UP $R_{LOAD} = 10\Omega$, $C_{LOAD} = 470\mu F$

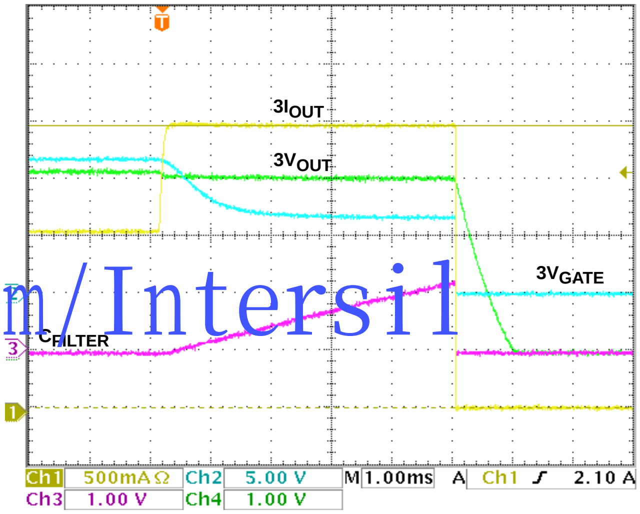


FIGURE 9. 3VMAIN CR AND SHUT-DOWN

Current Regulation (CR) Function

The ISL6112 provides a current regulation and limiting function that protects the input voltage supplies against excessive loads, including short circuits. When the current from any of a slots MAIN outputs exceeds the current limit threshold ($I_{LIM} = 50mV/R_{SENSE}$) for a duration greater than t_{FILTER}, the isolation protection is tripped and both related MAIN supplies are shut off, as shown in Figures 8 and 9. Should the load current cause a MAIN outputs V_{SENSE} to exceed V_{THFAST}, the outputs are immediately shut off with no t_{FILTER} delay, as shown in Figures 10 and 11.

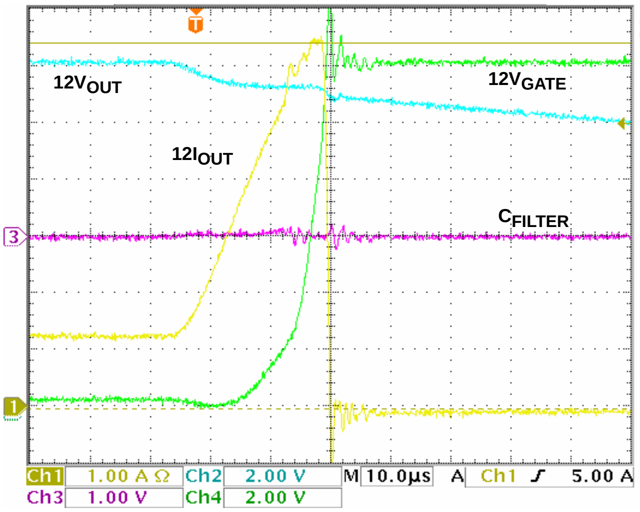


FIGURE 10. 12VMAIN WOC SHUT-DOWN

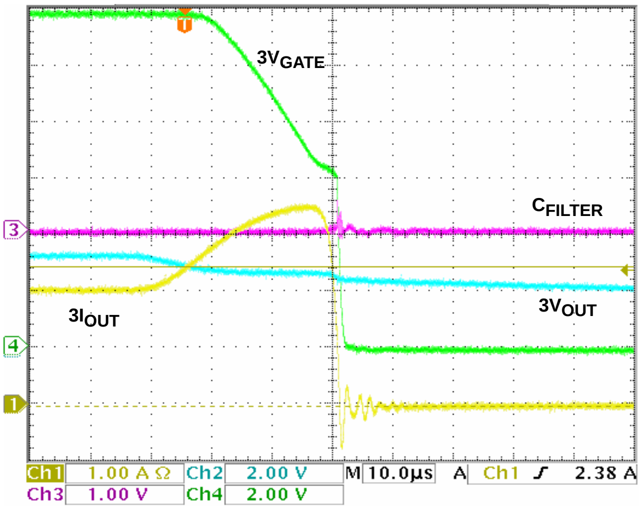


FIGURE 11. 3VMAIN WOC SHUT-DOWN

The VAUX outputs have a different isolation protection function. The VAUX isolation circuit does not incorporate a fast-trip detector, instead they regulate the output current into a fault to avoid exceeding their operating current limit. The protection circuit will trip due to an overcurrent on VAUX when the programmable CR duration timer, t_{FILTER} expires. This use of the t_{FILTER} timer prevents the circuit from tripping prematurely due to brief current transients. See Figures 12 and 13 for illustrations of the VAUX protection performance into a slight OC and more severe OC condition respectively. The ISL6112 AUX current control responds proportionally to the severity of the OC condition resulting in faster VAUX pull-down and current regulation until t_{FILTER} has expired.

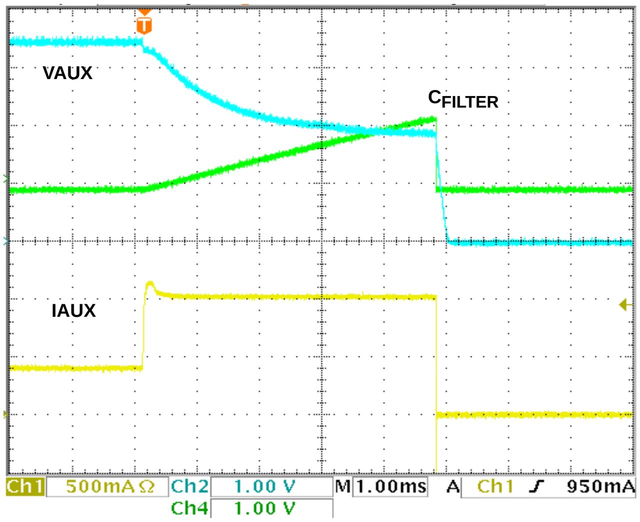


FIGURE 12. VAUX OC REGULATION AND SHUT-DOWN

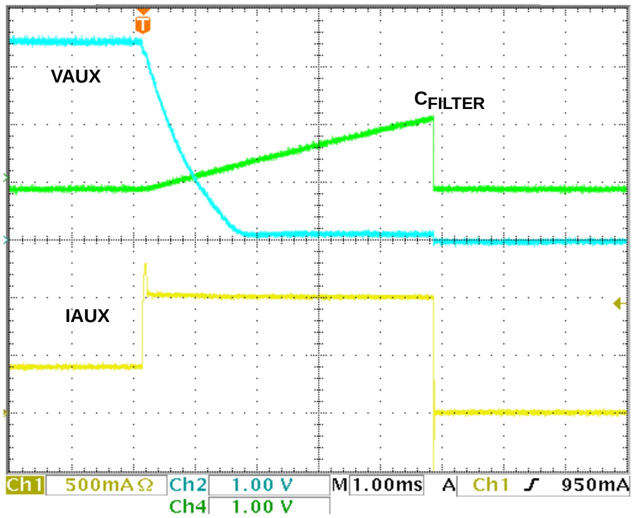


FIGURE 13. VAUX WOC REGULATION AND SHUT-DOWN

Following a fault condition, the outputs can be turned on again via the ON inputs (if the fault occurred on one of the MAIN outputs), via the AUXEN inputs (if the fault occurred on the AUX outputs), or by cycling both ON and AUXEN (if faults occurred on both the MAIN and AUX outputs). A fault condition can alternatively be cleared under SMI control of the ENABLE bits in the CNTRL registers (See “Control Register Bits D[1:0]” on page 19). When the circuit protection trips, $\overline{\text{FAULT}}$ will be asserted if the outputs were enabled through the Hot-Plug Interface inputs. If SMI is enabled, $\overline{\text{INT}}$ will be asserted (unless interrupts are masked). Note that $\overline{\text{INT}}$ is deasserted by writing a Logic 1 back into the respective fault bit position(s) in the STAT register or the “Common Status Register (CS) 8-Bits, Read/Write” on page 23.

The ISL6112 current regulation duration (t_{FILTER}) is individually set for each slot by an external capacitor at the CFILTER pin to GND. Once the CR mode is entered, the external cap is charged with a 2.5µA current source to 1.25V. Once this threshold has been reached, the IC then turns-off only the related faulted output(s), either both of the MAIN (external FETs) and or the AUX (internal FET) and sets the $\overline{\text{FAULT}}$ output low. For a desired t_{FILTER}, the value for C_{FILTER} is given by Equation 4:

$$C_{FILTER} = \frac{\text{nominal } t_{FILTER}}{500\text{k}\Omega} \qquad \text{(EQ. 4)}$$

where 500kΩ is the nominal V_{FILTER}/nominal I_{FILTER} and where t_{FILTER} is the desired response time with the values for I_{FILTER} and V_{FILTER} being found in the “Electrical Specifications Table” on page 6. See Table 2 for nominal t_{FILTER} times for given C_{FILTER} cap values.

For the ISL6112, there is a minimum t_{FILTER} consideration since the ISL6112 has its CR feature invoked as it turns-on the FETs into the load. There is a maximum bulk capacitance specified for each power level supported that needs to be charged at the CR limit. This in-rush current time must be considered when determining the t_{FILTER} duration.

TABLE 2.

NOMINAL t_{FILTER} DURATION	
C_{FILTER} CAPACITANCE (µF)	TIME (ms)
Open	0.01
0.01	5
0.022	11
0.047	24
0.1	50

NOTE: Nominal CR_DUR = C_{FILTER} cap (µF) * 500kΩ.

Power-Down Cycle

When a slot is turned off either under HPI or SMI control , internal discharge FETs are connected to the output load providing a discharge path for load capacitance connected to the part's outputs ensuring that the outputs are pulled to GND. This is a compliancy requirement if a replacement add in card will be inserted into the slot.

Thermal Shutdown

The internal VAUX MOSFETs are protected against damage not only by current limiting, but by a dual-mode over-temperature protection scheme as well. Each slot controller on the ISL6112 is thermally isolated from the other. Should an overcurrent condition raise the junction temperature of one slot's controller and pass elements to +140°C, all of the outputs for that slot (including VAUX) will be shut off and the slots $\overline{\text{FAULT}}$ output will be asserted. The other slots operating condition will remain unaffected. However, should the ISL6112's die temperature exceed +160°C, both slots (all outputs, including VAUXA and VAUXB) will be shut off, whether or not a current limit condition exists. A +160°C over-temperature condition additionally sets the over-temperature bit (OT_INT) in the "Common Status Register (CS) 8-Bits, Read/Write" on page 23.

$\overline{\text{PWRGD}}$ Outputs

The ISL6112 has two $\overline{\text{PWRGD}}$ outputs, one for each slot. These are open-drain, active-low outputs that require an external pull-up resistor to VSTBY. Each output is asserted when a slot has been enabled and has successfully begun delivering power to its respective +12V, +3.3V, and VAUX outputs. An equivalent logic diagram for $\overline{\text{PWRGD}}$ is shown in Figure 14.

$\overline{\text{FORCE\_ON}}$ Inputs

These level-sensitive, active-low inputs are provided to facilitate designing or debugging systems using the ISL6112. Asserting $\overline{\text{FORCE\_ON}}$ will turn on all three of the respective slot's outputs (12MAIN, 3MAIN, and VAUX), while specifically defeating all overcurrent and short circuit protections, and on-chip thermal protection for the VAUX supplies. Additionally, asserting $\overline{\text{FORCE\_ON}}$ will disable all of the input and output UVLO protections, with the sole exception of the VSTBY input UVLO.

Asserting $\overline{\text{FORCE\_ON}}$ will cause the slot $\overline{\text{PWRGD}}$ and $\overline{\text{FAULT}}$ outputs to enter their open-drain state. Additionally, there are two SMBus accessible register bits (See Control Register Bit D[2] in Tables 5 and 7), which can be set to disable the corresponding slot's $\overline{\text{FORCE\_ON}}$ pins. This allows system software to prevent these hardware overrides from being inadvertently activated during normal use. When not used, each $\overline{\text{FORCE\_ON}}$ pin can be connected to VSTBY using an external pull-up resistor or simply shorted to VSTBY.

General Purpose Input (GPI) Pins

Two pins on the ISL6112 are available for use as GPI pins. The logic state of each of these pins can be determined by polling Bits [4:5] of Common Status Register. Both of these inputs are compliant to 3.3V. If GPI is unused, connect each to GND.

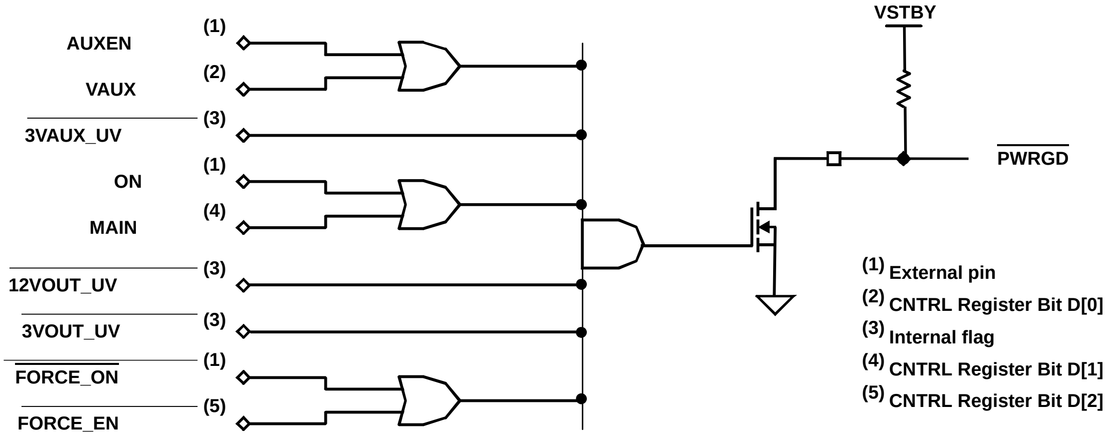


FIGURE 14. $\overline{\text{PWRGD}}$ LOGIC DIAGRAM

Timing Diagrams

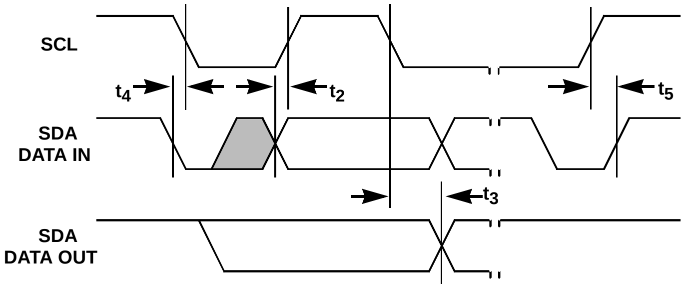
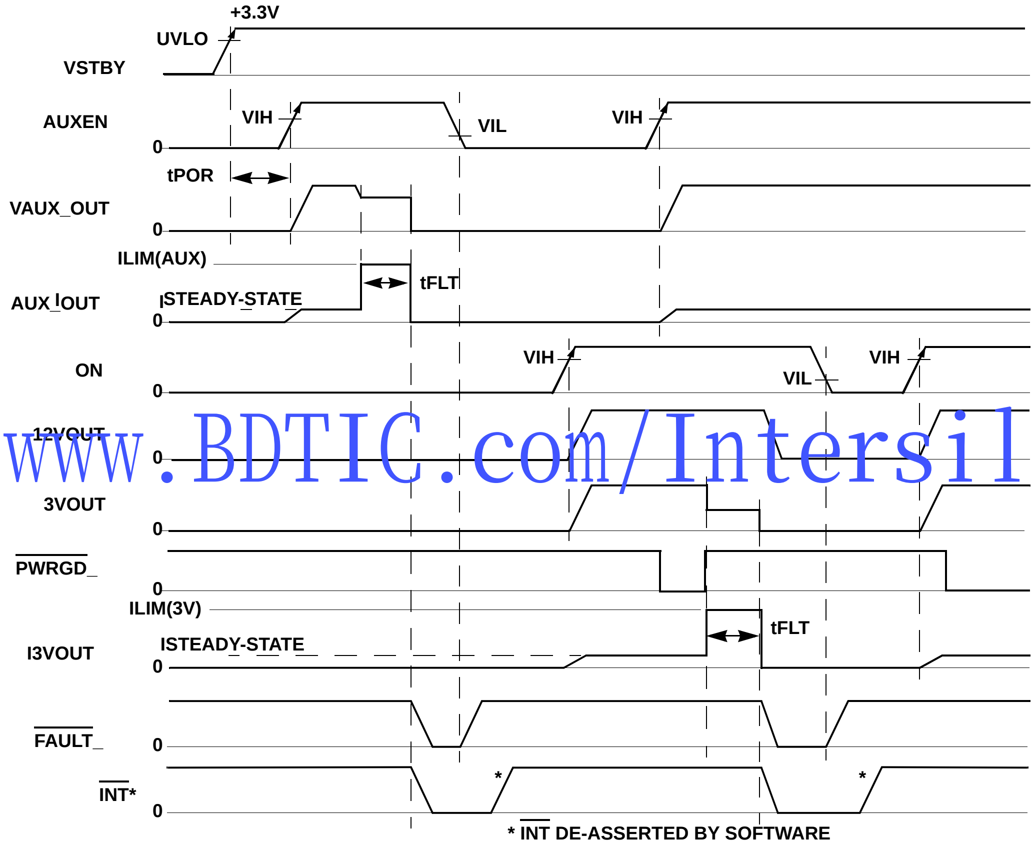


FIGURE 15. SMBUS TIMING



* INT DE-ASSERTED BY SOFTWARE

FIGURE 16. HOT-PLUG INTERFACE OPERATION

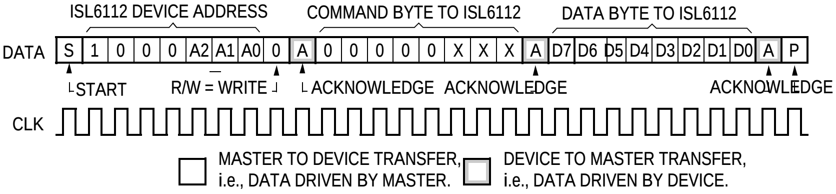


FIGURE 17. WRITE_BYTE PROTOCOL

Timing Diagrams (Continued)

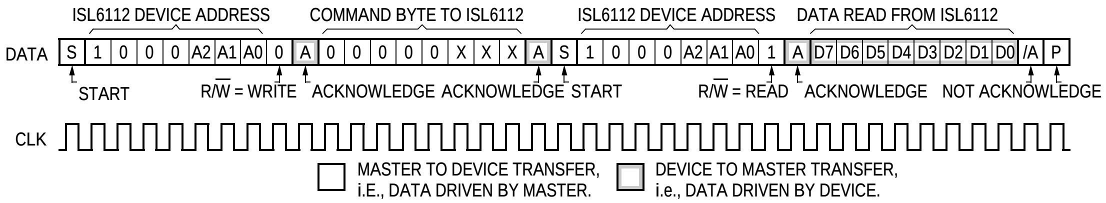


FIGURE 18. READ_BYTE PROTOCOL

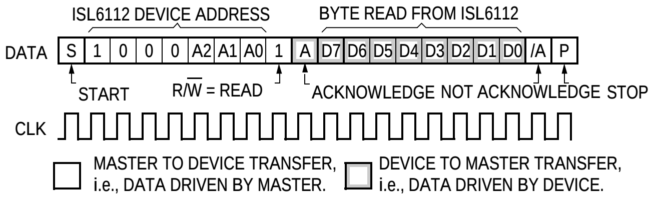


FIGURE 19. RECEIVE_BYTE PROTOCOL

Hot-Plug Interface (HPI)

Once the input supplies are above their respective UVLO thresholds, the Hot-Plug Interface can be utilized for power control by enabling the control input pins (AUXEN and ON) for each slot. In order for the ISL6112 to switch on the VAUX supply for either slot, the AUXEN control must be enabled after the power-on-reset delay, t_{POR} (typically, 250µs), has elapsed.

System Management Interface (SMI)

The ISL6112's System Management Interface uses the Read_Byte and Write_Byte subset of the SMBus protocols to communicate with its host via the System Management Interface bus. The $\overline{\text{INT}}$ output signals the controlling processor that one or more events need attention, if an interrupt-driven architecture is used. Note that the ISL6112 does not participate in the SMBus Alert Response Address (ARA) portion of the SMBus protocol.

Fault Reporting and Interrupt Generation

SMI ONLY CONTROL APPLICATIONS

In applications where the ISL6112 is controlled only by the SMI, ON and AUXEN are connected to GND and the $\overline{\text{FORCE\_ON}}$ pins are connected to VSTBY either as shown in Figure 1 or shorted. In these cases, the ISL6112's $\overline{\text{FAULT}}$ outputs and STATUS Register Bit D[7] (FAULT) are not activated as fault status is determined by polling STATUS Register Bits D[4], D[2], D[0] and CS (Common Status) Register Bits D[2:1]. Individual fault bits in STAT and CS registers are asserted after power-on-reset when:

- Either or both CNTRL Register Bits D[1:0] are asserted, AND
- 12VIN, 3VIN, or VSTBY input voltage is lower than its respective ULVO threshold, OR
- The fast OC circuit isolation protection has tripped, OR
- The slow OC circuit isolation protection has tripped AND its filter time-out has expired, OR
- The slow OC circuit isolation protection has tripped AND Slot die temperature > +140°C, OR
- The ISL6112's global die temperature > +160°C

Once asserted, to clear any one or all STATUS Register Bits D[4], D[2], D[0] and/or CS Register Bits D[2], D[1], a software subroutine can perform an “echo reset” where a Logical “1” is written back to those register bit locations that have indicated a fault. This method of “echo reset” allows data to be retained in the STATUS and/or CS registers until such time as the system is prepared to operate on that data.

The ISL6112 can operate in interrupt mode or polled mode. For interrupt-mode operation, the open-drain, active-LOW $\overline{\text{INT}}$ output signal is activated after power-on-reset if the INTMSK bit (CS Register Bit D[3]) has been reset to Logical “0”. Once activated, the $\overline{\text{INT}}$ output is asserted by any one of the fault conditions previously listed and deasserted when one or all STAT Register Bits D[4], D[2], D[0] and/or CS Register Bits D[2], D[1] are reset upon the execution of an SMBus “echo reset” WRITE_BYTE cycle. For polled-mode operation, the INTMSK bit should be set to Logical “1,” thereby inhibiting $\overline{\text{INT}}$ output pin operation.

For those SMI control applications where the FORCE_ON inputs are needed for diagnostic purposes, the FORCE_ON inputs must be enabled; that is, CNTRL Register Bit D[2] should read Logical “0.” Once FORCE_ON inputs are asserted, all output voltages are present with all circuit protection features disabled, including over-temperature protection on VAUX outputs. To inhibit FORCE_ON operation, a Logical “1” shall be written to the CNTRL Register Bit D[2] location(s)

HPI-ONLY CONTROL APPLICATIONS

In applications where the ISL6112 is controlled only by HPI, SMBus signals SCL, SDA, and INT signals are connected to VSTBY as shown in Figure 1. In this configuration, the ISL6112’s FAULT outputs are activated after power-on-reset and become asserted when:

Either or both external ON and AUXEN input signals are asserted, AND

- 12VIN, 3VIN, or VSTBY input voltage is lower than its respective ULVO threshold, OR
- The fast OC circuit isolation protection has tripped, OR
- The slow OC circuit isolation protection has tripped AND its filter time-out has expired, OR
- The slow OC circuit isolation protection has tripped AND Slot die temperature > +140°C, OR.
- The ISL6112’s global die temperature > +160°C

In order to clear FAULT outputs once asserted, either or both ON and AUXEN input signals must be deasserted. Please see FAULT pin description for additional information. If the FORCE_ON inputs are used for diagnostic purposes, both FAULT and PWRGD outputs are deasserted once FORCE_ON inputs are asserted.

Serial Port Operation

The ISL6112 uses standard SMBus Write_Byte and Read_Byte operations for communication with its host. The SMBus Write_Byte operation involves sending the devices target address, with the R/W bit (LSB) set to the low (write) state, followed by a command byte and a data byte. The SMBus Read_Byte operation is similar, but is a composite write and read operation: the host first sends the devices target address followed by the command byte, as in a write operation. A new “Start” bit must then be sent to the ISL6112, followed by a repeat of the device address with the R/W bit set to the high (read) state. The data to be read from the part may then be clocked out. There is one exception to this rule: If the location latched in the pointer register from the last write operation is known to be correct (i.e., points to the desired register within the ISL6112), then the “Receive_Byte” procedure may be used. To perform a Receive_Byte operation, the host sends an address byte to select the target ISL6112, with the R/W bit set to the high (read) state, and then retrieves the data byte. Figures 17, 18 and 19 show the formats for these data read and data write procedures.

The Command Register is eight bits (one byte) wide. This byte carries the address of the ISL6112’s register to be operated upon. The command byte values corresponding to the various ISL6112 register addresses are shown in Table 4. Command byte values other than 0000 $0XXX_b = 00_h – 07_h$ are reserved and should not be used.

ISL6112 SMBus Address Configuration

The ISL6112 responds to its own unique SMBus address, which is assigned using A2, A1, and A0. These represent the 3 LSBs of its 7-bit address, as shown in Table 3. These address bits are assigned only during power-up of the VSTBY supply input. These address bits allow up to eight ISL6112 devices in a single system. These pins are either grounded or left unconnected to specify a logical 0 or logical 1, respectively. A pin designated as a logical 1 may also be pulled up to VSTBY.

TABLE 3. ISL6112 SMBUS ADDRESSING

INPUTS			ISL6112 DEVICE ADDRESS	
A2	A1	A0	BINARY	HEX
0	0	0	1000 000X*b	80h
0	0	1	1000 001Xb	82h
0	1	0	1000 010Xb	84h
0	1	1	1000 011Xb	86h
1	0	0	1000 100Xb	88h
1	0	1	1000 101Xb	8Ah
1	1	0	1000 110Xb	8Ch
1	1	1	1000 111Xb	8Eh

* Where X = “1” for READ and “0” for WRITE

ISL6112 Register Set and Programmer’s Model

TABLE 4. ISL6112 REGISTER ADDRESSES

TARGET REGISTER		COMMAND BYTE VALUE		POWER-ON DEFAULT
LABEL	**DESCRIPTION**	**READ**	**WRITE**	
CNTRLA	Control Register Slot A	02h	02h	00h
CNTRLB	Control Register Slot B	03h	03h	00h
STATA	Slot A Status	04h	04h	00h
STATB	Slot B Status	05h	05h	00h
CS	Common Status Register	06h	06h	xxxx 0000b
Reserved	Reserved/Do Not Use	07h - FFh	07h - FFh	Undefined

Detailed Register Descriptions

Control Register, Slot A (CNTRLA)
8-Bits, Read/Write

TABLE 5. CONTROL REGISTER, SLOT A (CNTRLA)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
read-only	read-only	read only	read only	read-only	read/write	read/write	read/write
AUXAPG	MAINAPG	Reserved	Reserved	Reserved	FORCE_A ENABLE	MAINA	VAUXA

BIT(s)	FUNCTION	OPERATION
AUXAPG	AUX output power-good status, Slot A	1 = Power-is-Good (VAUXA Output is above its UVLO threshold)
MAINAPG	MAIN output power-good status, Slot A	1 = Power-is-Good (MAINA Outputs are above their UVLO thresholds)
D[5]	Reserved	Always read as zero
D[4]	Reserved	Always read as zero
D[3]	Reserved	Always read as zero
FORCE_A ENABLE	Allows or inhibits the operation of the FORCE_ONA input pin	0 = FORCE_ONA is enabled 1 = FORCE_ONA is disabled
MAINA	MAIN enable control, Slot A	0 = Off, 1 = On
VAUXA	VAUX enable control, Slot A	0 = Off, 1 = On

Power-Up Default Value: $0000\ 0000_b = 00_h$
Read Command_Byte Value (R/W): $0000\ 0010_b = 02_h$

The power-up default value is 00_h. Slot is disabled upon power-up, i.e., all supply outputs are off.

NOTES:

6. The state of the PWRGDA pin is the logical AND of the values of the AUXAPG and the MAINAPG bits, except when FORCE_ONA is asserted. If FORCE_ONA is asserted (the pin is pulled low), and FORCE_AENABLE is set to a logic zero, the PWRGDA pin will be unconditionally forced to its open-drain (“Power Not Good”) state.
7. The values of the MAINAPG and AUXAPG register bits are not affected by FORCE_ONA, but will instead continue to read as high if power is “Good,” and as low if the conditions which indicate that power is good are not met.

Status Register Slot A (STATUSA)
8-Bits, Read-Only

TABLE 6. STATUS REGISTER, SLOT A (STATA)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
read-only	read-only	read-only	read/write	read-only	read/write	read-only	read/write
FAULTA	MAINA	VAUXA	VAUXAF	Reserved	12VAF	Reserved	3VAF

BIT(s)	FUNCTION	OPERATION
FAULTA	FAULT Status - Slot A	1 = Fault pin asserted (FAULTA pin is LOW) 0 = Fault pin deasserted (FAULTA pin is HIGH) See Notes 8, 9, and 10.
MAINA	MAIN Enable Status - Slot A	Represents the actual state (on/off) of the two Main Power outputs for Slot A (+12V and +3.3V) 1 = Main Power ON 0 = Main Power OFF
VAUXA	VAUX Enable Status - Slot A	Represents the actual state (on/off) of the Auxiliary Power output for Slot A 1 = AUX Power ON 0 = AUX Power OFF
VAUXAF	Overcurrent Fault: VAUXA supply	1 = Fault 0 = No fault
D[3]	Reserved	Always read as zero
12VAF	Overcurrent Fault: +12V supply	1 = Fault 0 = No fault
D[1]	Reserved	Always read as zero
3VAF	Overcurrent Fault: 3.3V supply	1 = Fault 0 = No fault

Power-Up Default Value:	$0000\ 0000_b = 00_h$
Command_Byte Value (R/W):	$0000\ 0100_b = 04_h$

The power-up default value is 00_h. Both slots are disabled upon power-up, i.e., all supply outputs are off. In response to an overcurrent fault condition, writing a logical 1 back into the active (or set) bit position will clear the bit and deassert INT. The status of the FAULTA pin is not affected by reading the Status Register or by clearing active status bits.

NOTES:

8. If FAULTA has been set by an overcurrent condition on one or more of the MAIN outputs, the ONA input must go LOW to reset FAULTA. If FAULTA has been set by a VAUXA overcurrent event, the AUXENA input must go LOW to reset FAULTA. If an overcurrent has occurred on both a MAIN output and the VAUX output of slot A, both ONA and AUXENA of the slot must go low to reset FAULTA.
9. Neither the FAULTA bits nor the FAULTA pins are active when the ISL6112 power paths are controlled by the System Management Interface. When using SMI power path control, AUXENA and ONA pins for that slot must be tied to GND.
10. If FORCE_ONA is asserted (low), the FAULTA pin will be unconditionally forced to its open-drain state. Note, though, that the value in the FAULTA register bit is not affected by FORCE_ONA, but will instead continue to read as a high if no faults are present on Slot A, and as a low if any fault conditions exist, which would disable Slot A if FORCE_ONA was not asserted.

Control Register, Slot B (CNTRLB)
8-Bits, Read/Write

TABLE 7. CONTROL REGISTER, SLOT B (CNTRLB)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
read-only	read-only	read only	read only	read-only	read/write	read/write	read/write
AUXBPG	MAINBPG	Reserved	Reserved	Reserved	$\overline{\text{FORCE\_B}}$ ENABLE	MAINB	VAUXB

BIT(s)	FUNCTION	OPERATION
AUXBPG	AUX output power-good status, Slot B	1 = Power-is-Good (VAUXB Output is above its UVLO threshold)
MAINBPG	MAIN output power-good status, Slot B	1 = Power-is-Good (MAINB Outputs are above their UVLO thresholds)
D[5]	Reserved	Always read as zero
D[4]	Reserved	Always read as zero
D[3]	Reserved	Always read as zero
$\overline{\text{FORCE\_B}}$ ENABLE	Allows or inhibits the operation of the $\overline{\text{FORCE\_ONB}}$ input pin	0 = $\overline{\text{FORCE\_ONB}}$ is enabled 1 = $\overline{\text{FORCE\_ONB}}$ is disabled
MAINB	MAIN enable control, Slot B	0 = Off, 1 = On
VAUXB	VAUX enable control, Slot B	0 = Off, 1 = On

Power-Up Default Value:	$0000\ 0000_b = 00_h$
Command_Byte Value (R/W):	$0000\ 0011_b = 03_h$

The power-up default value is 00_h. Slot is disabled upon power-up, i.e., all supply outputs are off.

NOTES:

11. The state of the $\overline{\text{PWRGDB}}$ pin is the logical AND of the values of the AUXBPG and the MAINBPG bits, except when $\overline{\text{FORCE\_ONB}}$ is asserted. If $\overline{\text{FORCE\_ONB}}$ is asserted (the pin is pulled low), and $\overline{\text{FORCE\_BENABLE}}$ is set to a logic zero, the $\overline{\text{PWRGDB}}$ pin will be unconditionally forced to its open-drain (“Power Not Good”) state.
12. The values of the MAINBPG and AUXBPG register bits are not affected by $\overline{\text{FORCE\_ONB}}$, but will instead continue to read as high if power is “Good,” and as low if the conditions, which indicate that power is good, are not met.

Status Register Slot B (STATB) 8-Bits, Read-Only

TABLE 8. STATUS REGISTER, SLOT B (STATB)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
read-only	read-only	read-only	read/write	read-only	read/write	read-only	read/write
FAULTB	MAINB	VAUXB	VAUXBF	Reserved	12VBF	Reserved	3VBF

BIT(s)	FUNCTION	OPERATION
FAULTB	FAULT Pin Status - Slot B	1 = Fault pin asserted ($\overline{\text{FAULTB}}$ pin is LOW) 0 = Fault pin deasserted ($\overline{\text{FAULTB}}$ pin is HIGH) See Notes 13, 14, and 15.
MAINB	MAIN Enable Status - Slot B	Represents the actual state (on/off) of the four Main Power outputs for Slot B (+12V and +3.3V) 1 = MAIN Power ON 0 = MAIN Power OFF
VAUXB	VAUX Enable Status - Slot B	Represents the actual state (on/off) of the Auxiliary Power output for Slot B 1 = AUX Power ON 0 = AUX Power OFF
VAUXBF	Overcurrent Fault: VAUXB supply	1 = Fault 0 = No fault
D[3]	Reserved	Always read as zero
12VBF	Over current Fault: +12V supply	1 = Fault 0 = No fault
D[1]	Reserved	Always read as zero
3VBF	Over current Fault: 3.3V supply	1 = Fault 0 = No fault

Power-Up Default Value: $0000\ 0000_h = 00_h$
Command_Byte Value (R/W): $0000\ 0101_b = 05_h$

The power-up default value is 00_h. Both slots are disabled upon power-up, i.e., all supply outputs are off. In response to an overcurrent fault condition, writing a logical 1 back into the active (or set) bit position will clear the bit and deassert $\overline{\text{INT}}$. The status of the $\overline{\text{FAULTB}}$ pin is not affected by reading the Status Register or by clearing active status bits.

NOTES:

13. If FAULTB has been set by an overcurrent condition on one or more of the MAIN outputs, the ONB input must go LOW to reset FAULTB. If FAULTB has been set by a VAUXB overcurrent event, the AUXENB input must go LOW to reset FAULTB. If an overcurrent has occurred on both a MAIN output and the VAUX output of slot B, both ONB and AUXENB of the slot must go low to reset FAULTB.
14. Neither the FAULTB bits nor the $\overline{\text{FAULTB}}$ pins are active when the ISL6112 power paths are controlled by the System Management Interface. When using SMI power path control, the AUXENB and ONB pins for that slot must be tied to GND.
15. If $\overline{\text{FORCE\_ONB}}$ is asserted (low), the $\overline{\text{FAULTB}}$ pin will be unconditionally forced to its open-drain state. Note, though, that the value in the FAULTB register bit is not affected by $\overline{\text{FORCE\_ONB}}$, but will instead continue to read as a high if no faults are present on Slot B, and as a low if any fault conditions exist which would disable Slot B if $\overline{\text{FORCE\_ONB}}$ was not asserted.

Common Status Register (CS)
8-Bits, Read/Write

TABLE 9. COMMON STATUS REGISTER (CS)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
read-write	read-write	read-only	read-only	read-write	read-write	read-write	read-only
Reserved	Reserved	GPI_B0	GPI_A0	INTMSK	UV_INT	OT_INT	Reserved

BIT(s)	FUNCTION	OPERATION
D[7]	Reserved	Always read as zero
D[6]	Reserved	Always read as zero
GPI_B0	General Purpose Input 0, Slot B	State of GPI_B0 pin
GPI_A0	General Purpose Input 0, Slot A	State of GPI_A0 pin
INTMSK	Interrupt Mask	0 = $\overline{\text{INT}}$ generation is enabled 1 = INT generation is disabled. The ISL6112 does not participate in the SMBus Alert Response Address (ARA) protocol
UV_INT	undervoltage Interrupt	0 = No UVLO fault 1 = UVLO fault Set whenever a circuit isolation protection fault condition occurs as a result of an undervoltage lockout condition on one of the main supply inputs. This bit is only set if a UVLO condition occurs while the ON pin is asserted or the MAIN control bits are set
OT_INT	over-temperature Interrupt	0 = Die Temp < +160°C. 1 = Fault: Die Temp > +160°C. Set if a fault occurs as a result of the ISL6112's die temperature exceeding +160°C
D[0]	Reserved	Undefined

Power-Up Default Value: $00000000_b = 00_h$
Command_Byte Value (R/W): $00000110_b = 06_h$

To reset the OT_INT and UV_INT fault bits, a logical 1 must be written back to these bits.

PCI-Express Application Recommendations

For each of the 3.3VMAIN and +12VMAIN supplies, the CR level is set by an external sense resistor value depending on the maximum specified power for the various PCI-Express connector and application implemented (X1, 10W or 25W; X4, X8, 25W; X16, 25W or 75W; and X16 Graphics -ATX, 150W). The power rating is a combination of both main and the optional auxiliary supplies. This sense resistor is a low ohmic standard value current sense resistor (one for each slot) and the voltage across this resistor is compared to a 50mV reference. Since the 3.3VMAIN supply is rated for 3A max across all slots regardless of size and power, the use of a 15mΩ sense resistor compared to the 50mV reference provides a nominal CR of 3.3A or 11% above the 3A max spec.

On the 12VMAIN, for a 10W connector, a 75mΩ sense resistor provides a nominal CR level of 0.66A, 32% above the 0.5A max spec; for a 25W connector, a 20mΩ sense resistor provides a nominal CR level of 2.5A, 19% above the 2.1A max specification; for a 75W connector a 8mΩ sense resistor provides a nominal CR level of 6.25A, 14% above the 5.5A max specification. The X16 Graphics-ATX 150W card is a special case in that, the 150W is provided by 2 slots, each providing up to a maximum of 75W from the 12VMAIN as this type of card does not consume 3.3VMAIN or AUX supply power. For each of the slots a 7mΩ sense resistor provides a nominal CR level of 7.1A, 14% above the 6.25A max spec.

The ISL6112 provides a best in class ±5% current regulation threshold spec over temperature for the MAIN supples providing the highest accuracy and lowest variability for this critical parameter. Table 10 provides recommended 12VMAIN sense resistor values for particular power levels.

TABLE 10.

NOMINAL CURRENT REGULATION LEVEL		
12VMAIN R_{SENSE} (mΩ)	12VMAIN CR (A)	PCI-E ADD IN BOARD POWER LEVEL SUPPORTED (W)
75	0.7	10
20	2.5	25
8	6.2	75
7	7	150

NOTE: CR Level = VTH_{ILIMIT}/R_{SENSE}.

Providing a nominal CR protection level above the maximum specified limits of the card ensures that the card is able to draw its maximum specified loads, and, in addition has enough headroom before a regulated current limiter is invoked to protect against transients and other events. This headroom margin can be adjusted up or down by utilizing differing values of sense resistor.

Using the ISL6112EVAL1Z Platform

Description and Introduction

The primary ISL6112 evaluation platform is shown in Figure 34 photographically and schematically on page 28. This evaluation board highlights a PCB layout that confines all necessary active and passive components in an area measuring 12mmx55mm. This width is smaller than the specified PCI-Express socket to socket spacing, allowing for intimate co-location of the load power control and the load itself.

Around the central highlighted layout are numerous labeled test points and configuration jumpers where there are node names such as AO(L/$\overline{R}$). The pin name outside the parentheses relates to the ISL6112. The ISL6113 and ISL6114 also use this evaluation platform as all three parts have a common pinout for the common pin functions. The pin names in parentheses are for them. The specific evaluation board as ordered and received will reflect the part number in the area below the Intersil logo either by label or silk screened lettering. For those pins not common across the ISL6112 and ISL6113, ISL6114, there is a matrix detailing the differences in the bottom left corner.

The ISL6112EVAL1Z is default provided in HPI mode with the clock shorted to ground.

After correctly biasing the evaluation platform as noted through the 6 banana jacks, on VSTBY first then the other MAIN supplies, in any order. With the appropriate signaling to the AUXEN and ON inputs, the user should see turn-on waveforms as shown previously. The addition of external current loading is necessary to demonstrate the OC and WOC response performance.

For demonstration of SMI operation the SCL and SDA inputs are in the top right quadrant of the evaluation board. The board's default address is configured as '000' via three jumpers located to the right labeled A0, A1, and A2. The HPI inputs need to be disabled as shown in Figure 1. Additional software to configure and control is needed. If necessary, there is a LabView based program available from the factory for demonstration of the ISL6112 functionality. User lab test hardware and instrument support is not available.

Caution: The ISL6113EVAL1Z, ISL6114EVAL1Z get very hot to the touch after operating it for a few minutes. The hottest areas are marked on the evaluation board.

Typical Performance Curves

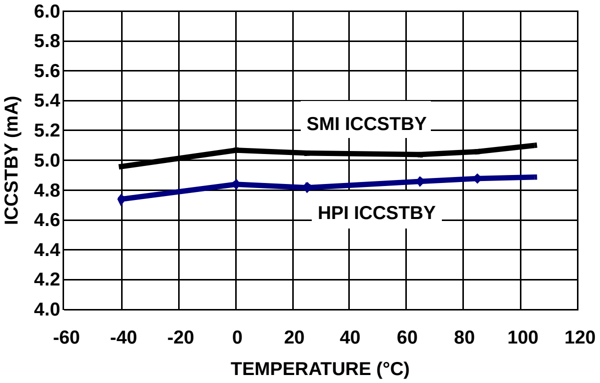


FIGURE 20. ICCSTBY CURRENT vs TEMPERATURE

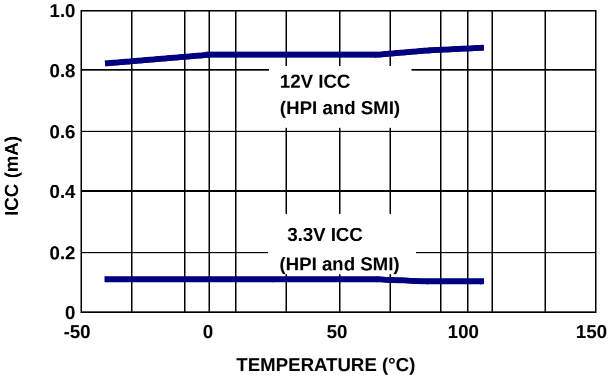


FIGURE 21. ICC CURRENT vs TEMERATURE

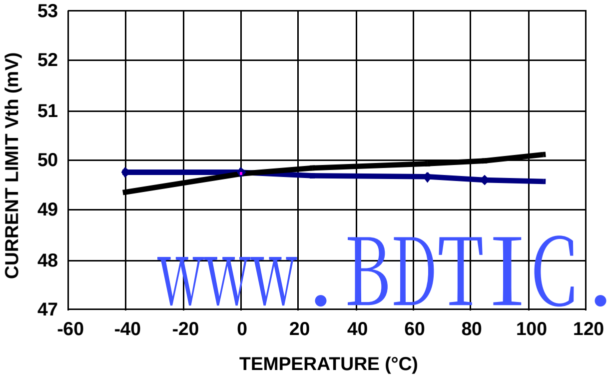


FIGURE 22. CURRENT LIMIT THRESHOLD VOLTAGE vs TEMPERATURE

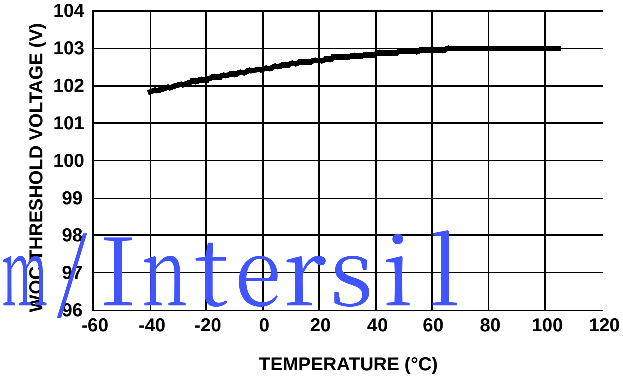


FIGURE 23. FAST TRIP THRESHOLD VOLTAGE vs TEMPERATURE

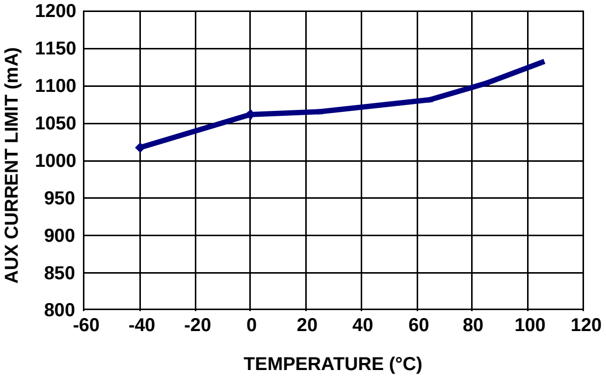


FIGURE 24. AUX. CURRENT LIMIT vs TEMPERATURE

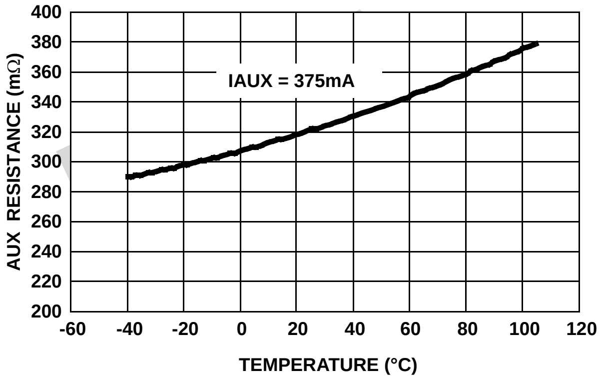


FIGURE 25. AUX $r_{DS(ON)}$ vs TEMPERATURE

Typical Performance Curves (Continued)

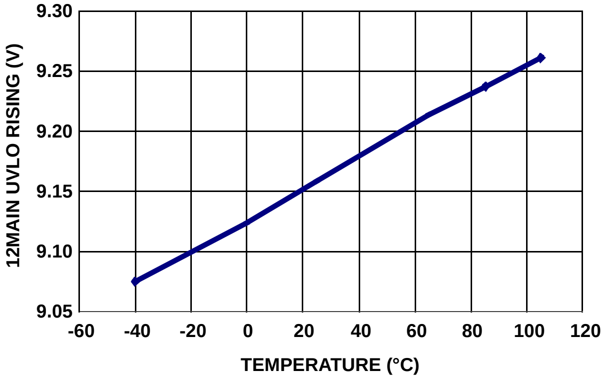


FIGURE 26. 12MAIN RISING UVLO THRESHOLD VOLTAGE vs TEMPERATURE

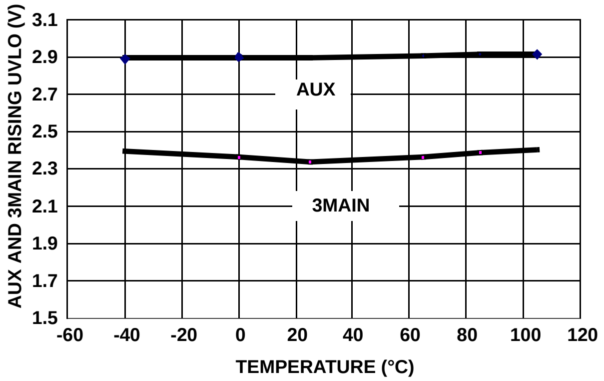


FIGURE 27. AUX AND 3.3MAIN RISING UVLO THRESHOLD VOLTAGE vs TEMPERATURE

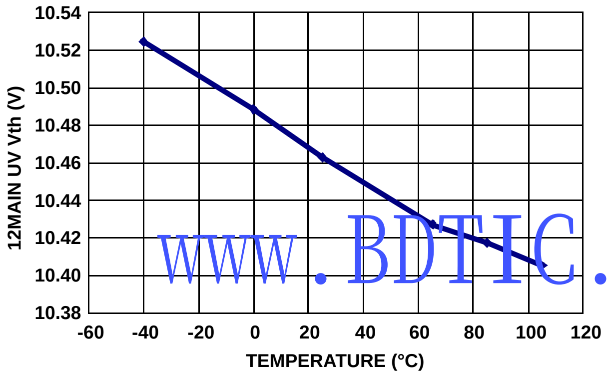


FIGURE 28. 12MAIN POWER GOOD THRESHOLD VOLTAGE vs TEMPERATURE

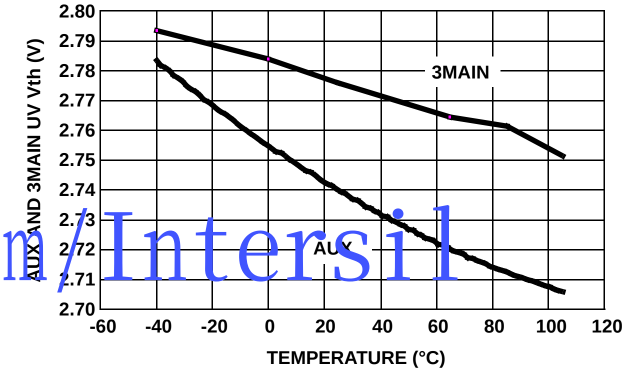


FIGURE 29. AUX AND 3MAIN POWER GOOD THRESHOLD VOLTAGE vs TEMPERATURE

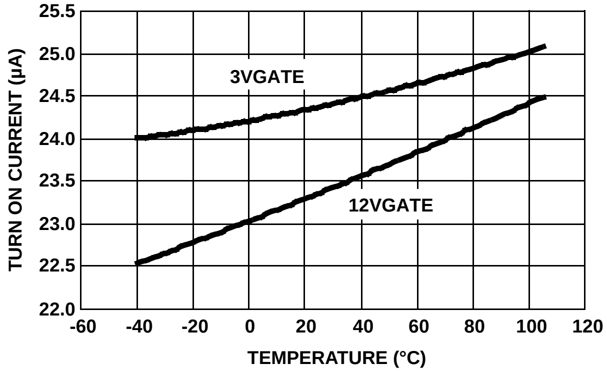


FIGURE 30. ISL6112 GATE TURN-ON CURRENT (ABS) vs TEMPERATURE

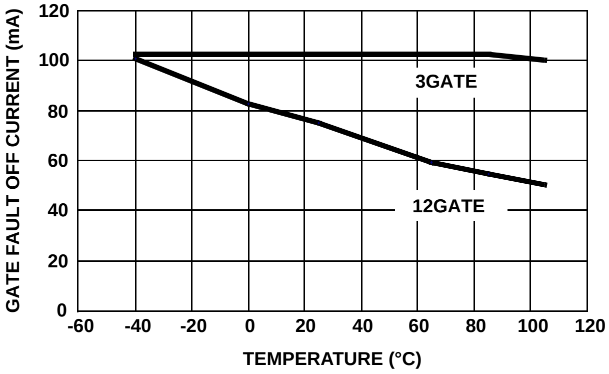


FIGURE 31. GATE FAULT OFF CURRENT (ABS) vs TEMPERATURE

Typical Performance Curves (Continued)

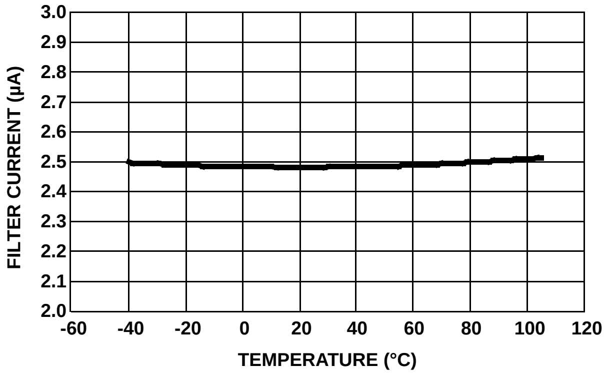


FIGURE 32. FILTER CHARGE CURRENT vs TEMPERATURE

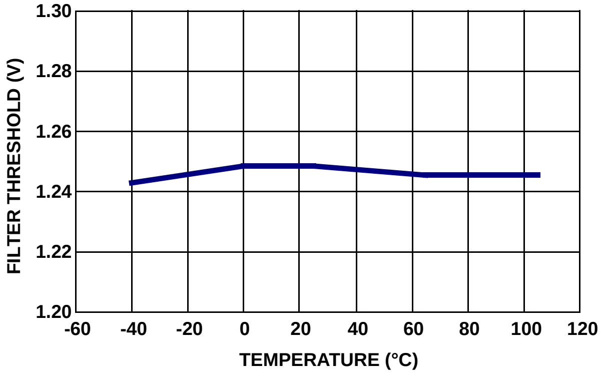


FIGURE 33. FILTER THRESHOLD VOLTAGE vs TEMPERATURE

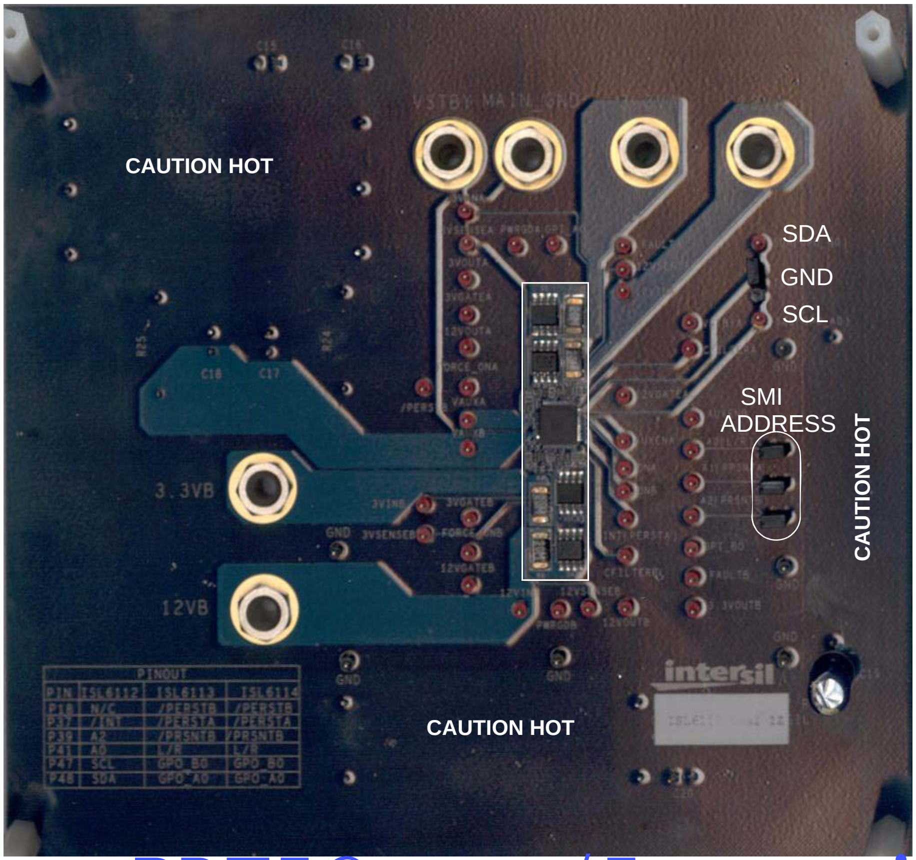
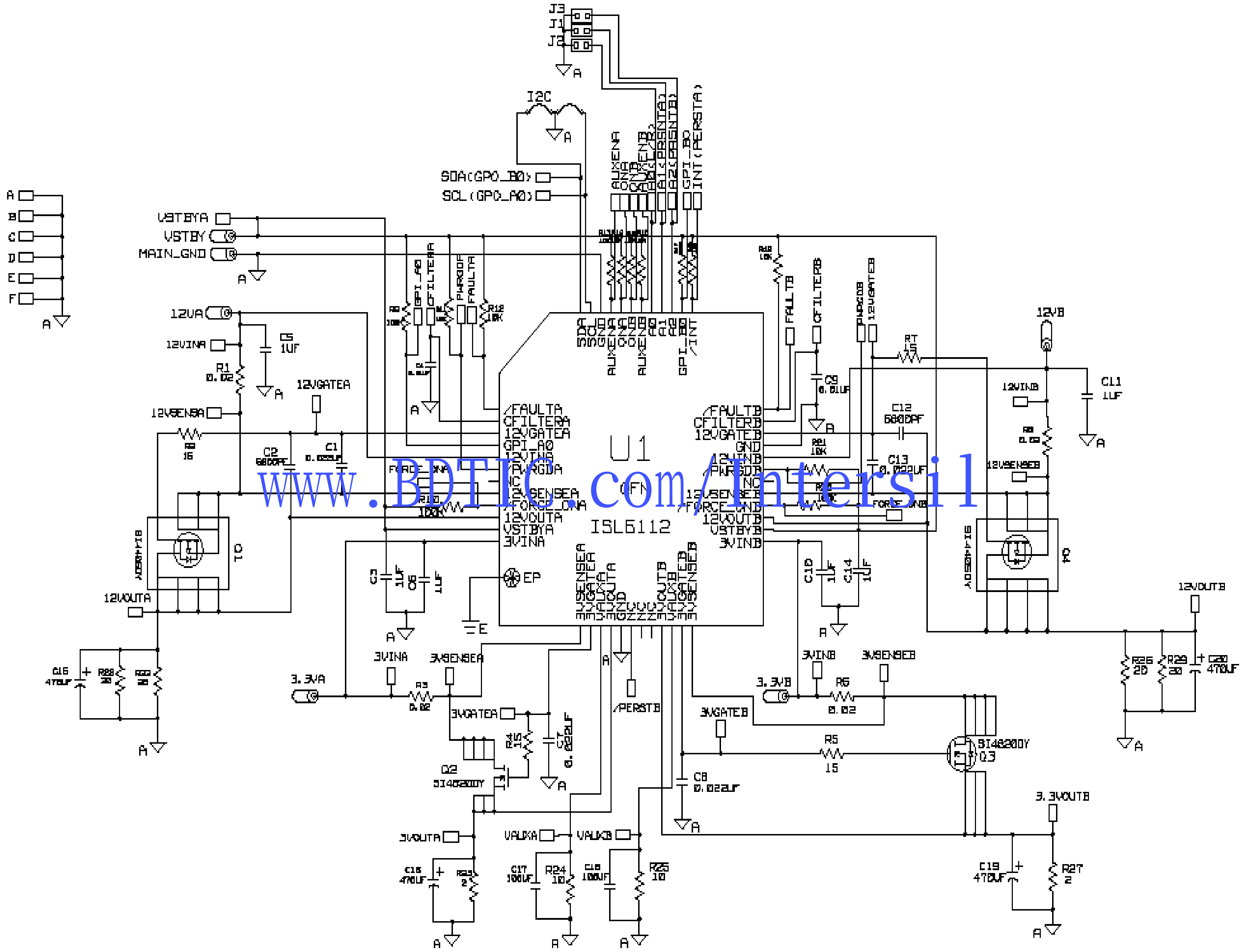


FIGURE 34. ISL6112EVAL1Z BOARD PHOTO

TABLE 11. ISL6112EVAL1Z BOARD COMPONENTS LISTING

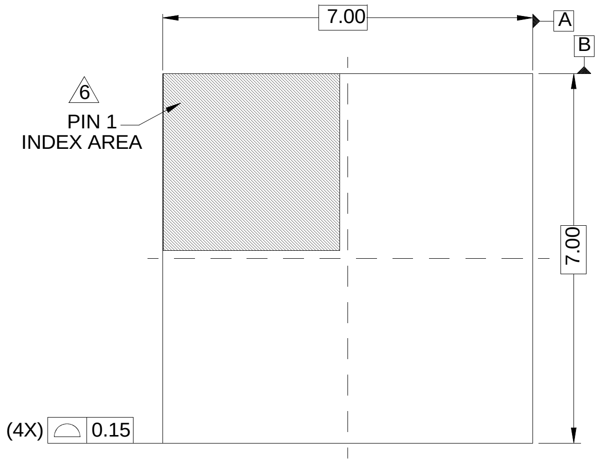
COMPONENT DESIGNATOR	COMPONENT FUNCTION	COMPONENT DESCRIPTION
U1	ISL6112	PCI- Express Dual Slot Hot Plug Controller
Q1, Q4	Voltage Rail Switches	SI4405DY or equivalent, P-Channel MOSFET
Q2, Q3	Voltage Rail Switches	SI4820DY or equivalent, N-Channel MOSFET
R1, R3, R6, R8	Current Sense Resistor	0.020Ω 1%, 2512
R9, R10, R17, R20	Pull up resistors on FORCEON and GPI Inputs	100kΩ, 0201
R11, R12, R13, 14, R15, R16, R18, 19, R21	I/O Pull up resistors	10kΩ, 0201
R2, R4, R5, R7	FET gate series resistance	15Ω, 0201
C1, C7, C8, C13	FET gate capacitance	22nF 10%, 16V, 0402
C3, C5, C6, C10, C11, C14	MAIN and VSTBY decoupling capacitance	1µF 10%, 6.3V, 0402
C2, C12	P-FET gate to drain capacitance	6.8nF 10%, 6.3V, 0201
C4, C9	CFILTER capacitance (5ms)	0.01µF 10%, 6.3V, 0201
R24, R25	AUX Load Resistance	10Ω 20%, 3W
C17, C18	AUX Load Capacitance	100µF 20%, 25V, Radial Electrolytic
R22, R26, R28, 29	12MAIN Load Resistance	20Ω 20%, 10W
R23, R27	3MAIN Load Resistance	2Ω 20%, 10W
C15, C16, C19, C20	12MAIN and 3MAIN Load Capacitance	470µF 20%, 16V, Radial Electrolytic


J3
J1
J2
I2C
SDA(GPO_B0)
SCL(GPO_A0)
AUXENA
ONA
ONB
AUXENB
A0(/CLR)
A1(PRSNTA)
A2(PRSNTB)
GPI_B0
INT(/PERSTA)
A
B
C
D
E
F
VSTBYA
VSTBY
MAIN_GND
12VA
12VINA
C5
1UF
R1
0.02
12VGATEA
12VSENSA
R8
15
C2
6800PF
C1
0.022UF
GPI_A0
CFILTERA
PWRGDA
FAULTA
R12
10K
FAULTB
CFILTERB
PWRGDB
12VGATEB
R10
10K
C9
0.01UF
RT
15
12VB
C11
1UF
12VINB
R6
0.02
12VSENSEB
C12
6800PF
C13
0.022UF
R21
10K
FORCE_ONA
FORCE_ONB
U1
QFN
ISL6112
SDA
SCL
GND
AUXENA
ONA
ONB
AUXENB
A0
A1
A2
GPI_B0
/INT
/FAULTA
CFILTERA
12VGATEA
GPI_A0
12VINA
PWRGDA
NC
12VSENSEA
/FORCE_ONA
12VOUTA
VSTBYA
3VINA
EP
/FAULTB
CFILTERB
12VGATEB
GND
12VINB
/PWRGDB
NC
12VSENSEB
/FORCE_ONB
12VOUTB
VSTBYB
3VINB
3VSENSEA
3VGATEA
VAUXA
3VOUTA
/PERST
3VOUTB
VAUXB
3VGATEB
3VSENSEB
SI4430DY
Q1
12VOUTA
C3
1UF
C6
1UF
E
C16
470UF
R23
R22
SI4430DY
Q4
12VOUTB
C10
1UF
C14
1UF
R26
20
R29
20
C20
470UF
3.3VA
3VINA
3VSENSEA
R3
0.02
3VGATEA
R4
15
C7
0.022UF
Q2
SI4420DY
/PERSTB
3VOUTA
C15
470UF
R25
2
VAUXA
C17
100UF
R24
10
VAUXB
C18
100UF
R25
10
3.3VB
3VINB
3VSENSEB
R6
0.02
3VGATEB
R5
15
SI4420DY
Q3
C8
0.022UF
3.3VOUTB
C19
470UF
R27
2
A

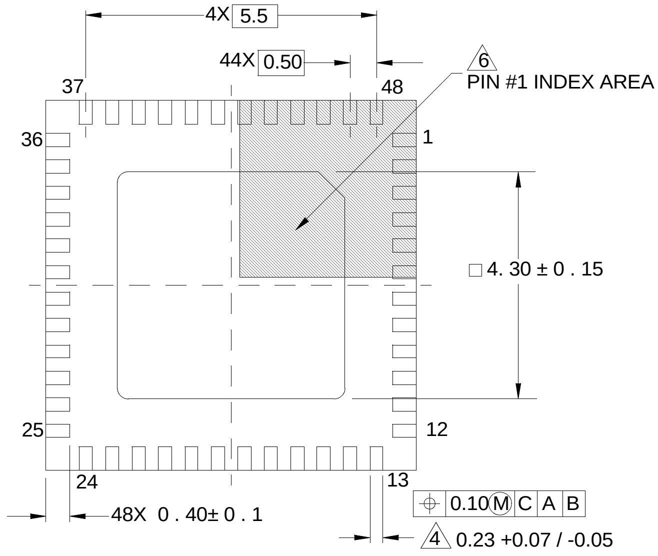
Package Outline Drawing

L48.7x7

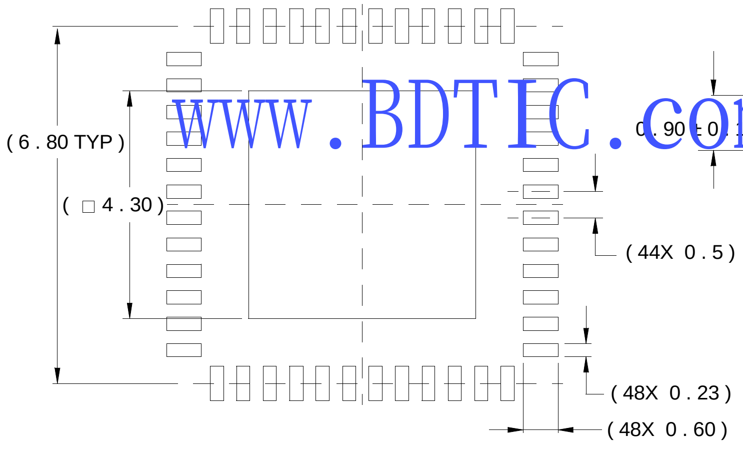
48 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 4, 10/06



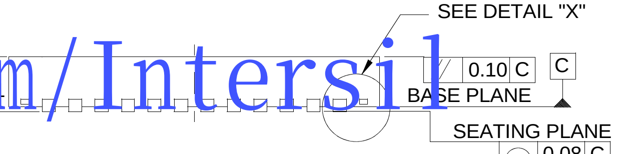
TOP VIEW



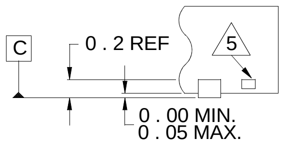
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW

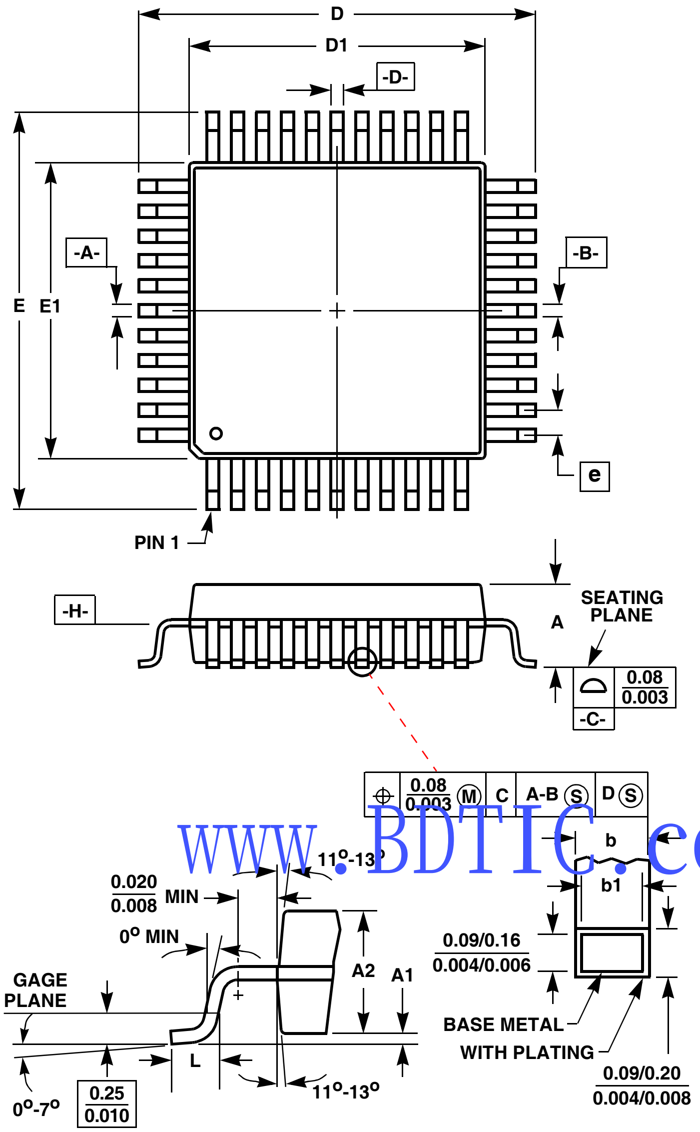


DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

Thin Plastic Quad Flatpack Packages (TQFP)



Q48.7x7 (JEDEC MS-026ABC ISSUE B)

48 LEAD THIN PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.005	0.05	0.15	-
A2	0.038	0.041	0.95	1.05	-
b	0.007	0.010	0.17	0.27	6
b1	0.007	0.009	0.17	0.23	-
D	0.350	0.358	8.90	9.10	3
D1	0.272	0.280	6.90	7.10	4, 5
E	0.350	0.358	8.90	9.10	3
E1	0.272	0.280	6.90	7.10	4, 5
L	0.018	0.029	0.45	0.75	-
N	48		48		7
e	0.020 BSC		0.50 BSC		-

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NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm (0.003 inch).
7. “N” is the number of terminal positions.