Data Sheet | August 2004 | FN6035.1

QFN Packaged, ±15kV ESD Protected, +3V to +5.5V, 150nA, 250kbps, RS-232 Transmitters/Receivers with Separate Logic Supply

The ISL4260E contains 3.0V to 5.5V powered RS-232 transmitters/receivers which meet EIA/TIA-232 and V.28/V.24 specifications, even at V_{CC} = 3.0V. Targeted applications are PDAs, Palmtops, and cell phones where the low operational, and even lower standby, power consumption is critical. Efficient on-chip charge pumps, coupled with a manual powerdown function reduces the standby supply current to a 150nA trickle. Tiny 5mm x 5mm **Quad Flat No-Lead (**QFN) packaging, and the use of small, low value capacitors ensure board space savings as well. Data rates greater than 250kbps are guaranteed at worst case load conditions.

The ISL4260E features a V_L pin that adjusts the logic pin (see Pin Descriptions table) output levels and input thresholds to values compatible with the V_{CC} powering the external logic (e.g., a UART).

The single pin powerdown function ($\overline{SHDN}$ = 0) disables all the receiver and transmitter outputs, while shutting down the charge pump to minimize supply current drain.

Table 1 summarizes the features of the ISL4260E, while Application Note AN9863 summarizes the features of each device comprising the 3V RS-232 family.

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Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
ISL4260EIR	-40 to 85	32 Lead QFN	L32.5x5
ISL4260EIRZ (See Note)	-40 to 85	32 Lead QFN (Pb-free)	L32.5x5

*Add “-T” suffix to part number for tape and reel packaging.

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

Features

- Available in Near Chip Scale QFN (5mmx5mm) Package
- V_L Pin for Compatibility with Mixed Voltage Systems
- ESD Protection for RS-232 I/O Pins to ±15kV (IEC61000)
- Single $\overline{SHDN}$ Pin Disables Transmitters and Receivers
- Meets EIA/TIA-232 and V.28/V.24 Specifications at 3V
- On-Chip Charge Pumps Require Only Four External 0.1µF Capacitors
- Receiver Hysteresis For Improved Noise Immunity
- Very Low Supply Current 300µA
- Guaranteed Minimum Data Rate 250kbps
- Wide Power Supply Range. . . . . Single +3V to +5.5V
- Low Supply Current in Powerdown State 150nA
- Pb-free available

Applications

- Any System Requiring RS-232 Communication Ports
  - Battery Powered, Hand Held, and Portable Equipment
  - Laptop Computers, Notebooks, Palmtops
  - Digital Cameras
  - PDAs and PDA Cradles
  - Cellular/Mobile Phones

TABLE 1. SUMMARY OF FEATURES

PART NUMBER	NO. OF Tx.	NO. OF Rx.	DATA RATE (kbps)	Rx. ENABLE FUNCTION?	V_L LOGIC SUPPLY PIN?	MANUAL POWER- DOWN?	AUTOMATIC POWERDOWN FUNCTION?
ISL4260E	3	2	250	NO	YES	YES	NO

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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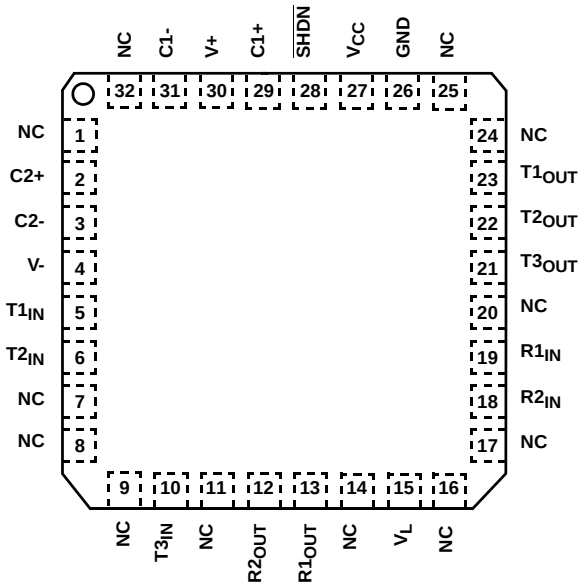
Pinout

ISL4260E (QFN)
TOP VIEW



Pin Descriptions

PIN	FUNCTION
V_{CC}	System power supply input (3.0V to 5.5V).
V+	Internally generated positive transmitter supply (+5.5V).
V-	Internally generated negative transmitter supply (-5.5V).
GND	Ground connection.
C1+	External capacitor (voltage doubler) is connected to this lead.
C1-	External capacitor (voltage doubler) is connected to this lead.
C2+	External capacitor (voltage inverter) is connected to this lead.
C2-	External capacitor (voltage inverter) is connected to this lead.
T_{IN}	TTL/CMOS compatible transmitter Inputs. The switching point is a function of the V_L voltage.
T_{OUT}	±15kV ESD Protected, RS-232 level (nominally ±5.5V) transmitter outputs.
R_{IN}	±15kV ESD Protected, RS-232 compatible receiver inputs.
R_{OUT}	TTL/CMOS level receiver outputs. Swings between GND and V_L.
V_L	Logic-Level Supply. All TTL/CMOS inputs and outputs are powered by this supply.
$\overline{SHDN}$	Active low TTL/CMOS input to tri-state receiver and transmitter outputs and to shut down the on-board power supply to place device in low power mode. The switching point is a function of the V_L voltage.
NC	No Connection

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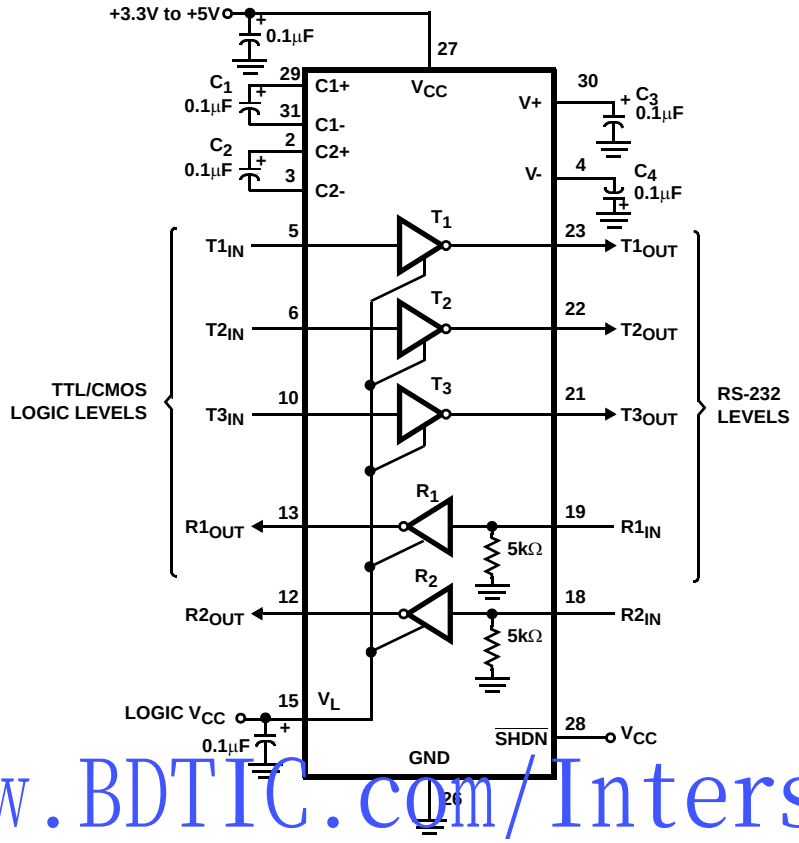
Typical Operating Circuit



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Absolute Maximum Ratings

V_{CC} to Ground . . . . . -0.3V to 6V
V_L to Ground . . . . . -0.3V to 7V
V+ to Ground . . . . . -0.3V to 7V
V- to Ground . . . . . +0.3V to -7V
V+ to V- 14V
Input Voltages
  T_{IN}, $\overline{SHDN}$ . . . . . -0.3V to 6V
  R_{IN} . . . . . ±25V
Output Voltages
  T_{OUT} . . . . . ±13.2V
  R_{OUT} . . . . . -0.3V to (V_L +0.3V)
Short Circuit Duration
  T_{OUT} . . . . . Continuous
ESD Rating . . . . . See Specification Table

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
32 Ld QFN Package	32

Moisture Sensitivity (see Technical Brief TB363)
  QFN Package . . . . . Level 1
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

Operating Conditions

Temperature Range
  ISL4260EIR . . . . . -40^oC to 85^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379, and Tech Brief TB389.

Electrical Specifications

Test Conditions: V_{CC} = 3V to 5.5V, C_1 - C_4 = 0.1µF, V_L = V_{CC}; Unless Otherwise Specified. Typicals are at T_A = 25^oC, V_{CC} = V_L = 3.3V

PARAMETER	TEST CONDITIONS		TEMP (^oC)	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
Supply Current, Powerdown	$\overline{SHDN}$ = GND, All Inputs at V_{CC} or GND		25	-	0.15	1	µA
Supply Current	All Outputs Unloaded, $\overline{SHDN}$ = V_{CC}, V_{CC} = 3.15V		25	-	0.3	1	mA
LOGIC AND TRANSMITTER INPUTS							
Input Logic Threshold Low	T_{IN}, $\overline{SHDN}$	V_L = 3.3V or 5V	Full	-	-	0.8	V
		V_L = 2.5V	Full	-	-	0.6	V
Input Logic Threshold High	T_{IN}, $\overline{SHDN}$	V_L = 5V	Full	2.4	-	-	V
		V_L = 3.3V	Full	2.0	-	-	V
		V_L = 2.5V	Full	1.4	-	-	V
		V_L = 1.8V	25	-	0.9	-	V
Transmitter Input Hysteresis			25	-	0.5	-	V
Input Leakage Current	T_{IN}, $\overline{SHDN}$		Full	-	±0.01	±1	µA
RECEIVER OUTPUTS							
Output Leakage Current	V_{CC} = 0V or 3V to 5.5V, $\overline{SHDN}$ = GND		Full	-	±0.05	±10	µA
Output Voltage Low	I_{OUT} = 1.6mA		Full	-	-	0.4	V
Output Voltage High	I_{OUT} = -1.0mA		Full	V_L - 0.6	V_L - 0.1	-	V
RECEIVER INPUTS							
Input Voltage Range			Full	-25	-	25	V
Input Threshold Low	V_L = 5.0V		25	0.8	1.5	-	V
	V_L = 3.3V		25	0.6	1.2	-	V
Input Threshold High	V_L = 5.0V		25	-	1.8	2.4	V
	V_L = 3.3V		25	-	1.5	2.4	V
Input Hysteresis			25	-	0.5	-	V
Input Resistance			25	3	5	7	kΩ

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Electrical Specifications Test Conditions: V_{CC} = 3V to 5.5V, C_1 - C_4 = 0.1µF, V_L = V_{CC}; Unless Otherwise Specified. Typicals are at T_A = 25°C, V_{CC} = V_L = 3.3V **(Continued)**

PARAMETER	TEST CONDITIONS		TEMP (°C)	MIN	TYP	MAX	UNITS
TRANSMITTER OUTPUTS							
Output Voltage Swing	All Transmitter Outputs Loaded with 3kΩ to Ground		Full	±5.0	±5.4	-	V
Output Resistance	V_{CC} = V+ = V- = 0V, Transmitter Output = ±2V		Full	300	10M	-	Ω
Output Short-Circuit Current	Shorted to GND		Full	-	-	±60	mA
Output Leakage Current	V_{OUT} = ±12V, V_{CC} = 0V or 3V to 5.5V, $\overline{SHDN}$ = GND		Full	-	-	±25	µA
TIMING CHARACTERISTICS							
Maximum Data Rate	R_L = 3kΩ, C_L = 1000pF, One Transmitter Switching		Full	250	500	-	kbps
Receiver Propagation Delay	Receiver Input to Receiver Output, C_L = 150pF	t_{PHL}	25	-	0.15	-	µs
		t_{PLH}	25	-	0.15	-	µs
Receiver Output Enable Time			25	-	200	-	ns
Receiver Output Disable Time			25	-	200	-	ns
Transmitter Output Enable Time	From $\overline{SHDN}$ Rising Edge to T_{OUT} = ±3.7V		25	-	100	-	µs
Transmitter Skew	t_{PHL} - t_{PLH} (Note 2)		25	-	100	-	ns
Receiver Skew	t_{PHL} - t_{PLH}		25	-	50	-	ns
Transition Region Slew Rate	R_L = 3kΩ to 7kΩ, Measured From 3V to -3V or -3V to 3V, V_{CC} = 3.3V	C_L = 150pF to 1000pF	25	6	18	30	V/µs
		C_L = 150pF to 2500pF	25	4	13	30	V/µs
ESD PERFORMANCE							
RS-232 Pins (T_{OUT}, R_{IN})	Human Body Model		25	-	±15	-	kV
	IEC61000-4-2 Air-Gap Discharge		25	-	±15	-	kV
	IEC61000-4-2 Contact Discharge		25	-	±8	-	kV

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NOTE:

2. Transmitter skew is measured at the transmitter zero crossing points.

Detailed Description

The ISL4260E operates from a single +3V to +5.5V supply, guarantees a 250kbps minimum data rate, requires only four small external 0.1µF capacitors, features low power consumption, and meets all EIA RS-232C and V.28 specifications. The circuit is divided into three sections: The charge pump, the transmitters, and the receivers.

Charge-Pump

Intersil's new ISL4260E utilizes regulated on-chip dual charge pumps as voltage doublers, and voltage inverters to generate ±5.5V transmitter supplies from a V_{CC} supply as low as 3.0V. This allows these devices to maintain RS-232 compliant output levels over the ±10% tolerance range of 3.3V powered systems. The efficient on-chip power supplies require only four small, external 0.1µF capacitors for the voltage doubler and inverter functions over the full V_{CC} range; other capacitor combinations can be used as shown in Table 3. The charge pumps operate discontinuously (i.e., they turn off as soon as the V+ and V- supplies are pumped up to the nominal values), resulting in significant power savings.

Transmitters

The transmitters are proprietary, low dropout, inverting drivers that translate TTL/CMOS inputs to EIA/TIA-232 output levels. Coupled with the on-chip ±5.5V supplies, these transmitters deliver true RS-232 levels over a wide range of single supply system voltages.

All transmitter outputs disable and assume a high impedance state when the device enters the powerdown mode (see Table 2). These outputs may be driven to ±12V when disabled.

All devices guarantee a 250kbps data rate for full load conditions (3kΩ and 1000pF), $V_{CC} \geq$ 3.0V, with one transmitter operating at full speed. Under more typical conditions of $V_{CC} \geq$ 3.3V, R_L = 3kΩ, and C_L = 250pF, one transmitter easily operates at 1.25Mbps.

The transmitter input threshold is set by the voltage applied to the V_L pin. Transmitter inputs float if left unconnected

(there are no pull-up resistors), and may cause I_{CC} increases. Connect unused inputs to GND for the best performance.

TABLE 2. POWERDOWN TRUTH TABLE

$\overline{SHDN}$ INPUT	TRANSMITTER OUTPUTS	RECEIVER OUTPUTS	MODE OF OPERATION
L	High-Z	High-Z	Manual Powerdown
H	Active	Active	Normal Operation

Receivers

The ISL4260E contains standard inverting receivers that convert RS-232 signals to CMOS output levels and accept inputs up to ±25V while presenting the required 3kΩ to 7kΩ input impedance (see Figure 1) even if the power is off (V_{CC} = 0V). The receivers' Schmitt trigger input stage uses hysteresis to increase noise immunity and decrease errors due to slow input signal transitions. Receiver outputs swing from GND to V_L, and tristate in powerdown.

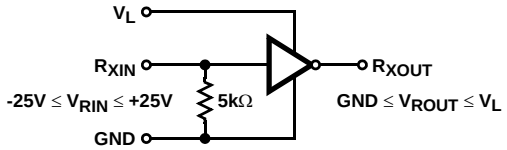

FIGURE 1. RECEIVER CONNECTIONS

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Low Power Operation

This 3V device requires a nominal supply current of 0.3mA, even at V_{CC} = 5.5V, during normal operation (not in powerdown mode). This is considerably less than the 11mA current required by comparable 5V RS-232 devices, allowing users to reduce system power simply by replacing the old style device with the ISL4260E in new designs.

Powerdown Functionality

The already low current requirement drops significantly when the device enters powerdown mode. In powerdown, supply current drops to 150nA, because the on-chip charge pump turns off (V+ collapses to V_{CC}, V- collapses to GND), and the transmitter and receiver outputs tristate. This micro-power mode makes these devices ideal for battery powered and portable applications.

Software Controlled (Manual) Powerdown

The ISL4260E may be forced into its low power, standby state via a simple shutdown ($\overline{SHDN}$) pin (see Figure 2). Driving this pin high enables normal operation, while driving it low forces the IC into its powerdown state. The time required to exit powerdown, and resume transmission is less than 100µs. Connect $\overline{SHDN}$ to V_{CC} if the powerdown function isn't needed.

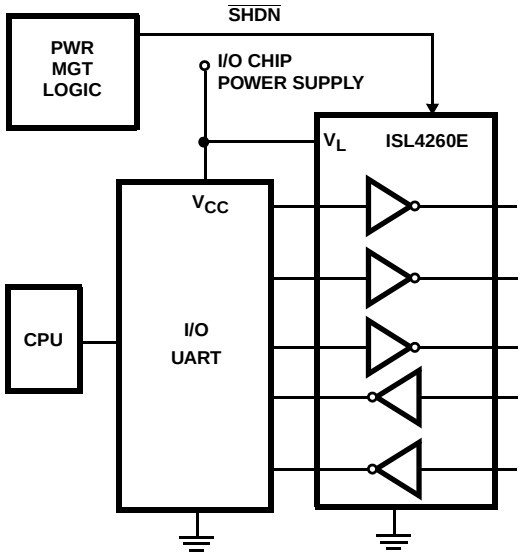

FIGURE 2. CONNECTIONS FOR MANUAL POWERDOWN

V_L Logic Supply Input

Unlike other RS-232 interface devices where the CMOS outputs swing between 0 and V_{CC}, the ISL4260E features a separate logic supply input (V_L; 1.8V to 5V, regardless of V_{CC}) that sets V_{OH} for the receiver outputs. Connecting V_L to a host logic supply lower than V_{CC}, prevents the ISL4260E outputs from forward biasing the input diodes of a logic device powered by that lower supply. Connecting V_L to a logic supply greater than V_{CC} ensures that the receiver output levels are compatible even with the CMOS input V_{IH} of AC, HC, and CD4000 devices. Note that the V_L supply current increases to 100µA with V_L = 5V and V_{CC} = 3.3V (see Figure 11). V_L also powers the transmitter and logic inputs, thereby setting their switching thresholds to levels compatible with the logic supply. This separate logic supply pin allows a great deal of flexibility in interfacing to systems with different logic supplies. If logic translation isn't required, connect V_L to the ISL4260E V_{CC}.

Capacitor Selection

The ISL4260E charge pumps only require 0.1µF capacitors for the full operational voltage range. Table 3 lists other acceptable capacitor values for various supply voltage ranges. Do not use values smaller than those listed in Table 3. Increasing the capacitor values (by a factor of 2) reduces ripple on the transmitter outputs and slightly reduces power consumption.

TABLE 3. REQUIRED CAPACITOR VALUES

V_{CC} (V)	C_1 (µF)	C_2, C_3, C_4 (µF)
3.0 to 3.6	0.1	0.1
4.5 to 5.5	0.047	0.33
3.0 to 5.5	0.22	1

When using minimum required capacitor values, make sure that capacitor values do not degrade excessively with temperature. If in doubt, use capacitors with a larger nominal value. The capacitor's equivalent series resistance (ESR) usually rises at low temperatures and it influences the amount of ripple on V+ and V-.

Power Supply Decoupling

In most circumstances a 0.1µF bypass capacitor is adequate. In applications that are particularly sensitive to power supply noise, decouple V_{CC} to ground with a capacitor of the same value as the charge-pump capacitor C_1. Connect the bypass capacitor as close as possible to the IC.

Transmitter Outputs when Exiting Powerdown

Figure 3 shows the response of two transmitter outputs when exiting powerdown mode. As they activate, the two transmitter outputs properly go to opposite RS-232 levels, with no glitching, ringing, nor undesirable transients. Each transmitter is loaded with 3kΩ in parallel with 2500pF. Note that the transmitters enable only when the magnitude of the supplies exceed approximately 3V.

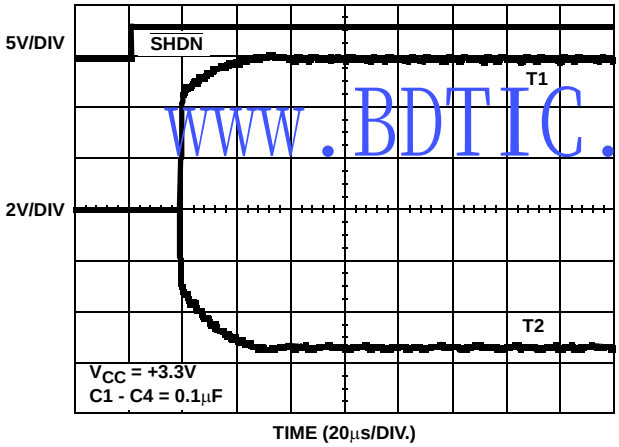

FIGURE 3. TRANSMITTER OUTPUTS WHEN EXITING POWERDOWN

High Data Rates

The ISL4260E maintains the RS-232 ±5V minimum transmitter output voltages even at high data rates. Figure 4 details a transmitter loopback test circuit, and Figure 5 illustrates the loopback test result at 120kbps. For this test, all transmitters were simultaneously driving RS-232 loads in parallel with 1000pF, at 120kbps. Figure 6 shows the loopback results for a single transmitter driving 1000pF and an RS-232 load at 250kbps. The static transmitters were also loaded with an RS-232 receiver.

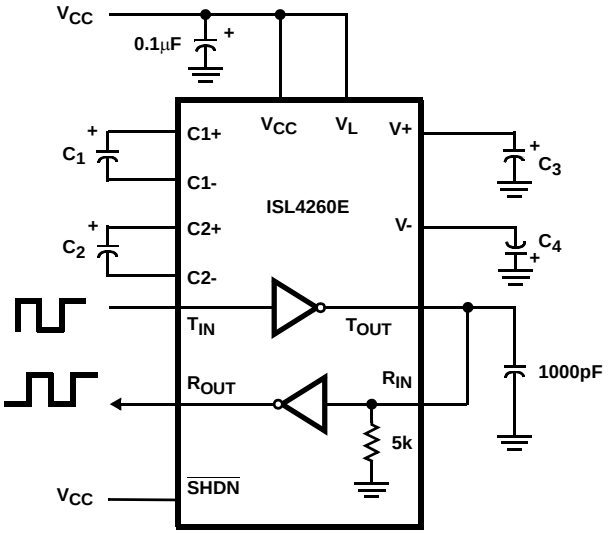

FIGURE 4. TRANSMITTER LOOPBACK TEST CIRCUIT

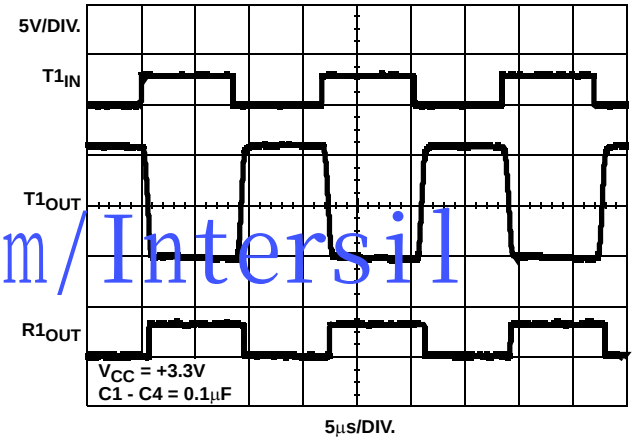

FIGURE 5. LOOPBACK TEST AT 120kbps

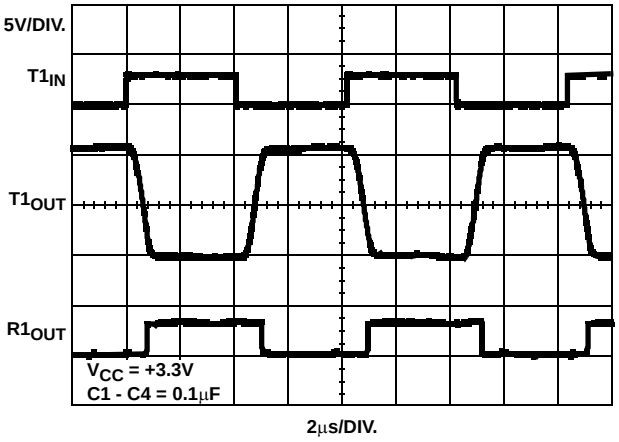

FIGURE 6. LOOPBACK TEST AT 250kbps

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Interconnection with 3V and 5V Logic

Standard 3.3V powered RS-232 devices interface well with 3V and 5V powered TTL compatible logic families (e.g., ACT and HCT), but the logic outputs (e.g., R_{OUTS}) fail to reach the V_{IH} level of 5V powered CMOS families like HC, AC, and CD4000. The ISL4260E V_L supply pin solves this problem. By connecting V_L to the same supply (1.8V to 5V) powering the logic device, the ISL4260E logic outputs will swing from GND to the logic V_{CC}.

±15kV ESD Protection

All pins on the 3V interface devices include ESD protection structures, but the ISL4260E incorporates advanced structures which allow the RS-232 pins (transmitter outputs and receiver inputs) to survive ESD events up to ±15kV. The RS-232 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins, or connecting a cable, can cause an ESD event that might destroy unprotected ICs. These new ESD structures protect the device whether or not it is powered up, protect without allowing any latchup mechanism to activate, and don't interfere with RS-232 signals as large as ±25V.

Human Body Model (HBM) Testing

As the name implies, this test method emulates the ESD event delivered to an IC during human handling. The tester delivers the charge through a 1.5kΩ current limiting resistor, making the test less severe than the IEC61000 test which utilizes a 330Ω limiting resistor. The HBM method determines an ICs ability to withstand the ESD transients typically present during handling and manufacturing. Due to the random nature of these events, each pin is tested with respect to all other pins. The RS-232 pins on "E" family devices can withstand HBM ESD events to ±15kV.

IEC61000-4-2 Testing

The IEC61000 test method applies to finished equipment, rather than to an individual IC. Therefore, the pins most likely to suffer an ESD event are those that are exposed to the outside world (the RS-232 pins in this case), and the IC is tested in its typical application configuration (power applied) rather than testing each pin-to-pin combination. The lower current limiting resistor coupled with the larger charge storage capacitor yields a test that is much more severe than the HBM test. The extra ESD protection built into this device's RS-232 pins allows the design of equipment meeting level 4 criteria without the need for additional board level protection on the RS-232 port.

AIR-GAP DISCHARGE TEST METHOD

For this test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on approach speed, humidity, temperature, etc., so it is difficult to obtain repeatable results. The "E" device RS-232 pins withstand ±15kV air-gap discharges.

CONTACT DISCHARGE TEST METHOD

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized, thereby eliminating the variables associated with the air-gap discharge. The result is a more repeatable and predictable test, but equipment limits prevent testing devices at voltages higher than ±8kV. All "E" family devices survive ±8kV contact discharges on the RS-232 pins.

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Typical Performance Curves V_{CC} = 3.3V, T_A = 25°C

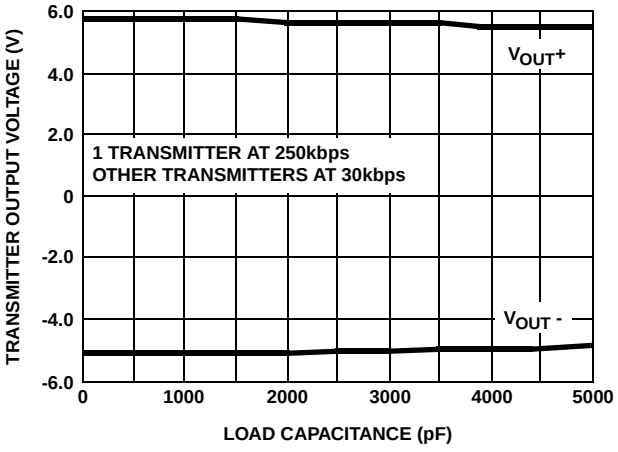

FIGURE 7. TRANSMITTER OUTPUT VOLTAGE vs LOAD CAPACITANCE

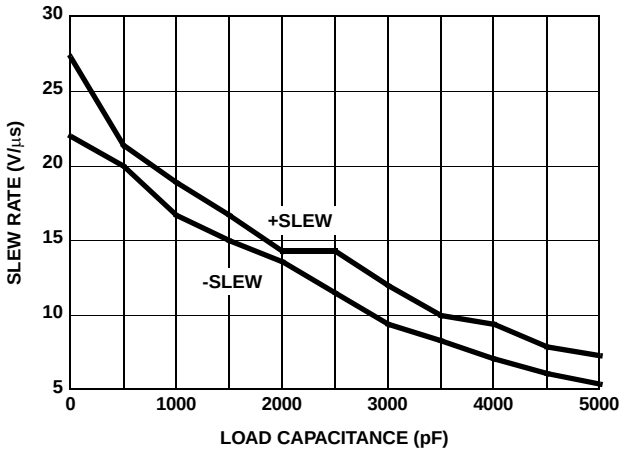

FIGURE 8. SLEW RATE vs LOAD CAPACITANCE

Typical Performance Curves V_{CC} = 3.3V, T_A = 25°C (Continued)

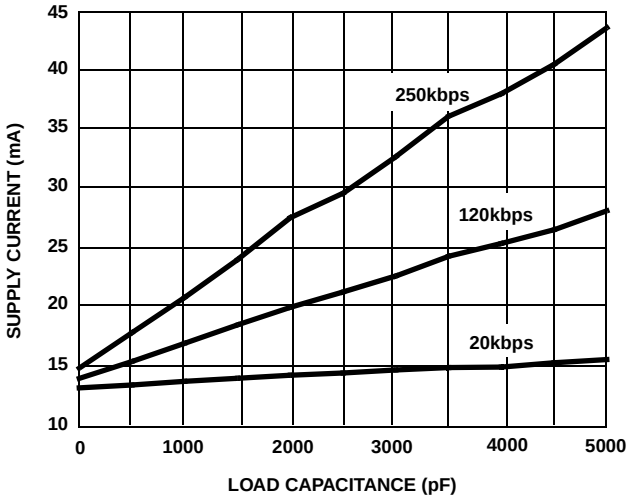

FIGURE 9. SUPPLY CURRENT vs LOAD CAPACITANCE WHEN TRANSMITTING DATA

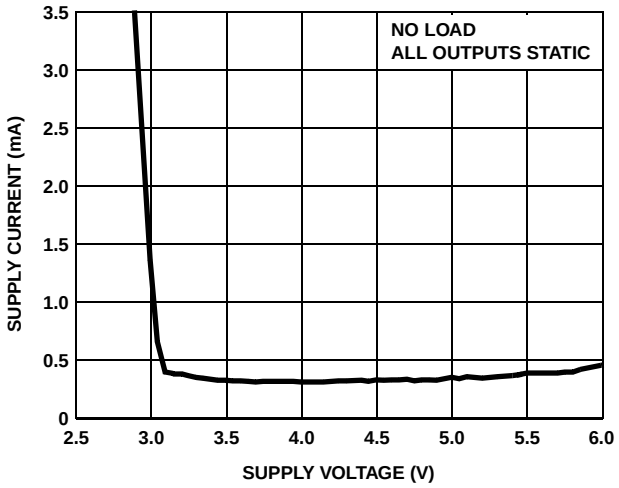

FIGURE 10. SUPPLY CURRENT vs SUPPLY VOLTAGE

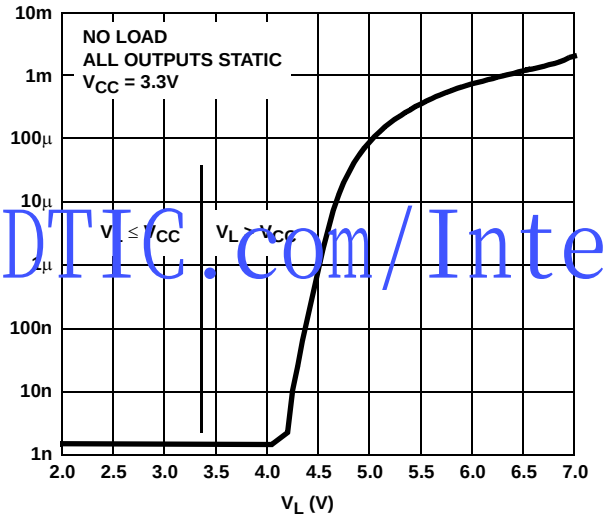

FIGURE 11. V_L SUPPLY CURRENT vs V_L VOLTAGE

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Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP)

GND

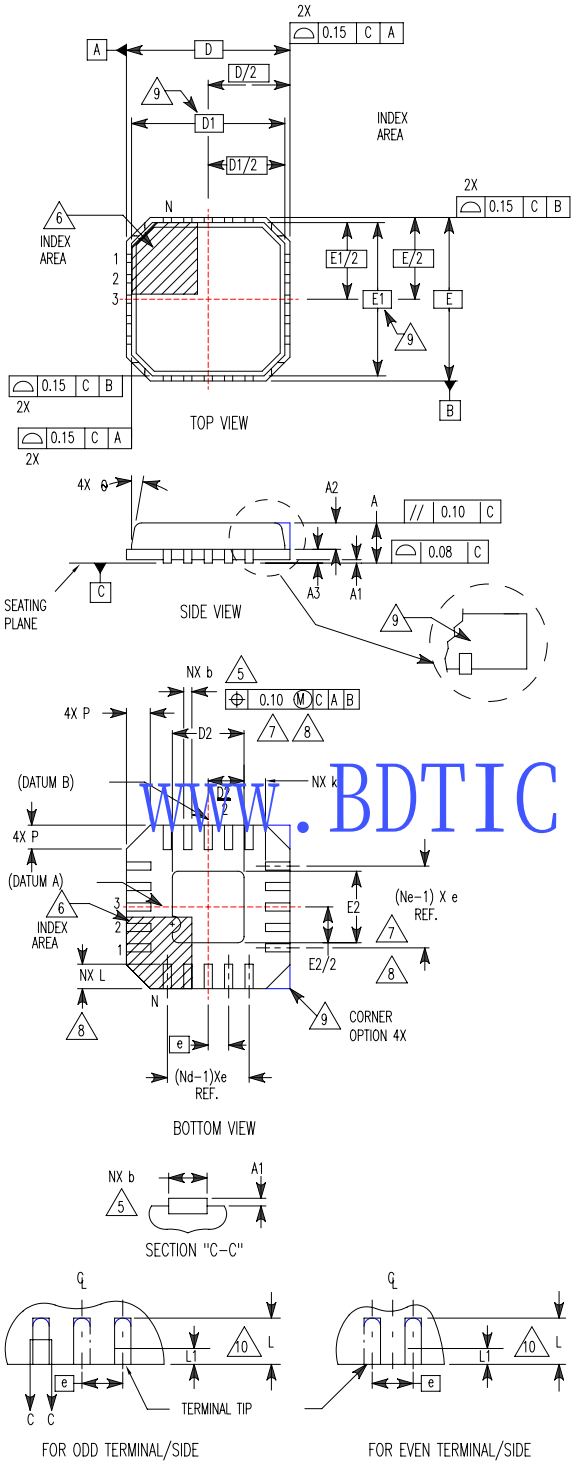
TRANSISTOR COUNT

422

PROCESS

Si Gate CMOS

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L32.5x5

32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VHHD-2 ISSUE C

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.23	0.30	5,8
D		5.00 BSC		-
D1		4.75 BSC		9
D2	2.95	3.10	3.25	7,8
E		5.00 BSC		-
E1		4.75 BSC		9
E2	2.95	3.10	3.25	7,8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
L1	-	-	0.15	10
N		32		2
Nd		8		3
Ne	8	8		3
P	-	-	0.60	9
θ	-	-	12	9

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

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