Data Sheet | February 13, 2008 | FN6045.3

QFN Packaged, ±15kV ESD Protected, +2.7V to +5.5V, 150nA, 250kbps, RS-232 Transmitters/Receivers

The Intersil ISL3232E and ISL4221E, ISL4223E devices are 2.7V to 5.5V powered RS-232 transmitters/receivers which meet EIA/TIA-232 and V.28/V.24 specifications, even at V_{CC} = 3.0V. Additionally, they provide ±15kV ESD protection (IEC61000-4-2 Air Gap and Human Body Model) on transmitter outputs and receiver inputs (RS-232 pins). Targeted applications are PDAs, Palmtops, and hand-held products where the low operational, and even lower standby, power consumption is critical. Efficient on-chip charge pumps, coupled with manual and automatic power-down functions, reduce the standby supply current to a 150nA trickle. Tiny 5mmx5mm **Quad Flat No-Lead** (QFN) packaging and the use of small, low value capacitors ensure board space savings as well. Data rates greater than 250kbps are guaranteed at worst case load conditions.

The ISL4221E is a 1 driver, 1 receiver device and the ISL3232E and ISL4223E are 2 driver, 2 receiver devices that, coupled with the 5mmx5mm QFN package, provide the industry's smallest, lowest power serial port suitable for PDAs, and hand-held applications. The 5mmx5mm QFN requires 40% less board area than a 20 Ld TSSOP, and is nearly 20% thinner.

The **ISL4221E, ISL4223E** versions feature an ***automatic power-down*** function that powers down the on-chip power supply and driver circuits. This occurs when an attached peripheral device is shut off or the RS-232 cable is removed, conserving system power automatically without changes to the hardware or operating system. It powers up again when a valid RS-232 voltage is applied to any receiver input.

Table 1 summarizes the features of the IC's, while Application Note AN9863 summarizes the features of each device comprising the 3V RS-232 family.

Features

- Available in Near Chip Scale QFN (5mmx5mm) Package, which is 40% Smaller than a 20 Ld TSSOP
- ESD Protection for RS-232 I/O Pins to ±15kV (IEC61000)
- Meets EIA/TIA-232 and V.28/V.24 Specifications at 3V
- RS-232 Compatible with V_{CC} = 2.7V
- On-Chip Voltage Converters Require Only Four External 0.1µF Capacitors
- Manual and Automatic Power-down Features (Except ISL3232E)
- Receiver Hysteresis For Improved Noise Immunity
- Guaranteed Minimum Data Rate 250kbps
- Wide Power Supply Range . . . . . Single +2.7V to +5.5V
- Low Supply Current in Power-down State 150nA
- Pb-Free Available (RoHS Compliant)

Applications

- Any Space Constrained System Requiring RS-232 Ports
  - Battery Powered, and Portable Equipment
  - Hand-Held Products (GPS Receivers, Bar Code Scanners, etc.)
  - PDAs and Palmtops, Data Cables
  - Cellular/Mobile Phones, Digital Cameras

Related Literature

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices
- Technical Brief TB379 "Thermal Characterization of Packages for ICs"
- Technical Brief TB389 "PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages"

TABLE 1. SUMMARY OF FEATURES

PART NUMBER	NO. OF Tx.	NO. OF Rx.	QFN PKG. AVAILABLE?	DATA RATE (kbps)	Rx. ENABLE FUNCTION?	MANUAL POWER-DOWN?	AUTOMATIC POWER-DOWN FUNCTION?
ISL4221E	1	1	YES	250	YES	YES	YES
ISL3232E	2	2	YES	250	NO	NO	NO
ISL4223E	2	2	YES	250	YES	YES	YES

Ordering Information

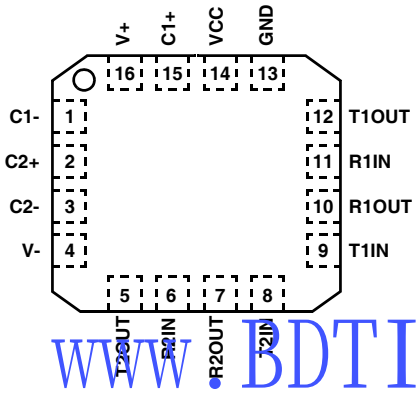
PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL3232EIRZ* (Note)	ISL3232 EIRZ	-40 to +85	16 Ld QFN (Pb-free)	L16.5x5B
ISL4221EIR*	ISL 4221EIR	-40 to +85	16 Ld QFN	L16.5x5B
ISL4221EIRZ* (Note)	ISL4221 EIRZ	-40 to +85	16 Ld QFN (Pb-free)	L16.5x5B
ISL4223EIR*	ISL 4223EIR	-40 to +85	20 Ld QFN	L20.5x5
ISL4223EIRZ* (Note)	ISL4223 EIRZ	-40 to +85	20 Ld QFN (Pb-free)	L20.5x5

*Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

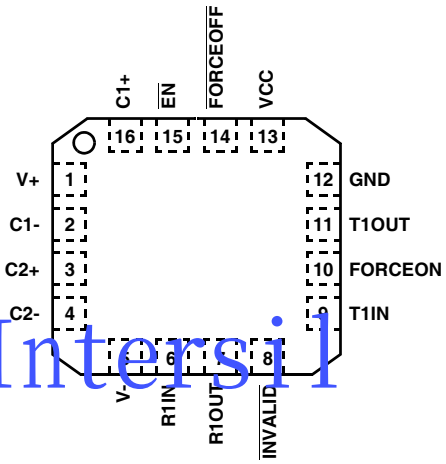
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinouts

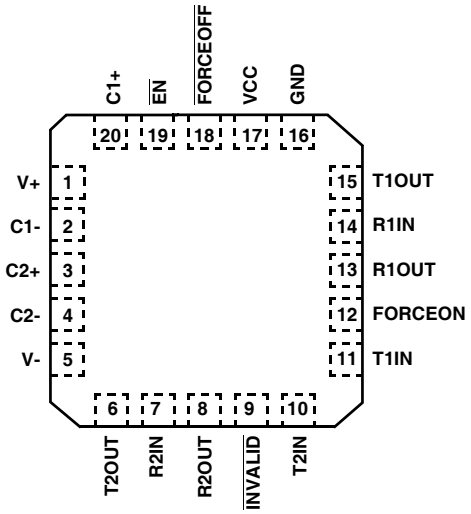
ISL3232E
(16 LD QFN)
TOP VIEW



ISL4221E
(16 LD QFN)
TOP VIEW



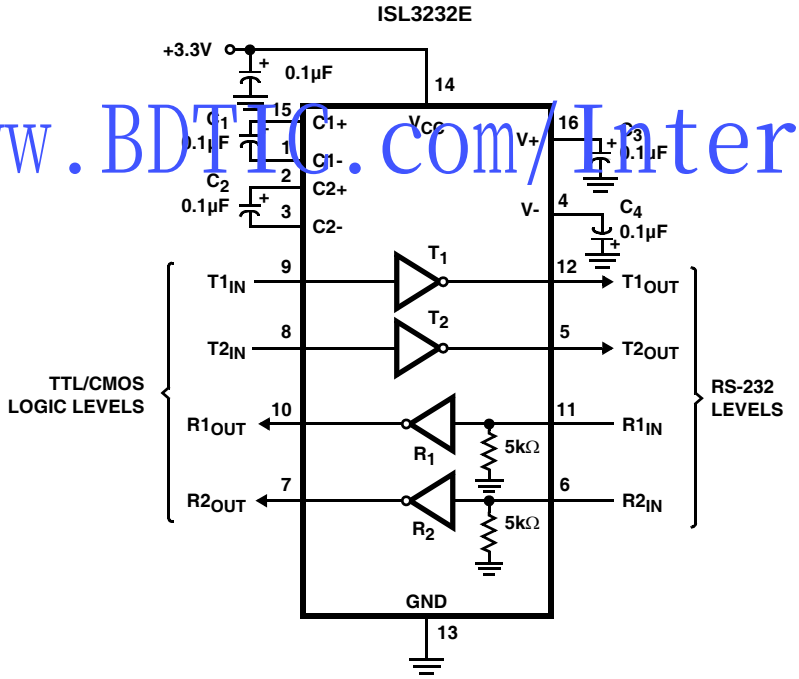
ISL4223E
(20 LD QFN)
TOP VIEW



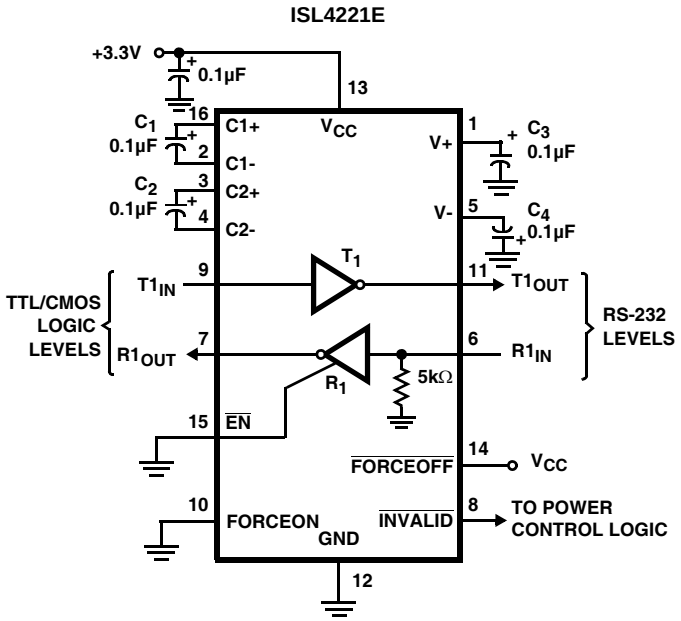
Pin Descriptions

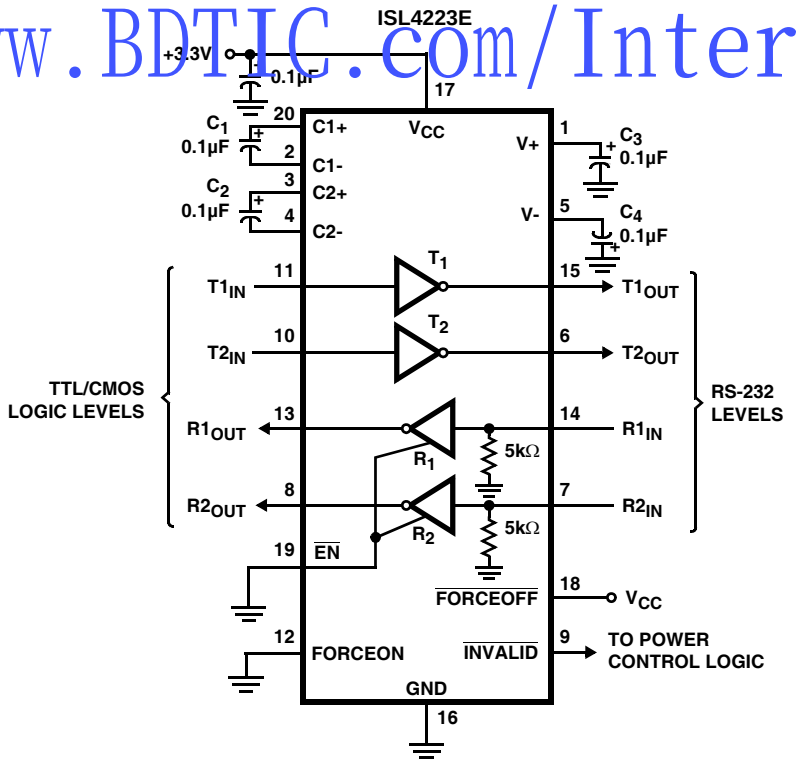
PIN	FUNCTION
VCC	System power supply input (2.7V to 5.5V).
V+	Internally generated positive transmitter supply (+5.5V).
V-	Internally generated negative transmitter supply (-5.5V).
GND	Ground connection.
C1+	External capacitor (voltage doubler) is connected to this lead.
C1-	External capacitor (voltage doubler) is connected to this lead.
C2+	External capacitor (voltage inverter) is connected to this lead.
C2-	External capacitor (voltage inverter) is connected to this lead.
TIN	TTL/CMOS compatible transmitter Inputs.
TOUT	±15kV ESD Protected, RS-232 level (nominally ±5.5V) transmitter outputs.
RIN	±15kV ESD Protected, RS-232 compatible receiver inputs.
ROUT	TTL/CMOS level receiver outputs.
$\overline{\text{INVALID}}$	Active low output that indicates if no valid RS-232 levels are present on any receiver input.
$\overline{\text{FORCEOFF}}$	Active low to shut down transmitters and on-chip power supply. This overrides any automatic circuitry and FORCEON (see Table 2).
FORCEON	Active high input to override automatic power-down circuitry thereby keeping transmitters active. ($\overline{\text{FORCEOFF}}$ must be high).
$\overline{\text{EN}}$	Active low receiver enable control.

Typical Operating Circuits



Typical Operating Circuits





Absolute Maximum Ratings

V_{CC} to GND . . . . . -0.3V to 6V
V+ to GND . . . . . -0.3V to 7V
V- to GND. . . . . +0.3V to -7V
V+ to V- 14V
Input Voltages
T_{IN}, $\overline{FORCEOFF}$, FORCEON, $\overline{EN}$ . . . . . -0.3V to 6V
R_{IN} . . . . . ±25V
Output Voltages
T_{OUT} . . . . . ±13.2V
R_{OUT}, $\overline{INVALID}$. . . . . -0.3V to V_{CC} +0.3V
Short Circuit Duration
T_{OUT} . . . . . Continuous
ESD Rating . . . . . See Specification Table

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld QFN Package (Notes 1, 2).	35	4.3
20 Ld QFN Package (Notes 1, 2).	32	4.3

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range. . . . . .-65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range. . . . . .-40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379, and Tech Brief TB389.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Test Conditions: V_{CC} = 3V to 5.5V, C_1 through C_4 = 0.1µF; Unless Otherwise Specified. Typicals are at T_A = +25°C

PARAMETER	TEST CONDITIONS		TEMP (°C)	MIN (Note 4)	TYP	MAX (Note 4)	UNITS
DC CHARACTERISTICS							
Supply Current, Automatic Power-down	All R_{IN} Open, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC} (Except ISL3232E)		25	-	0.15	1	µA
Supply Current, Power-down	$\overline{FORCEOFF}$ = GND (Except ISL3232E)		25	-	0.15	1	µA
Supply Current, Automatic Power-down Disabled	All Outputs Unloaded, FORCEON = $\overline{FORCEOFF}$ = V_{CC}	V_{CC} = 3.15V	25	-	0.3	1.0	mA
LOGIC AND TRANSMITTER INPUTS AND RECEIVER OUTPUTS							
Input Logic Threshold Low	T_{IN}, FORCEON, $\overline{FORCEOFF}$, $\overline{EN}$		Full	-	-	0.8	V
Input Logic Threshold High	T_{IN}, FORCEON, $\overline{FORCEOFF}$, $\overline{EN}$	V_{CC} = 3.3V	Full	2.0	-	-	V
		V_{CC} = 5.0V	Full	2.4	-	-	V
Input Leakage Current	T_{IN}, FORCEON, $\overline{FORCEOFF}$, $\overline{EN}$		Full	-	±0.01	±1.0	µA
Output Leakage Current	$\overline{EN}$ = V_{CC} (Except ISL3232E)		Full	-	±0.05	±10	µA
Output Voltage Low	I_{OUT} = 1.6mA		Full	-	-	0.4	V
Output Voltage High	I_{OUT} = -1.0mA		Full	V_{CC} - 0.6	V_{CC} - 0.1	-	V
AUTOMATIC POWER-DOWN (FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}, Except ISL3232E)							
Receiver Input Thresholds to Enable Transmitters	ISL4221E, ISL4223E Powers Up (See Figure 6)		Full	-2.7	-	2.7	V
Receiver Input Thresholds to Disable Transmitters	ISL4221E, ISL4223E Powers Down (See Figure 6)		Full	-0.3	-	0.3	V
$\overline{INVALID}$ Output Voltage Low	I_{OUT} = 1.6mA		Full	-	-	0.4	V
$\overline{INVALID}$ Output Voltage High	I_{OUT} = -1.0mA		Full	V_{CC} - 0.6	-	-	V
Receiver Threshold to Transmitters Enabled Delay (t_{WU})			25	-	100	-	µs
Receiver Positive or Negative Threshold to $\overline{INVALID}$ High Delay (t_{INVH})			25	-	1	-	µs
Receiver Positive or Negative Threshold to $\overline{INVALID}$ Low Delay (t_{INVL})			25	-	30	-	µs

Electrical Specifications Test Conditions: V_{CC} = 3V to 5.5V, C_1 through C_4 = 0.1µF; Unless Otherwise Specified. Typicals are at T_A = +25°C **(Continued)**

PARAMETER	TEST CONDITIONS		TEMP (°C)	MIN (Note 4)	TYP	MAX (Note 4)	UNITS
RECEIVER INPUTS							
Input Voltage Range			25	-25	-	25	V
Input Threshold Low	V_{CC} = 3.3V		25	0.6	1.2	-	V
	V_{CC} = 5.0V		25	0.8	1.5	-	V
Input Threshold High	V_{CC} = 3.3V		25	-	1.5	2.4	V
	V_{CC} = 5.0V		25	-	1.8	2.4	V
Input Hysteresis			25	-	0.5	-	V
Input Resistance			25	3	5	7	kΩ
TRANSMITTER OUTPUTS							
Output Voltage Swing	All Transmitter Outputs Loaded with 3kΩ to Ground		Full	±5.0	±5.4	-	V
Output Resistance	V_{CC} = V+ = V- = 0V, Transmitter Output = ±2V		Full	300	10M	-	Ω
Output Short-Circuit Current			Full	-	±35	±60	mA
Output Leakage Current	V_{OUT} = ±12V, V_{CC} = 0V, or V_{CC} = 3V to 5.5V, with Automatic Power-down or $\overline{FORCEOFF}$ = GND		Full	-	-	±25	µA
TIMING CHARACTERISTICS							
Maximum Data Rate	R_L = 3kΩ, C_L = 1000pF, One Transmitter Switching		Full	250	500	-	kbps
Receiver Propagation Delay	Receiver Input to Receiver Output, C_L = 150pF	t_{PHL}	25	-	0.15	-	µs
		t_{PLH}	25	-	0.15	-	µs
Receiver Output Enable Time	Normal Operation (Except ISL3232E)		25	-	200	-	ns
Receiver Output Disable Time	Normal Operation (Except ISL3232E)		25	-	200	-	ns
Transmitter Skew	t_{PHL} - t_{PLH} (Note 3)		25	-	100	-	ns
Receiver Skew	t_{PHL} - t_{PLH}		25	-	50	-	ns
Transition Region Slew Rate	V_{CC} = 3.3V, R_L = 3kΩ to 7kΩ, Measured From 3V to -3V or -3V to 3V	C_L = 150pF to 2500pF	25	4	-	30	V/µs
		C_L = 150pF to 1000pF	25	6	-	30	V/µs
ESD PERFORMANCE							
RS-232 Pins (TOUT, RIN)	Human Body Model		25	-	±15	-	kV
	IEC61000-4-2 Contact Discharge		25	-	±8	-	kV
	IEC61000-4-2 Air Gap Discharge		25	-	±15	-	kV
All Other Pins	Human Body Model		25	-	±2	-	kV

NOTES:

3. Transmitter skew is measured at the transmitter zero crossing points.
4. Parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested.

Detailed Description

The ISL4221E, ISL4223E and ISL3232E operate from a single +2.7V to +5.5V supply, guarantee a 250kbps minimum data rate, require only four small external 0.1µF capacitors, feature low power consumption, and meet all EIA RS-232C and V.28 specifications even with V_{CC} = 3.0V. The circuit is divided into three sections: The charge pump, the transmitters and the receivers.

Charge-Pump

Intersil's new RS-232 devices utilize regulated on-chip dual charge pumps as voltage doublers, and voltage inverters to generate ±5.5V transmitter supplies from a V_{CC} supply as low as 3.0V. This allows them to maintain RS-232 compliant output levels over the ±10% tolerance range of 3.3V powered systems. The efficient on-chip power supplies require only four small, external 0.1µF capacitors for the voltage doubler and inverter functions. The charge pumps operate discontinuously (i.e., they turn off as soon as the V+ and V- supplies are pumped up to the nominal values), resulting in significant power savings.

Transmitters

The transmitters are proprietary, low dropout, inverting drivers that translate TTL/CMOS inputs to EIA/TIA-232 output levels. Coupled with the on-chip ±5.5V supplies, these transmitters deliver true RS-232 levels over a wide range of single supply system voltages.

All ISL4221E, ISL4223E transmitter outputs disable and assume a high impedance state when the device enters the power-down mode (see Table 2). These outputs may be driven to ±12V when disabled.

The devices guarantee a 250kbps data rate for full load conditions (3kΩ and 1000pF), $V_{CC} \geq 3.0V$, with one transmitter operating at full speed. Under more typical conditions of $V_{CC} \geq 3.3V$, R_L = 3kΩ, and C_L = 250pF, one transmitter easily operates at 900kbps.

Transmitter inputs float if left unconnected, and may cause I_{CC} increases. Connect unused inputs to GND for the best performance.

Receivers

All these RS-232 devices contain standard inverting receivers, and the ISL4221E, ISL4223E receivers three-state via the $\overline{EN}$ control line. All the receivers convert RS-232 signals to CMOS output levels and accept inputs up to ±25V while presenting the required 3kΩ to 7kΩ input impedance (see Figure 1) even if the power is off (V_{CC} = 0V). The receivers' Schmitt trigger input stage uses hysteresis to increase noise immunity and decrease errors due to slow input signal transitions.

Receivers driving a powered down UART must be disabled to prevent current flow through, and possible damage to, the UART's protection diodes (see Figures 2 and 3). This can be accomplished on the ISL4221E, ISL4223E by driving the $\overline{EN}$ input high whenever the UART powers down. Figure 3 also shows that the $\overline{INVALID}$ output can be used to determine when the UART should be powered down. When the RS-232 cable is disconnected, $\overline{INVALID}$ switches low indicating that the UART is no longer needed. Reconnecting the cable drives $\overline{INVALID}$ back high, indicating that the UART should be powered up.

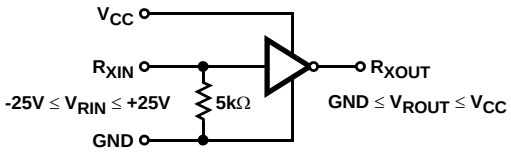


FIGURE 1. INVERTING RECEIVER CONNECTIONS

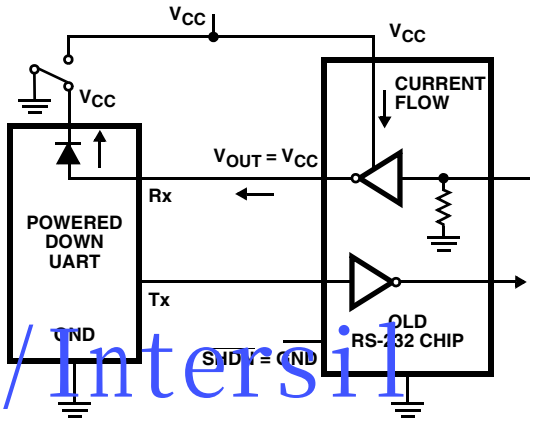


FIGURE 2. POWER DRAIN THROUGH POWERED DOWN PERIPHERAL

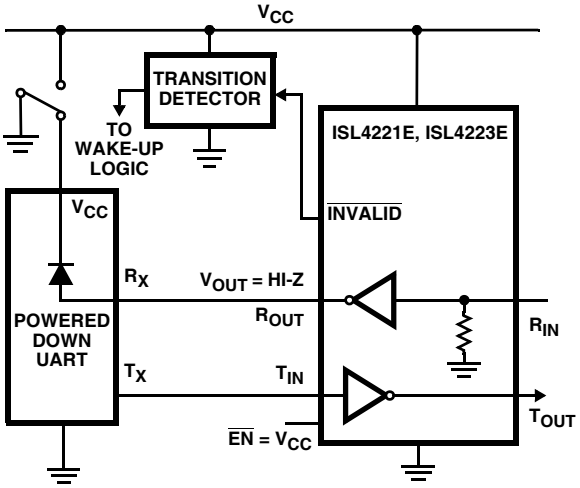


FIGURE 3. DISABLED RECEIVERS PREVENT POWER DRAIN

TABLE 2. POWER-DOWN AND ENABLE LOGIC TRUTH TABLE (EXCLUDING ISL3232E)

RS-232 SIGNAL PRESENT AT RECEIVER INPUT?	$\overline{\text{FORCEOFF}}$ INPUT	FORCEON INPUT	$\overline{\text{EN}}$ INPUT	TRANSMITTER OUTPUTS	RECEIVER OUTPUTS	$\overline{\text{INVALID}}$ OUTPUT	MODE OF OPERATION
NO	H	H	L	Active	Active	L	Normal Operation (Auto Power-down Disabled)
NO	H	H	H	Active	High-Z	L	
YES	H	L	L	Active	Active	H	Normal Operation (Auto Power-down Enabled)
YES	H	L	H	Active	High-Z	H	
NO	H	L	L	High-Z	Active	L	Power-down Due to Auto Power-down Logic
NO	H	L	H	High-Z	High-Z	L	
YES	L	X	L	High-Z	Active	H	Manual Power-down
YES	L	X	H	High-Z	High-Z	H	Manual Power-down w/Rcvr. Disabled
NO	L	X	L	High-Z	Active	L	Manual Power-down
NO	L	X	H	High-Z	High-Z	L	Manual Power-down w/Rcvr. Disabled

Low Power Operation

These 3V devices require a nominal supply current of 0.3mA, even at V_{CC} = 5.5V, during normal operation (not in power-down mode). This is considerably less than the 5mA to 11mA current required by comparable 5V RS-232 devices, allowing users to reduce system power simply by switching to this new family.

Power-down Functionality (Excluding ISL3232E)

The already low current requirement drops significantly when the device enters power-down mode. In power-down, supply current drops to 150nA because the on-chip charge pump turns off (V+ collapses to V_{CC}, V- collapses to GND) and the transmitter outputs three-state. Receiver outputs are unaffected by power-down; refer to Table 2 for details. This micro-power mode makes the ISL4221E, ISL4223E ideal for battery-powered and portable applications.

Software Controlled (Manual) Power-down

The ISL4221E, ISL4223E family provides pins that allow the user to force the IC into the low power, standby state.

The ISL4221E, ISL4223E utilize a two pin approach where the FORCEON and $\overline{\text{FORCEOFF}}$ inputs determine the IC's mode. For always enabled operation, FORCEON and $\overline{\text{FORCEOFF}}$ are both strapped high. To switch between active and power-down modes, under logic or software control, only the $\overline{\text{FORCEOFF}}$ input need be driven. The FORCEON state isn't critical, as $\overline{\text{FORCEOFF}}$ dominates over FORCEON. Nevertheless, if strictly manual control over power-down is desired, the user must strap FORCEON high to disable the automatic power-down circuitry.

Connecting $\overline{\text{FORCEOFF}}$ and FORCEON together disables the automatic power-down feature, enabling them to function as a manual $\overline{\text{SHUTDOWN}}$ input (see Figure 4).

The time to recover from automatic power-down mode is typically 100µs.

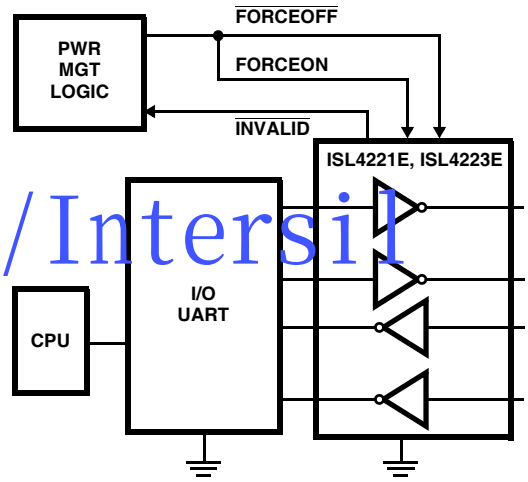


FIGURE 4. CONNECTIONS FOR MANUAL POWER-DOWN WHEN NO VALID RECEIVER SIGNALS ARE PRESENT

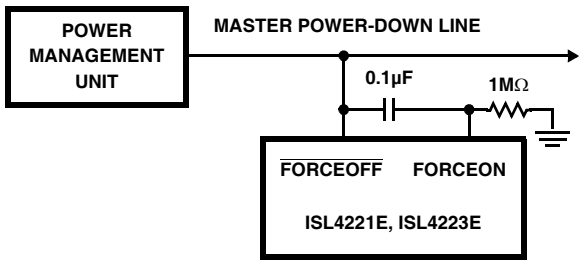


FIGURE 5. CIRCUIT TO PREVENT AUTO POWER-DOWN FOR 100ms AFTER FORCED POWER-UP

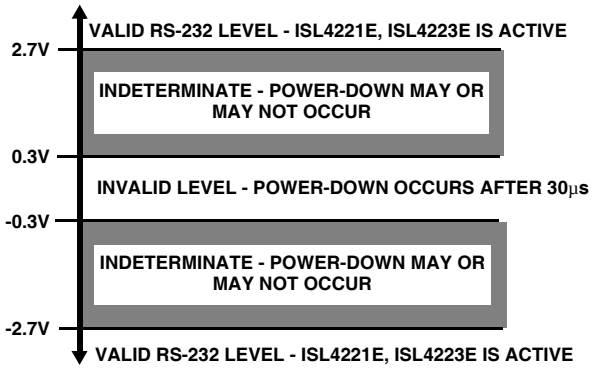


FIGURE 6. DEFINITION OF VALID RS-232 RECEIVER LEVELS

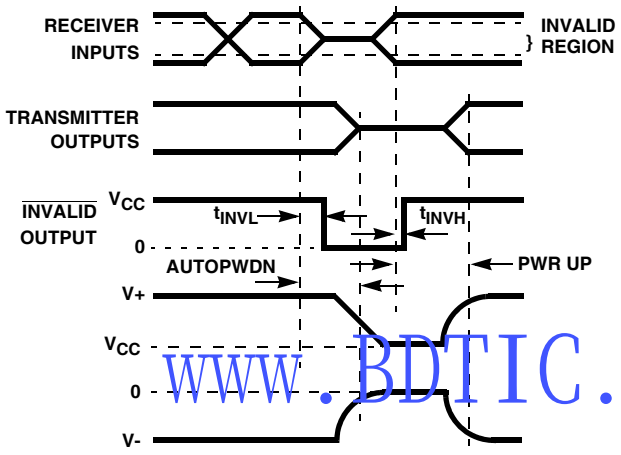


FIGURE 7. AUTOMATIC POWER-DOWN AND $\overline{\text{INVALID}}$ TIMING DIAGRAMS

Automatic Power-down (Excluding ISL3232E)

Even greater power savings is available by using the automatic power-down function. When no valid RS-232 voltages (see Figure 6) are sensed on any receiver input for 30µs, the charge pump and transmitters power-down, thereby reducing supply current to 150nA. Invalid receiver levels occur whenever the driving peripheral's outputs are shut off (powered down) or when the RS-232 interface cable is disconnected. The ISL4221E, ISL4223E powers back up whenever it detects a valid RS-232 voltage level on any receiver input. This automatic power-down feature provides additional system power savings without changes to the existing operating system.

Automatic power-down operates when the FORCEON input is low, and the $\overline{\text{FORCEOFF}}$ input is high. Tying FORCEON high disables automatic power-down, but manual power-down is always available via the overriding $\overline{\text{FORCEOFF}}$ input. Table 2 summarizes the automatic power-down functionality.

Some applications may need more time to wake up from shutdown. If automatic power-down is being utilized, the RS-232 device will re-enter power-down if valid receiver levels aren't reestablished within 30µs of the ISL4221E, ISL4223E powering up. Figure 5 illustrates a circuit that keeps the ISL4221E, ISL4223E from initiating automatic power-down for 100ms after powering up. This gives the slow-to-wake peripheral circuit time to re-establish valid RS-232 output levels.

The time to recover from automatic power-down mode is typically 100µs.

$\overline{\text{INVALID}}$ Output (Excluding ISL3232E)

The $\overline{\text{INVALID}}$ output always indicates whether or not a valid RS-232 signal (see Figure 6) is present at any of the receiver inputs (see Table 2), giving the user an easy way to determine when the interface block should power down. Invalid receiver levels occur whenever the driving peripheral's outputs are shut off (powered down) or when the RS-232 interface cable is disconnected. In the case of a disconnected interface cable where all the receiver inputs are floating (but pulled to GND by the internal receiver pull down resistors), the $\overline{\text{INVALID}}$ logic detects the invalid levels and drives the output low. The power management logic then uses this indicator to power-down the interface block. Reconnecting the cable restores valid levels at the receiver inputs, $\overline{\text{INVALID}}$ switches high, and the power management logic wakes up the interface block. $\overline{\text{INVALID}}$ can also be used to indicate the DTR or RING INDICATOR signal, as long as the other receiver inputs are floating, or driven to GND (as in the case of a powered down driver).

$\overline{\text{INVALID}}$ switches low after invalid levels have persisted on all of the receiver inputs for more than 30µs (see Figure 7). $\overline{\text{INVALID}}$ switches back high 1µs after detecting a valid RS-232 level on a receiver input. $\overline{\text{INVALID}}$ operates in all modes (forced or automatic power-down, or forced on), so it is also useful for systems employing manual power-down circuitry. When automatic power-down is utilized, $\overline{\text{INVALID}}$ = 0 indicates that the ISL4221E, ISL4223E is in power-down mode.

Capacitor Selection

The charge pumps require 0.1µF, or greater, capacitors for proper operation. Increasing the capacitor values (by a factor of 2) reduces ripple on the transmitter outputs and slightly reduces power consumption.

When using minimum required capacitor values, make sure that capacitor values do not degrade excessively with temperature. If in doubt, use capacitors with a larger nominal value. The capacitor's equivalent series resistance (ESR) usually rises at low temperatures and it influences the amount of ripple on V+ and V-.

Power Supply Decoupling

In most circumstances a 0.1µF bypass capacitor is adequate. In applications that are particularly sensitive to power supply noise, decouple V_{CC} to ground with a capacitor of the same value as the charge-pump capacitor C_1. Connect the bypass capacitor as close as possible to the IC.

Transmitter Outputs when Exiting Power-down

Figure 8 shows the response of two transmitter outputs when exiting power-down mode. As they activate, the two transmitter outputs properly go to opposite RS-232 levels, with no glitching, ringing, nor undesirable transients. Each transmitter is loaded with 3kΩ in parallel with 2500pF.

Note that the transmitters enable only when the magnitude of the supplies exceed approximately 3V.

Operation Down to 2.7V

ISL4221E, ISL4223E and ISL3232E transmitter outputs meet RS-562 levels (±3.7V), at the full data rate, with V_{CC} as low as 2.7V. RS-562 levels typically ensure inter operability with RS-232 devices.

High Data Rates

The ISL4221E, ISL4223E and ISL3232E maintain the RS-232 ±5V minimum transmitter output voltages even at high data rates. Figure 9 details a transmitter loopback test circuit, and Figure 10 illustrates the loopback test result at 120kbps. For this test, all transmitters were simultaneously driving RS-232 loads in parallel with 1000pF, at 120kbps. Figure 11 shows the loopback results for a single transmitter driving 1000pF and an RS-232 load at 250kbps. The static transmitters were also loaded with an RS-232 receiver.

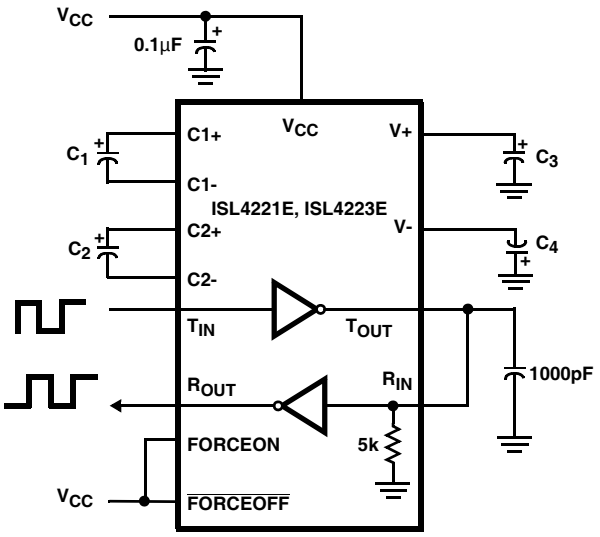


FIGURE 9. TRANSMITTER LOOPBACK TEST CIRCUIT

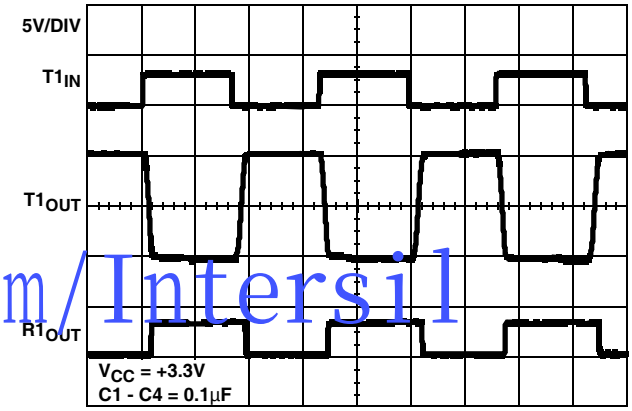


FIGURE 10. LOOPBACK TEST AT 120kbps

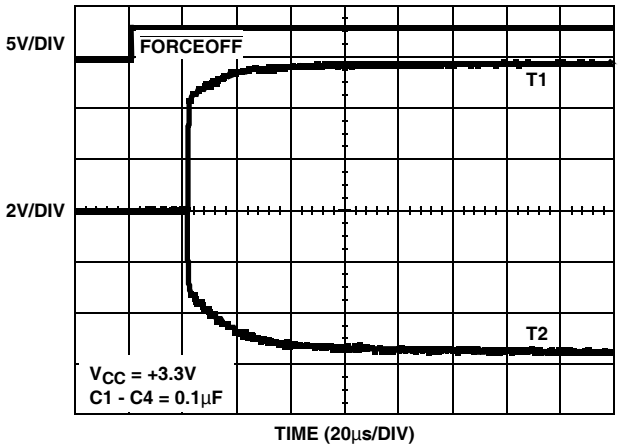


FIGURE 8. TRANSMITTER OUTPUTS WHEN EXITING POWER-DOWN

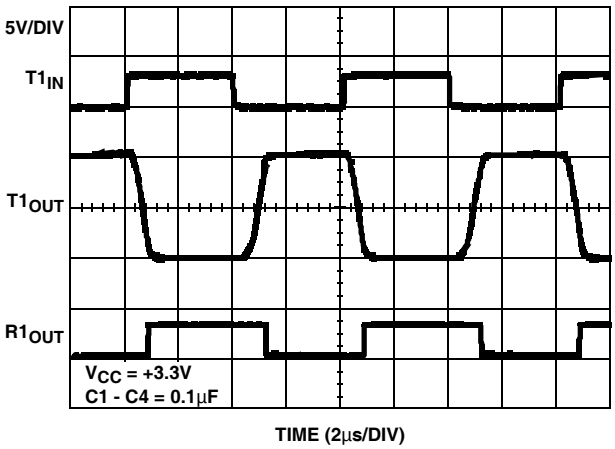


FIGURE 11. LOOPBACK TEST AT 250kbps

Interconnection with 3V and 5V Logic

The ISL4221E, ISL4223E and ISL3232E directly interface with 5V CMOS and TTL logic families. Nevertheless, with the ISL4221E, ISL4223E and ISL3232E at 3.3V, and the logic supply at 5V, AC, HC, and CD4000 outputs can properly drive ISL4221E, ISL4223E and ISL3232E inputs, but ISL4221E, ISL4223E and ISL3232E outputs do not reach the minimum V_{IH} for these logic families. See Table 3 for more information.

TABLE 3. LOGIC FAMILY COMPATIBILITY WITH VARIOUS SUPPLY VOLTAGES

SYSTEM POWER-SUPPLY VOLTAGE (V)	V_{CC} SUPPLY VOLTAGE (V)	COMPATIBILITY
3.3	3.3	Compatible with all CMOS families.
5	5	Compatible with all TTL and CMOS logic families.
5	3.3	Compatible with ACT and HCT CMOS, and with TTL. ISL4221E, ISL4223E and ISL3232E outputs are incompatible with AC, HC, and CD4000 CMOS inputs.

±15kV ESD Protection

All pins on ISL4221E, ISL4223E and ISL3232E devices include ESD protection structures, but the RS-232 pins (transmitter outputs and receiver inputs) incorporate advanced structures, which allow them to survive ESD events up to ±15kV. The RS-232 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins, or connecting a cable, can cause an ESD event that might destroy unprotected ICs. These new ESD structures protect the device whether or not it is powered-up, protect without allowing any latchup mechanism to activate, and don't interfere with RS-232 signals as large as ±25V.

Human Body Model (HBM) Testing

As the name implies, this test method emulates the ESD event delivered to an IC during human handling. The tester delivers the charge through a 1.5kΩ current limiting resistor, making the test less severe than the IEC61000 test which utilizes a 330Ω limiting resistor. The HBM method determines an ICs ability to withstand the ESD transients typically present during handling and manufacturing. Due to the random nature of these events, each pin is tested with respect to all other pins. The RS-232 pins on "E" family devices can withstand HBM ESD events to ±15kV.

IEC61000-4-2 Testing

The IEC61000-4-2 test method applies to finished equipment, rather than to an individual IC. Therefore, the pins most likely to suffer an ESD event are those that are exposed to the outside world (the RS-232 pins in this case), and the IC is tested in its typical application configuration (power applied) rather than testing each pin-to-pin combination. The lower current limiting resistor coupled with the larger charge storage capacitor yields a test that is much more severe than the HBM test. The extra ESD protection built into this device's RS-232 pins allows the design of equipment meeting level 4 criteria without the need for additional board level protection on the RS-232 port.

AIR-GAP DISCHARGE TEST METHOD

For this test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on approach speed, humidity, temperature, etc., so it is difficult to obtain repeatable results. The "E" device RS-232 pins withstand ±15kV air-gap discharges.

CONTACT DISCHARGE TEST METHOD

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized, thereby eliminating the variables associated with the air-gap discharge. The result is a more repeatable and predictable test, but equipment limits prevent testing devices at voltages higher than ±8kV. All "E" family devices survive ±8kV contact discharges on the RS-232 pins.

Typical Performance Curves V_{CC} = 3.3V, T_A = +25°C

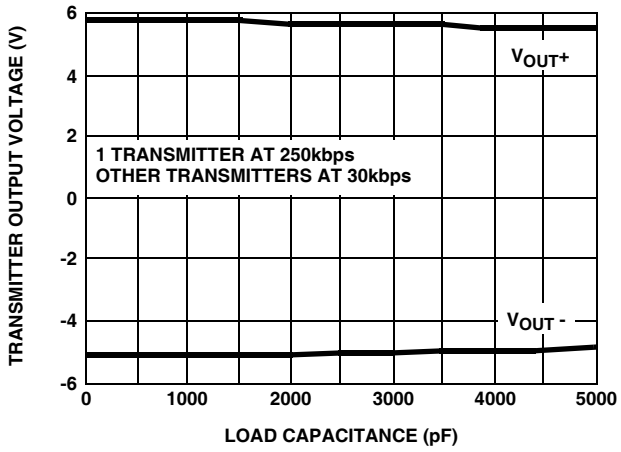


FIGURE 12. TRANSMITTER OUTPUT VOLTAGE vs LOAD CAPACITANCE

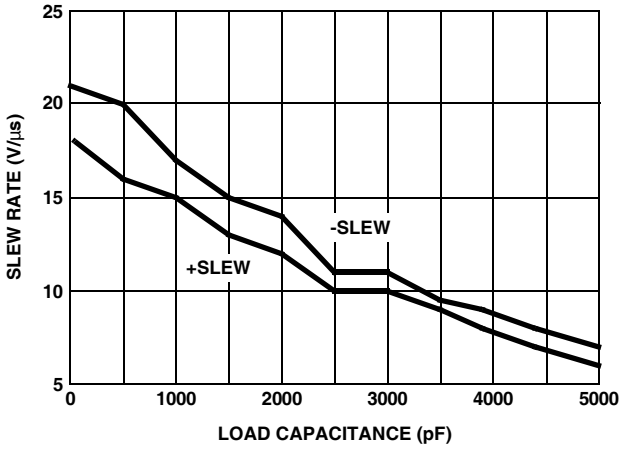


FIGURE 13. SLEW RATE vs LOAD CAPACITANCE

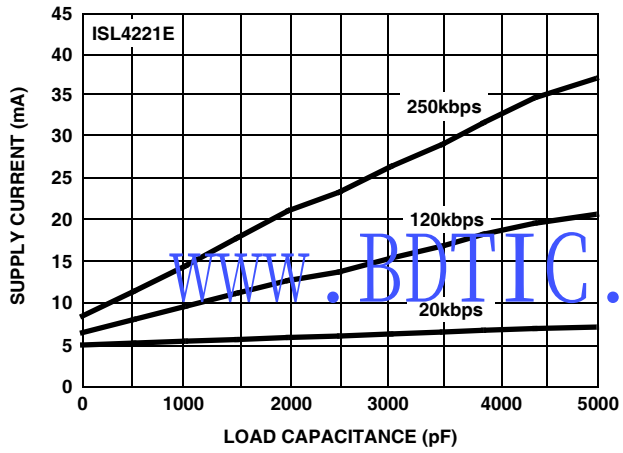


FIGURE 14. SUPPLY CURRENT vs LOAD CAPACITANCE WHEN TRANSMITTING DATA

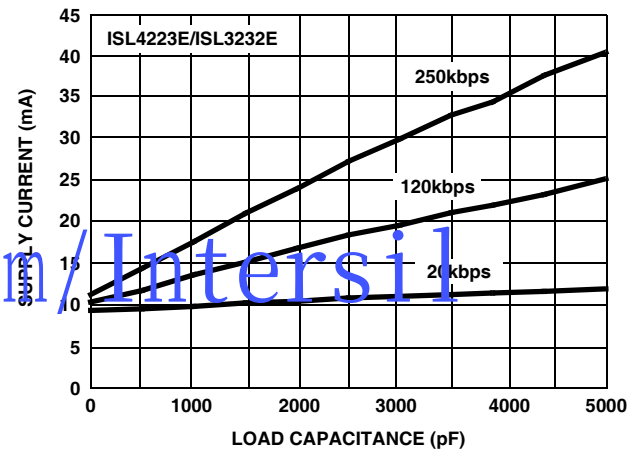


FIGURE 15. SUPPLY CURRENT vs LOAD CAPACITANCE WHEN TRANSMITTING DATA

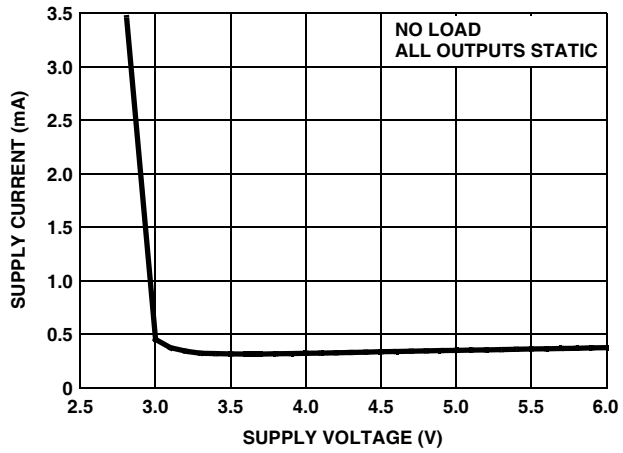


FIGURE 16. SUPPLY CURRENT vs SUPPLY VOLTAGE

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND

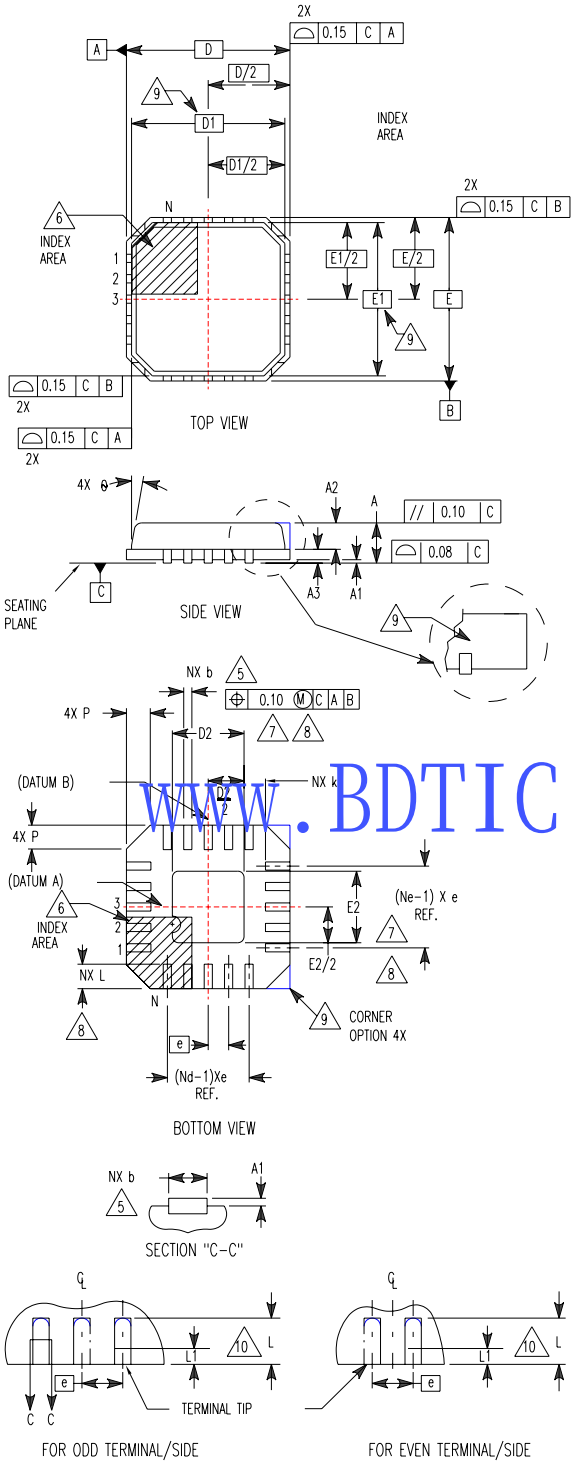
TRANSISTOR COUNT:

ISL3232E: 296
ISL4221E: 286
ISL4223E: 357

PROCESS:

Si Gate CMOS

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.5x5B

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VHHB ISSUE C)

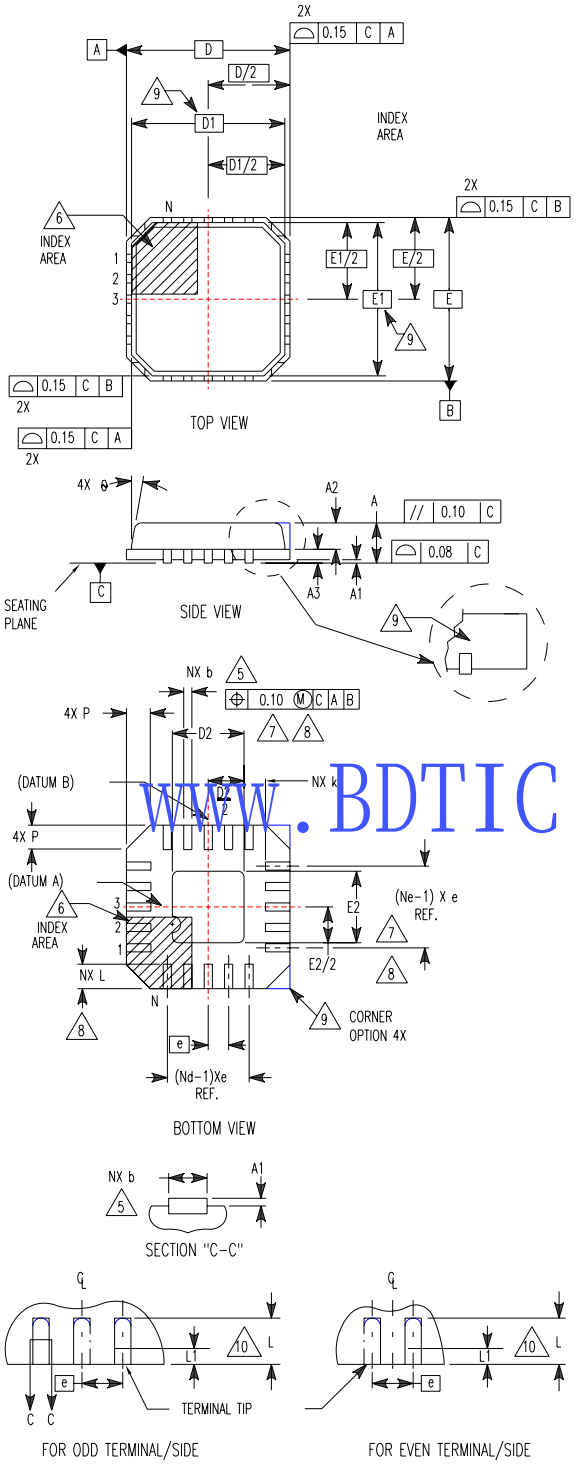
SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.28	0.33	0.40	5, 8
D		5.00 BSC		-
D1		4.75 BSC		9
D2	2.95	3.10	3.25	7, 8
E		5.00 BSC		-
E1		4.75 BSC		9
E2	2.95	3.10	3.25	7, 8
e		0.80 BSC		-
k	0.25	-	-	-
L	0.35	0.60	0.75	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 1 10/02

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L20.5x5
20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	0.02	0.05	-
A2	-	0.65	1.00	9
A3		0.20 REF		9
b	0.23	0.30	0.38	5, 8
D		5.00 BSC		-
D1		4.75 BSC		9
D2	2.95	3.10	3.25	7, 8
E		5.00 BSC		-
E1		4.75 BSC		9
E2	2.95	3.10	3.25	7, 8
e		0.65 BSC		-
k	0.20	-	-	-
L	0.35	0.60	0.75	8
N		20		2
Nd		5		3
Ne		5		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 4 11/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Compliant to JEDEC MO-220VHHC Issue I except for the "b" dimension.