

### Low Noise, Low Power I<sup>2</sup>C® Bus, 128 Taps

The ISL22316WMUEP integrates a single digitally controlled potentiometer (DCP) and non-volatile memory on a monolithic CMOS integrated circuit.

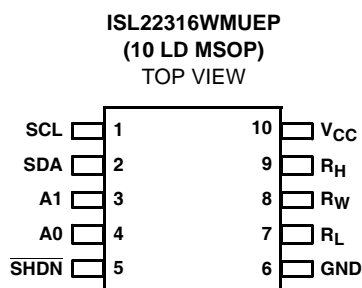
The digitally controlled potentiometer is implemented with a combination of resistor elements and CMOS switches. The position of the wipers are controlled by the user through the I<sup>2</sup>C bus interface. The potentiometer has an associated volatile Wiper Register (WR) and a non-volatile Initial Value Register (IVR) that can be directly written to and read by the user. The contents of the WR controls the position of the wiper. At power-up, the device recalls the contents of the DCP's IVR to the WR.

The DCP can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including control, parameter adjustments and signal processing.

### Device Information

The specifications for an Enhanced Product (EP) device are defined in a Vendor Item Drawing (VID), which is controlled by the Defense Supply Center in Columbus (DSCC). "Hot-links" to the applicable VID and other supporting application information are provided on our website.

### Pinout



### Ordering Information

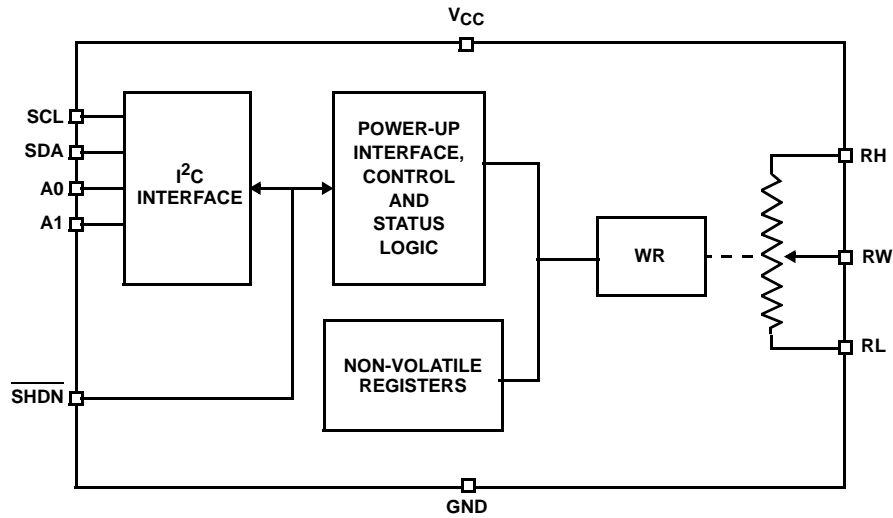
VENDOR PART NUMBER (Notes 1, 2)	VENDOR ITEM DRAWING	PART MARKING	RESISTANCE OPTION (kΩ)	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL22316WMUEP	V62/08603-01XB	2316M	10	-55 to +125	10 Ld MSOP	M10.118

#### NOTES:

1. Add "-TK" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. Devices must be procured to the VENDOR PART NUMBER.

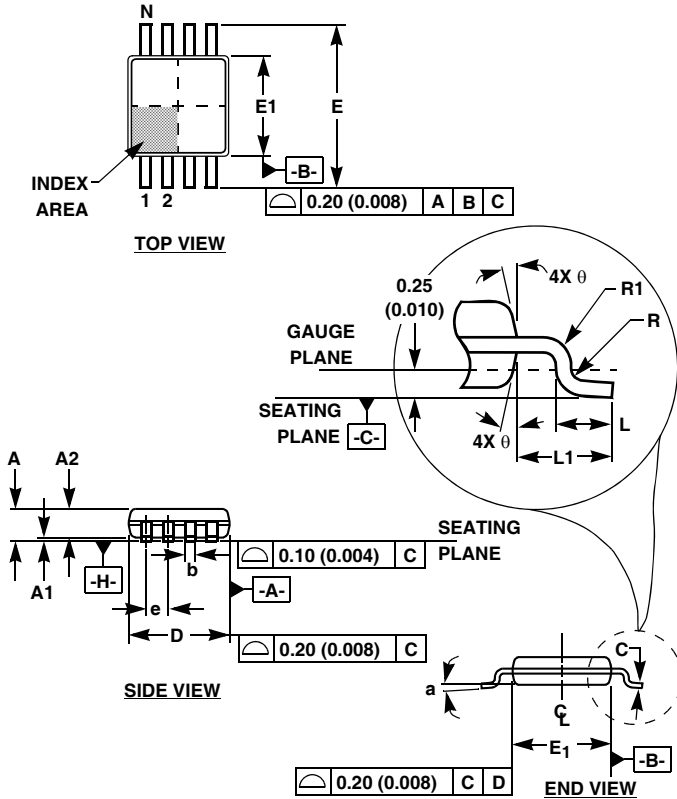
### Features

- Specifications per DSCC VID V62/08603-01XB
- Full Mil-Temp Electrical Performance from -55°C to +125°C
- Controlled Baseline with One Wafer Fabrication Site and One Assembly/Test Site
- Full Homogeneous Lot Processing in Wafer Fab
- No Combination of Wafer Fabrication Lots in Assembly
- Full Traceability Through Assembly and Test by Date/Trace Code Assignment
- Enhanced Process Change Notification
- Enhanced Obsolescence Management
- Eliminates Need for Up-Screening a COTS Component
- 128 Resistor Taps
- I<sup>2</sup>C Serial Interface
  - Two Address Pins, Up To Four Devices/Bus
- Non-volatile Storage of Wiper Position
- Wiper Resistance: 70Ω Typical @ 3.3V Shutdown Mode
- Shutdown Current 5μA Max
- Power Supply: 2.7V to 5.5V
- 10kΩ Total Resistance
- High Reliability
  - Endurance: 1,000,000 Data Changes Per Bit Per Register
  - Register Data Retention:
    - 10 years @ T ≤ +125°C
    - 15 years @ T ≤ +90°C
    - 50 years @ T ≤ +55°C
- 10 Ld MSOP

**Block Diagram****Pin Descriptions**

MSOP PIN	SYMBOL	DESCRIPTION
1	SCL	Open drain I <sup>2</sup> C interface clock input
2	SDA	Open drain Serial data I/O for the I <sup>2</sup> C interface
3	A1	Device address input for the I <sup>2</sup> C interface
4	A0	Device address input for the I <sup>2</sup> C interface
5	SHDN	Shutdown active low input
6	GND	Device ground pin
7	R <sub>L</sub>	"Low" terminal of DCP
8	R <sub>W</sub>	"Wiper" terminal of DCP
9	R <sub>H</sub>	"High" terminal of DCP
10	V <sub>CC</sub>	Power supply pin

## Mini Small Outline Plastic Packages (MSOP)



**M10.118 (JEDEC MO-187BA)**  
10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.007	0.011	0.18	0.27	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.020 BSC		0.50 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	10		10		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
θ	5°	15°	5°	15°	-
α	0°	6°	0°	6°	-

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## NOTES:

- These package dimensions are within allowable dimensions of JEDEC MO-187BA.
- Dimensioning and tolerancing per ANSI Y14.5M-1994.
- Dimension "D" does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
- Dimension "E1" does not include interlead flash or protrusions and are measured at Datum Plane.  $\boxed{-H-}$  Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
- Formed leads shall be planar with respect to one another within 0.10mm (.004) at seating Plane.
- "L" is the length of terminal for soldering to a substrate.
- "N" is the number of terminal positions.
- Terminal numbers are shown for reference only.
- Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
- Datums  $\boxed{-A-}$  and  $\boxed{-B-}$  to be determined at Datum plane  $\boxed{-H-}$ .
- Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

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