Data Sheet | August 2002 | FN2914.4

150MHz, Fast Settling Operational Amplifiers

HA-5190/5195 are operational amplifiers featuring a combination of speed, precision, and bandwidth. Employing monolithic bipolar construction coupled with Dielectric Isolation, these devices are capable of delivering 200V/µs slew rate with a settling time of 70ns (0.1%, 5V output step). These truly differential amplifiers are designed to operate at gains ≥ 5 without the need for external compensation. Other outstanding HA-5190/5195 features are 150MHz gain bandwidth product and 6.5MHz full power bandwidth. In addition to these dynamic characteristics, these amplifiers also have excellent input characteristics such as 3mV offset voltage and 6.0nV/√Hz input voltage noise at 1kHz.

With 200V/µs slew rate and 70ns settling time, these devices make ideal output amplifiers for accurate, high speed D/A converters or the main components in high speed sample/hold circuits. The 5190/5195 are also ideally suited for a variety of pulse and wideband video amplifiers. Please refer to Application Notes AN525 and AN526 for some of these application designs.

At temperatures above 75°C a heat sink is required for the HA-5190 (see Note 2 and Application Note AN550). For military versions, please request the HA-5190/883 data sheet.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA1-5190-2	-55 to 125	14 Ld CERDIP	F14.3
HA1-5195-5	0 to 75	14 Ld CERDIP	F14.3

Features

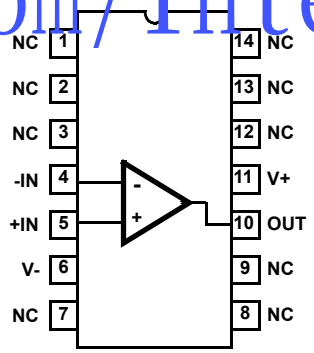
- Fast Settling Time (0.1%) 70ns
- Very High Slew Rate 200V/µs
- Wide Gain-Bandwidth ($A_V \geq 5$) 150MHz
- Full Power Bandwidth 6.5MHz
- Low Offset Voltage 3mV
- Input Noise Voltage . . . . . 6nV/√Hz
- Bipolar D.I. Construction

Applications

- Fast, Precise D/A Converters
- High Speed Sample-Hold Circuits
- Pulse and Video Amplifiers
- Wideband Amplifiers

Pinout

HA-5190/95 (CERDIP)
TOP VIEW



Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (V+ to V-) 35V
Differential Input Voltage 6V
Output Current . . . . . 50mA (Peak)

Operating Conditions

Temperature Range
HA-5190-2 . . . . . -55^oC to 125^oC
HA-5195-5 . . . . . 0^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	75	20

Maximum Junction Temperature (Hermetic Package, Note 1) . . 175^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Heat sinking may be required, especially at $T_A \geq 75^oC$.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{SUPPLY} = \pm15V$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (^oC)	HA-5190-2			HA-5195-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Offset Voltage		25	-	3	5	-	3	6	mV
		Full	-	-	10	-	-	10	mV
Average Offset Voltage Drift		Full	-	20	-	-	20	-	$\mu V/^oC$
Bias Current		25	-	5	15	-	5	15	µA
		Full	-	-	20	-	-	20	µA
Offset Current		25	-	1	4	-	1	4	µA
		Full	-	-	6	-	-	6	µA
Input Resistance		25	-	10	-	-	10	-	MΩ
Input Capacitance		25	-	1	-	-	1	-	pF
Common Mode Range		Full	±5	-	-	±5	-	-	V
Input Noise Current	f = 1kHz, R_G = 0Ω	25	-	5	-	-	5	-	$pA/\sqrt{Hz}$
Input Noise Voltage	f = 1kHz, R_G = 0Ω	25	-	6	-	-	6	-	$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain (Note 3)		25	15	30	-	10	30	-	kV/V
		Full	5	-	-	5	-	-	kV/V
Common Mode Rejection Ratio	ΔV_{CM} = ±5V	Full	74	95	-	74	95	-	dB
Minimum Stable Gain		25	5	-	-	5	-	-	V/V
Gain-Bandwidth-Product	V_{OUT} = 90mV, A_V = 10	25	-	150	-	150	-	-	MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing (Note 3)		Full	±5	±8	-	±5	±8	-	V
Output Current (Note 3)		25	±25	±30	-	±25	±30	-	mA
Output Resistance	Open Loop	25	-	30	-	-	30	-	Ω
Full Power Bandwidth (Notes 3, 4)		25	5	6.5	-	5	6.5	-	MHz
TRANSIENT RESPONSE (Note 5)									
Rise Time		25	-	13	18	-	13	18	ns
Overshoot		25	-	8	-	-	8	-	%
Slew Rate		25	160	200	-	160	200	-	V/µs
Settling Time (Note 5)	5V Step to 0.1%	25	70	-	-	70	-	-	ns
	5V Step to 0.01%	25	-	100	-	-	100	-	ns
	2.5V Step to 0.1%	25	-	50	-	-	50	-	ns
	2.5V Step to 0.01%	25	-	80	-	-	80	-	ns

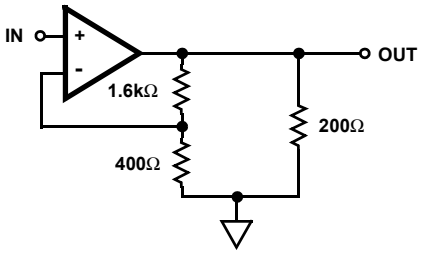
Electrical Specifications V_{SUPPLY} = ±15V, Unless Otherwise Specified (Continued)

PARAMETER	TEST CONDITIONS	TEMP (°C)	HA-5190-2			HA-5195-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY CHARACTERISTICS									
Supply Current		Full	-	19	28	-	19	28	mA
Power Supply Rejection Ratio	ΔV_S = ±10V to ±20V	Full	70	90	-	70	90	-	dB

NOTES:

3. R_L = 200Ω, C_L < 10pF, V_{OUT} = ±5V.
4. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
5. Refer to Test Circuits section of the data sheet.

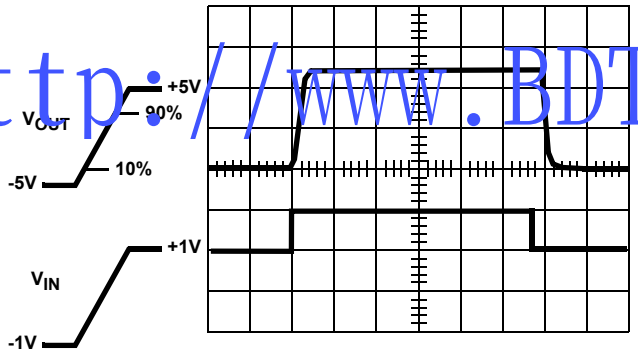
Test Circuits and Waveforms



NOTES:

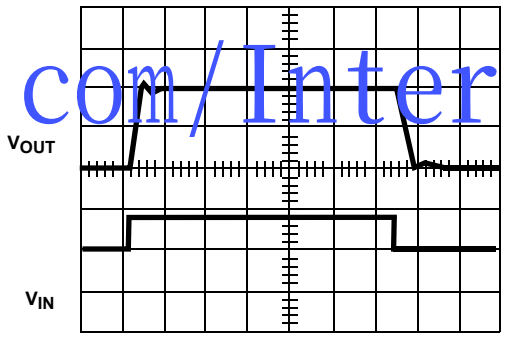
6. A_V = 5.
7. C_L < 10pF.

FIGURE 1. LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT



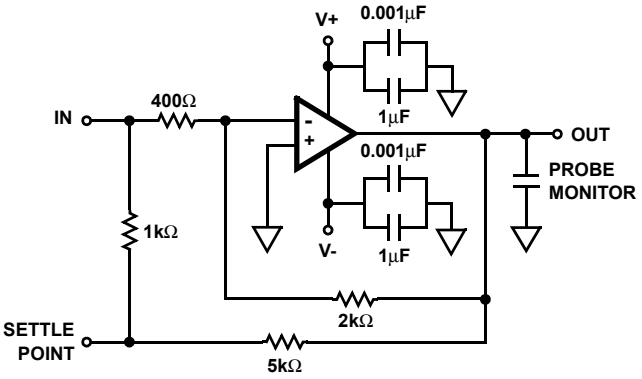
Vertical Scale: V_{IN} = 2.0V/Div., V_{OUT} = 4.0/Div.
Horizontal Scale: 100ns/Div.

LARGE SIGNAL RESPONSE



Vertical Scale: V_{IN} = 50mV/Div., V_{OUT} = 100mV/Div.
Horizontal Scale: 100ns/Div

SMALL SIGNAL RESPONSE

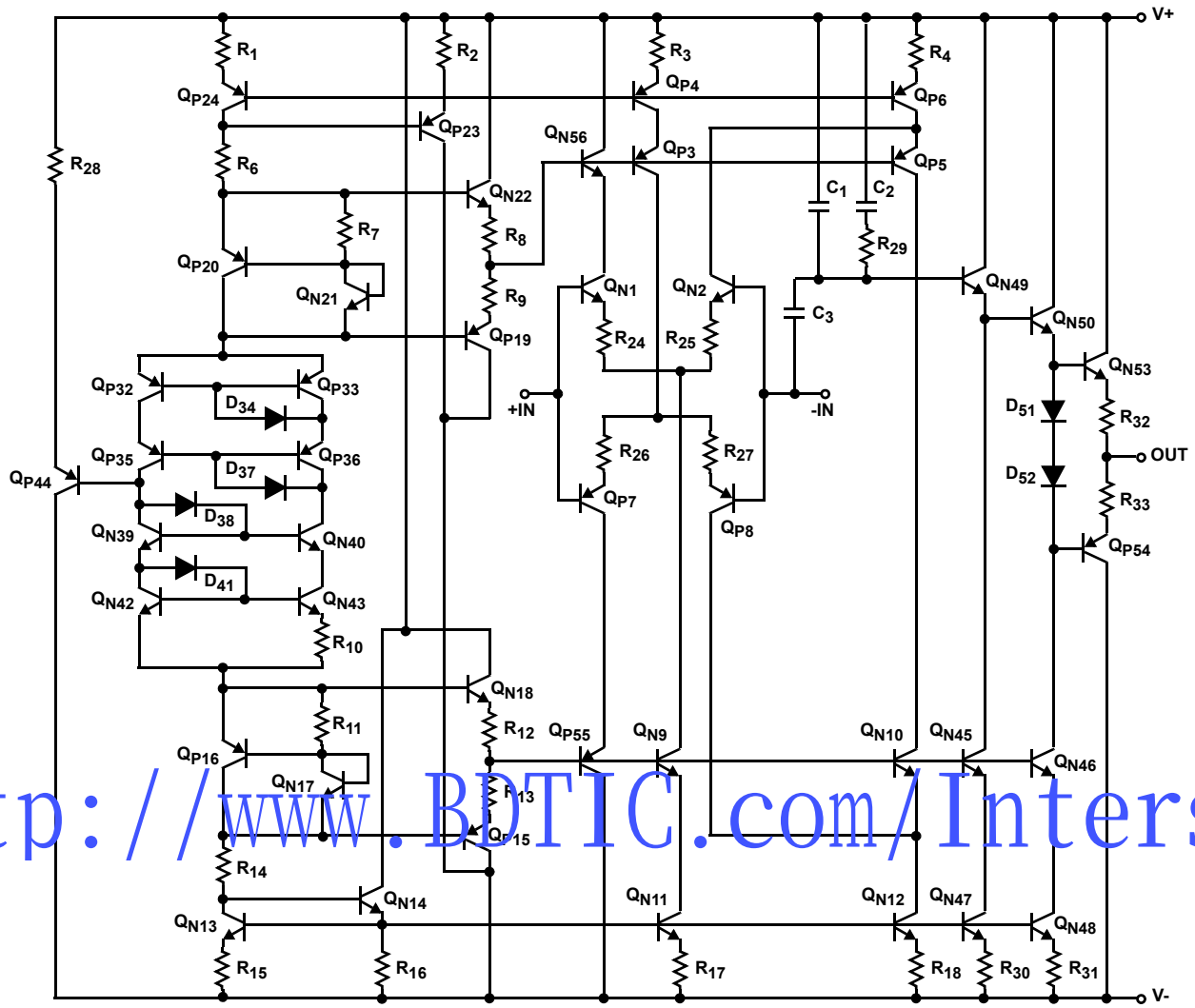


NOTES:

8. A_V = -5.
9. Load Capacitance should be less than 10pF.
10. It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched to 0.1%.
11. Settle Point (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

FIGURE 2. SETTLING TIME TEST CIRCUIT

Schematic Diagram



Application Information

Power Supply Decoupling

Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01µF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

Stability Considerations

HA-5190/5195 is stable at gains > 5. Gains < 5 are covered below. Feedback resistors should be of carbon composition located as near to the input terminals as possible.

Wiring Considerations

Video pulse circuits should be built on a ground plane. Minimum point to point connections directly to the amplifier terminals should be used. When ground planes cannot be used, good single point grounding techniques should be applied.

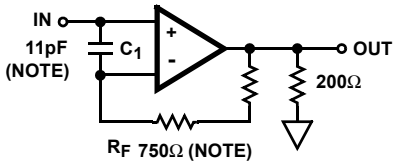
Output Short Circuit

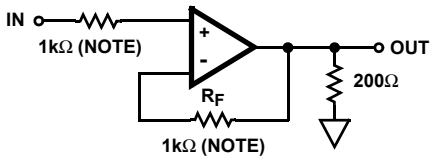
HA-5190/5195 does not have output short circuit protection. Short circuits to ground can be tolerated for approximately 10 seconds. Short circuits to either supply will result in immediate destruction of the device.

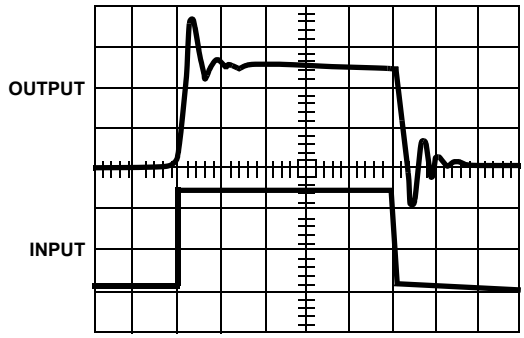
Heavy Capacitive Loads

When driving heavy capacitive loads (>100pF) a small resistor (100Ω) should be connected in series with the output and inside the feedback loop.

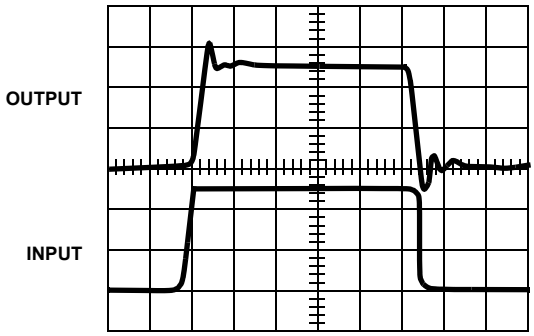
Typical Applications (Also see Application Notes AN525 and AN526)







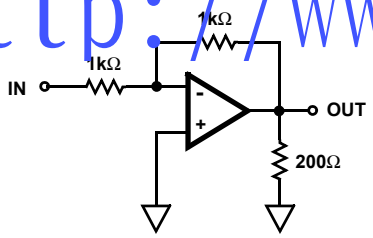
Vertical Scale: 2V/Div.
Horizontal Scale: 100ns/Div.

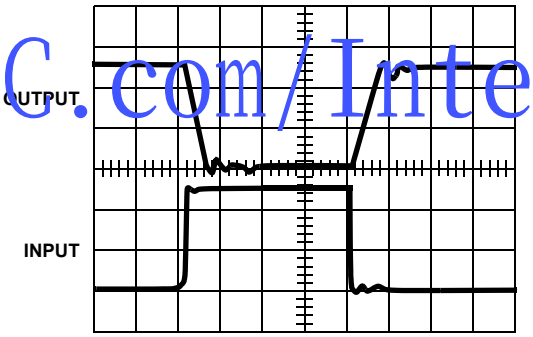


Vertical Scale: 2V/Div.
Horizontal Scale: 100ns/Div

NOTE: Values were determined experimentally for optimum speed and settling time. R_F and C_1 should be optimized for each particular application to ensure best overall frequency response.

FIGURE 3. SUGGESTED COMPENSATION FOR NONINVERTING UNITY GAIN AMPLIFIER





Vertical Scale: 2V/Div.
Horizontal Scale: 50ns/Div.

FIGURE 4. SUGGESTED COMPENSATION FOR INVERTING UNITY GAIN AMPLIFIER

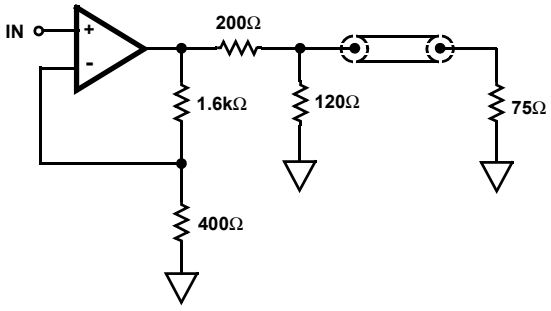


FIGURE 5. VIDEO PULSE AMPLIFIER/75Ω COAXIAL DRIVER

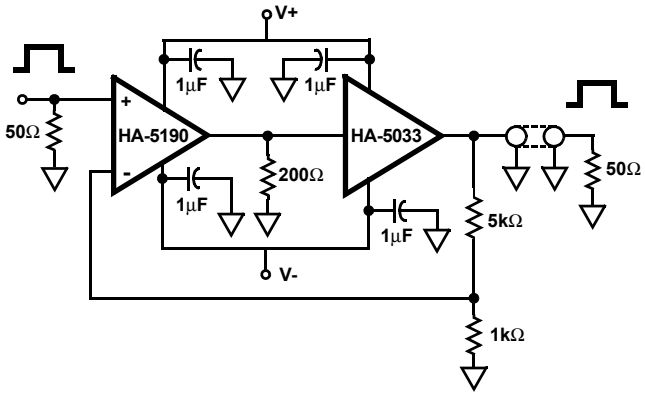


FIGURE 6. VIDEO PULSE AMPLIFIER COAXIAL LINE DRIVER

Typical Performance Curves $V_S = \pm15V$, $T_A = 25^oC$, Unless Otherwise Specified

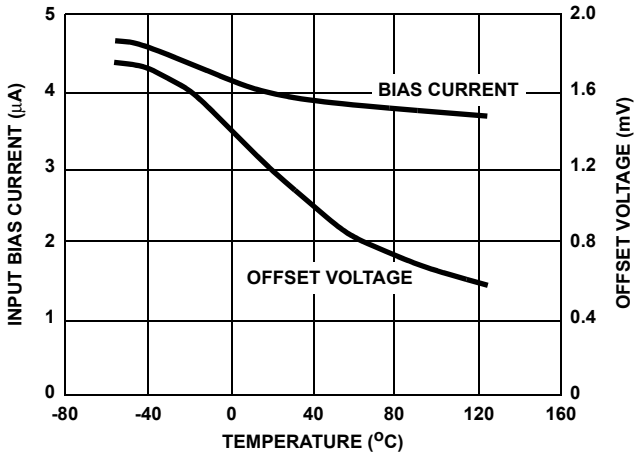


FIGURE 7. INPUT OFFSET VOLTAGE AND BIAS CURRENT vs TEMPERATURE

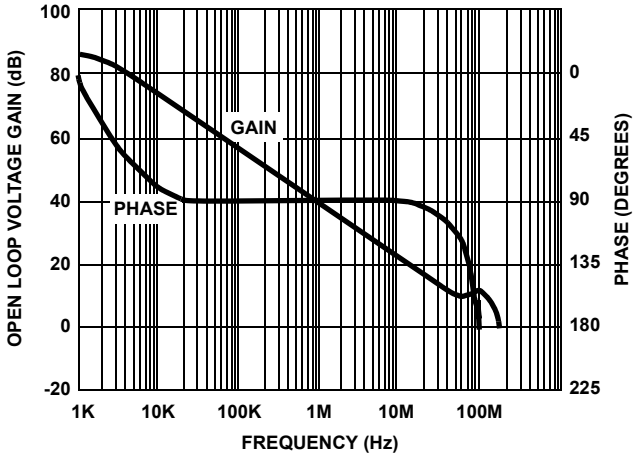


FIGURE 8. OPEN LOOP FREQUENCY RESPONSE

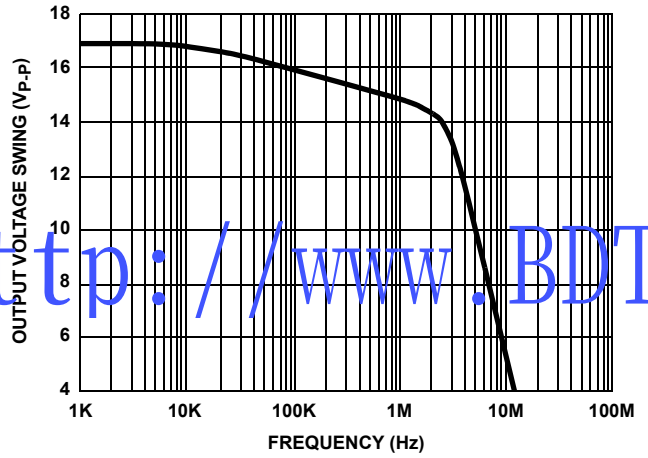


FIGURE 9. OUTPUT VOLTAGE SWING vs FREQUENCY

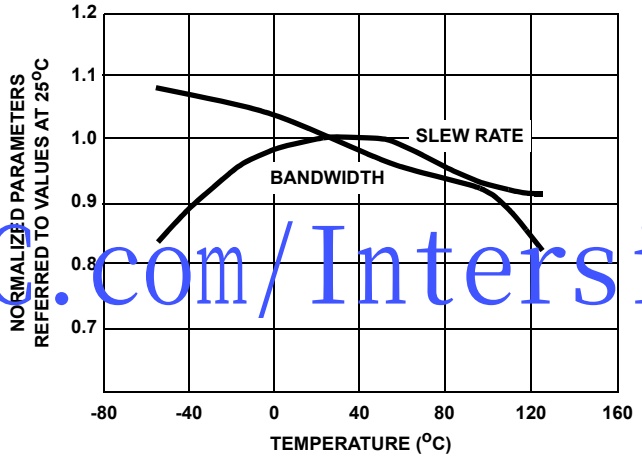


FIGURE 10. NORMALIZED AC PARAMETERS vs TEMPERATURE

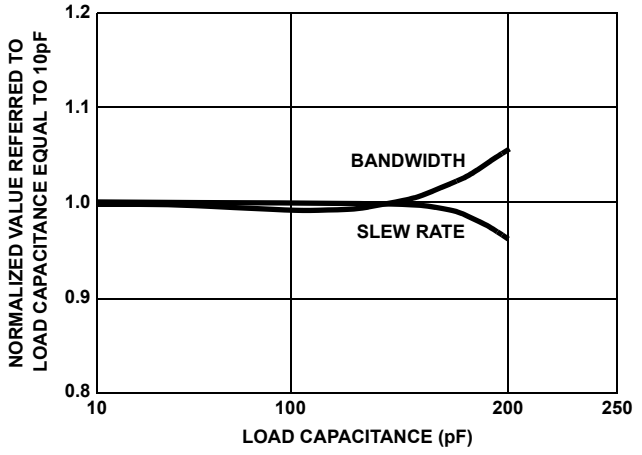


FIGURE 11. NORMALIZED AC PARAMETERS vs LOAD CAPACITANCE

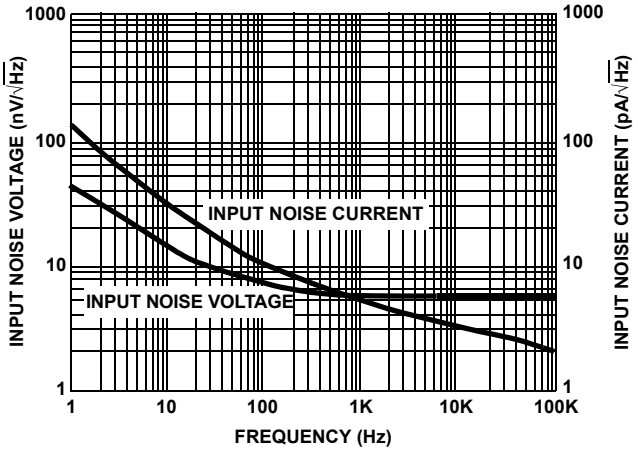


FIGURE 12. INPUT NOISE VOLTAGE AND NOISE CURRENT vs FREQUENCY

Typical Performance Curves $V_S = \pm15V$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

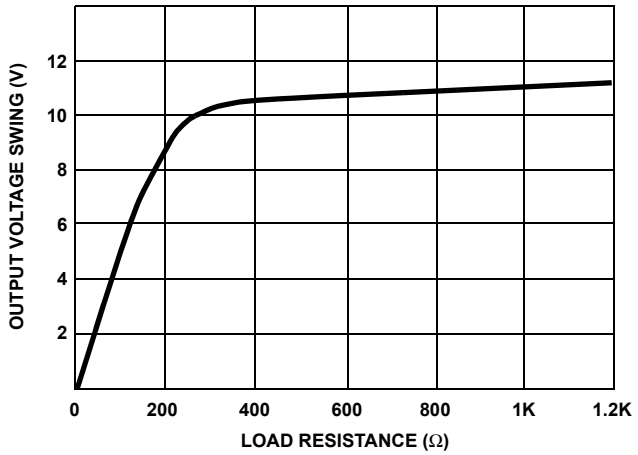


FIGURE 13. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

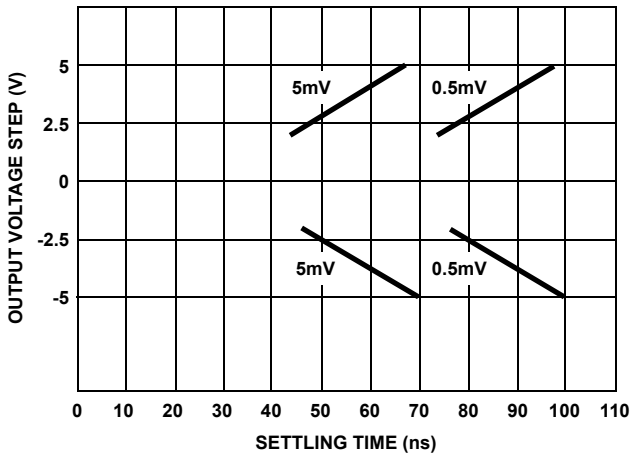


FIGURE 14. SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES

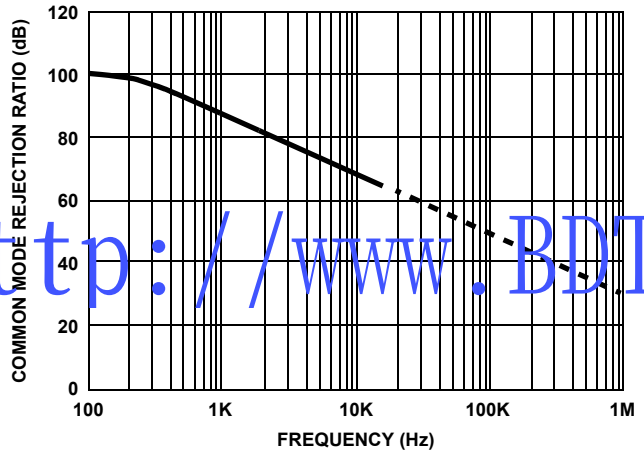


FIGURE 15. COMMON MODE REJECTION RATIO vs FREQUENCY

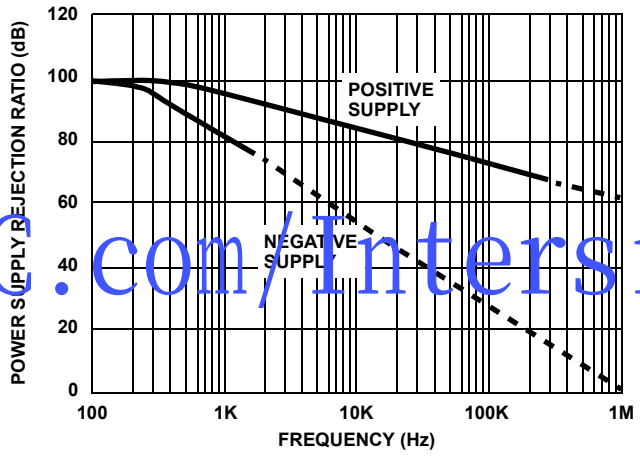


FIGURE 16. POWER SUPPLY REJECTION RATIO vs FREQUENCY

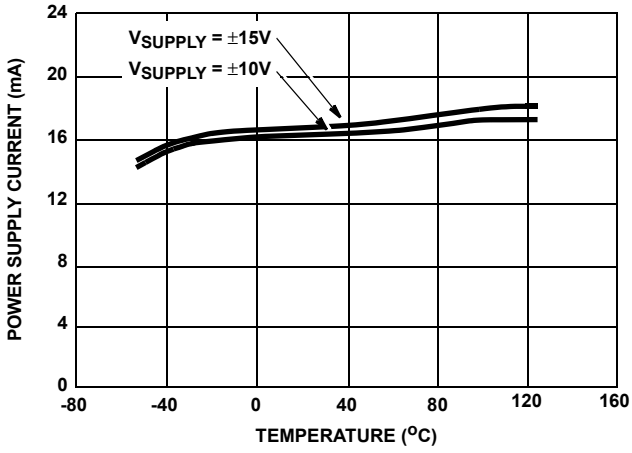


FIGURE 17. POWER SUPPLY CURRENT vs TEMPERATURE

Die Characteristics

DIE DIMENSIONS:

54 mils x 88 mils x 19 mils
1360µm x 2240µm x 483µm

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

TRANSISTOR COUNT:

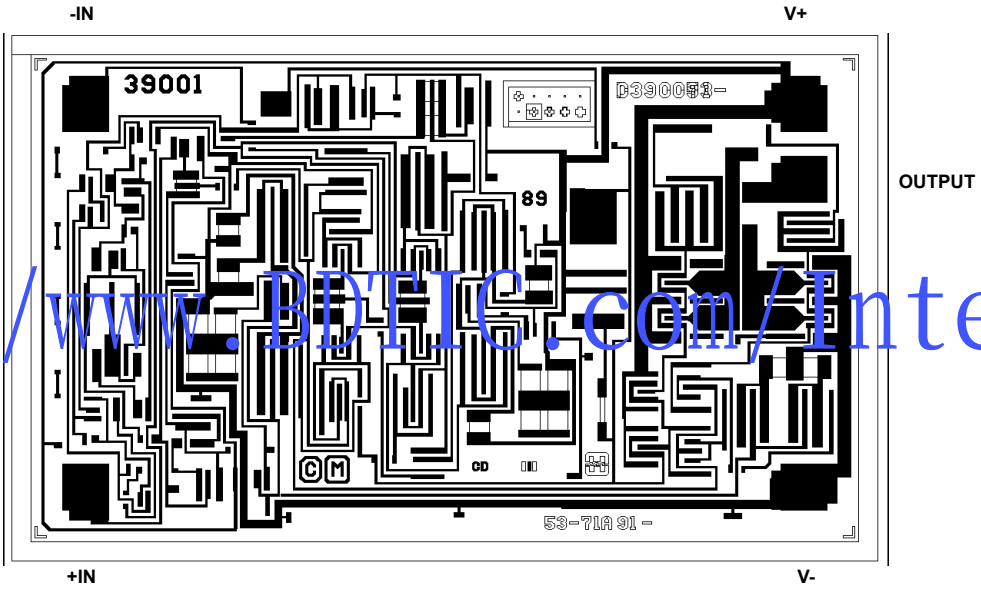
49

PROCESS:

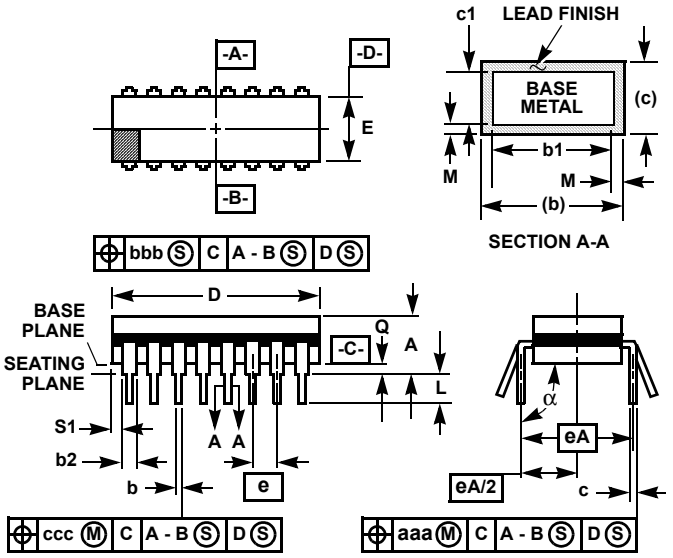
Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5190



Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



F14.3 MIL-STD-1835 GDIP1-T14 (D-1, CONFIGURATION A)
14 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	14		14		8

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.