Data Sheet | August 17, 2005 | FN3931.1

Low Noise, High Performance Operational Amplifier

The HA-5101/883 is a dielectrically isolated operational amplifier featuring low noise and high performance. This amplifier has an excellent noise voltage density of 4.5nV/$\sqrt{Hz}$ (max) at 1kHz. The unity gain stable HA-5101/883 yields a 10MHz unity gain bandwidth and a 6V/µs slew rate.

DC characteristics of the HA-5101/883 assure accurate performance. The 3mV (max) offset voltage is externally adjustable and offset voltage drift is just 3µV/°C. Low bias currents (200nA max) reduce input current errors and the high open loop voltage gain of 100kV/V, over temperature, increases the loop gain for low distortion amplification.

The HA-5101/883 is ideal for audio applications, especially low-level signal amplifiers such as microphone, tape head and preamplifiers. Additionally, it is well suited for low distortion oscillators, low noise function generators and high Q filters.

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Noise Voltage @ 1kHz . . . . . 4.5nV/$\sqrt{Hz}$ Max
- Low Noise Current @ 1kHz . . . . . 3pA/$\sqrt{Hz}$ Max
- Wide Unity Gain Bandwidth . . . . . 10MHz Min
- High Gain (Full Temp) . . . . . 100kV/V Min
  (Room Temp) . . . . . 1MV/V Typ
- Slew Rate. . . . . 6V/µs Min
- High CMRR/PSRR (Full Temp) . . . . . 80dB Min
- High Output Drive Capability (Full Temp). 25mA

Applications

- High Quality Audio Preamplifiers
- High Q Active Filters
- Low Noise Function Generators
- Low Distortion Oscillators
- Low Noise Comparators

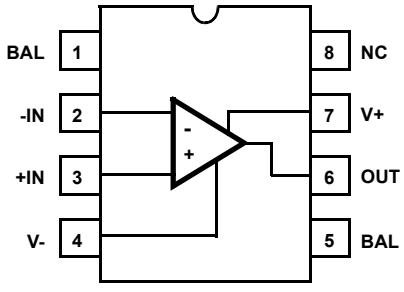
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HA7-5101/883	-55 to 125	8 Ld CerDIP	F8.3A
5962-89636012A	-55 to 125	20 Ld Ceramic LCC	J20.A

Pinouts

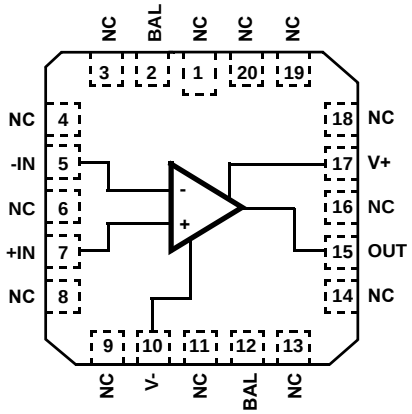
HA7-5101/883 (CERDIP)

TOP VIEW



5962-896360 (CLCC)

TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 7V
Voltage at Either Input Terminal . . . . . V+ to V-
Input Current 25mA
Output Short Circuit Duration. . . . . Indefinite
Junction Temperature (T_J). . . . . +175°C
Storage Temperature Range . . . . . -65°C to +150°C
ESD Rating . . . . . <2000V
Lead Temperature (Soldering 10s) . . . . . +300°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Ceramic DIP Package	120	30
Ceramic LCC Package	86	26

Package Power Dissipation Limit at +75°C for $T_J \leq +175°C$
Ceramic DIP Package 1.22W
Ceramic LCC Package. 1.35W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package . . . . . 12.2mW/°C
Ceramic LCC Package. . . . . 13.5mW/°C

Operating Conditions

Operating Temperature Range . . . . . -55°C to +125°C
Operating Supply Voltage . . . . . ±5V to ±15V
$V_{INcm} \leq 1/2$ (V+ - V-)
$R_L \geq 500\Omega$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V_S= ±15V, R_S = 100Ω, R_L = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	GROUP A SUBGROUP	TEMP (°C)	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V	1	+25	-3	3	mV
			2, 3	+125, -55	-4	4	mV
Input Bias Current	$+I_B$	V_{CM} = 0V $+R_S$ = 100kΩ -RS = 100Ω	1	+25	-200	200	nA
			2, 3	+125, -55	-325	325	nA
	$-I_B$	V_{CM} = 0V $+R_S$ = 100Ω -RS = 100kΩ	1	+25	-200	200	nA
			2, 3	+125, -55	-325	325	nA
Input Offset Current	I_{IO}	V_{CM} = 0V $+R_S$ = 100kΩ -RS = 100kΩ	1	+25	-75	75	nA
			2, 3	+125, -55	-125	125	nA
Common Mode Range	+CMR	V+ = 3V V- = -27V	1	+25	12	-	V
			2, 3	+125, -55	12	-	V
	-CMR	V+ = 27V V- = -3V	1	+25	-	-12	V
			2, 3	+125, -55	-	-12	V
Large Signal Voltage Gain	$+A_{VOL}$	V_{OUT} = 0V and +10V R_L = 2kΩ	4	+25	100	-	kV/V
			5, 6	+125, -55	100	-	kV/V
	$-A_{VOL}$	V_{OUT} = 0V and −10V R_L = 2kΩ	4	+25	100	-	kV/V
			5, 6	+125, -55	100	-	kV/V
Common Mode Rejection Ratio	+CMRR	ΔV_{CM} = +10V V+ =+5V V- = -25V V_{OUT} = -10V	1	+25	80	-	dB
			2, 3	+125, -55	80	-	dB
	-CMRR	ΔV_{CM} = -10V V+ = +25V V- = -5V V_{OUT} = +10V	1	+25	80	-	dB
			2, 3	+125, -55	80	-	dB

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: V_S= ±15V, R_S = 100Ω, R_L = 500kΩ, V_{OUT} = 0V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	GROUP A SUBGROUP	TEMP (°C)	LIMITS MIN	LIMITS MAX	UNITS
Output Voltage Swing	$+V_{OUT1}$	R_L = 2kΩ	1	+25	12	-	V
			2, 3	+125, -55	12	-	V
	$-V_{OUT1}$	R_L = 2kΩ	1	+25	-	-12	V
			2, 3	+125, -55	-	-12	V
	$+V_{OUT2}$	V_S = ±18V R_L = 600Ω	1	+25	15	-	V
			2, 3	+125, -55	15	-	V
	$-V_{OUT2}$	V_S = ±18V R_L = 600Ω	1	+25	-	-15	V
			2, 3	+125, -55	-	-15	V
Output Current	$+I_{OUT}$	V_{OUT} = -15V V_S = ±18V	1	+25	25	-	mA
			2, 3	+125, -55	25	-	mA
	$-I_{OUT}$	V_{OUT} = +15V V_S = ±18V	1	+25	-	-25	mA
			2, 3	+125, -55	-	-25	mA
Quiescent Power Supply Current	$+I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25	-	6	mA
			2, 3	+125, -55	-	6	mA
	$-I_{CC}$	V_{OUT} = 0V I_{OUT} = 0mA	1	+25	-6	-	mA
			2, 3	+125, -55	-6	-	mA
Power Supply Rejection Ratio	+PSRR	ΔV_S = 10V V+ = +10V, V- = -15V V+ = +20V, V- = -15V	1	+25	80	-	dB
			2, 3	+125, -55	80	-	dB
	-PSRR	ΔV_S = 10V V+ = +15V, V- = -10V V+ = +15V, V- = -20V	1	+25	80	-	dB
			2, 3	+125, -55	80	-	dB
Offset Voltage Adjustment	$+V_{IO}$Adj	Note 4 R_L = 2kΩ, C_L = 50pF A_V = +1V/V	1	+25	V_{IO}-1	-	mV
			2, 3	+125, -55	V_{IO}-1	-	mV
	$-V_{IO}$Adj		1	+25	V_{IO}+1	-	mV
			2, 3	+125, -55	V_{IO}+1	-	mV

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V_S= ±15V, R_S = 50Ω, R_L = 2kΩ, C_L = 50pF, A_{VCL} = +1V/V, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	GROUP A SUBGROUP	TEMP (°C)	LIMITS MIN	LIMITS MAX	UNITS
Slew Rate	+SR	V_{OUT} = -3V to +3V	4	+25	6	-	V/µs
	-SR	V_{OUT} = +3V to -3V	4	+25	6	-	V/µs
Rise and Fall Time	t_R	V_{OUT} = 0V to +200mV 10% ≤ t_R ≤ 90%	4	+25	-	200	ns
			5, 6	+125, -55	-	400	ns
	t_F	V_{OUT} = 0V to -200mV 10% ≤ t_F ≤ 90%	4	+25	-	200	ns
			5, 6	+125, -55	-	400	ns
Overshoot	+OS	V_{OUT} = 0V to +200mV	4	+25	-	35	%
			5, 6	+125, -55	-	35	%
	-OS	V_{OUT} = 0V to -200mV	4	+25	-	35	%
			5, 6	+125, -55	-	35	%

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: V_S= ±15V, R_L = 2kΩ, C_L = 50pF, A_V = +1, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	NOTES	TEMP (°C)	LIMITS		UNITS
					MIN	MAX	
Differential Input Resistance	R_{IN}	V_{CM} = 0V	1	+25	250	-	kΩ
Low Frequency Peak-to-Peak Noise	E_{nP-P}	0.1Hz to 10Hz	1	+25	-	0.2	μV_{P-P}
Input Noise Voltage Density	E_n	R_S = 20Ω, f_o = 1000Hz	1	+25	-	4.5	$nV/\sqrt{Hz}$
Input Noise Current Density	I_n	R_S = 2MΩ, f_o = 1000Hz	1	+25	-	3	$pA/\sqrt{Hz}$
Unity Gain Bandwidth	UGBW	V_O = 100mV	1	+25	10	-	MHz
Full Power Bandwidth	FPBW	V_{PEAK} = 10V	1, 2	+25	95	-	kHz
Minimum Closed Loop Stable Gain	CLSG		1	-55 to +125	+1	-	V/V
Output Resistance	R_{OUT}	Open Loop	1	+25	-	150	Ω
Quiescent Power Consumption	PC	V_{OUT} = 0V, I_{OUT} = 0mA	1, 3	-55 to +125	-	180	mW

NOTES:

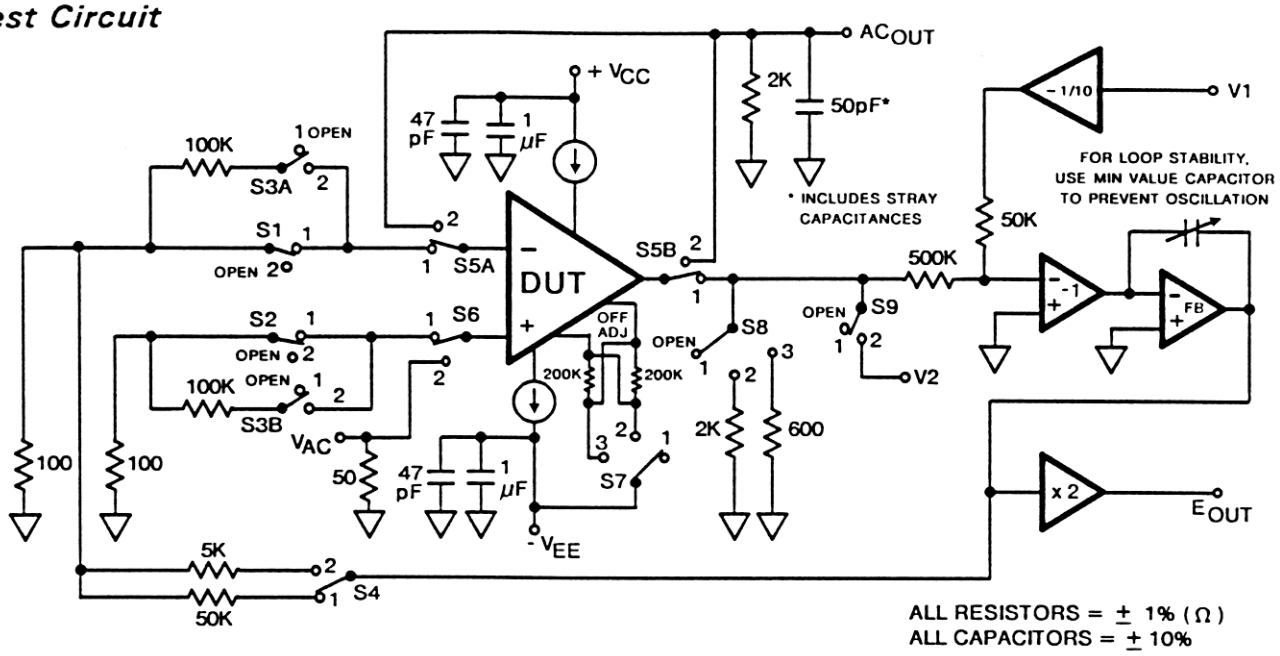
1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. Full Power Bandwidth guarantee based on Slew Rate measurement using FPBW = Slew Rate/($2\pi V_{PEAK}$).
3. Quiescent Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)
4. Offset adjustment range is [$V_{IO\ (Measured)}$ ±1mV] minimum referred to output. This test is for functionality only to assure adjustment through 0V.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 4, 5, 6
Group A Test Requirements	1, 2, 3, 4, 5, 6
Groups C & D Endpoints	1

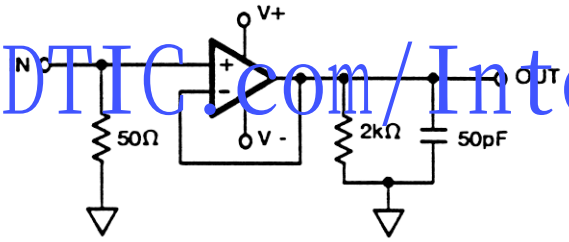
*PDA applies to Subgroup 1 only.

Test Circuit

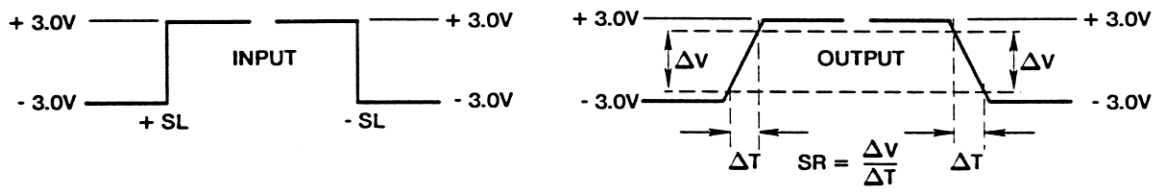


Test Waveforms

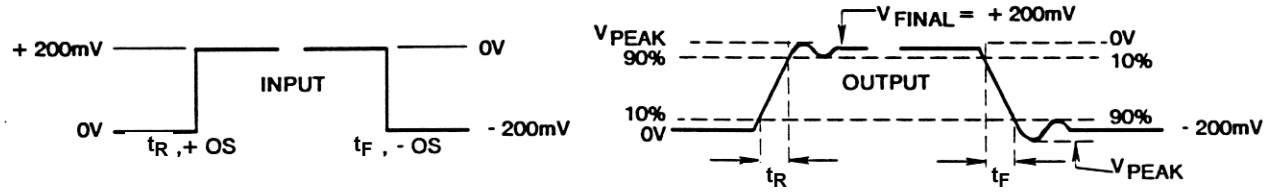
SIMPLIFIED TEST CIRCUIT (Applies To Tables 2 And 3)



SLEW RATE WAVEFORMS

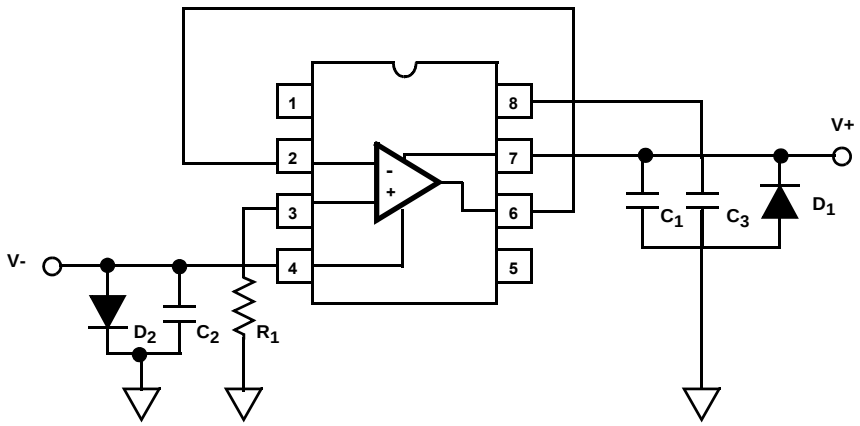


OVERSHOOT, RISE/FALL TIME WAVEFORMS

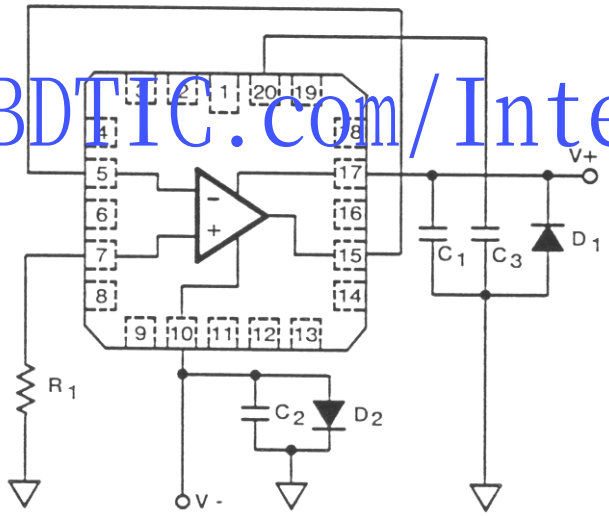


Burn-in Circuits

CERAMIC MINI-DIP

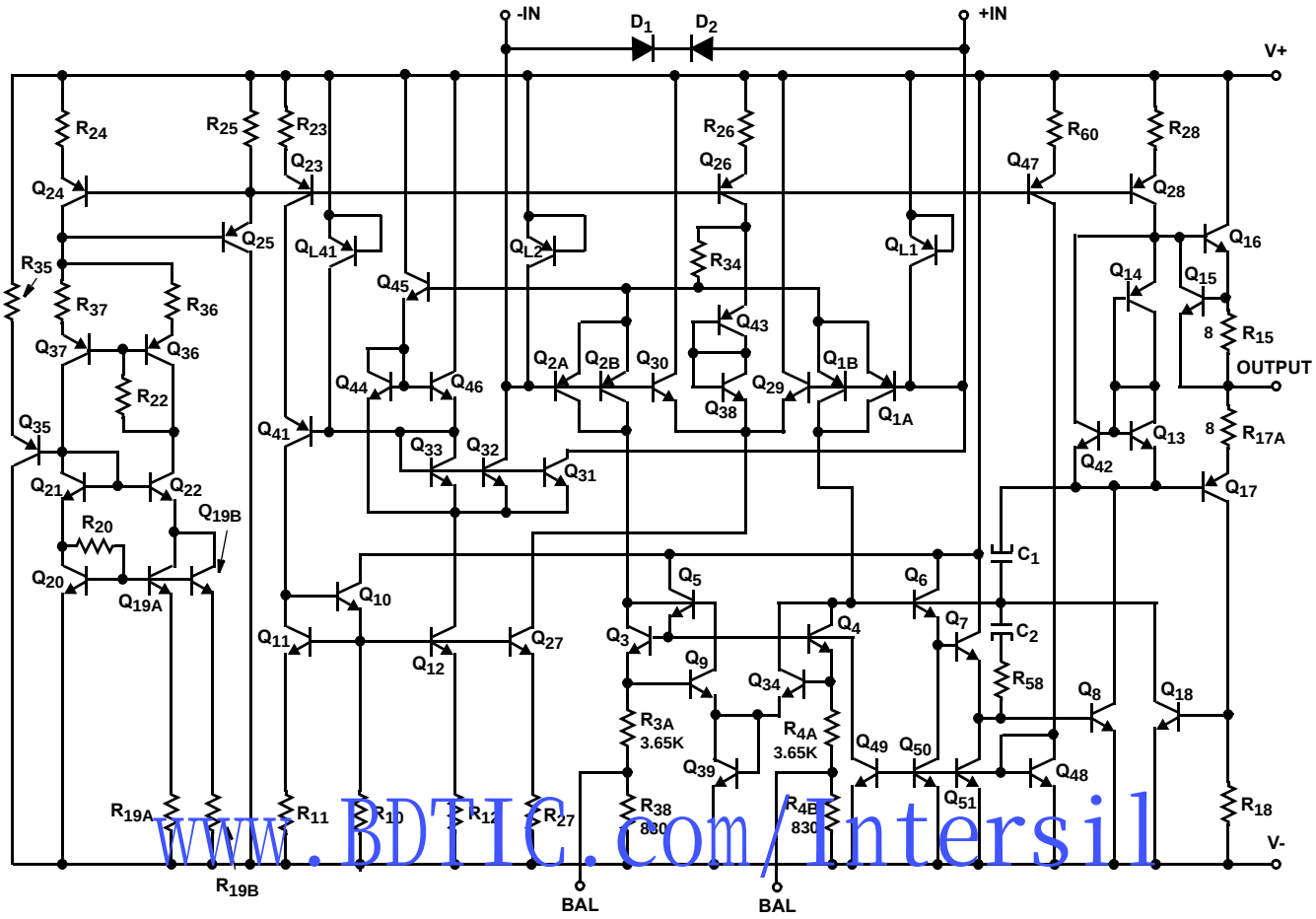


CERAMIC LCC



NOTES:
R_1 = 1MΩ, ±5%, 1/4W (Min)
$C_1 = C_2$ = 0.01µF/Socket (Min) or 0.1µF/Row, (Min)
C_3 = 0.01µF/Socket, 10%
$D_1 = D_2$ = 1N4002 or Equivalent/Board
$|(V+) - (V-)|$ = 30V

Schematic



Die Characteristics

DIE DIMENSIONS

70 X 70 X 19 mils ±1mil
1790 x 1780 x 483µm ±25.4µm

METALLIZATION

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

GLASSIVATION

Type: Nitride (Si3N4) over Silox (SiO2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

WORST CASE CURRENT DENSITY:

$1.38 \times 10^5 A/cm^2$

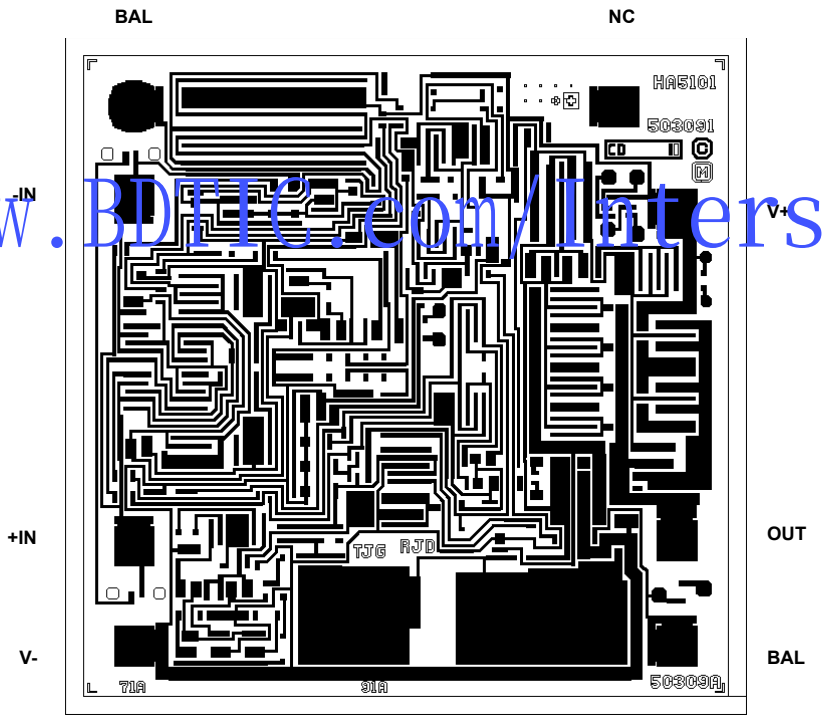
SUBSTRATE POTENTIAL (Powered Up): V-

TRANSISTOR COUNT: 54

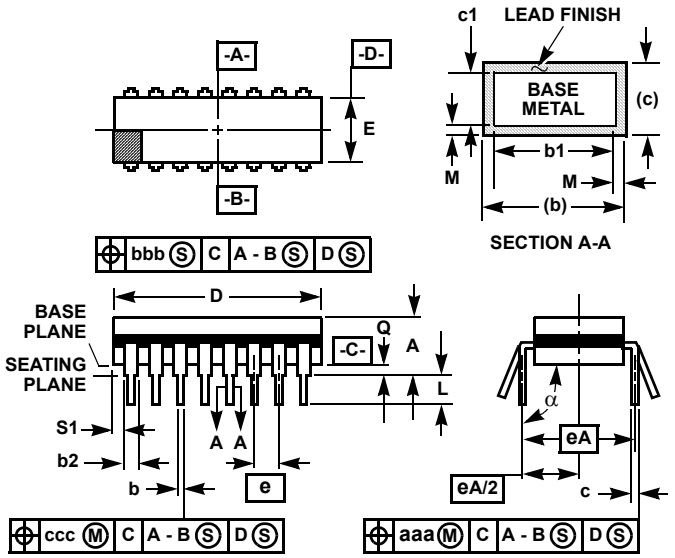
PROCESS: Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5101/883



Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

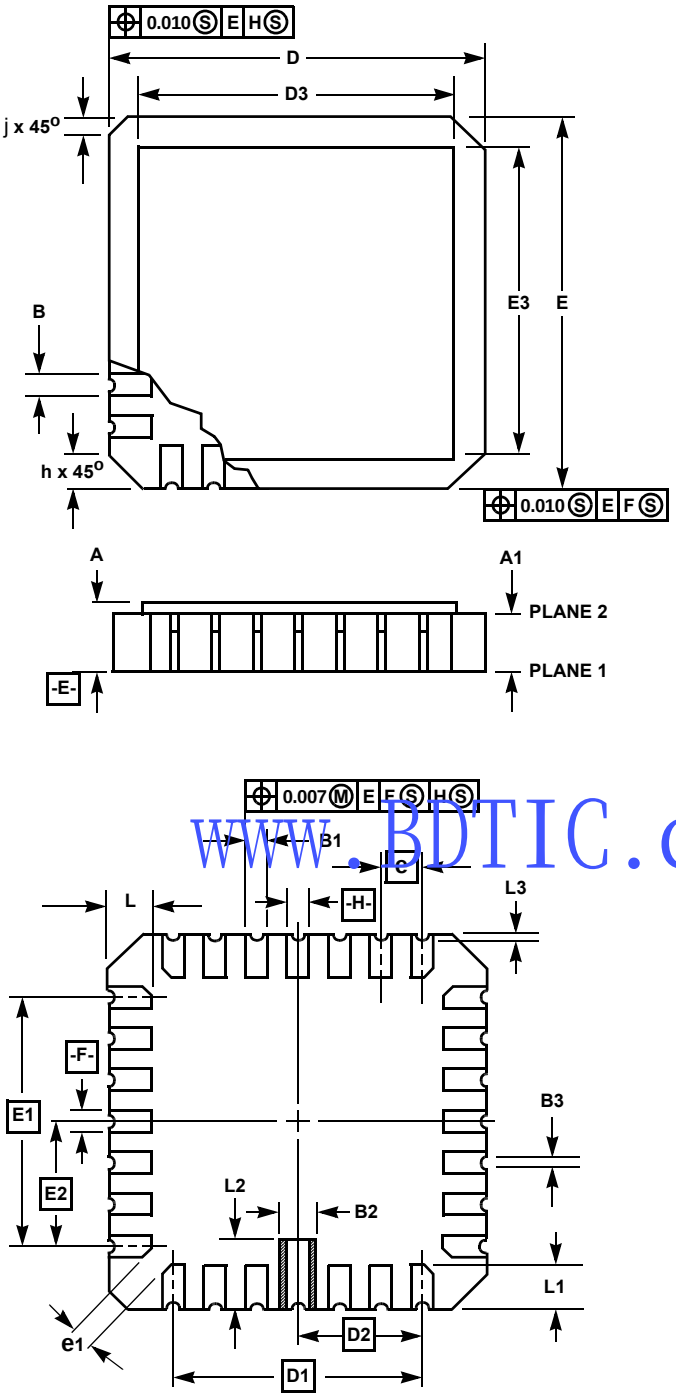
1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH

F8.3A MIL-STD-1835 GDIP1-T8 (D-4, CONFIGURATION A)
8 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	8		8		8

Rev. 0 4/94

Ceramic Leadless Chip Carrier Packages (CLCC)



J20.A MIL-STD-1835 CQCC1-N20 (C-2)
20 PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.060	0.100	1.52	2.54	6, 7
A1	0.050	0.088	1.27	2.23	-
B	-	-	-	-	-
B1	0.022	0.028	0.56	0.71	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.342	0.358	8.69	9.09	-
D1	0.200 BSC		5.08 BSC		-
D2	0.100 BSC		2.54 BSC		-
D3	-	0.358	-	9.09	2
E	0.342	0.358	8.69	9.09	-
E1	0.200 BSC		5.08 BSC		-
E2	0.100 BSC		2.54 BSC		-
E3	-	0.358	-	9.09	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.91	2.41	-
L3	0.003	0.015	0.08	0.38	-
ND	5		5		3
NE	5		5		3
N	20		20		3

Rev. 0 5/18/94

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.38mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol “N” is the maximum number of terminals. Symbols “ND” and “NE” are the number of terminals along the sides of length “D” and “E”, respectively.
4. The required plane 1 terminals and optional plane 2 terminals (if used) shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer’s option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Dimension “A” controls the overall package thickness. The maximum “A” dimension is package height before being solder dipped.
8. Dimensioning and tolerancing per ANSI Y14.5M-1982.
9. Controlling dimension: INCH.

The information contained on the following pages has been developed through characterization by Intersil Semiconductor and is for use as application and design information only. No guarantee is implied.

Typical Performance Curves

Unless Otherwise Specified: V_S = ±15V, T_A = +25°C

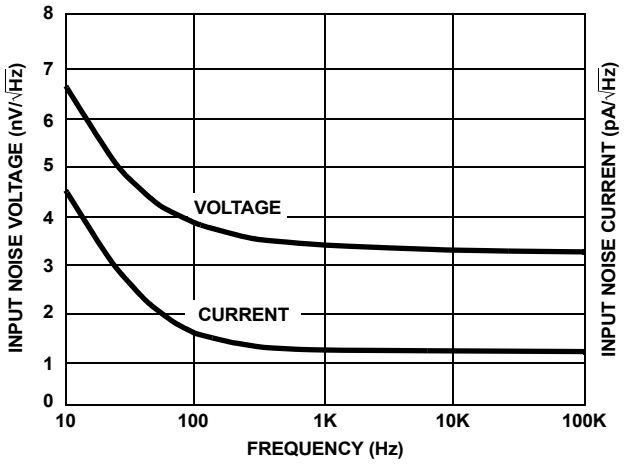


FIGURE 1. NOISE SPECTRUM

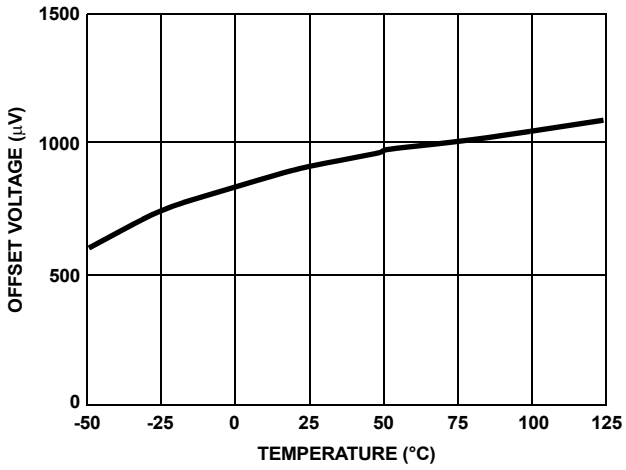
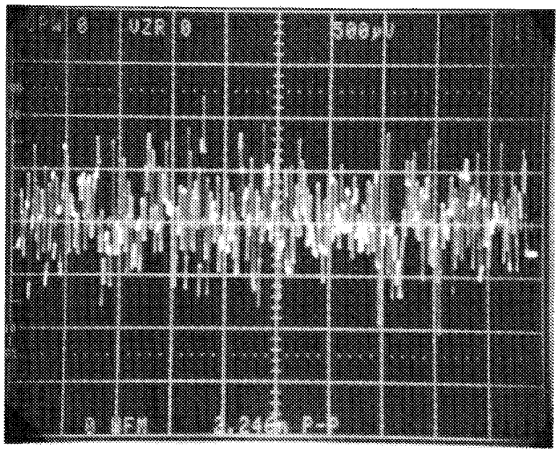
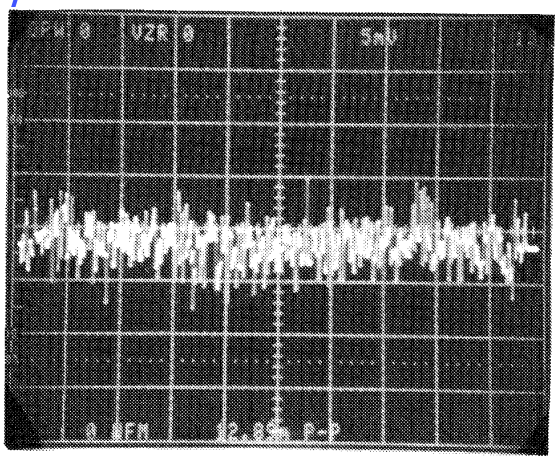


FIGURE 2. OFFSET VOLTAGE vs TEMPERATURE



A_V = 25,000, V_S = ±15V (0.09nV$_{P-P}$ RTI)

PEAK-TO-PEAK NOISE 0.1Hz TO 10Hz



A_V = 25,000, V_S = ±15V (12.89mV$_{P-P}$ RTO or 0.52µV$_{P-P}$ RTI)

PEAK-TO-PEAK TOTAL NOISE 0.1Hz TO 1MHz

Typical Performance Curves Unless Otherwise Specified: V_S = ±15V, T_A = +25°C **(Continued)**

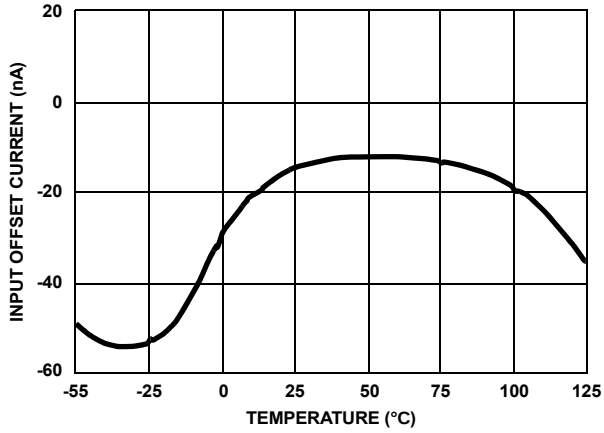


FIGURE 3. INPUT OFFSET CURRENT vs TEMPERATURE

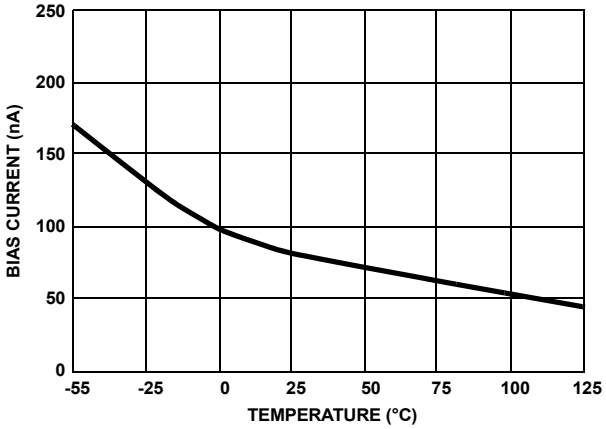


FIGURE 4. INPUT BIAS CURRENT vs TEMPERATURE

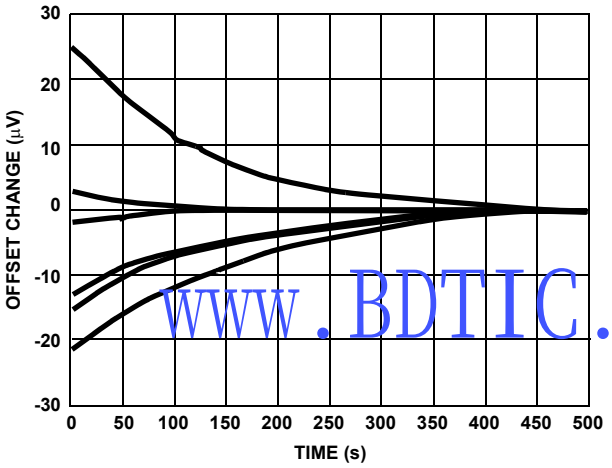


FIGURE 5. INPUT OFFSET WARMUP DRIFT vs TIME (NORMALIZED TO ZERO FINAL VALUE) (SIX REPRESENTATIVE UNITS)

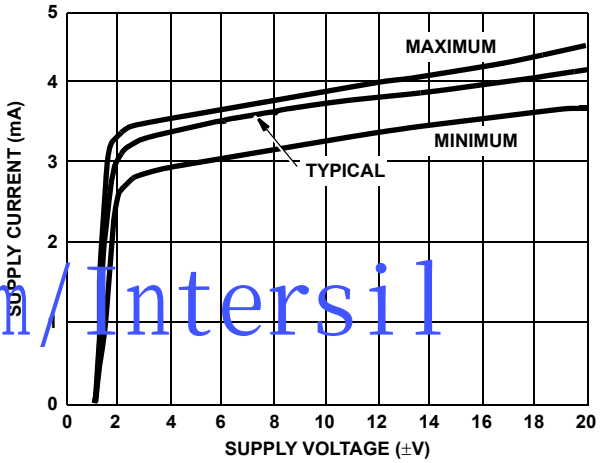


FIGURE 6. SUPPLY CURRENT vs SUPPLY VOLTAGE

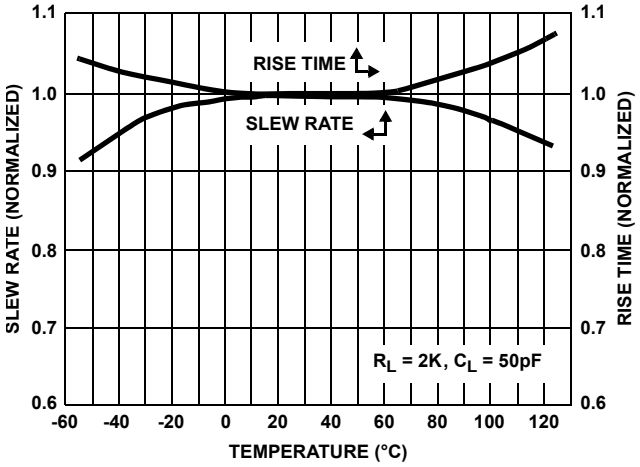
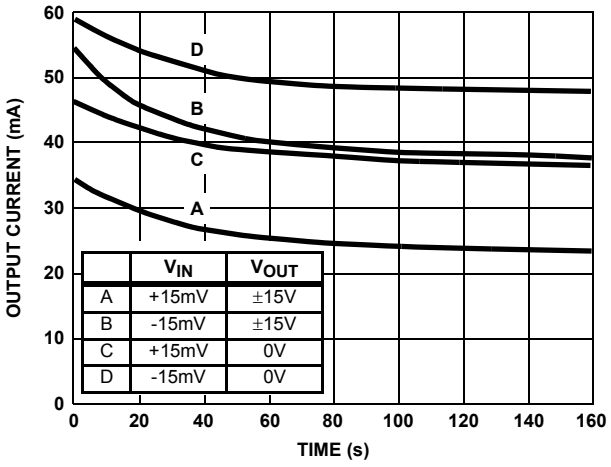


FIGURE 7. SLEW RATE/RISE TIME vs TEMPERATURE



	V_{IN}	V_{OUT}
A	+15mV	±15V
B	-15mV	±15V
C	+15mV	0V
D	-15mV	0V

FIGURE 8. SHORT CIRCUIT CURRENT vs TIME

Typical Performance Curves Unless Otherwise Specified: V_S = ±15V, T_A = +25°C **(Continued)**

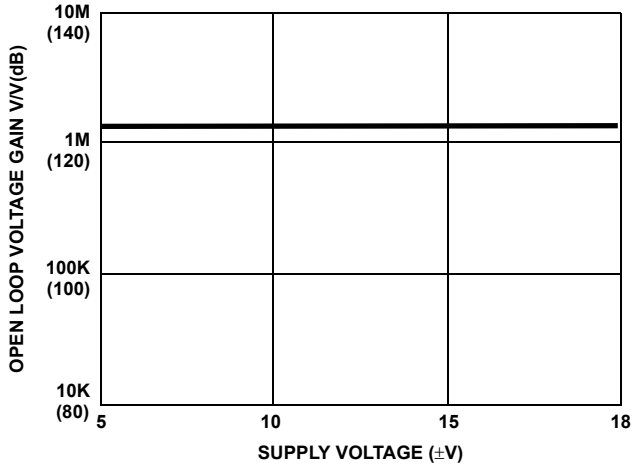


FIGURE 9. DC OPEN-LOOP VOLTAGE GAIN vs SUPPLY VOLTAGE

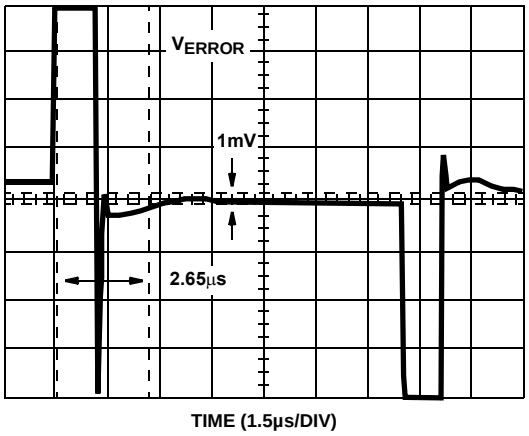


FIGURE 10. SETTLING WAVEFORM

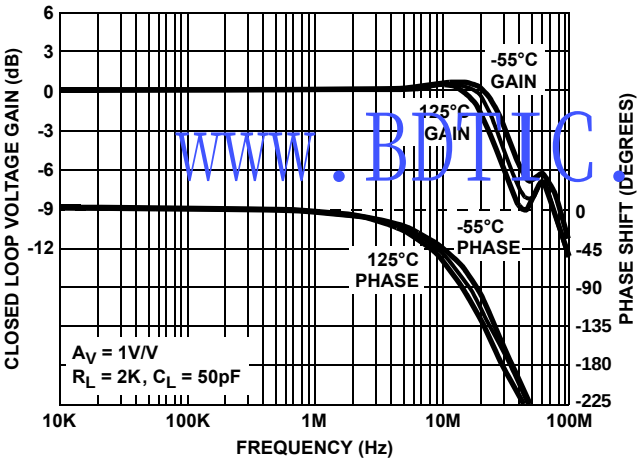


FIGURE 11. CLOSED LOOP GAIN AND PHASE AT HIGH AND LOW TEMPERATURES

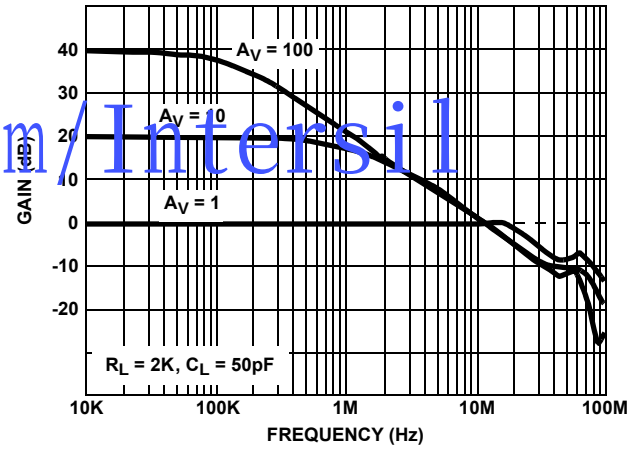


FIGURE 12. CLOSED-LOOP VOLTAGE GAIN vs FREQUENCY AT DIFFERENT CLOSED LOOP GAINS

Typical Performance Curves Unless Otherwise Specified: V_S = ±15V, T_A = +25°C **(Continued)**

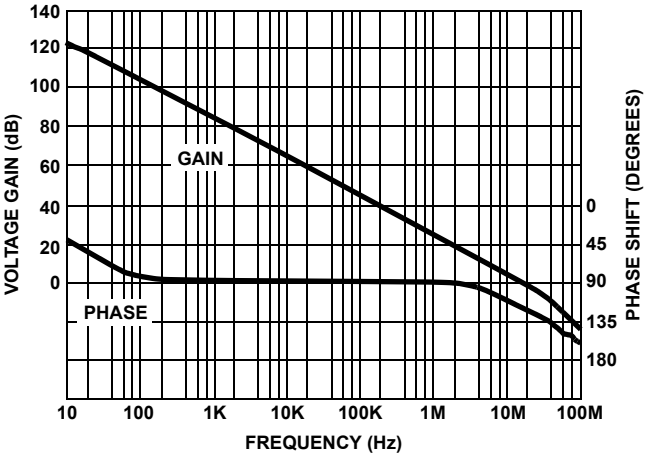


FIGURE 13. OPEN-LOOP GAIN/PHASE vs FREQUENCY

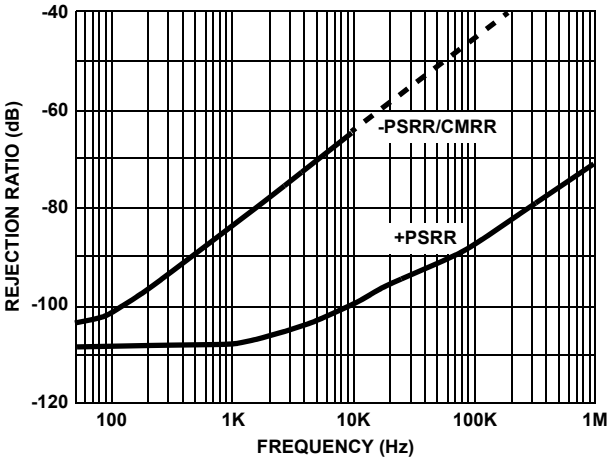
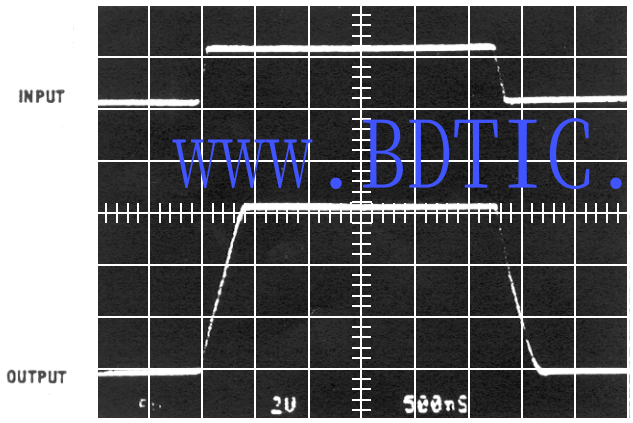
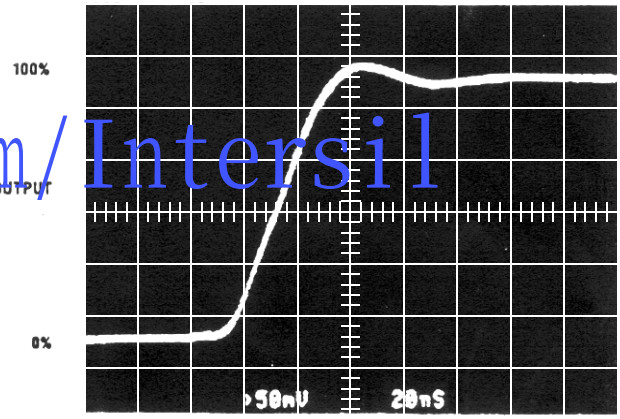


FIGURE 14. REJECTION RATIOS vs FREQUENCY



V_{IN} = V_{OUT} = ±3V, A_V = +1, R_L = 2kΩ, C_L = 50pF
Timescale = 500ns/Div., Scale: Input = 5V/Div, Output = 2V/Div

FIGURE 15. SLEW RATE WAVEFORM



Rise Time and Overshoot
V_{IN} = V_{OUT} = 0V to +200mV, A_V = +1, R_L = 2K, C_L = 50pF
Timescale = 20ns/Div.

FIGURE 16. SMALL SIGNAL WAVEFORM

Applications Information

Operation At ±5V Supply

The HA-5101 performs well at V_S = ±5V exhibiting typical characteristics as listed below:

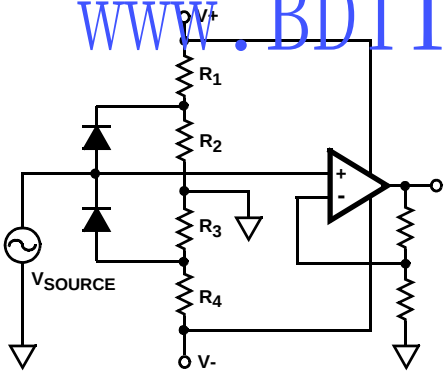
I_{CC}	3.7mA
V_{IO}	0.5mV
I_{BIAS}	56nA
A_{VOL} (V_O = ±3V)	106kV/V
V_{OUT}	3.7V
I_{OUT}	13mA
CMRR (ΔV_{CM} = ±2.5V)	90dB
PSRR (ΔV_{CC} = 0.5V)	90dB
Unity Gain Bandwidth	10MHz
Slew Rate	7V/µs

Input Protection

The HA-5101 has built-in back-to-back protection diodes which will limit the differential input voltage to approximately 7V. If the HA-5101 will be used in conditions where that voltage may be exceeded, then current limiting resistors must be used. No more than 25mA should be allowed to flow in the HA-5101's input.

Output Saturation

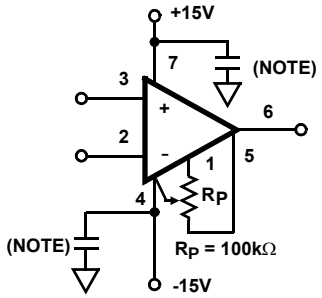
When an op amp is overdriven, output devices can saturate and sometimes take a long time to recover. Saturation can be avoided (sometimes) by using circuits such as:



If saturation cannot be avoided the HA-5101 recovers from a 25% overdrive in about 6.5µs (see photo).

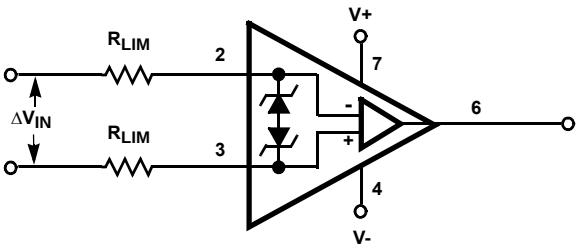
Offset Adjustment

The following is the recommended V_{IO} adjust configuration:

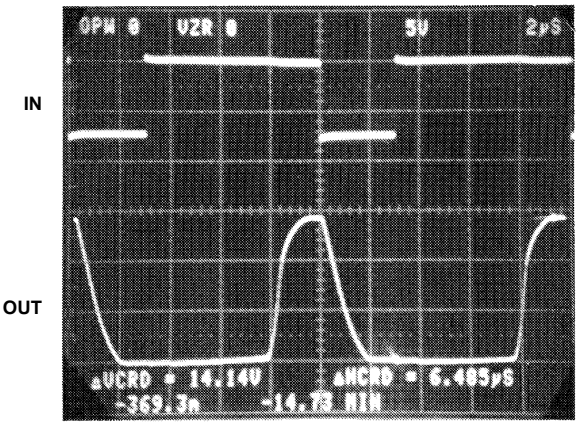


NOTE: Proper decoupling is always recommended, 0.1µF high quality capacitor should be at or very near the device's supply pins.

Comparator Circuit



Choose R_{LIM} Such That: $\frac{(\Delta V_{IN}MAX - 7V)}{25mA} \leq 2R_{LIM}$



Top: Input
Bottom: Output, 5V/Div., 2µs/Div.
Output is overdriven negative and recovers in 6µs.

TABLE 1. TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized At: V_S = ±15V, R_L = 2kΩ, C_L = 50pF, A_{VCL} = +1V/V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	TYP	DESIGN LIMITS	UNITS
Offset Voltage	V_{CM} = 0V	+25	0.8	Table 1	mV
Offset Voltage Average Drift	Versus Temperature	-55 to +125	3	7	µV/°C
Offset Current Average Drift	Versus Temperature	-55 to +125	100	250	pA/°C
Input Bias Current	V_{CM} = 0V	+25	65	Table 1	nA
Input Offset Current	V_{CM} = 0V	+25	35	Table 1	nA
Differential Input Resistance	V_{CM} = 0V	+25	500	Table 3	kΩ
Input Noise Voltage Density	f_o = 10Hz	+25	5.4	9	nV/√Hz
	f_o = 100Hz	+25	3.4	5.5	nV/√Hz
	f_o = 1kHz	+25	3.2	Table 3	nV/√Hz
Input Noise Current Density	f_o = 10Hz	+25	6	20	pA/√Hz
	f_o = 100Hz	+25	1.5	5	pA/√Hz
	f_o = 1kHz	+25	0.52	Table 3	pA/√Hz
Large Signal Voltage Gain	V_{OUT} = ±10V	-55	400K	Table 1	V/V
		+25	1M	Table 1	V/V
		+125	1M	Table 1	V/V
Slew Rate	V_{OUT} = ±3V	-55 to +125	10	5.4	V/µs
Full Power Bandwidth	V_{PEAK} = 10V, (Note 2)	-55 to +125	159	85	kHz
Rise and Fall Times	V_{OUT} = ±200mV	-55 to +125	50	Table 2	ns
Overshoot	V_{OUT} = ±200mV	-55 to +125	20	35	%
Settling Time	To 0.1% for 10V Step	+25	4.5	6	µs
	To 0.01% for 10V Step	+25	6	10	µs
Output Short Circuit Current	t < 10s, V_{OUT} = ±15V	+25	±35	±50	mA
Output Resistance	Open Loop	+25	110	Table 3	Ω
Supply Current	No Load	+25	4.3	Table 1	mA
Minimum Supply Voltage	Functional Operation Only, Other Parameters Will Vary	+25	±4	±5	V