Data Sheet | April 10, 2007 | FN7016.2

Medium Power Differential Line Driver

The EL1511 is a dual operational amplifier designed for customer premise line driving in DMT ADSL solutions. This device features a high drive capability of 360mA while consuming only 7.5mA of supply current per amplifier and operating from a single 5V to 15V supply. This driver achieves a typical distortion of less than -85dBc, at 150kHz into a 25Ω load. The EL1511 is available in the thermally-enhanced 16 Ld SOIC (0.150") and a 16 Ld QFN (4x4mm) packages. The EL1511 is specified for operation over the full -40°C to +85°C temperature range. Electrical characteristics are given for typical 15V supply operation.

The EL1511 has two control pins, C_0 and C_1, which allow the selection of full I_S power, 3/4-I_S, 1/2-I_S, and power-down modes.

The EL1511 is ideal for ADSL, SDSL, and HDSL2 line driving applications for single power supply, high voltage swing, and low power.

The EL1511 maintains excellent distortion and load driving capabilities even in the lowest power settings.

Features

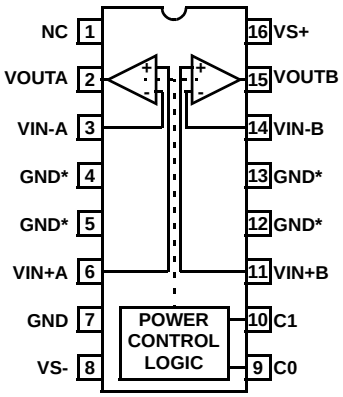
- Drives up to 360mA from a +15V supply
- $24V_{P-P}$ differential output drive into 25Ω and $26V_{P-P}$ differential output drive into 100Ω
- -85dBc typical driver output distortion at full output at 150kHz
- Low quiescent current of 3.5mA per amplifier at 1/2-I_S current mode
- Disable down to 1.5mA
- Pb-free plus anneal available (RoHS compliant)

Applications

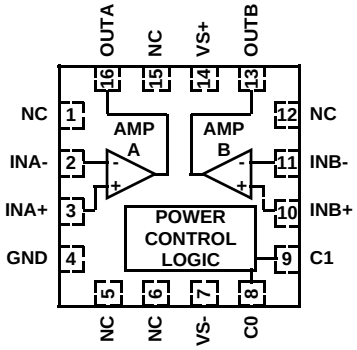
- ADSL CSA line driving
- ADSL full rate CPE line driving
- G.SHDSL, HDSL2 line driver
- Video distribution amplifier
- Video twisted-pair line driver

Pinouts

EL1511
[16 LD SO (0.150")]
TOP VIEW



EL1511
(16 LD QFN)
TOP VIEW



NOTE: * These GND pins are heat spreaders

Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
EL1511CS	EL1511CS	-	16 Ld SO (0.150”)	MDP0027
EL1511CS-T7	EL1511CS	7”	16 Ld SO (0.150”)	MDP0027
EL1511CS-T13	EL1511CS	13”	16 Ld SO (0.150”)	MDP0027
EL1511CSZ (See Note)	EL1511CSZ	-	16 Ld SO (0.150”) (Pb-Free)	MDP0027
EL1511CSZ-T7 (See Note)	EL1511CSZ	7”	16 Ld SO (0.150”) (Pb-Free)	MDP0027
EL1511CSZ-T13 (See Note)	EL1511CSZ	13”	16 Ld SO (0.150”) (Pb-Free)	MDP0027
EL1511CL	1511CL	-	16 Ld QFN	MDP0046
EL1511CL-T7	1511CL	7”	16 Ld QFN	MDP0046
EL1511CL-T13	1511CL	13”	16 Ld QFN	MDP0046
EL1511CLZ (See Note)	1511CLZ	-	16 Ld QFN (Pb-Free)	MDP0046
EL1511CLZ-T7 (See Note)	1511CLZ	7”	16 Ld QFN (Pb-Free)	MDP0046
EL1511CLZ-T13 (See Note)	1511CLZ	13”	16 Ld QFN (Pb-Free)	MDP0046

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings (T_A = +25°C)

V_S+ to V_S- Supply Voltage. 16.5V
V_S+ Voltage to Ground . . . . . -0.3V to +16.5V
V_S- Voltage to Ground . . . . . -16.5V to 0.3V
Input C_0/C_1 to Ground 7V
V_{IN}+ Voltage . . . . . V_S- to V_S+

Current into any Input 8mA
Continuous Output Current 75mA
Operating Temperature Range . . . . . -40°C to +85°C
Storage Temperature Range . . . . . -60°C to +150°C
Operating Junction Temperature . . . . . -40°C to +150°C
Power Dissipation . . . . . See Curves

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

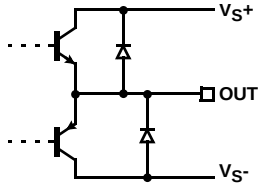
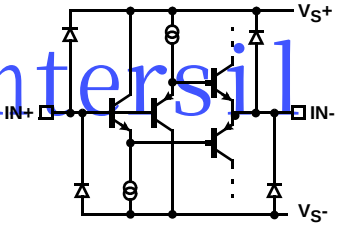
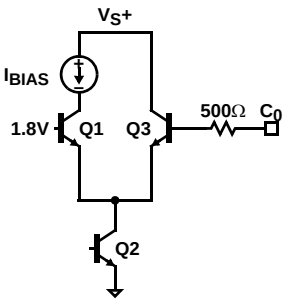
V_S = ±7.5V, R_F = 1.5kΩ, R_L = 100Ω to mid supply, T_A = +25°C unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
BW	-3dB Bandwidth	A_V = +4		70		MHz
HD	Total Harmonic Distortion	f = 150kHz, V_O = 16V_{P-P}, R_L = 25Ω		-85		dBc
dG	Differential Gain	A_V = +2, R_L = 37.5Ω		0.15		%
dθ	Differential Phase	A_V = +2, R_L = 37.5Ω		0.1		°
SR	Slewrate	V_{OUT} from -3V to +3V		500		V/µs
DC PERFORMANCE						
V_{OS}	Offset Voltage		-20		20	mV
ΔV_{OS}	V_{OS} Mismatch		-10		10	mV
R_{OL}	Transimpedance	V_{OUT} from -4.5V to +4.5V	0.7	1.4	2.5	MΩ
INPUT CHARACTERISTICS						
I_B+	Non-Inverting Input Bias Current		-5		5	µA
I_B-	Inverting Input Bias Current		-30		30	µA
ΔI_B-	I_B- Mismatch		-30		30	µA
e_N	Input Noise Voltage			2.8		nV/√Hz
i_N	-Input Noise Current			19		pA/√Hz
V_{IH}	Input High Voltage	C_0 and C_1 inputs	2.3			V
V_{IL}	Input Low Voltage	C_0 and C_1 inputs			1.5	V
I_{IH1}	Input High Current for C_1	C_1 = 5V	0.2		8	µA
I_{IH0}	Input High Current for C_0	C_0 = 5V	0.1		4	µA
I_{IL}	Input Low Current for C_1or C_0	C_1 = 0V, C_0 = 0V	-1		1	µA
OUTPUT CHARACTERISTICS						
V_{OUT}	Loaded Output Swing (single ended)	V_S = ±7.5, R_L = 100Ω to GND	±6.3	±6.5		V
		V_S = ±7.5, R_L = 25Ω to GND	±5.7	±6.0		V
I_{OUT}	Output Current	R_L = 0Ω		450		mA
SUPPLY						
V_S	Supply Voltage	Single supply	5		15	V
I_S+ (Full Power)	Positive Supply Current per Amplifier	All outputs at 0V, C_0 = C_1 = 0V		7	9.25	mA
I_S- (Full Power)	Negative Supply Current per Amplifier	All outputs at 0V, C_0 = C_1 = 0V		-6.4	-8.75	mA
I_S+ (3/4 Power)	Positive Supply Current per Amplifier	All outputs at 0V, C_0 = 5V, C_1 = 0V		5.3	7.25	mA

Electrical Specifications V_S = ±7.5V, R_F = 1.5kΩ, R_L = 100Ω to mid supply, T_A = +25°C unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
I_S- (3/4 Power)	Negative Supply Current per Amplifier	All outputs at 0V, C_0 = 5V, C_1 = 0V		-4.7	-6.75	mA
I_S+ (1/2 Power)	Positive Supply Current per Amplifier	All outputs at 0V, C_0 = 0V, C_1 = 5V		3.3	5.75	mA
I_S- (1/2 Power)	Negative Supply Current per Amplifier	All outputs at 0V, C_0 = 0V, C_1 = 5V		-2.7	-5.2	mA
I_S+ (Power Down)	Positive Supply Current per Amplifier	All outputs at 0V, C_0 = C_1 = 5V		0.6	1.025	mA
I_S- (Power Down)	Negative Supply Current per Amplifier	All outputs at 0V, C_0 = C_1 = 5V		0	-0.525	mA
I_{GND}	GND Supply Current per Amplifier	All outputs at 0V		0.6	1	mA

Pin Descriptions

EL1511CS 16 Ld SO (0.150")	EL1511CL 16 Ld QFN	PIN NAME	PIN FUNCTION	EQUIVALENT CIRCUIT
1	1, 5, 6, 12, 15	NC	Not Connected	
2, 15	13, 16	OUT	Output	 CIRCUIT 1
3, 14	2, 11	VIN-	Inverting Input	 CIRCUIT 2
4, 5, 7, 12, 13	4	GND	Ground Pins	
6, 11	3, 10	VIN+	Non-inverting Input	Reference Circuit 2
8	7	VS-	Negative Supply	
9	8	C0	Power Control	 CIRCUIT 3
10	9	C1	Power Control	Reference Circuit 3

Typical Performance Curves

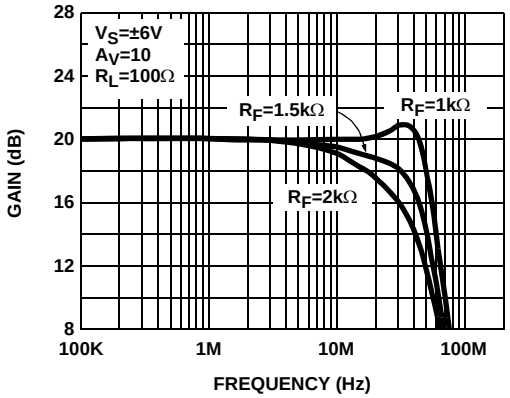


FIGURE 1. DIFFERENTIAL FREQUENCY RESPONSE (FULL POWER MODE)

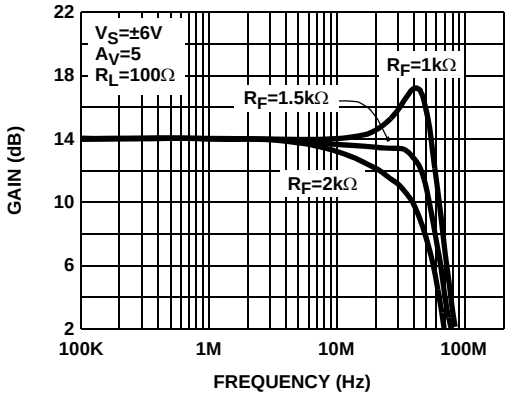


FIGURE 2. DIFFERENTIAL FREQUENCY RESPONSE (FULL POWER MODE)

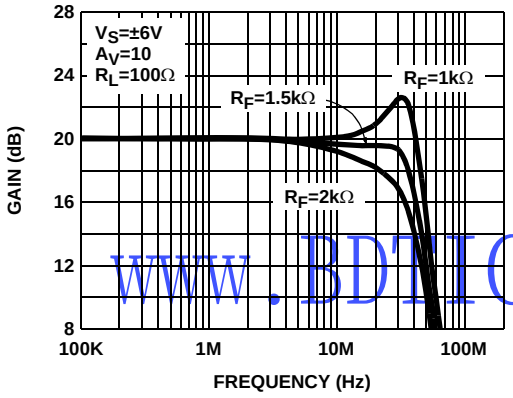


FIGURE 3. DIFFERENTIAL FREQUENCY RESPONSE (3/4 POWER MODE)

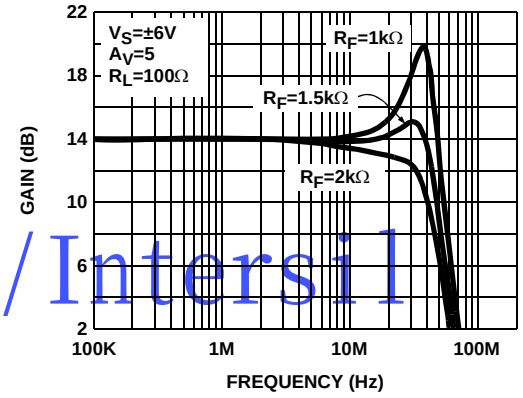


FIGURE 4. DIFFERENTIAL FREQUENCY RESPONSE (3/4 POWER MODE)

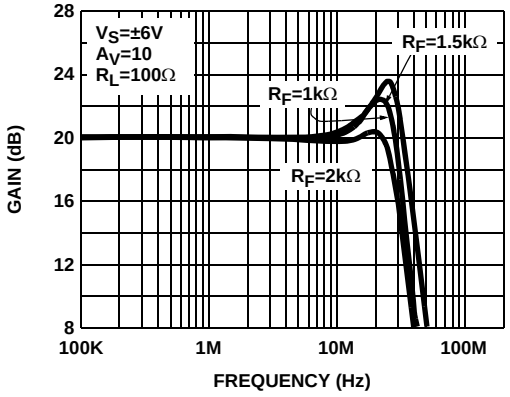


FIGURE 5. DIFFERENTIAL FREQUENCY RESPONSE (1/2 POWER MODE)

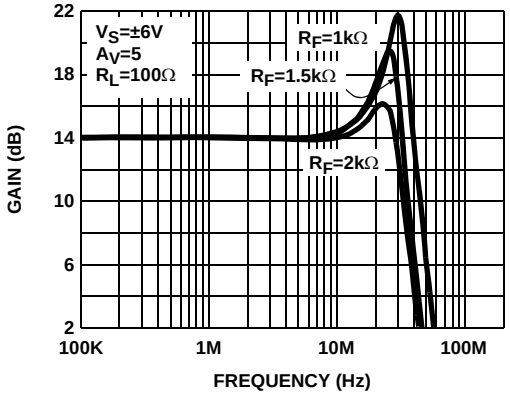


FIGURE 6. DIFFERENTIAL FREQUENCY RESPONSE (1/2 POWER MODE)

Typical Performance Curves (Continued)

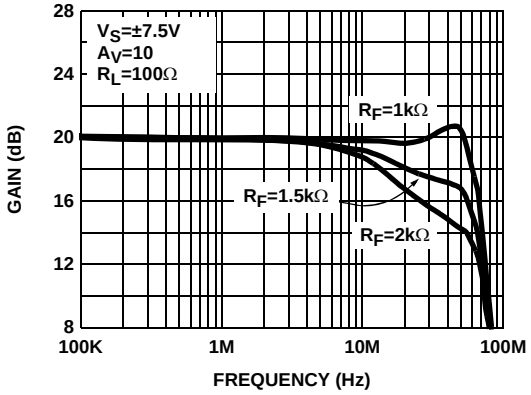


FIGURE 7. DIFFERENTIAL FREQUENCY RESPONSE (FULL POWER MODE)

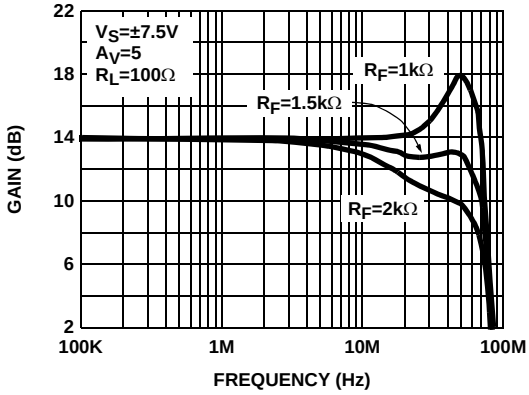


FIGURE 8. DIFFERENTIAL FREQUENCY RESPONSE (FULL POWER MODE)

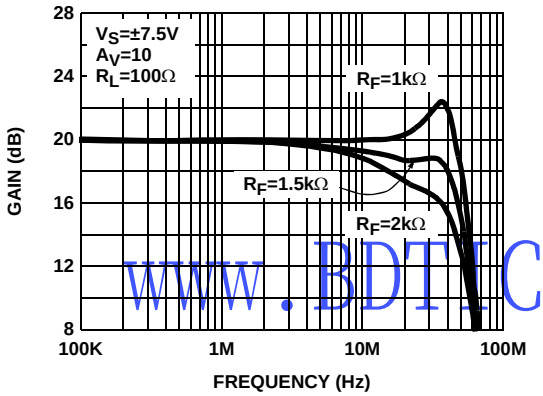


FIGURE 9. DIFFERENTIAL FREQUENCY RESPONSE (3/4 POWER MODE)

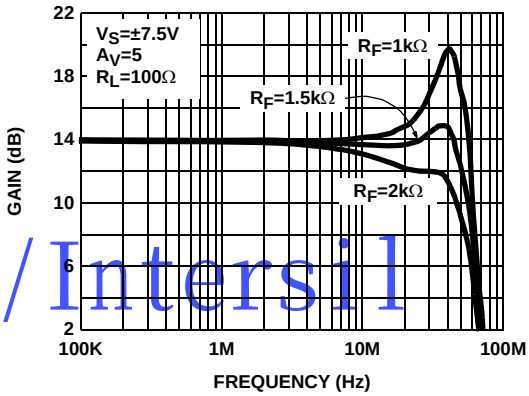


FIGURE 10. DIFFERENTIAL FREQUENCY RESPONSE (3/4 POWER MODE)

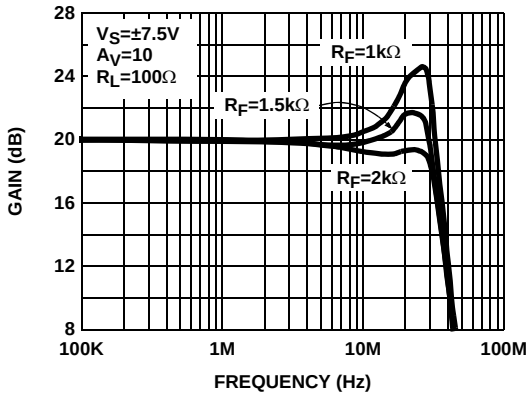


FIGURE 11. DIFFERENTIAL FREQUENCY RESPONSE (1/2 POWER MODE)

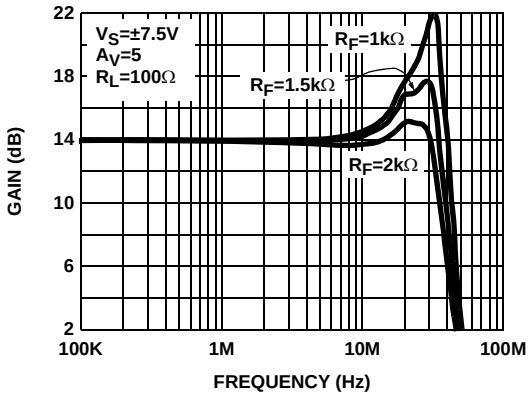


FIGURE 12. DIFFERENTIAL FREQUENCY RESPONSE (1/2 POWER MODE)

Typical Performance Curves (Continued)

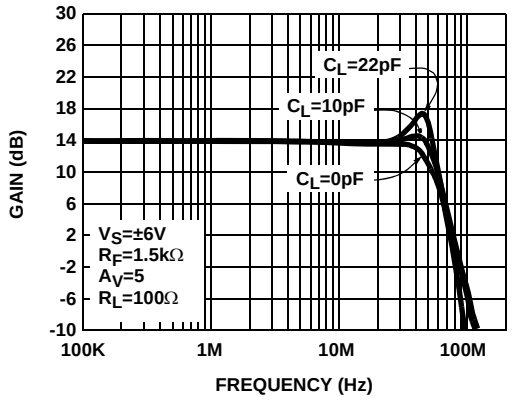


FIGURE 13. DIFFERENTIAL FREQUENCY RESPONSE vs C_L (FULL POWER MODE)

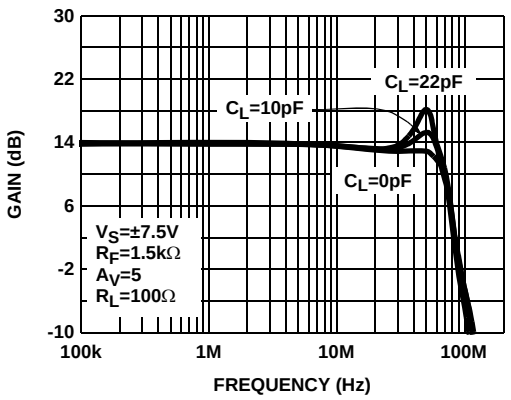


FIGURE 14. DIFFERENTIAL FREQUENCY RESPONSE vs C_L (FULL POWER MODE)

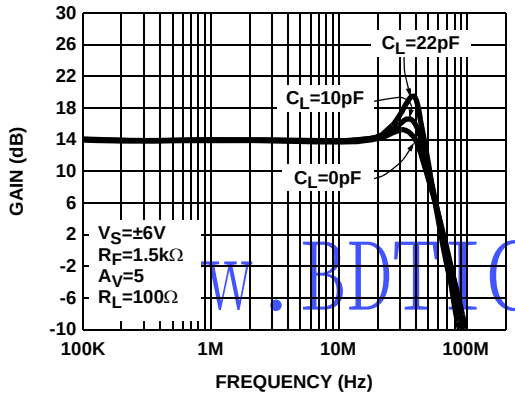


FIGURE 15. DIFFERENTIAL FREQUENCY RESPONSE vs C_L (3/4 POWER MODE)

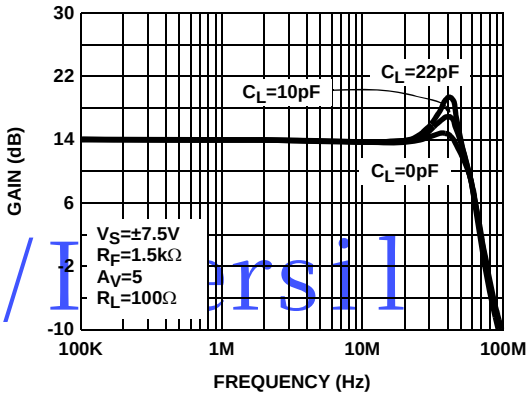


FIGURE 16. DIFFERENTIAL FREQUENCY RESPONSE vs C_L (3/4 POWER MODE)

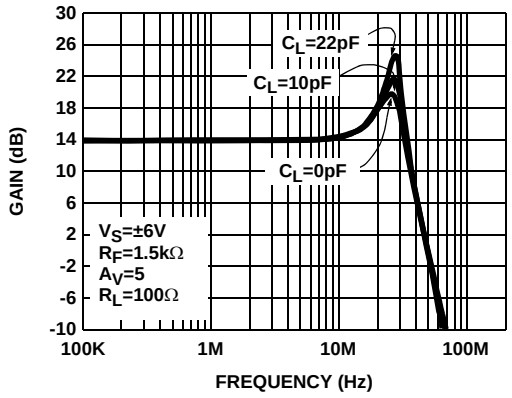


FIGURE 17. DIFFERENTIAL FREQUENCY RESPONSE vs C_L (1/2 POWER MODE)

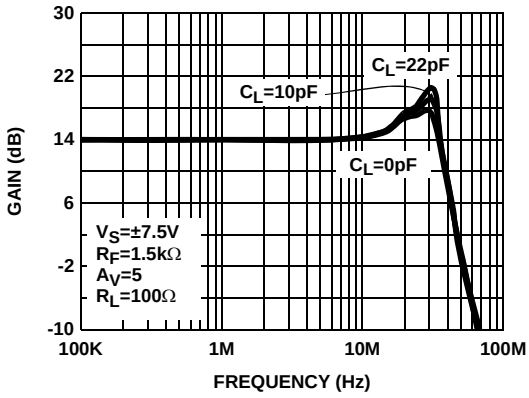


FIGURE 18. DIFFERENTIAL FREQUENCY RESPONSE vs C_L (1/2 POWER MODE)

Typical Performance Curves (Continued)

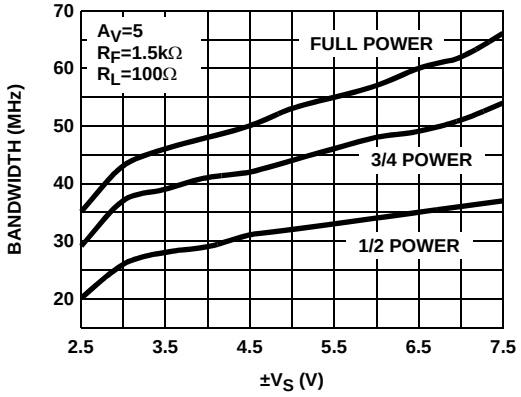


FIGURE 19. DIFFERENTIAL BANDWIDTH vs SUPPLY VOLTAGE

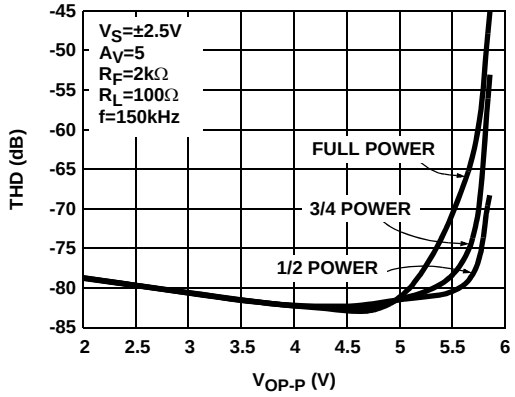


FIGURE 20. DIFFERENTIAL TOTAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE

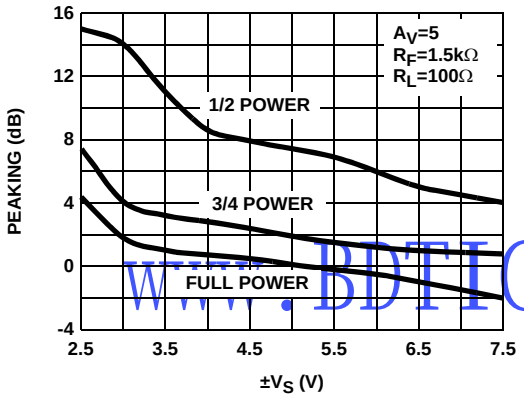


FIGURE 21. DIFFERENTIAL PEAKING vs SUPPLY VOLTAGE

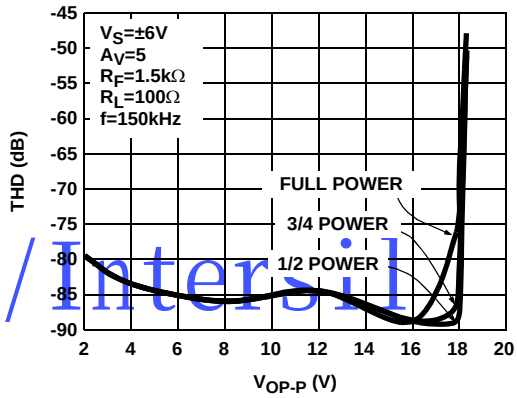


FIGURE 22. DIFFERENTIAL TOTAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE

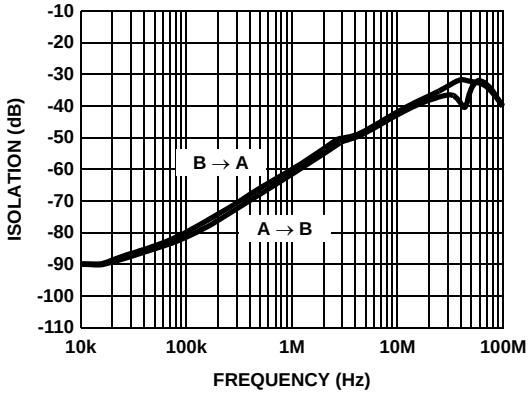


FIGURE 23. CHANNEL ISOLATION vs FREQUENCY

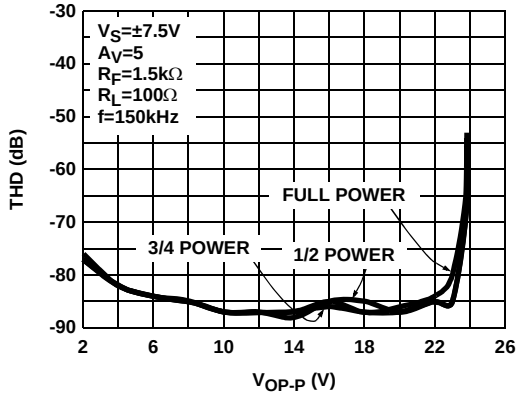


FIGURE 24. DIFFERENTIAL TOTAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE

Typical Performance Curves (Continued)

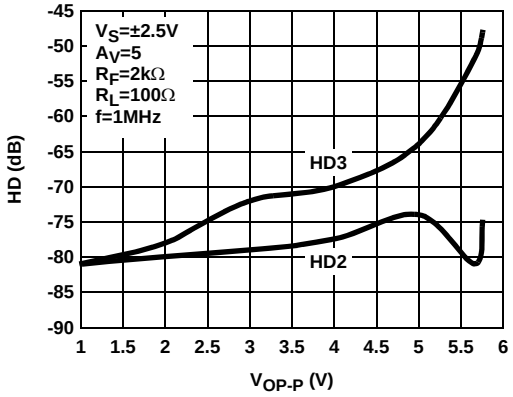


FIGURE 25. DIFFERENTIAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (FULL POWER MODE)

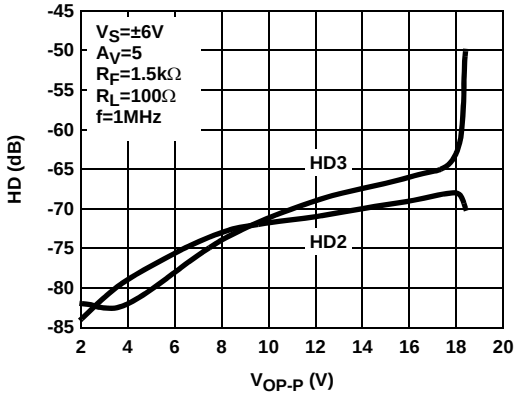


FIGURE 26. DIFFERENTIAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (FULL POWER MODE)

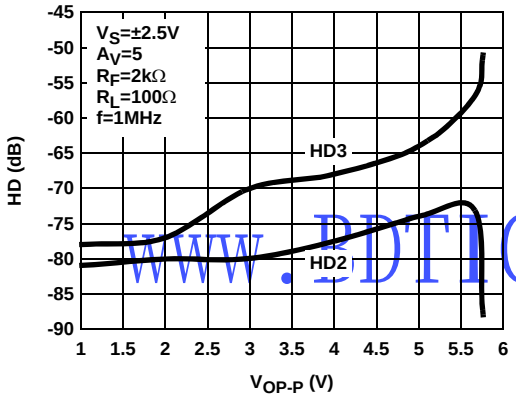


FIGURE 27. DIFFERENTIAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (3/4 POWER MODE)

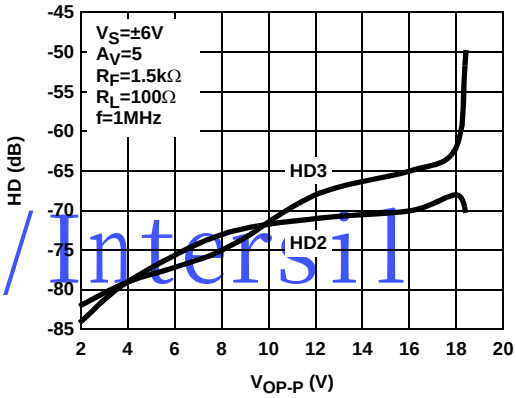


FIGURE 28. DIFFERENTIAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (3/4 POWER MODE)

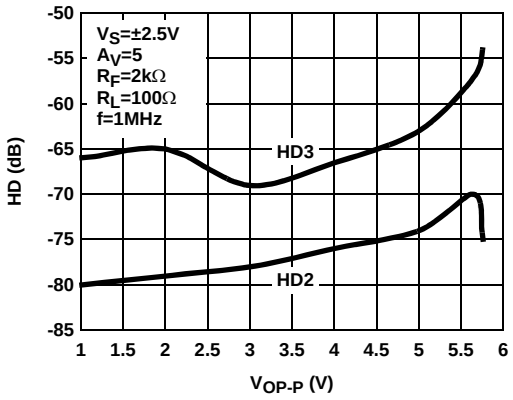


FIGURE 29. DIFFERENTIAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (1/2 POWER MODE)

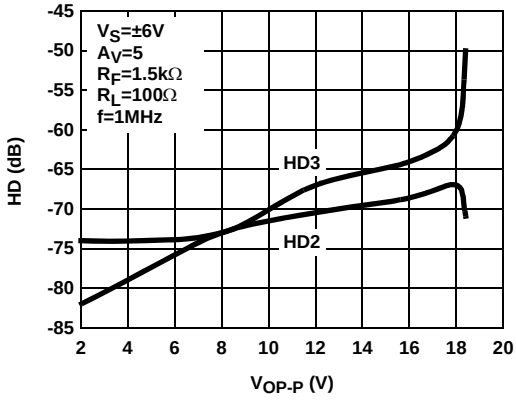


FIGURE 30. DIFFERENTIAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (1/2 POWER MODE)

Typical Performance Curves (Continued)

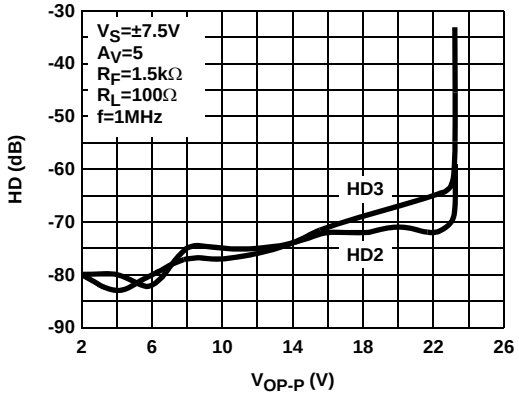


FIGURE 31. DIFFERENTIAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (FULL POWER MODE)

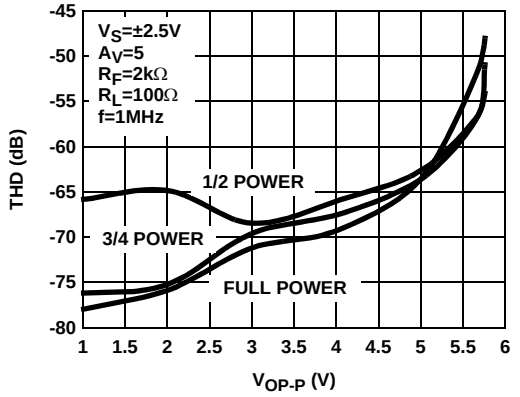


FIGURE 32. DIFFERENTIAL TOTAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE

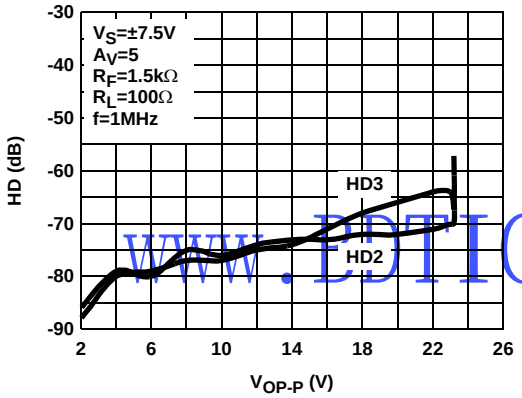


FIGURE 33. DIFFERENTIAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (3/4 POWER MODE)

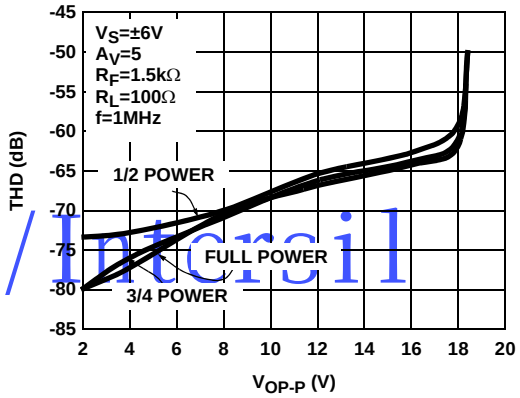


FIGURE 34. DIFFERENTIAL TOTAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE

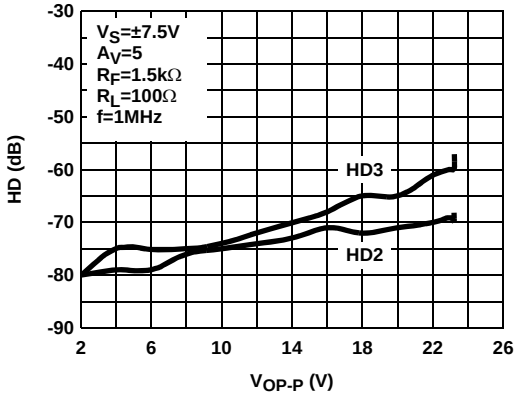


FIGURE 35. DIFFERENTIAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE (1/2 POWER MODE)

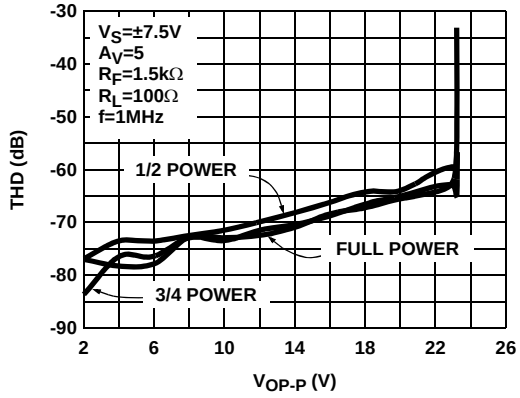


FIGURE 36. DIFFERENTIAL TOTAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE

Typical Performance Curves (Continued)

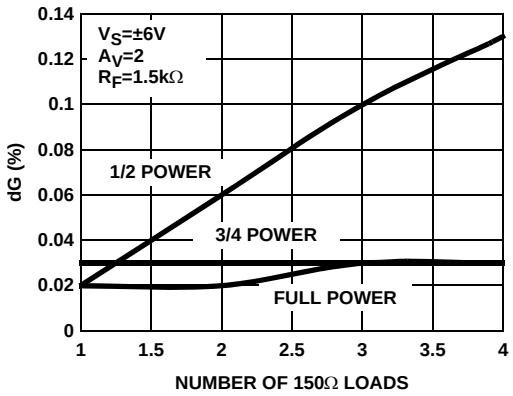


FIGURE 37. DIFFERENTIAL GAIN

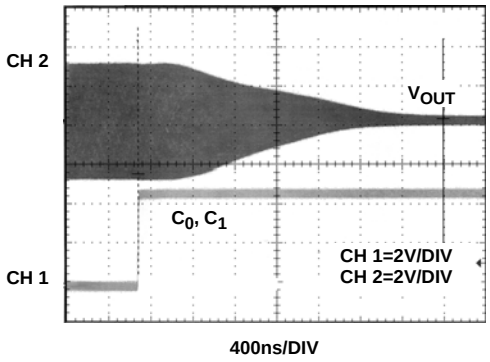


FIGURE 38. DISABLE TIME

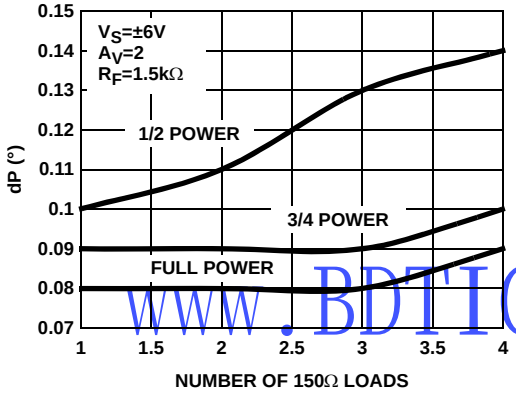


FIGURE 39. DIFFERENTIAL PHASE

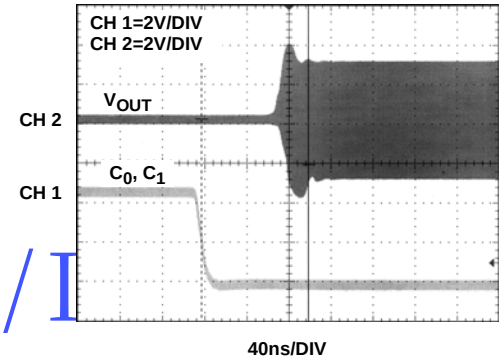


FIGURE 40. ENABLE TIME

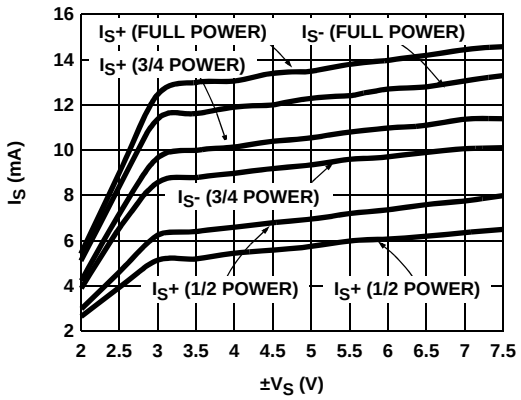


FIGURE 41. SUPPLY CURRENT vs SUPPLY VOLTAGE

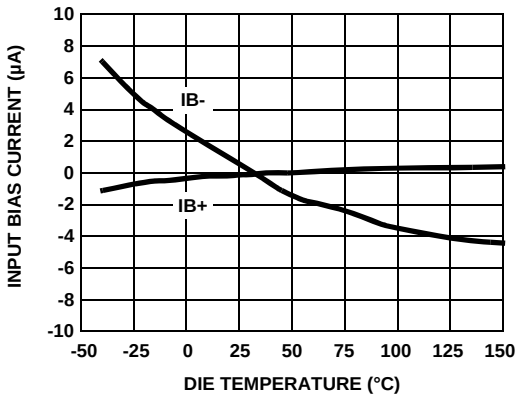


FIGURE 42. INPUT BIAS CURRENT vs TEMPERATURE

Typical Performance Curves (Continued)

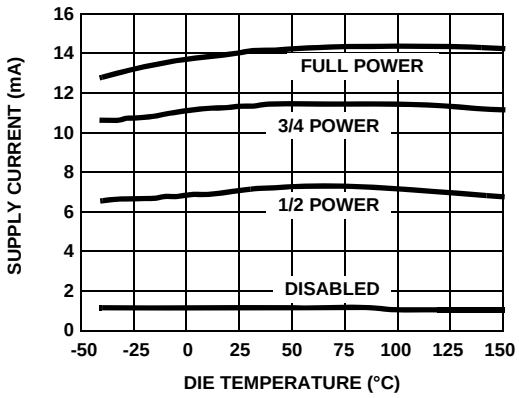


FIGURE 43. POSITIVE SUPPLY CURRENT vs TEMPERATURE

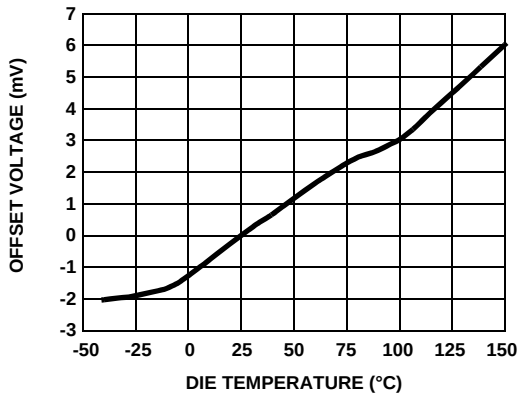


FIGURE 44. OFFSET VOLTAGE vs TEMPERATURE

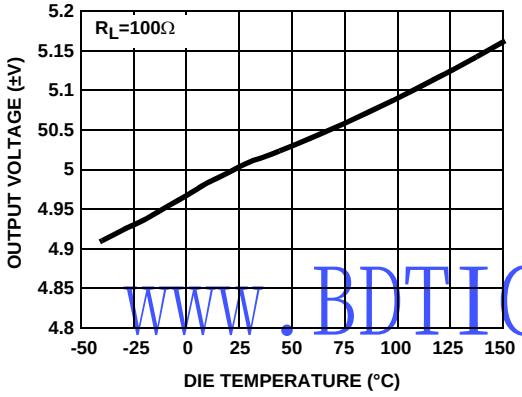


FIGURE 45. OUTPUT VOLTAGE vs TEMPERATURE

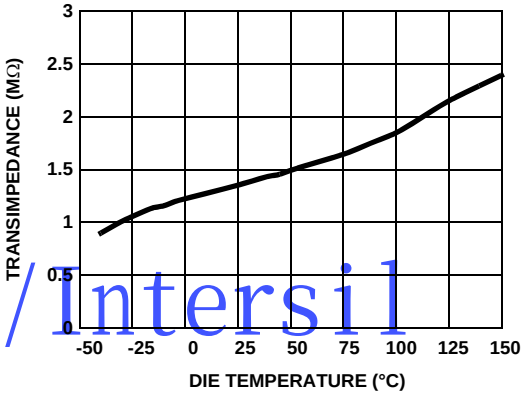


FIGURE 46. TRANSIMPEDANCE vs TEMPERATURE

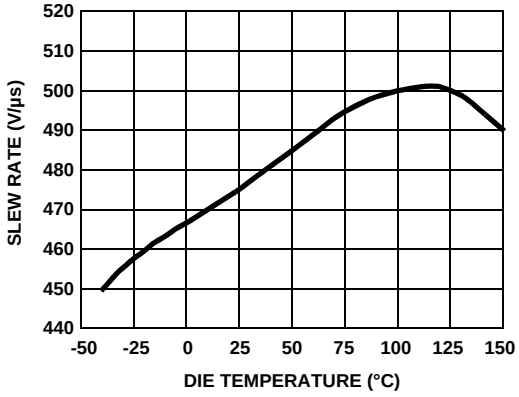


FIGURE 47. SLEW RATE vs TEMPERATURE

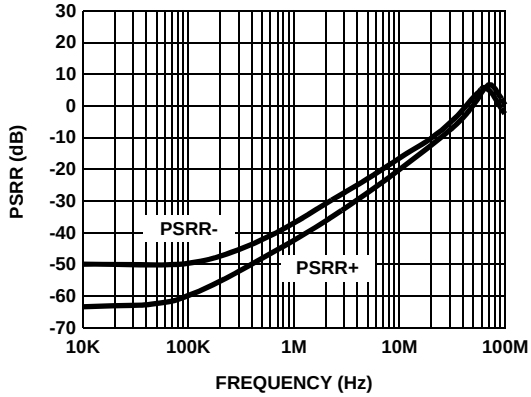


FIGURE 48. POWER SUPPLY REJECTION vs FREQUENCY

Typical Performance Curves (Continued)

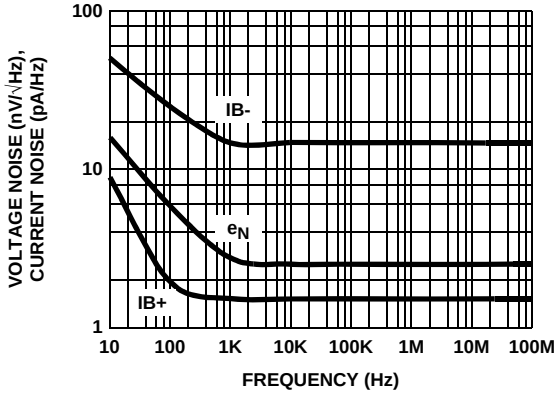


FIGURE 49. VOLTAGE AND CURRENT NOISE vs FREQUENCY

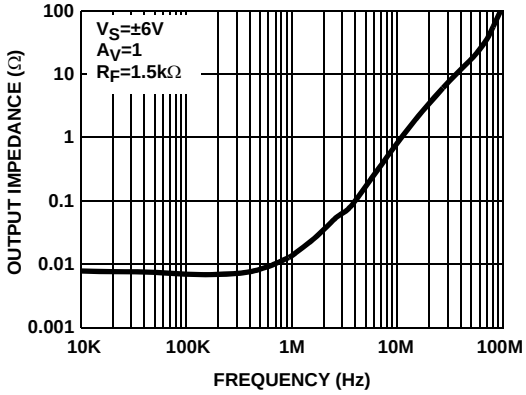


FIGURE 50. OUTPUT IMPEDANCE vs FREQUENCY (ALL POWER LEVELS)

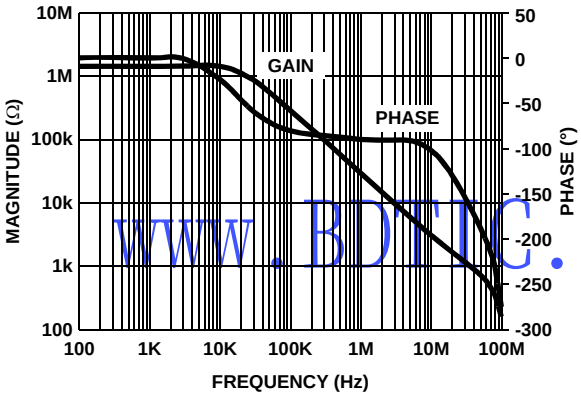


FIGURE 51. TRANSIMPEDANCE (ROL) vs FREQUENCY

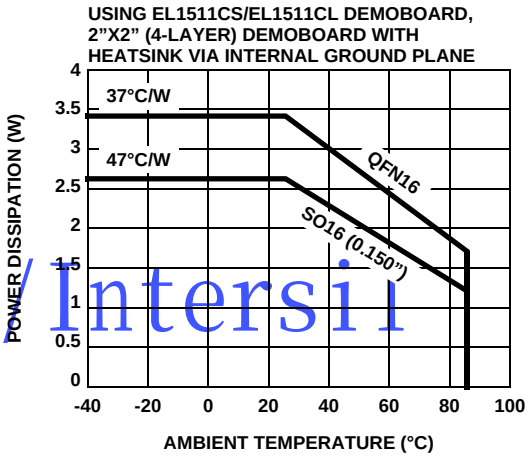


FIGURE 52. PACKAGE POWER DISSIPATION AND THERMAL RESISTANCE

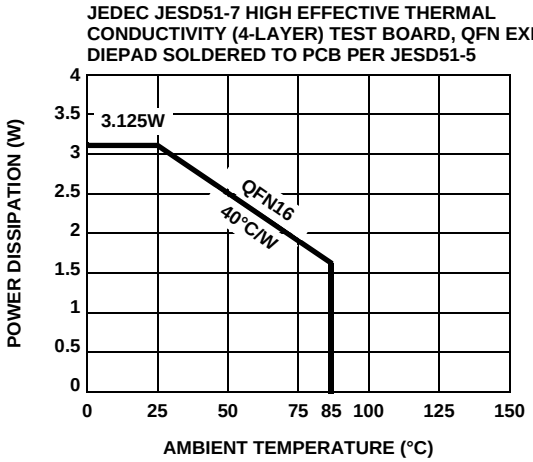


FIGURE 53. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Applications Information

Product Description

The EL1511 is a dual operational amplifier designed for customer premise driver functions in DMT ADSL solutions and is built using Elantec's proprietary complimentary bipolar process. Due to the current feedback architecture, the EL1511 closed-loop 3dB bandwidth is dependent on the value of the feedback resistor. First the desired bandwidth is selected by choosing the feedback resistor, R_F, and then the gain is set by picking the gain resistor, R_G. The curves at the beginning of the Typical Performance Curves section show the effect of varying both R_F and R_G.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible, below ¼. The power supply pins must be well bypassed to reduce the risk of oscillation. A 1.0µF tantalum capacitor in parallel with a 0.01µF ceramic capacitor is adequate for each supply pin.

For good AC performance, parasitic capacitances should be kept to a minimum, especially at the inverting input (see Capacitance at the Inverting Input section). This implies keeping the ground plane away from this pin. Carbon resistors are acceptable, while use of wire-wound resistors should not be used because of their parasitic inductance. Similarly, capacitors should be low inductance for best performance. Use of sockets, particularly for the SO (0.150") package, should be avoided. Sockets add parasitic inductance and capacitance which will result in peaking and overshoot.

Capacitance at the Inverting Input

Due to the topology of the current feedback amplifier, stray capacitance at the inverting input will affect the AC and transient performance of the EL1511 when operating in the non-inverting configuration.

In the inverting gain mode, added capacitance at the inverting input has little effect since this point is at a virtual ground and stray capacitance is therefore not “seen” by the amplifier.

Feedback Resistor Values

The EL1511 has been designed and specified with R_F = 1.5kΩ for A_V = +5. This value of feedback resistor yields relatively flat frequency response with <1.5dB peaking out to 60MHz. As is the case with all current feedback amplifiers, wider bandwidth, at the expense of slight peaking, can be obtained by reducing the value of the feedback resistor. Inversely, larger values of feedback resistor will cause rolloff to occur at a lower frequency. By reducing R_F to 1kΩ, bandwidth can be extended to 70MHz with 3.0dB of peaking. See the curves in the Typical Performance Curves section which show 3dB bandwidth and peaking vs frequency for various feedback resistors.

Power Dissipation

The EL1511 amplifier combines both high speed and large output current drive capability at a moderate supply current in very small packages. It is possible to exceed the maximum junction temperature allowed under certain supply voltage, temperature, and loading conditions. To ensure that the EL1511 remains within its absolute maximum ratings, the following discussion will help to avoid exceeding the maximum junction temperature.

The maximum power dissipation allowed in a package is determined by its thermal resistance and the amount of temperature rise according to:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}}$$

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage plus the power in the IC due to the load, or:

$$P_{DMAX} = 2 \times V_S + (V_S - V_{OUT}) \times \frac{V_{OUT}}{R_L}$$

where I_S is the supply current. (To be more accurate, the quiescent supply current flowing in the output driver transistor should be subtracted from the first term because, under loading and due to the class AB nature of the output stage, the output driver current is now included in the second term.)

In general, an amplifier's AC performance degrades at higher operating temperature and lower supply current. Unlike some amplifiers, the EL1511 maintains almost constant supply current over temperature so that AC performance is not degraded as much over the entire operating temperature range.

Estimating Line Driver Power Dissipation in ADSL CPE Application

The below figure shows a typical ADSL CPE line driver implementation. The average line power requirement for the ADSL CPE application is 13dBM (20mW) into a 100W line. The average line voltage is $1.41V_{RMS}$. The ADSL DMT peak to average ratio (crest factor) of 5.3 implies peak voltage of 7.5V into the line. Using a differential drive configuration and transformer coupling with standard back termination, a transformer ratio of 1:2 is selected. With 1:2 transformer ratio, the impedance across the driver side of the transformer is 25Ω, the average voltage is $0.705V_{RMA}$ and the average current is 28.2mA. The power dissipated in the EL1511 is a combination of the quiescent power and the output stage power when driving the line:

$$PD = P_{quiescent} + P_{output\text{-}stage}$$

$$PD = V_S \times I_Q + (V_S - 2 \times V_{OUT\text{-}RMS}) \times I_{OUT\text{-}RMS}$$

In the ½ power mode, the EL1511 consumes typically 6.6mA quiescent current and still able to maintain very low distortion. The distortion results are shown in typical

performance section of the data sheet. When driving a load, a large portion (about 50%) of the quiescent current becomes output load current:

$$PD = 12 \times (6.6mA \times 50\%) + (12V - 2 \times 0.705) \times 28.2mA$$

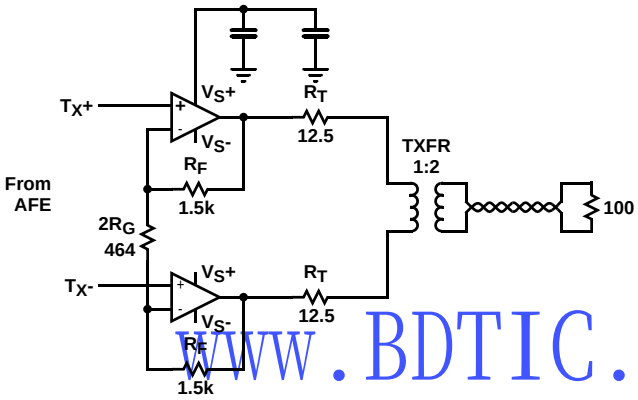
where:

PD = 338mW

Assuming a maximum ambient temperature of 85°C and keeping the junction temperature less than 150°C, the maximum thermal resistance from junction to ambient required is:

$$\Theta_{JA} = \frac{150 - 85}{338mW} = 192°C/W$$

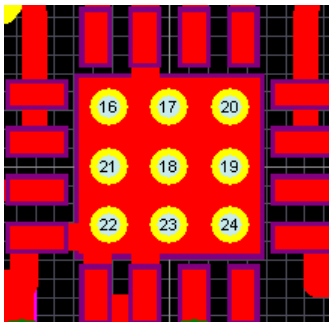
With proper layout, the EL1511CS package can achieve 47°C/W, well below the thermal resistance required by the application.



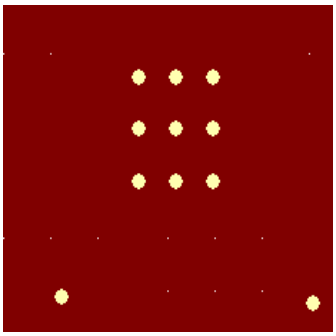
PCB Layout Considerations for Thermal Packages

The EL1511 die is packaged in two different thermal efficient packages, the 16 Ld SO and 16 Ld QFN packages. The 16 Ld SO package has the same dimensions as standard 0.15" wide narrow body 16 Ld SO package with a special fused lead frame that extends out through the center ground pins. Both packages can use PCB surface metal vias areas and internal ground planes, to spread heat away from the package. The larger the PCB area the lower the junction temperature of the device will be. In XDSL applications, multiple layer circuit boards with internal ground plane are generally used. 13 mil vias are recommended to connect the metal area under the device with the internal ground plane. Examples of the PCB layouts are shown in the figures below that result in thermal resistance θ_{JA} of 37°C/W for the QFN package and 47°C/W for the SO package. The thermal resistance is obtained with the EL1511CL and CS demo boards. The demo board is a 4-layer board built with 2oz. copper and has a dimension of $4in^2$. Note, the user must follow the thermal layout guideline to achieve these results.

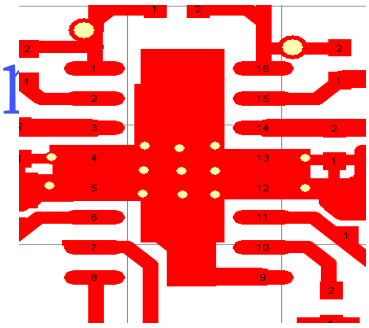
A separate Application Note for the QFN package and layout recommendations is also available.



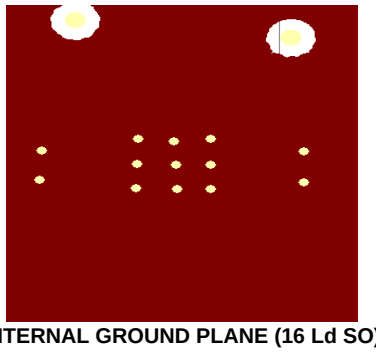
TOP (16 Ld QFN)



INTERNAL GROUND PLANE (16 Ld QFN)

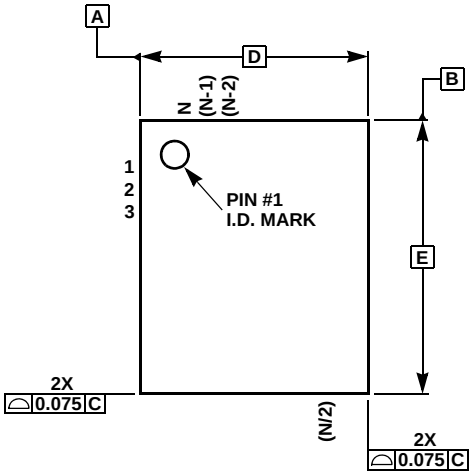


TOP (16 Ld SO)

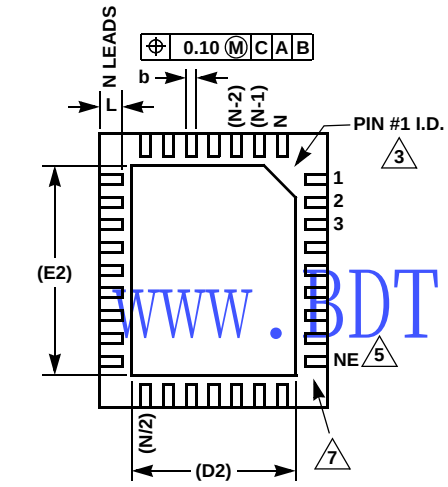


INTERNAL GROUND PLANE (16 Ld SO)

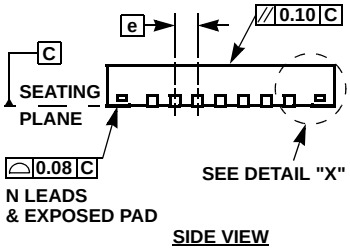
QFN (Quad Flat No-Lead) Package Family



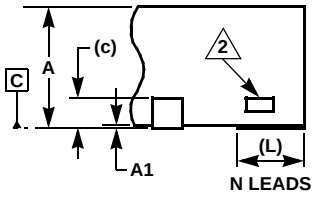
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL X

MDP0046

QFN (QUAD FLAT NO-LEAD) PACKAGE FAMILY (COMPLIANT TO JEDEC MO-220)

SYMBOL	MILLIMETERS				TOLERANCE	NOTES
	QFN44	QFN38	QFN32			
A	0.90	0.90	0.90	0.90	±0.10	-
A1	0.02	0.02	0.02	0.02	+0.03/-0.02	-
b	0.25	0.25	0.23	0.22	±0.02	-
c	0.20	0.20	0.20	0.20	Reference	-
D	7.00	5.00	8.00	5.00	Basic	-
D2	5.10	3.80	5.80	3.60/2.48	Reference	8
E	7.00	7.00	8.00	6.00	Basic	-
E2	5.10	5.80	5.80	4.60/3.40	Reference	8
e	0.50	0.50	0.80	0.50	Basic	-
L	0.55	0.40	0.53	0.50	±0.05	-
N	44	38	32	32	Reference	4
ND	11	7	8	7	Reference	6
NE	11	12	8	9	Reference	5

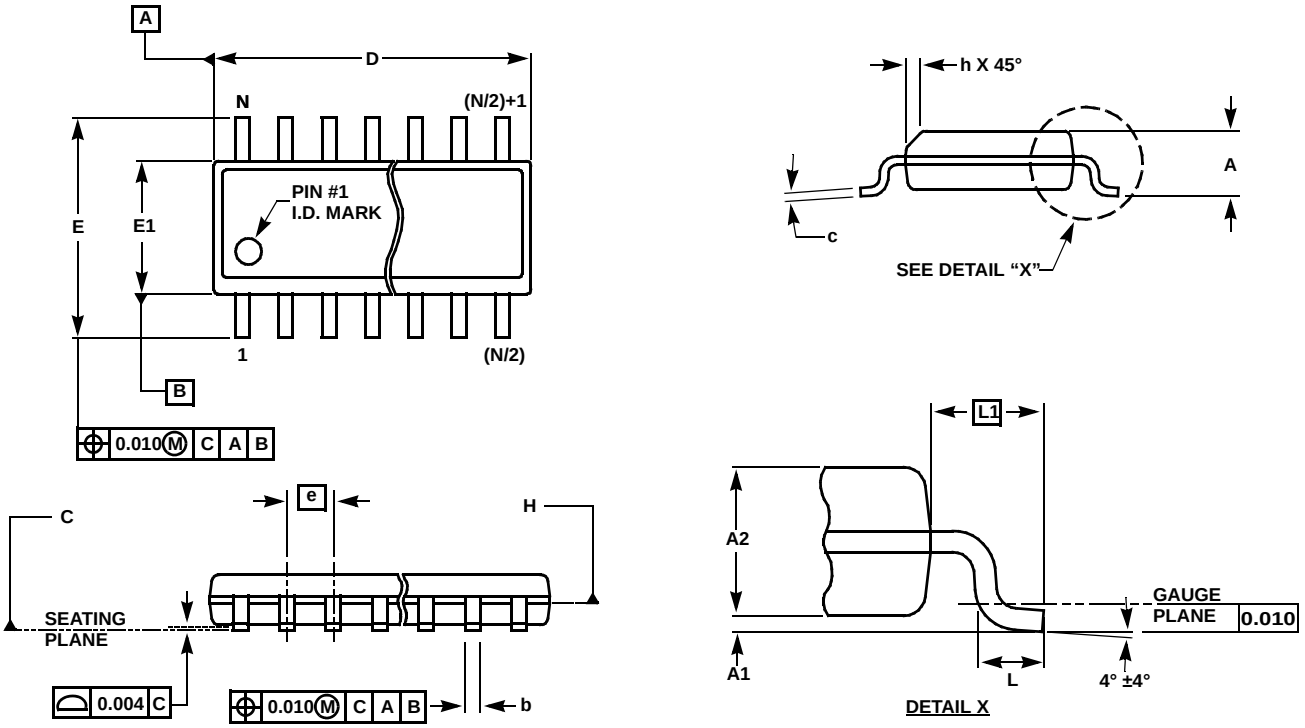
SYMBOL	MILLIMETERS					TOLER-ANCE	NOTES
	QFN28	QFN24	QFN20		QFN16		
A	0.90	0.90	0.90	0.90	0.90	±0.10	-
A1	0.02	0.02	0.02	0.02	0.02	+0.03/ -0.02	-
b	0.25	0.25	0.30	0.25	0.33	±0.02	-
c	0.20	0.20	0.20	0.20	0.20	Reference	-
D	4.00	4.00	5.00	4.00	4.00	Basic	-
D2	2.65	2.80	3.70	2.70	2.40	Reference	-
E	5.00	5.00	5.00	4.00	4.00	Basic	-
E2	3.65	3.80	3.70	2.70	2.40	Reference	-
e	0.50	0.50	0.65	0.50	0.65	Basic	-
L	0.40	0.40	0.40	0.40	0.60	±0.05	-
N	28	24	20	20	16	Reference	4
ND	6	5	5	5	4	Reference	6
NE	8	7	5	5	4	Reference	5

Rev 11 2/07

NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Tiebar view shown is a non-functional feature.
3. Bottom-side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the “E” side of the package (or Y-direction).
6. ND is the number of terminals on the “D” side of the package (or X-direction). ND = (N/2)-NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device-specific datasheet.

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994