**2**

**ATE ICs**

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# Pin Electronics
## Venus

| Overview | | | | | | Pin Electronics | | | | | PMU | | | Deskew | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Device | Description | # Channels | Status | Package | Pdq | $F_{MAX}$ (MHz) | Driver | Comparator (V) | Load | DC Levels | PMU | DC Levels | $I_{MAX}$ (mA) | Delay (ns) | FEA | Resolution (ps) |
| Venus | P/E + PMU + DAC + Deskew | 2 | Production | 10x10 TQFP with exposed slug up | 750mW/ Channel | 133 | 3 Level/ 8V | 16 | Resistive/ 14V | On Chip | 1/ Channel | On Chip | 32 | 8 to 20 | ±25% of Delay | 15 to 37.5 |
| Venus Plus | P/E + PMU + DAC + Deskew | 2 | Production | 10x10 TQFP with exposed slug up | 750mW/ Channel | 166 | 3 Level/ 8V | 16 | Resistive/ 14V | On Chip | 1/ Channel | On Chip | 32 | 8 to 13.3 | ±25% of Delay | 15 to 26 |
| Venus 2 | P/E + PMU + DAC + Deskew | 2 | Pre-Production | 10x10 TQFP with exposed slug up | 1W/ Channel | 266 | 3 Level/ 8V | 16 | Resistive/ 14V | On Chip | 1/ Channel | On Chip | 32 | 8 to 16 | ±12.5% of Delay | 15 to 30 |
| Venus 3 | P/E + PMU + DAC + Deskew | 2 | Pre-Production | 10x10 TQFP with exposed slug up | 1W/ Channel | 400 | 3 Level/ 8V | 16 | Resistive/ 14V | On Chip | 1/ Channel | On Chip | 32 | 6.4 to 12.8 | ±12.5 of Delay | 12 to 25 |
| Venus 4 | P/E + PMU + Load + DAC + Deskew | 2 | Engineering Sample | 10x10 TQFP with exposed slug up | 600mW/ Channel | 400 | 3 Level/ 8V | 16 | Active/ ±24mA | On Chip | 1/ Channel | On Chip | 32 | 3.2 to 5.0 | ±50% of Delay | 12 to 20 |
| Venus 4 MLF | P/E + PMU + Load + DAC + Deskew | 2 | Engineering Sample | 9x9 MLF TEP (Top Exposed Paddle) | 600mW/ Channel | 400 | 3 Level/ 8V | 16 | Active/ ±24mA | On Chip | 1/ Channel | On Chip | 32 | 3.2 to 5.0 | ±50% of Delay | 12 to 20 |

## Non-Venus

| Overview | | | | | | Pin Electronics | | | | | PMU | | | Deskew | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Device | Description | # Channels | Status | Package | Pdq | $F_{MAX}$ (MHz) | Driver | Comparator (V) | Load | DC Levels | PMU | DC Levels | $I_{MAX}$ (mA) | Delay (ns) | FEA | Resolution (ps) |
| Mercury | P/E + PMU + DAC + Deskew | 8 | Production | 14x20 TQFP with exposed slug up | 350mW/ Channel | 50 | 2 Level/ 8V | 16 | | On Chip | 1/ Chip | On Chip | 32 | 10 to 20 | ±25% of Delay | 312.5 to 625 |
| Saturn | P/E + PMU + DAC + Deskew + DPS | 2 | Pre-Production | 14x20 TQFP with exposed slug up | 1.5W/ Channel | 100 | 2 Level/ 24V | 32 | Active/ 24mA/32V | On Chip | 1/ Channel | On Chip | 200 | 10 to 20 | ±25% of Delay | 312.5 to 625 |
| Pluto | P/E + PMU + DAC | 8 | Production | 14x20 TQFP with exposed slug up | 500mW/ Channel | 5 | 2 Level/ 14V | 16 | Resistive 14V | On Chip | 1/ Channel | On Chip | 64 Gangable | | | |
| Pluto 2 | P/E + PMU + DAC | 8 | Engineering Sample | 14x20 TQFP with exposed slug up | 125mW/ Channel | 10 | 2 Level/ 14V | 16 | Resistive 14V | On Chip | 1/ Channel | On Chip | 64 Gangable | | | |

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## DPS/PMU/VI

| Overview | | | | | | PMU | | | |
|---|---|---|---|---|---|---|---|---|---|
| Device | Description | # Channels | Status | Package | Pdq | PMU | DC Levels | I$_{MAX}$ | FV Range (V) |
| Neptune | PMU + DAC | 2 | Production | 8x8 MLF with exposed slug down | 300mW/Channel | 1/Channel | On Chip | 64mA Gangable | 14 |
| Pluto | P/E + PMU/VI + DAC | 8 | Production | 14x20 TQFP with exposed slug up | 500mW/Channel | 1/Channel | On Chip | 64mA Gangable | 14 |
| Pluto 2 | P/E + PMU/VI /DPS + DAC | 8 | Engineering Sample | 14x20 TQFP with exposed slug up | 125mW/Channel | 1/Channel | On Chip | 64mA Gangable | 14 |
| Jupiter | DPS/VI/PMU | 1 | Pre-Production | 10x10 TQFP with exposed slug up | 1W/Channel | 1/Channel | On Chip | 1A Gangable | 26 |
| Triton | DPS/VI/PMU | 8 | Engineering Sample | 14x20 TQFP with exposed slug up | 350mV/Channel | 1/Channel | On Chip | 50mA | 26 |

## Pin Drivers

| Device | # of Drivers | Max Operating Frequency (MHz) | Peak Output I$_{PK}$ (A) | Rise Time (ns) | Fall Time (ns) | Turn Off Delay (ns) | I$_S$ (mA) | R$_{ON}$ (Ω) | Input Signal Range (V) | Input Supply Range (V$_P$) | Max Input Signal (V) | Output Signal Range (V) | Max Output Signal Range (V) | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| EL7154 | 1 | 10 | 4 | 20 | 20 | 20 | 2.5 | 1.5 | 0 to V$_P$ | -4.5 to +18 | 16 | -3 to +15.5 | 15.5 | 8 Ld PDIP, 8 Ld SOIC |
| EL7155 | 1 | 40 | 3.5 | 14.5 | 15 | 9.5 | 3 | 2 | 0 to V$_P$ | +4.5 to +16 | 16 | -5 to +16 | 16 | 8 Ld PDIP, 8 Ld SOIC |
| EL7156 | 1 | 40 | 3.5 | 14.5 | 15 | 9.5 | 3 | 2 | 0 to V$_P$ | +4.5 to +16 | 16 | -5 to +16 | 16 | 8 Ld PDIP, 8 Ld SOIC |
| EL7158 | 1 | 40 | 12 | 8 | 8 | 22 | 3 | 0.5 | 0 to V$_P$ | +4.5 to +18 | 18 | -5 to +12 | 12 | 8 Ld SOIC |
| ISL55100A | 4 | 65 | 1 | 2.5 | 2.5 | 18 | 70 | 5 | -V$_P$ to +V$_P$ | -18 to +18 | 18 | -V$_P$ to +V$_P$ | 18 | 72 Ld QFN |
| ISL55100B | 4 | 50 | 1 | 3 | 3 | 18 | 70 | 9 | -V$_P$ to +V$_P$ | -18 to +18 | 18 | -V$_P$ to +V$_P$ | 18 | 72 Ld QFN |
| ISL55110 | 2 | 100 | 3.5 | 1.5 | 1.5 | 20 QFN Only | 3.5 | 3 | 0 to V$_P$ | +2.7 to +5.5 | 5.5 | 0 to +13.2 | 13.2 | 8 Ld TSSOP, 16 Ld QFN |
| ISL55111 | 2 | 100 | 3.5 | 1.5 | 1.5 | 20 QFN Only | 3.5 | 3 | 0 to V$_P$ | +2.7 to +5.5 | 5.5 | 0 to +13.2 | 13.2 | 8 Ld TSSOP, 16 Ld QFN |

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