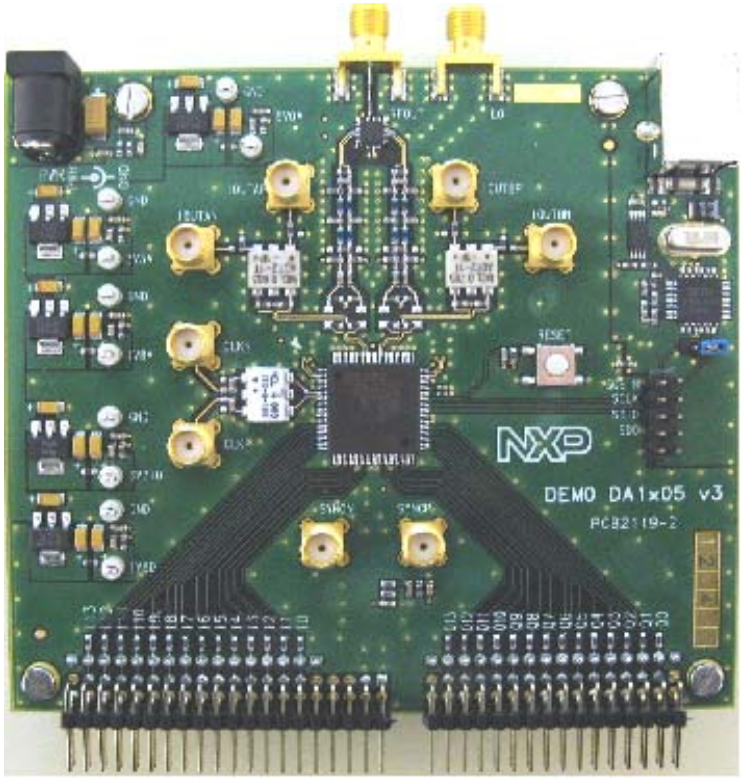
Quick Start

DEMO DA1x05 v3 Demonstration Board for DAC1405D750

Document information

Info	Content
Keywords	DEMO DA1x05 v3, PCB2119-2, Demonstration board, DAC, Converter, DAC1405D750, DAC1205D750, DAC1005D750
Abstract	This document describes how to use the demonstration board DEMO DA1x05 v3 for the digital-to-analog converters DAC1405D750, DAC1205D750 and DAC1005D750.
Overview	

Revision history

Rev	Date	Description
02	20110311	Updated version.

1. Quick start

1.1 Setup overview

Figure Fig 1 presents the connections to measure DEMO DA1x05 v3.

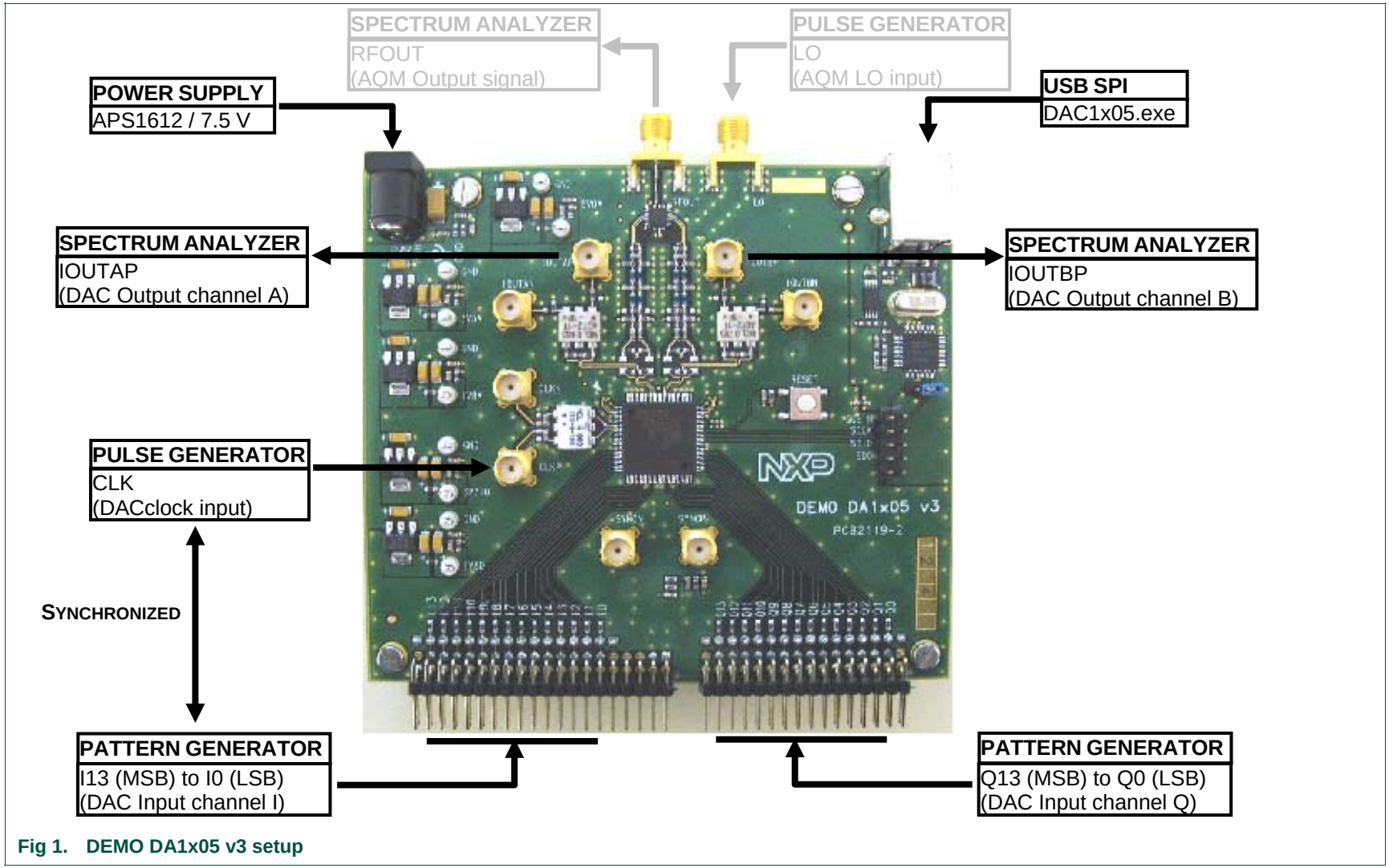
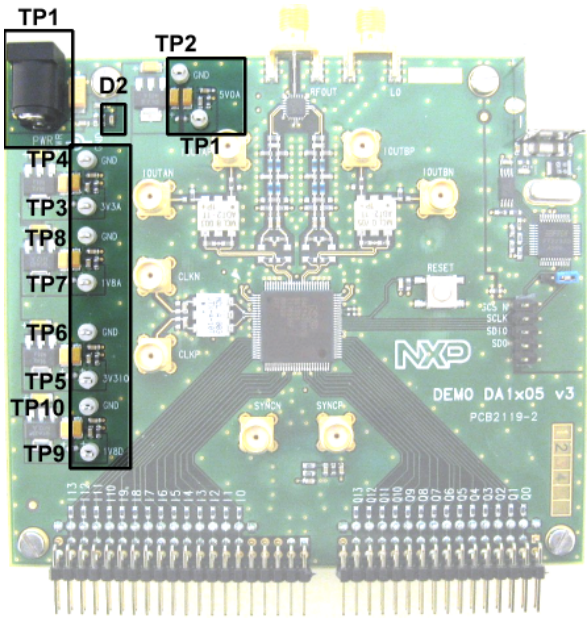


Fig 1. DEMO DA1x05 v3 setup

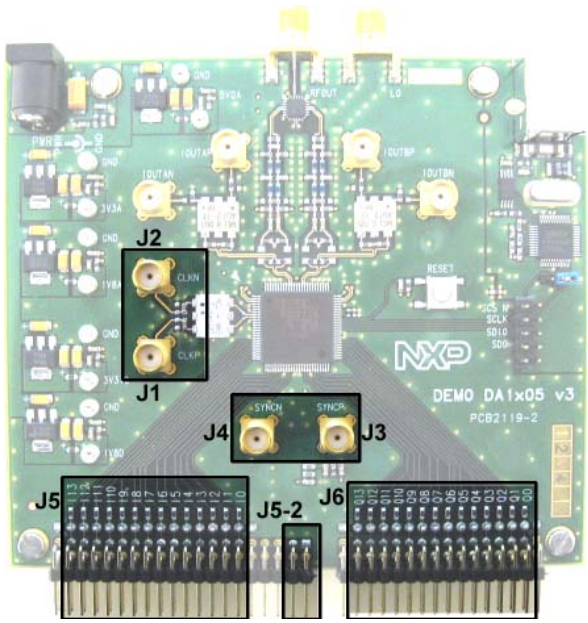
1.2 Power supply

Table 1. Power supply

Name	Function	View
J15	PWR – General power supply 7.5V V_{DC}	
D2	Power-on diode (active red)	
TP1	5V0A test point – Analog power supply 5.0 V_{DC}	
TP3	3V3A test point – Analog power supply 3.3 V_{DC}	
TP7	1V8A test point – Analog power supply 1.8 V_{DC}	
TP5	3V3IO test point – I/O power supply 3.3 V_{DC}	
TP9	1V8A test point – Analog power supply 1.8 V_{DC}	
TP2, TP4, TP8, TP6, TP10	GND test point – Ground	

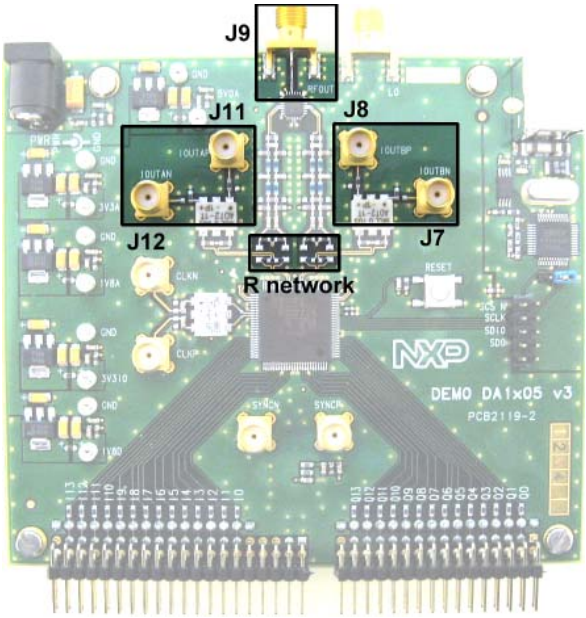
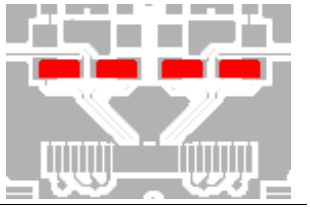
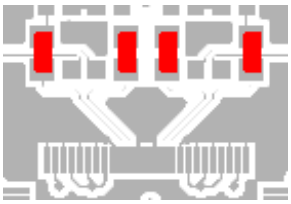
1.3 Digital signals

Table 2. Digital signals

Name	Function	View
J1, J2	CLKP, CLKN connectors – DAC clock input	
J5	I data connector – Channel I digital input (I0 to I13)	
J6	Q data connector – Channel Q digital input (Q0 to Q13)	
J3, J4	SYNCP, SYNCN connectors – Data sampling clock output	
J5-2	I data connector – SYNCP & SYNCN output	
Resistor network (bottom side)	SYNC output connected to J3 and J4 	
	SYNC output connected to J5-2 	

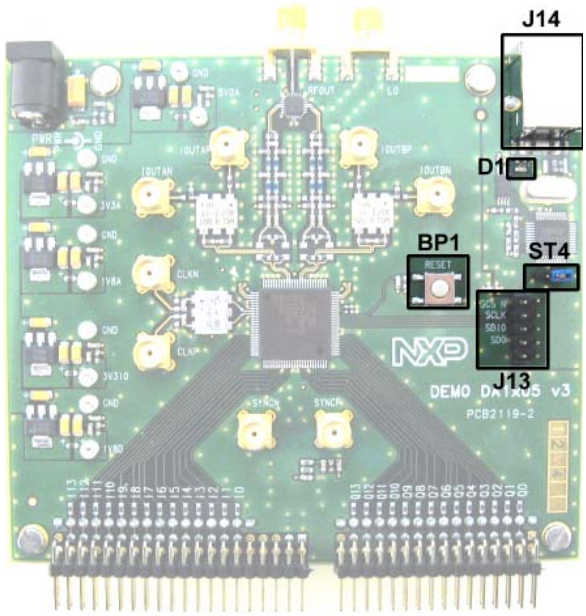
1.4 Analog signals

Table 3. Analog signals

Name	Function	View
J11, J12	IOUTAP, IOUTAN connectors – DAC channel A analog output signal	
J8, J7	IOUTBP, IOUTBN connector – DAC channel B analog output signal	
J9	RFOUT connector – AQM analog output	
J10	LO connector – AQM LO input	
Resistor network	DAC output connected to the output transformers 	
	DAC output connected to the AQM 	

1.5 SPI interface

Table 4. **SPI interface**

Name	Function	View
J14	SPI connector – USB input for SPI programming	
D1	SPI diode – Red indicates the proper USB connection	
ST4	Jumper - Open for 4-wire SPI interface / Closed for 3-wire SPI interface	
BP1	RESET button – Hardware reset of the DAC registers	
J13	SPI test point – External connection to SCS_N, SCLK, SDIO and SDO	

2. SPI quick start

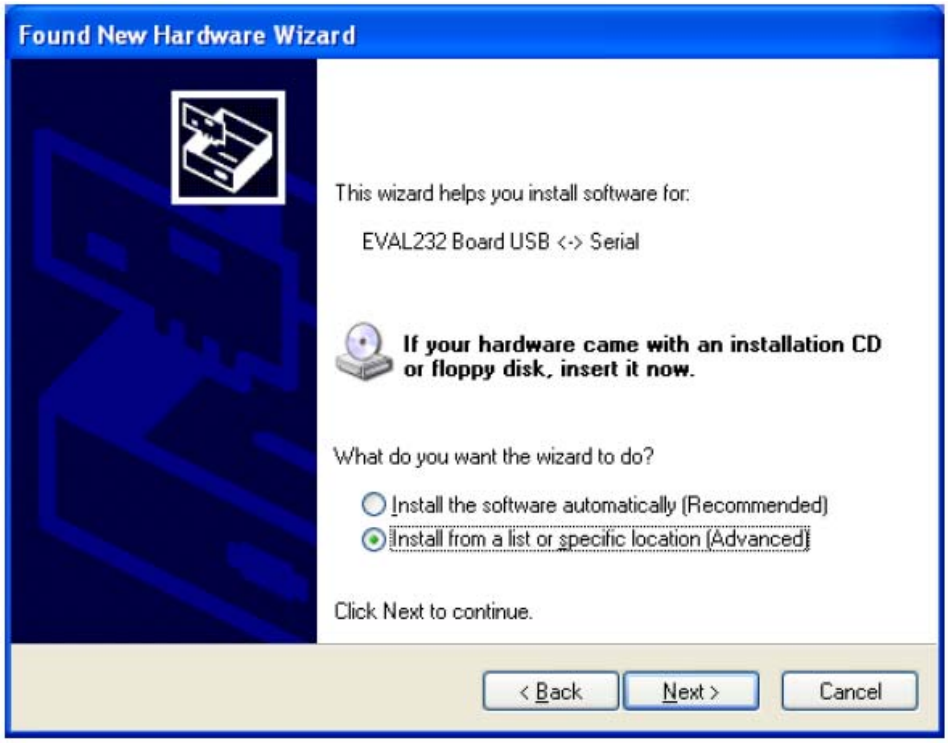
2.1 Install

STEP 1

Connect the device to a USB port on your PC. Windows '**Found New Hardware Wizard**' will be launched. Select '**No, not this time**' from the options available and then click '**Next**' to proceed with the installation.

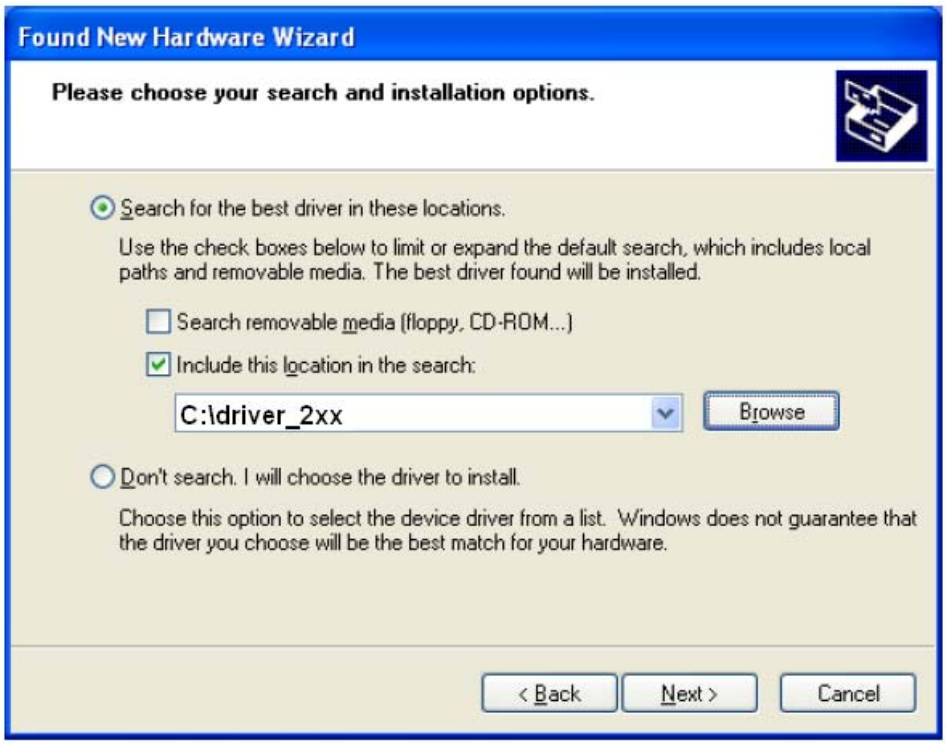
STEP 2

Select '**Install from a list or specific location (Advanced)**' as shown below and then click '**Next**'.



STEP 3

Select '**Search for the best driver in these locations**' and enter the file path of the folder '**driver_2xx**' in the combo-box ('C:\driver_2xx' in the example below) or browse to it by clicking the browse button. Once the file path has been entered in the box, click '**next**' to proceed.



STEP 4

Windows should then display a message indicating that the installation was successful. Click '**Finish**' to complete the installation for the first port of the device.

STEP 5

The Found New Hardware Wizard will continue by installing the USB Serial Converter driver for the second port of the device. The procedure for installing the second port is identical to that for installing the first port from the first screen of the Found New Hardware Wizard.

Once the second port is installed, the device should be ready to be used.

2.2 SPI interface

STEP 1

Install the LabVIEW Run-time Engine 'LabVIEW85RuntimeEngineFull.exe' (if not already installed).

STEP 2

Start the LabVIEW application "DAC1x05.exe".

See configuration example below.

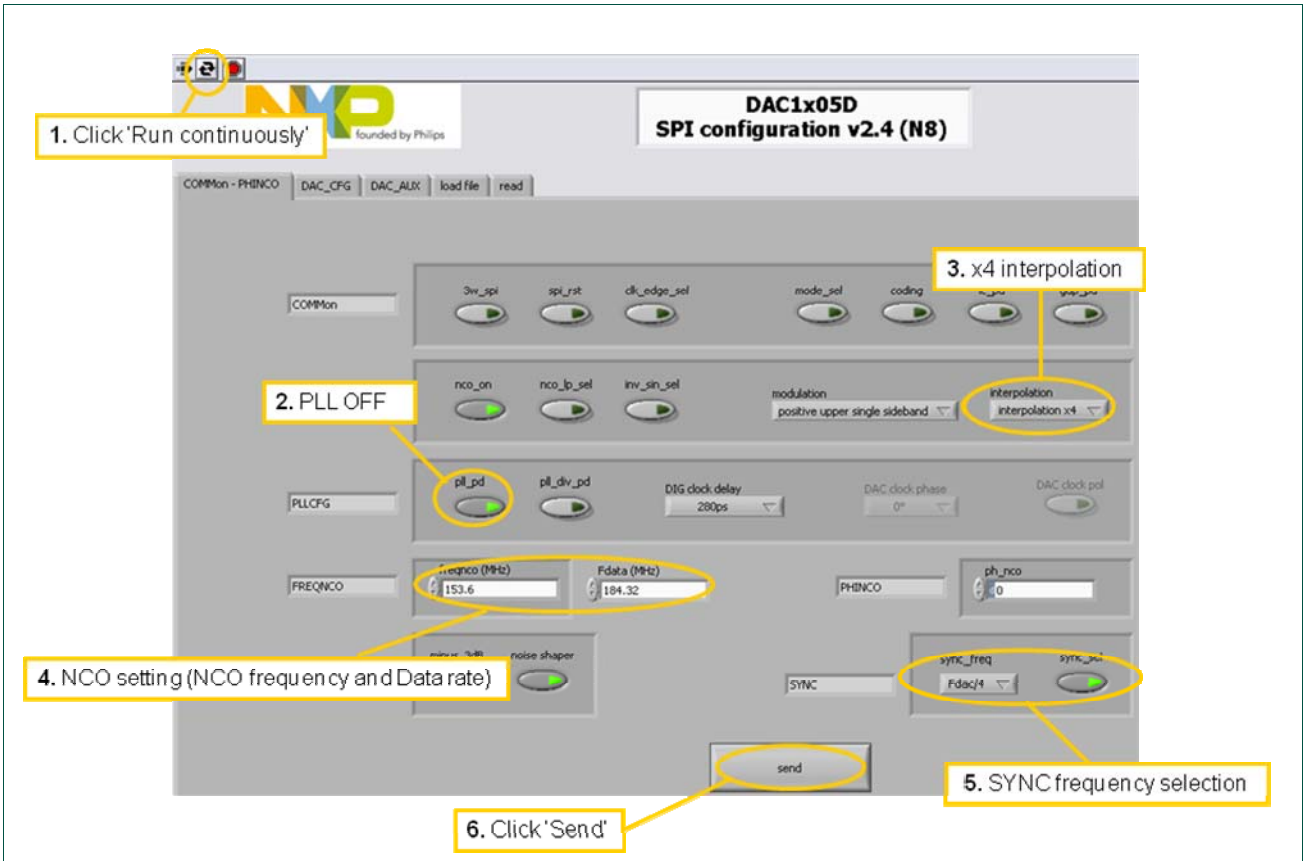


Fig 2. "USBConfigSetup" window: step 1

The page 'COMMon-PHINCO' allows to adjust the main settings of the DAC1x05D750.

The page 'DAC_CFG' allows to adjust the gain and the digital offset of each DAC.

The page 'DAC_AUX' allows to adjust the current of each auxiliary DAC.

The page 'load file' allows to load directly a text file with the register addresses and values.

The page 'read' allows to read the register in the DAC and to save them in a text file.

3. HSDC extension module: generation board

3.1 Overview

The figure 17 shows an overview of the extension module HSDC-EXTMOD01/DB generation board.

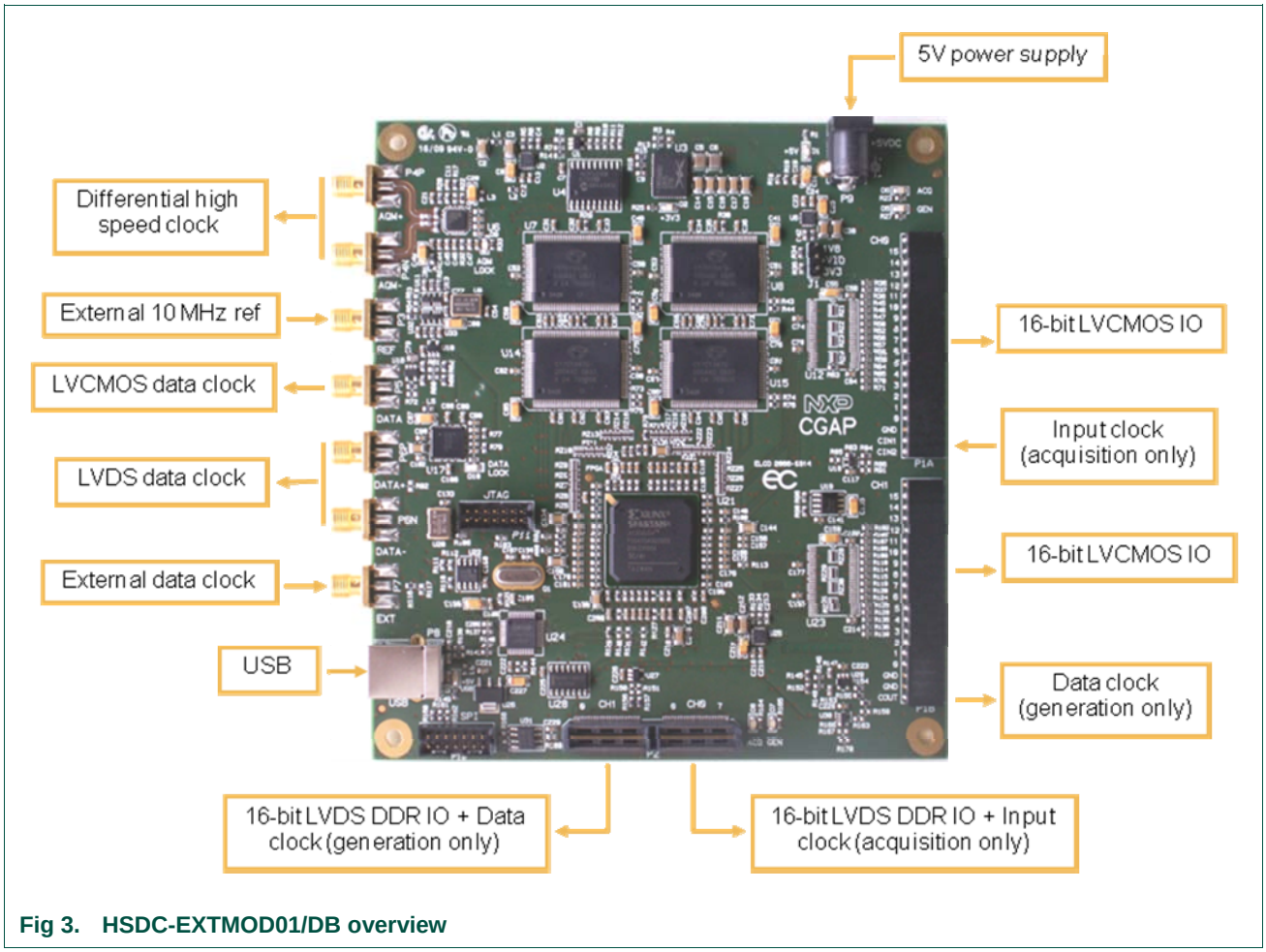


Fig 3. HSDC-EXTMOD01/DB overview

The HSDC extension module is intended for acquisition/generation and clock generation purpose. When connected to an ADC demo-board it is intended as an acquisition system for digital output bits delivered by ADC, either CMOS (HE14 P1 connector) or LVDS DDR (SAMTEC QTH_060_02 P2 connector).

The board brief specification is shown below:

- 8MB memory size for acquisition pattern;
- 2 x 16-bit channels CMOS up to 200MHz;
- 2 x 16-bit LVDS DDR input data stream up to 320MHz;
- On-board or external reference for signal generation.

3.2 HSDC extension module: software initialization

Before using the generation board, the user needs to install software to control the board. The steps are described below.

Run the application ‘USBConfigSetup.msi’, this will display the following window:

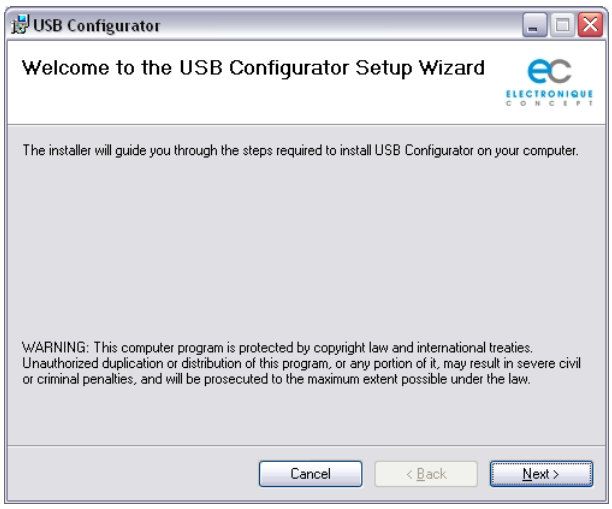


Fig 4. 'USBConfigSetup' window: step 1

Click 'Next' to proceed with installation process:

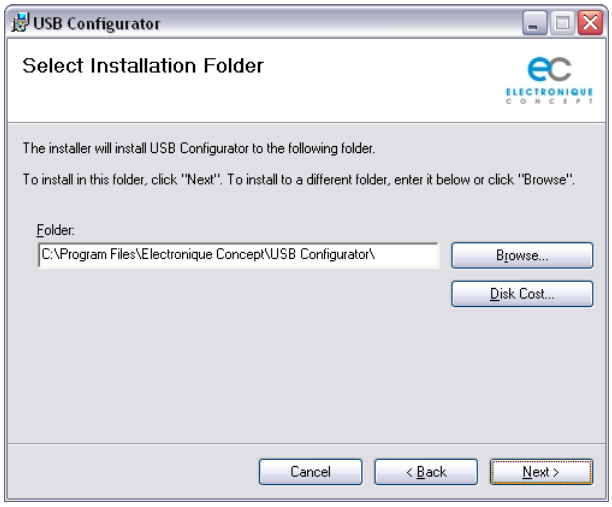


Fig 5. 'USBConfigSetup' window: step 2

Click 'Next' to continue:

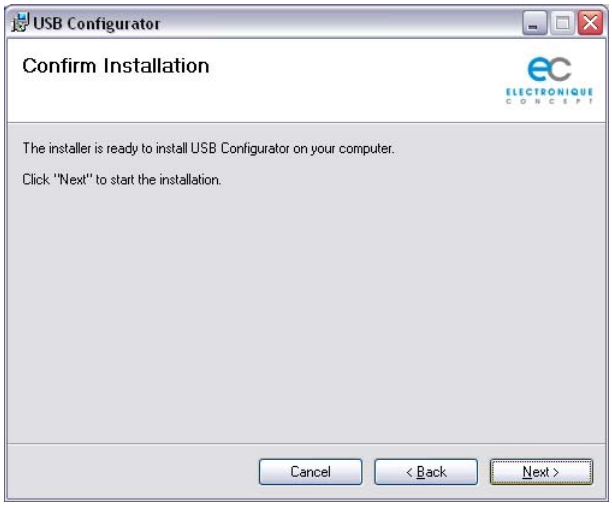


Fig 6. 'USBConfigSetup' window: step 3

Click 'Next' to finish the installation process.

3.3 HSDC extension module: CMOS connector description

The figure 7 shows a brief description of the hardware connection on the HE14 connector:

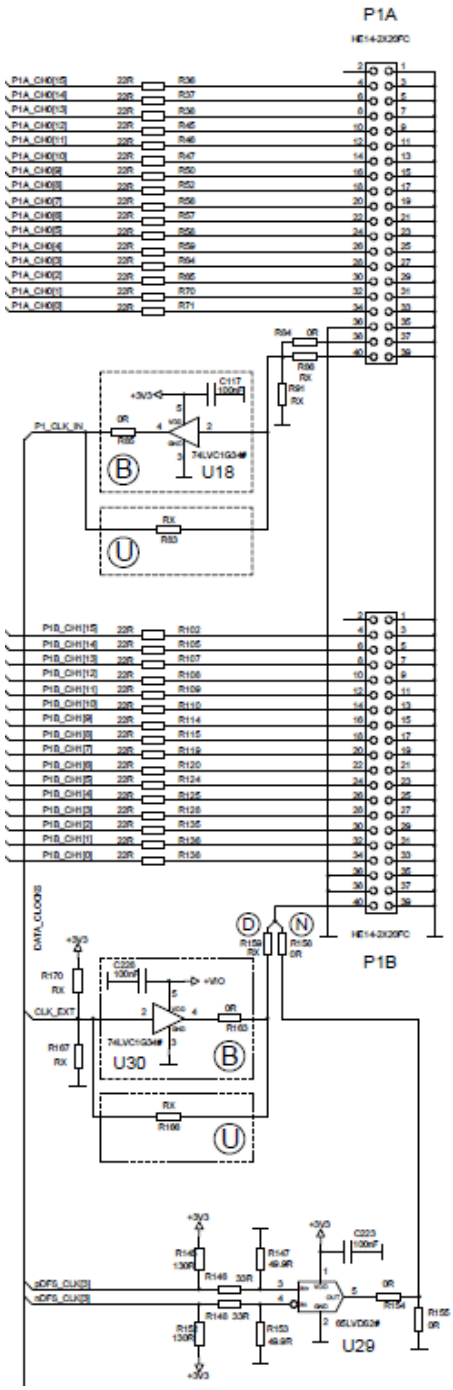


Fig 7. HSDC extension module: HE14 CMOS hardware schematic overview

The HSDC extension module will generate data in CMOS level using the on-board clock generated by the internal PLL, refer to as pDFS_CLK[0]/nDFS_CLK[0] that will be used by the FPGA.

3.4 HSDC extension module: FPGA flash

To get access to the software control of the generation system, run the 'USB Configurator.exe'. If a HSDC extension module is connected to the user system it will display the following window:

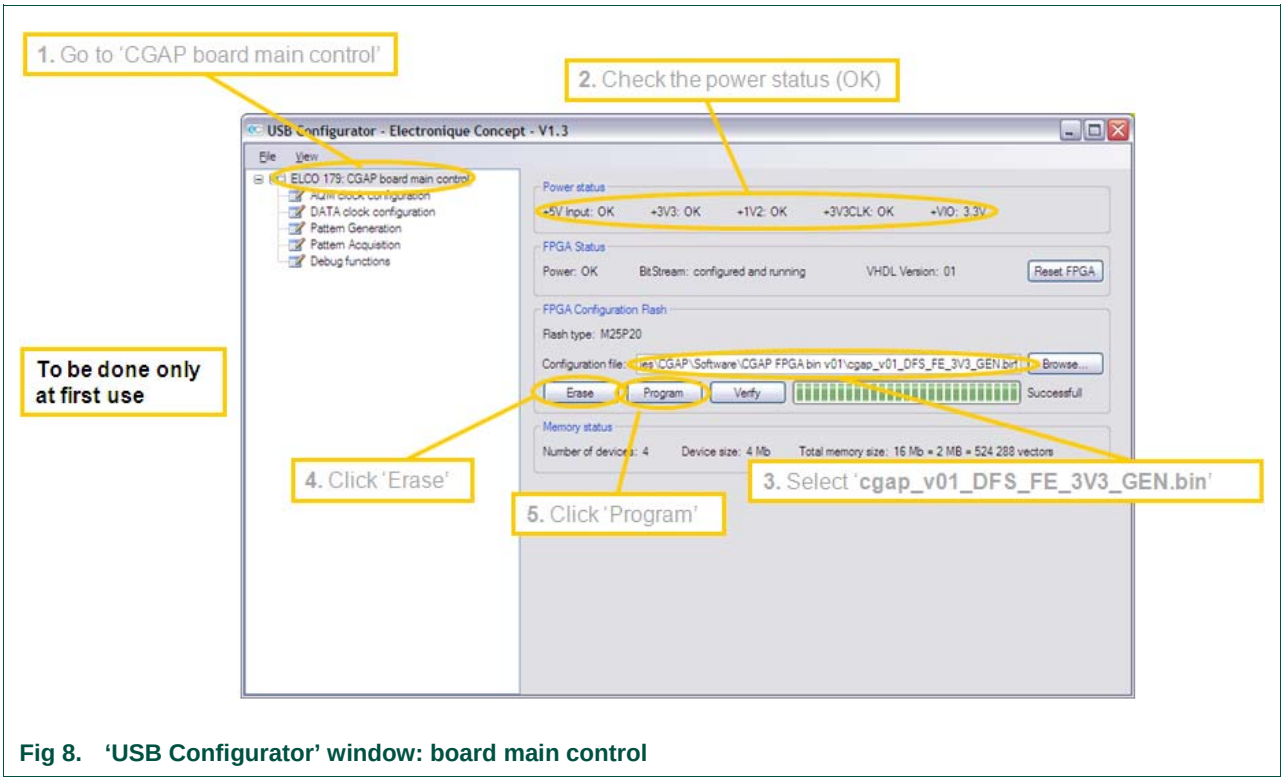


Fig 8. 'USB Configurator' window: board main control

This window gives an overview of the current status of the board connected. If supply is not connected, a FAIL status appears on the Power status field.

The user needs to flash the FPGA with the appropriate bin file. With 'cgap_v03_DFS_FE_3V3_GEN.bin', the FPGA will use the falling edge (RE for rising edge) of the clock delivered by the on-board DFS (Data Frequency Synthesizer) that refers to the embedded PLL, which is either LMK03000C or LMK03001C.

3.5 HSDC extension module: DATA clock configuration

To generate the digital input pattern on P1 connector (CMOS mode), the user needs to choose the wanted data and clock frequency. In our example, the frequency used for acquisition is 76.8MHz:

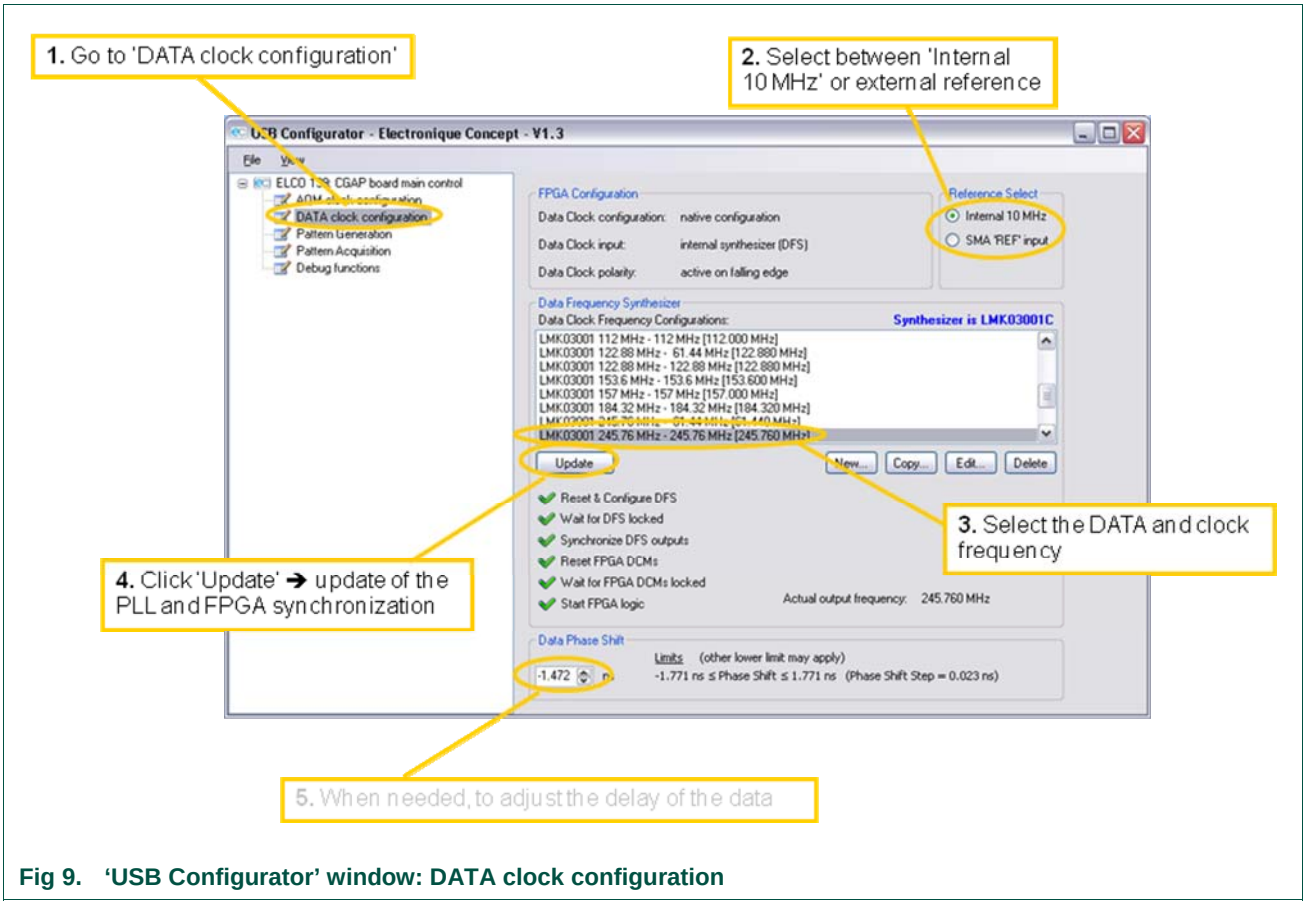


Fig 9. 'USB Configurator' window: DATA clock configuration

The FPGA configuration indicates which configuration file has been programmed in FPGA.

Depending on the wanted frequency, it leads to a certain range of the embedded PLL. The combination of the 2 proposed PLL allows the user as many frequencies as possible. Unfortunately, that requires to have 2 boards, one for each PLL.

On the CD, there are 2 configurations files that already defines frequencies for the DFS and AFS (AQM clock configuration that we don't use here). Copy these files to the directory "C:\Documents and Settings\All Users\Application Data\Electronique Concept\UsbConfig" to get access to these frequencies.

In the example, we use the PLL LMK03001. When selecting the file 'LMK03001 245.76 MHz – 245.76 MHz', both data and clock frequencies are set to 245.76 MHz. The pattern will be generated at data clock frequency and the clock provided on connectors DATA (CMOS) and DATA+/DATA- (LVDS) will provided at clock frequency. Pin DATA can go only up to 250 MHz.

If one or several red cross appear, check that the reference is available (if external) or that the setting fits with the PLL.

Note: you can edit the LMK file by clicking on the "Edit…" button to define your own frequency, as long as you respect the frequency range defined by the PLL.

3.6 HSDC extension module: pattern generation

The clock frequency is defined, and the board is ready to generate the pattern:

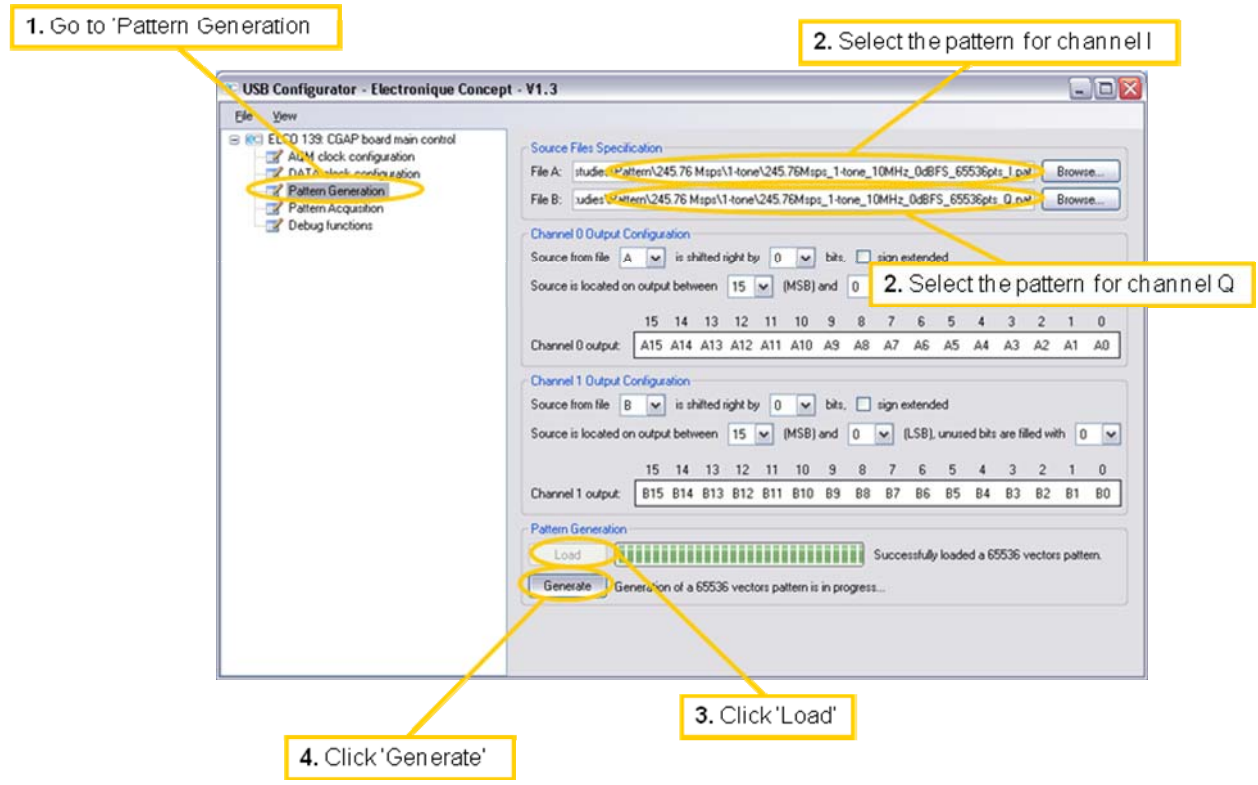


Fig 10. 'USB Configurator' window: pattern generation

4. Example

The figure 11 shows an overview of the extension module HSDC-EXTMOD01/DB generation board with DAC1405D750 demoboard.

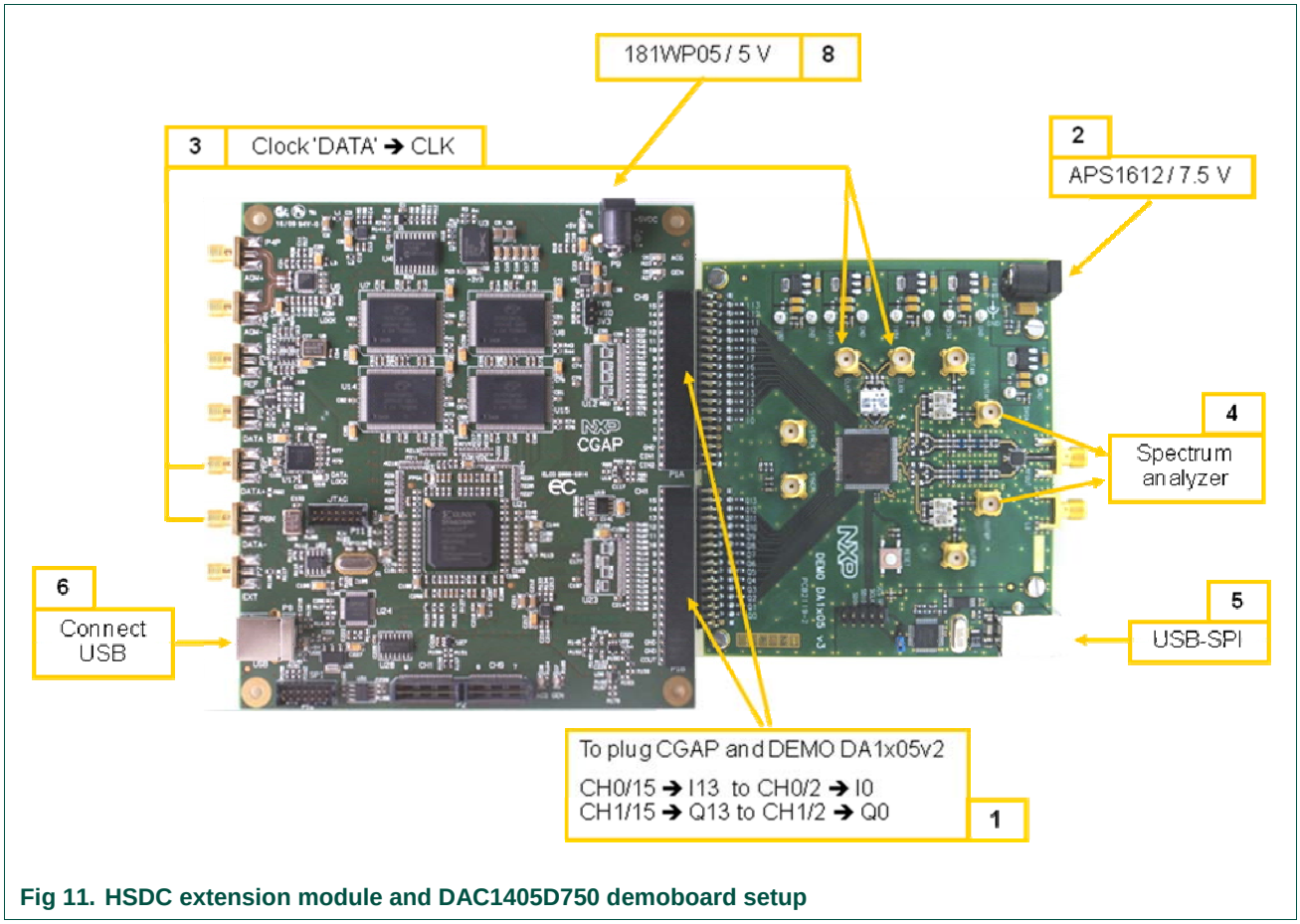


Fig 11. HSDC extension module and DAC1405D750 demoboard setup