SPI Serial EEPROMs
8K (1024 x 8)
16K (2048 x 8)

AT25080B
AT25160B

Preliminary

Features

- Serial Peripheral Interface (SPI) Compatible
- Supports SPI Modes 0 (0,0) and 3 (1,1)
  - Datasheet Describes Mode 0 Operation
- Low-voltage and Standard-voltage Operation
  - 1.8 (V_{CC} = 1.8V to 5.5V)
- 20 MHz Clock Rate (5V)
- 32-byte Page Mode
- Block Write Protection
  - Protect 1/4, 1/2, or Entire Array
- Write Protect ($\overline{\text{WP}}$) Pin and Write Disable Instructions for Both Hardware and Software Data Protection
- Self-timed Write Cycle (5 ms max)
- High Reliability
  - Endurance: One Million Write Cycles
  - Data Retention: 100 Years
- 8-lead JEDEC PDIP, 8-lead JEDEC SOIC, 8-lead Ultra Thin Mini-MAP (MLP 2x3), 8-lead TSSOP and 8-ball dBGA2 Packages
- Die Sales: Wafer Form, Tape and Reel, and Bumped Wafers

Description

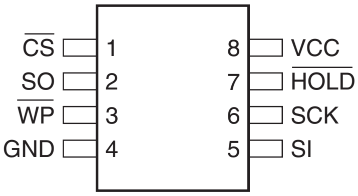
The AT25080B/160B provides 8192/16384 bits of serial electrically-erasable programmable read-only memory (EEPROM) organized as 1024/2048 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The AT25080B/160B is available in space-saving 8-lead PDIP, 8-lead JEDEC SOIC, 8-lead Ultra Thin Mini-MAP (MLP 2x3) and 8-lead TSSOP packages.

The AT25080B/160B is enabled through the Chip Select pin ($\overline{\text{CS}}$) and accessed via a three-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). All programming cycles are completely self-timed, and no separate erase cycle is required before write.

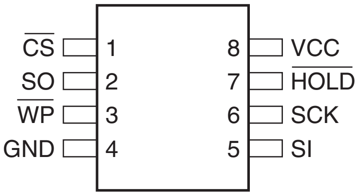
Table 0-1. Pin Configuration

Pin Name	Function
$\overline{\text{CS}}$	Chip Select
SCK	Serial Data Clock
SI	Serial Data Input
SO	Serial Data Output
GND	Ground
VCC	Power Supply
$\overline{\text{WP}}$	Write Protect
$\overline{\text{HOLD}}$	Suspends Serial Input

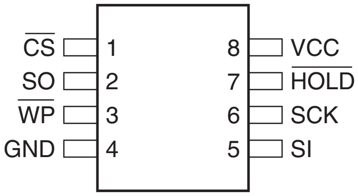
8-lead PDIP



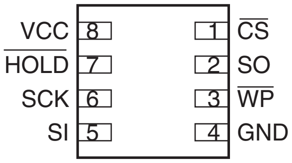
8-lead TSSOP



8-lead SOIC

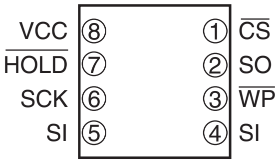


8-lead Ultra Thin Mini-MAP (MLP 2x3)



Bottom View

8-ball dBGA2



Bottom View

Block write protection is enabled by programming the status register with one of four blocks of write protection. Separate program enable and program disable instructions are provided for additional data protection. Hardware data protection is provided via the $\overline{\text{WP}}$ pin to protect against inadvertent write attempts to the status register. The $\overline{\text{HOLD}}$ pin may be used to suspend any serial communication without resetting the serial sequence.

Absolute Maximum Ratings*

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 0-1. Block Diagram

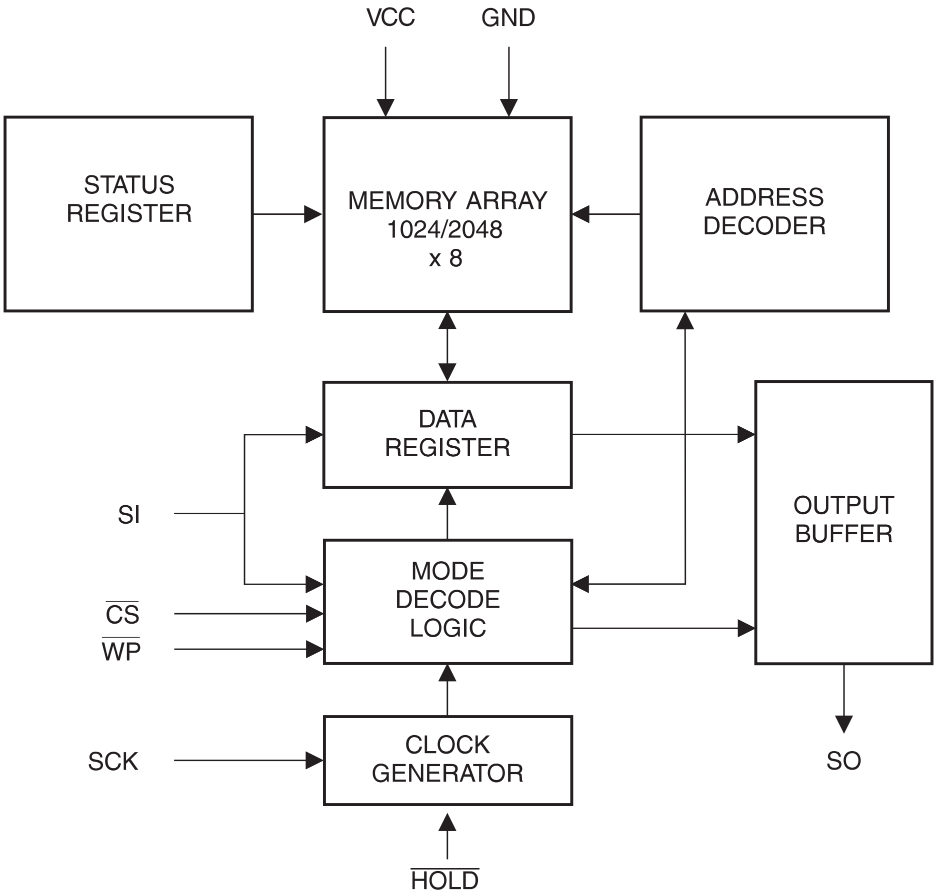


Table 0-2. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0V (unless otherwise noted)

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

Table 0-3. DC Characteristics

Applicable over recommended operating range from: T_{AI} = –40°C to +85°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC1}	Supply Voltage		1.8		5.5	V
V_{CC2}	Supply Voltage		2.7		5.5	V
V_{CC3}	Supply Voltage		4.5		5.5	V
I_{CC1}	Supply Current	V_{CC} = 5.0V at 20 MHz, SO = Open, Read		7.5	10.0	mA
I_{CC2}	Supply Current	V_{CC} = 5.0V at 20 MHz, SO = Open, Read, Write		4.0	10.0	mA

Applicable over recommended operating range from: T_{AI} = –40°C to +85°C, V_{CC} = +1.8V to +5.5V (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
I_{CC3}	Supply Current	V_{CC} = 5.0V at 5 MHz, SO = Open, Read, Write			4.0	6.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.8V, $\overline{CS}$ = V_{CC}			< 0.1	6.0(2)	µA
I_{SB2}	Standby Current	V_{CC} = 2.7V, $\overline{CS}$ = V_{CC}			0.3	7.0(2)	µA
I_{SB3}	Standby Current	V_{CC} = 5.0V, $\overline{CS}$ = V_{CC}			2.0	10.0(2)	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}		–3.0		3.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}, T_{AC} = 0°C to 70°C		–3.0		3.0	µA
V_{IL}(1)	Input Low-voltage			–0.6		V_{CC} x 0.3	V
V_{IH}(1)	Input High-voltage			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL1}	Output Low-voltage	$4.5V \leq V_{CC} \leq 5.5V$	I_{OL} = 3.0 mA			0.4	V
V_{OH1}	Output High-voltage		I_{OH} = –1.6 mA	V_{CC} - 0.8			V
V_{OL2}	Output Low-voltage	$1.8V \leq V_{CC} \leq 3.6V$	I_{OL} = 0.15 mA			0.2	V
V_{OH2}	Output High-voltage		I_{OH} = –100 µA	V_{CC} - 0.2			V

Notes:
1. V_{IL} min and V_{IH} max are reference only and are not tested.
2. Worst case measured at 85°C

Table 0-4. AC Characteristics
Applicable over recommended operating range from T_{AI} = –40°C to +85°C, V_{CC} = As Specified, CL = 1 TTL Gate and 30 pF (unless otherwise noted)

Symbol	Parameter	Voltage	Min	Max	Units
f_{SCK}	SCK Clock Frequency	4.5–5.5 2.7–5.5 1.8–5.5	0 0 0	20 10 5	MHz
t_{RI}	Input Rise Time	4.5–5.5 2.7–5.5 1.8–5.5		2 2 2	µs
t_{FI}	Input Fall Time	4.5–5.5 2.7–5.5 1.8–5.5		2 2 2	µs
t_{WH}	SCK High Time	4.5–5.5 2.7–5.5 1.8–5.5	20 40 80		ns
t_{WL}	SCK Low Time	4.5–5.5 2.7–5.5 1.8–5.5	20 40 80		ns
t_{CS}	$\overline{\text{CS}}$ High Time	4.5–5.5 2.7–5.5 1.8–5.5	25 50 100		ns
t_{CSS}	$\overline{\text{CS}}$ Setup Time	4.5–5.5 2.7–5.5 1.8–5.5	25 50 100		ns
t_{CSH}	$\overline{\text{CS}}$ Hold Time	4.5–5.5 2.7–5.5 1.8–5.5	25 50 100		ns
t_{SU}	Data In Setup Time	4.5–5.5 2.7–5.5 1.8–5.5	5 10 20		ns
t_H	Data In Hold Time	4.5–5.5 2.7–5.5 1.8–5.5	5 10 20		ns
t_{HD}	$\overline{\text{HOLD}}$ Setup Time	4.5–5.5 2.7–5.5 1.8–5.5	5 10 20		
t_{CD}	$\overline{\text{HOLD}}$ Hold Time	4.5–5.5 2.7–5.5 1.8–5.5	5 10 20		ns
t_V	Output Valid	4.5–5.5 2.7–5.5 1.8–5.5	0 0 0	20 40 80	ns
t_{HO}	Output Hold Time	4.5–5.5 2.7–5.5 1.8–5.5	0 0 0		ns

Table 0-4. AC Characteristics (Continued)

Applicable over recommended operating range from T_{AI} = –40°C to +85°C, V_{CC} = As Specified, CL = 1 TTL Gate and 30 pF (unless otherwise noted)

Symbol	Parameter	Voltage	Min	Max	Units
t_{LZ}	$\overline{\text{HOLD}}$ to Output Low Z	4.5–5.5 2.7–5.5 1.8–5.5	0 0 0	25 50 100	ns
t_{HZ}	$\overline{\text{HOLD}}$ to Output High Z	4.5–5.5 2.7–5.5 1.8–5.5		40 80 200	ns
t_{DIS}	Output Disable Time	4.5–5.5 2.7–5.5 1.8–5.5		40 80 200	ns
t_{WC}	Write Cycle Time	4.5–5.5 2.7–5.5 1.8–5.5		5 5 5	ms
Endurance(1)	3.3V, 25°C, Page Mode		1M		Write Cycles

Note: 1. This parameter is characterized and is not 100% tested.

1. Serial Interface Description

MASTER: The device that generates the serial clock.

SLAVE: Because the Serial Clock pin (SCK) is always an input, the AT25080B/160B always operates as a slave.

TRANSMITTER/RECEIVER: The AT25080B/160B has separate pins designated for data transmission (SO) and reception (SI).

MSB: The Most Significant Bit (MSB) is the first bit transmitted and received.

SERIAL OP-CODE: After the device is selected with $\overline{\text{CS}}$ going low, the first byte will be received. This byte contains the op-code that defines the operations to be performed.

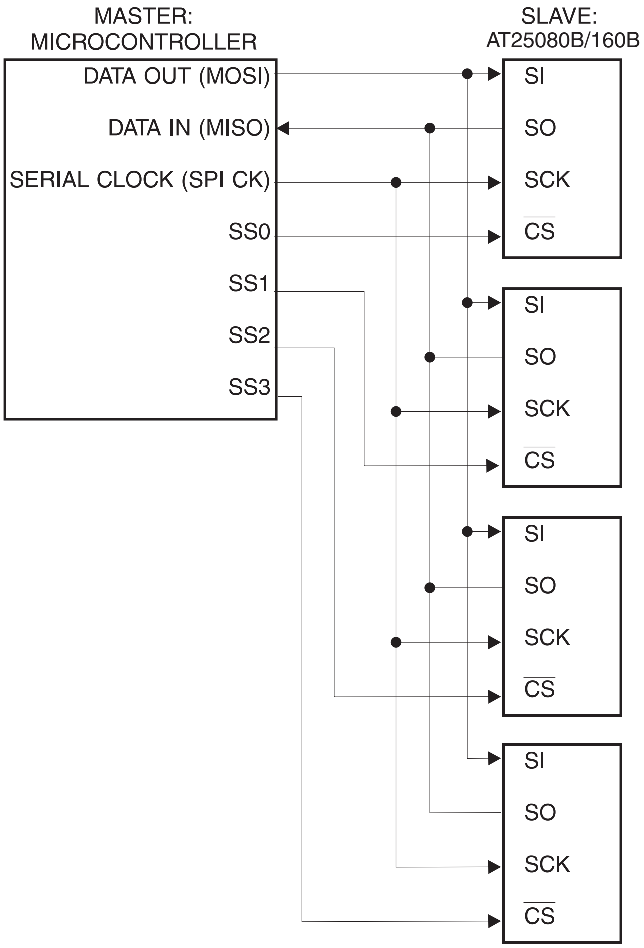
INVALID OP-CODE: If an invalid op-code is received, no data will be shifted into the AT25080B/160B, and the serial output pin (SO) will remain in a high impedance state until the falling edge of $\overline{\text{CS}}$ is detected again. This will reinitialize the serial communication.

CHIP SELECT: The AT25080B/160B is selected when the $\overline{\text{CS}}$ pin is low. When the device is not selected, data will not be accepted via the SI pin, and the serial output pin (SO) will remain in a high impedance state.

HOLD: The $\overline{\text{HOLD}}$ pin is used in conjunction with the $\overline{\text{CS}}$ pin to select the AT25080B/160B. When the device is selected and a serial sequence is underway, $\overline{\text{HOLD}}$ can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the $\overline{\text{HOLD}}$ pin must be brought low while the SCK pin is low. To resume serial communication, the $\overline{\text{HOLD}}$ pin is brought high while the SCK pin is low (SCK may still toggle during $\overline{\text{HOLD}}$). Inputs to the SI pin will be ignored while the SO pin is in the high impedance state.

WRITE PROTECT: The write protect pin ($\overline{\text{WP}}$) will allow normal read/write operations when held high. When the $\overline{\text{WP}}$ pin is brought low and WPEN bit is "1", all write operations to the status register are inhibited. $\overline{\text{WP}}$ going low while $\overline{\text{CS}}$ is still low will interrupt a write to the status register. If the internal write cycle has already been initiated, $\overline{\text{WP}}$ going low will have no effect on any write operation to the status register. The $\overline{WP}$ pin function is blocked when the WPEN bit in the status register is “0”. This will allow the user to install the AT25080B/160B in a system with the $\overline{WP}$ pin tied to ground and still be able to write to the status register. All $\overline{WP}$ pin functions are enabled when the WPEN bit is set to “1”.

Figure 1-1. SPI Serial Interface



2. Functional Description

The AT25080B/160B is designed to interface directly with the synchronous serial peripheral interface (SPI) of the 6805 and 68HC11 series of microcontrollers.

The AT25080B/160B utilizes an 8-bit instruction register. The list of instructions and their operation codes are contained in Table 2-1. All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low CS transition.

Table 2-1. Instruction Set for the AT25080B/160B

Instruction Name	Instruction Format	Operation
WREN	0000 X110	Set Write Enable Latch
WRDI	0000 X100	Reset Write Enable Latch
RDSR	0000 X101	Read Status Register

Table 2-1. Instruction Set for the AT25080B/160B

Instruction Name	Instruction Format	Operation
WRSR	0000 X001	Write Status Register
READ	0000 X011	Read Data from Memory Array
WRITE	0000 X010	Write Data to Memory Array

WRITE ENABLE (WREN): The device will power up in the write disable state when V_{CC} is applied. All programming instructions must therefore be preceded by a Write Enable instruction.

WRITE DISABLE (WRDI): To protect the device against inadvertent writes, the Write Disable instruction disables all programming modes. The WRDI instruction is independent of the status of the $\overline{\text{WP}}$ pin.

READ STATUS REGISTER (RDSR): The Read Status Register instruction provides access to the status register. The READY/BUSY and Write Enable status of the device can be determined by the RDSR instruction. Similarly, the Block Write Protection Bits indicate the extent of protection employed. These bits are set by using the WRSR instruction.

Table 2-2. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN	X	X	X	BP1	BP0	WEN	$\overline{\text{RDY}}$

Table 2-3. Read Status Register Bit Definition

Bit	Definition
Bit 0 ($\overline{\text{RDY}}$)	Bit 0 = “0” ($\overline{\text{RDY}}$) indicates the device is READY. Bit 0 = “1” indicates the write cycle is in progress.
Bit 1 (WEN)	Bit 1= “0” indicates the device is not WRITE ENABLED. Bit 1 = “1” indicates the device is write enabled.
Bit 2 (BP0)	See Table 2-4 on page 9.
Bit 3 (BP1)	See Table 2-4 on page 9.
Bits 4–6 are “0”s when device is not in an internal write cycle.	
Bit 7 (WPEN)	See Table 2-5 on page 9.
Bits 0–7 are “1”s during an internal write cycle.	

WRITE STATUS REGISTER (WRSR): The WRSR instruction allows the user to select one of four levels of protection. The AT25080B/160B is divided into four array segments. One-quarter, one-half, or all of the memory segments can be protected. Any of the data within any selected segment will therefore be read only. The block write protection levels and corresponding status register control bits are shown in Table 2-4.

The three bits BP0, BP1, and WPEN are nonvolatile cells that have the same properties and functions as the regular memory cells (e.g., WREN, t_{WC}, RDSR).

Table 2-4. Block Write Protect Bits

Level	Status Register Bits		Array Addresses Protected	
	BP1	BP0	AT25080B	AT25160B
0	0	0	None	None
1(1/4)	0	1	0300–03FF	0600–07FF
2(1/2)	1	0	0200–03FF	0400–07FF
3(All)	1	1	0000–03FF	0000–07FF

The WRSR instruction also allows the user to enable or disable the write protect ($\overline{\text{WP}}$) pin through the use of the Write Protect Enable (WPEN) bit. Hardware write protection is enabled when the $\overline{\text{WP}}$ pin is low and the WPEN bit is “1”. Hardware write protection is disabled when either the $\overline{\text{WP}}$ pin is high or the WPEN bit is “0”. When the device is hardware write protected, writes to the status register, including the block protect bits and the WPEN bit, and the block-protected sections in the memory array are disabled. Writes are only allowed to sections of the memory that are not block-protected.

NOTE: When the WPEN bit is hardware write protected, it cannot be changed back to “0” as long as the $\overline{\text{WP}}$ pin is held low.

Table 2-5. WPEN Operation

WPEN	$\overline{\text{WP}}$	WEN	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writeable	Writeable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writeable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writeable	Writeable

READ SEQUENCE (READ): Reading the AT25080B/160B via the Serial Output (SO) pin requires the following sequence. After the $\overline{\text{CS}}$ line is pulled low to select a device, the read op-code is transmitted via the SI line followed by the byte address to be read (A15–A0, see Table 2-6). Upon completion, any data on the SI line will be ignored. The data (D7–D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the $\overline{\text{CS}}$ line should be driven high after the data comes out. The read sequence can be continued since the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached, the address counter will roll over to the lowest address allowing the entire memory to be read in one continuous read cycle.

WRITE SEQUENCE (WRITE): In order to program the AT25080B/160B, two separate instructions must be executed. First, the device ***must be write enabled*** via the WREN instruction. Then a write (WRITE) instruction may be executed. Also, the address of the memory location(s) to be programmed must be outside the protected address field location selected by the block write protection level. During an internal write cycle, all commands will be ignored except the RDSR instruction.

A write instruction requires the following sequence. After the $\overline{CS}$ line is pulled low to select the device, the WRITE op-code is transmitted via the SI line followed by the byte address (A15–A0) and the data (D7–D0) to be programmed (see Table 2-6). Programming will start after the $\overline{CS}$ pin is brought high. The low-to-high transition of the $\overline{CS}$ pin must occur during the SCK low-time immediately after clocking in the D0 (LSB) data bit.

The READY/BUSY status of the device can be determined by initiating a read status register (RDSR) instruction. If Bit 0 = “1”, the write cycle is still in progress. If Bit 0 = “0”, the write cycle has ended. Only the RDSR instruction is enabled during the write programming cycle.

The AT25080B/160B is capable of a 32-byte page write operation. After each byte of data is received, the five low-order address bits are internally incremented by one; the high-order bits of the address will remain constant. If more than 32 bytes of data are transmitted, the address counter will roll over and the previously written data will be overwritten. The AT25080B/160B is automatically returned to the write disable state at the completion of a write cycle.

NOTE: If the device is not write-enabled (WREN), the device will ignore the write instruction and will return to the standby state, when $\overline{CS}$ is brought high. A new $\overline{CS}$ falling edge is required to reinitiate the serial communication.

Table 2-6. Address Key

Address	AT25080B	AT25160B
A_N	$A_9–A_0$	$A_{10}–A_0$
Don’t Care Bits	$A_{15}–A_{10}$	$A_{15}–A_{11}$

3. Timing Diagrams

Figure 3-1. Synchronous Data Timing (for Mode 0)

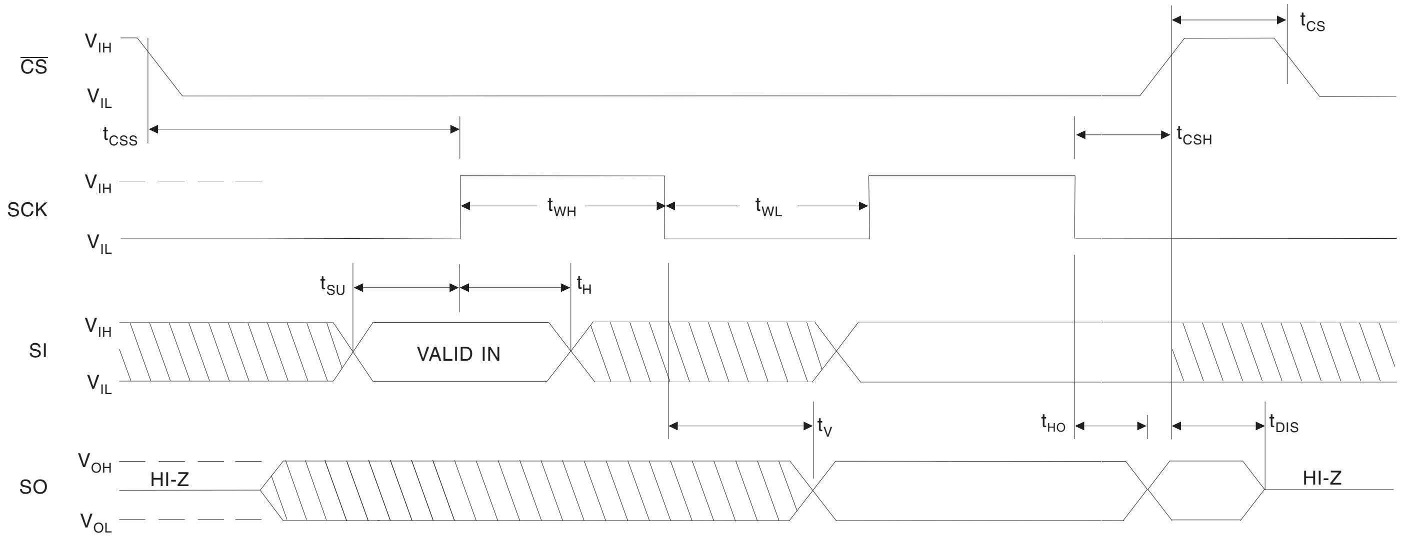


Figure 3-2. WREN Timing

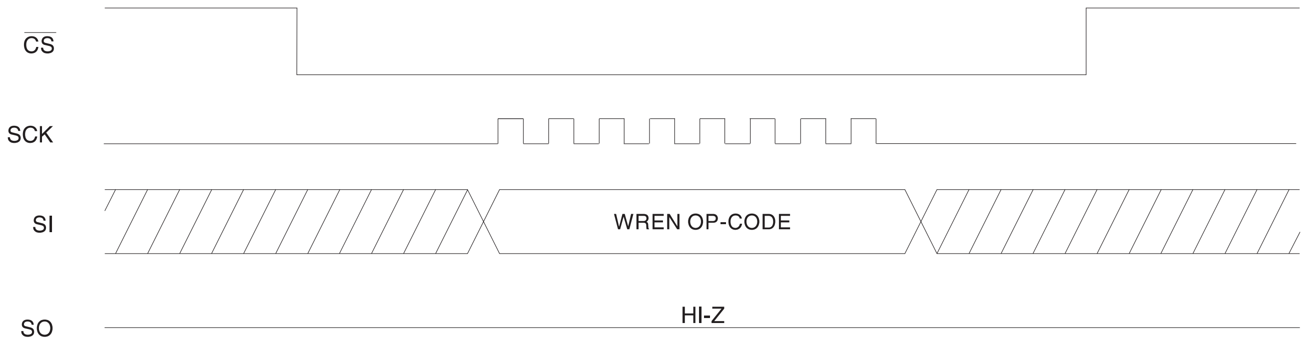


Figure 3-3. WRDI Timing

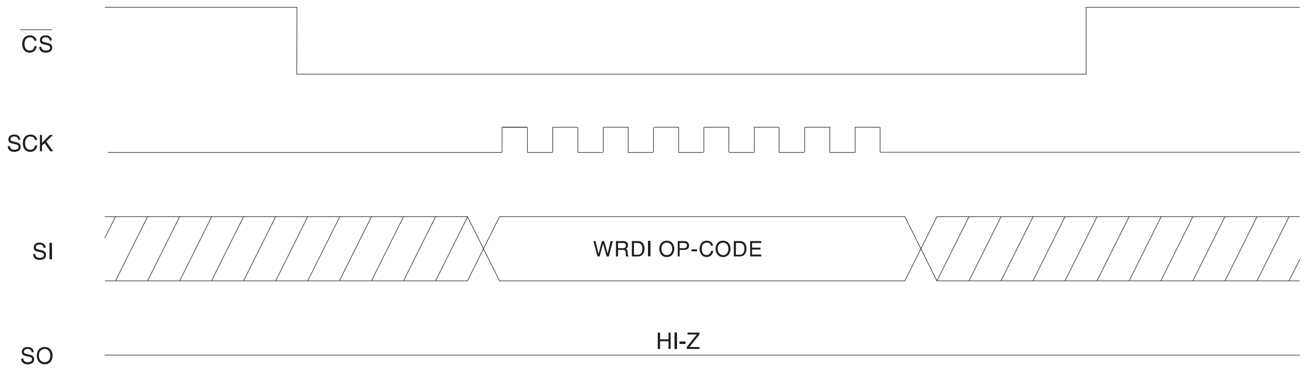


Figure 3-4. RDSR Timing

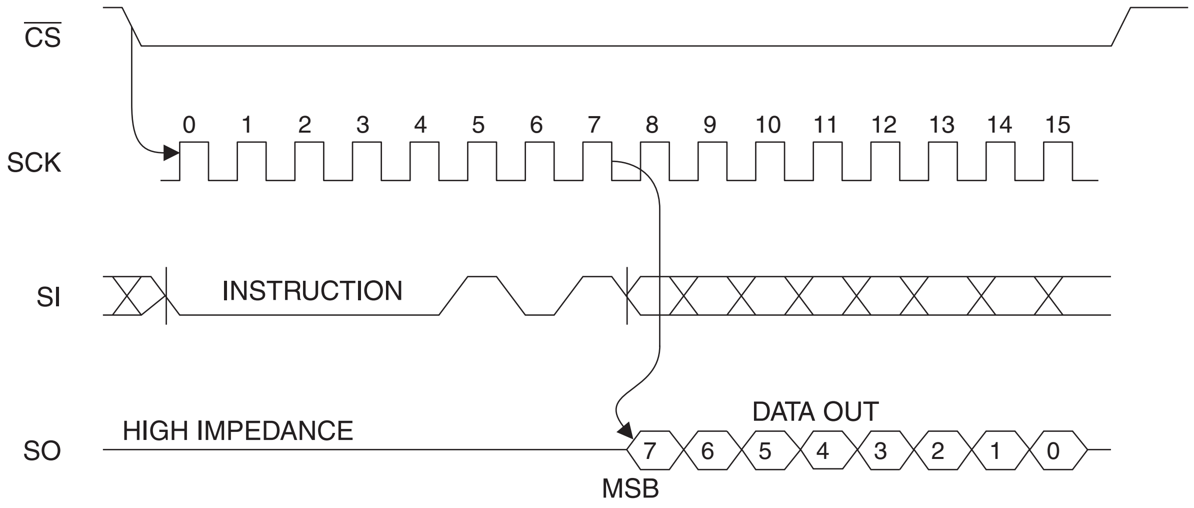


Figure 3-5. WRSR Timing

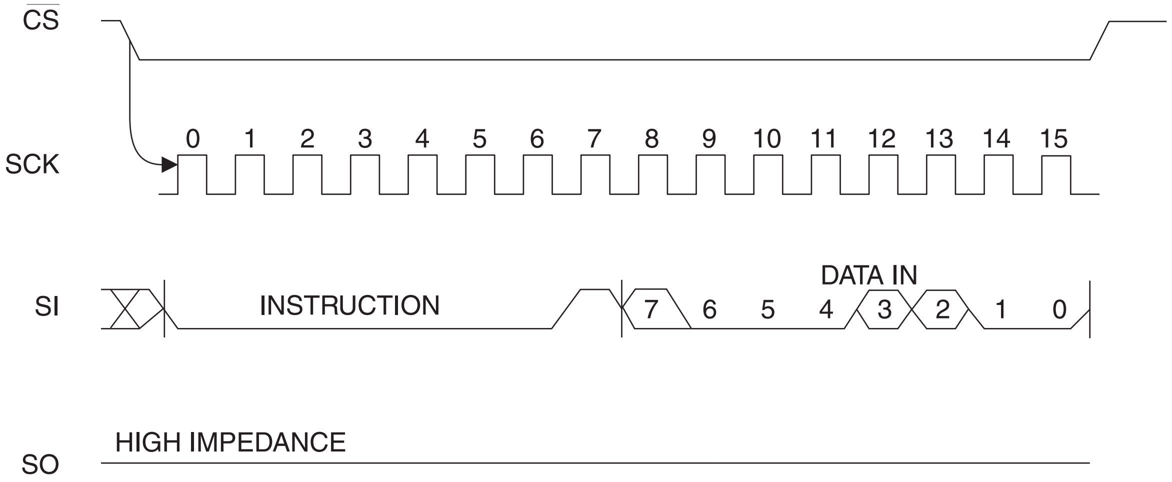


Figure 3-6. READ Timing

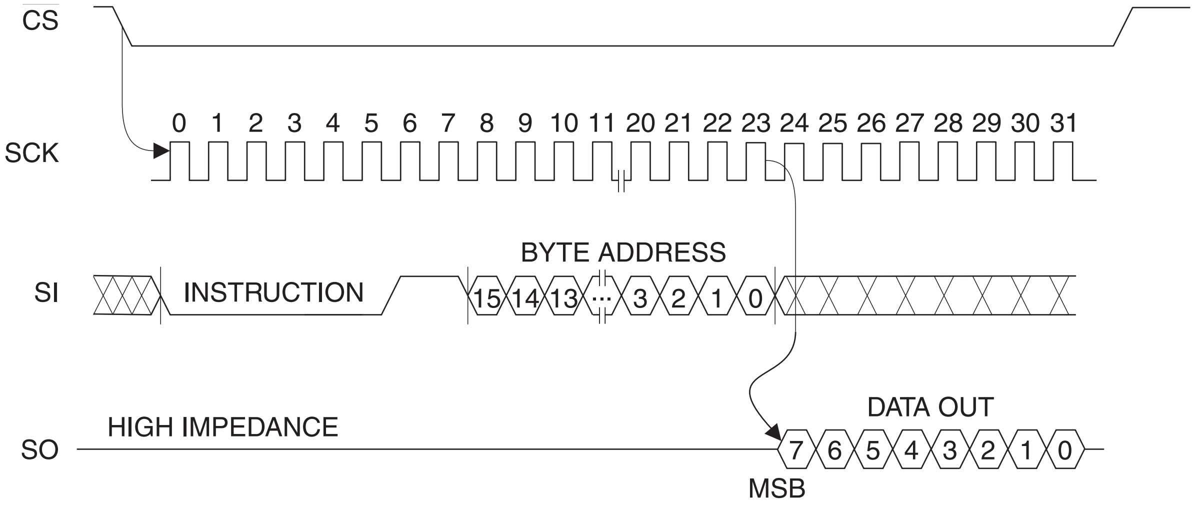


Figure 3-7. WRITE Timing

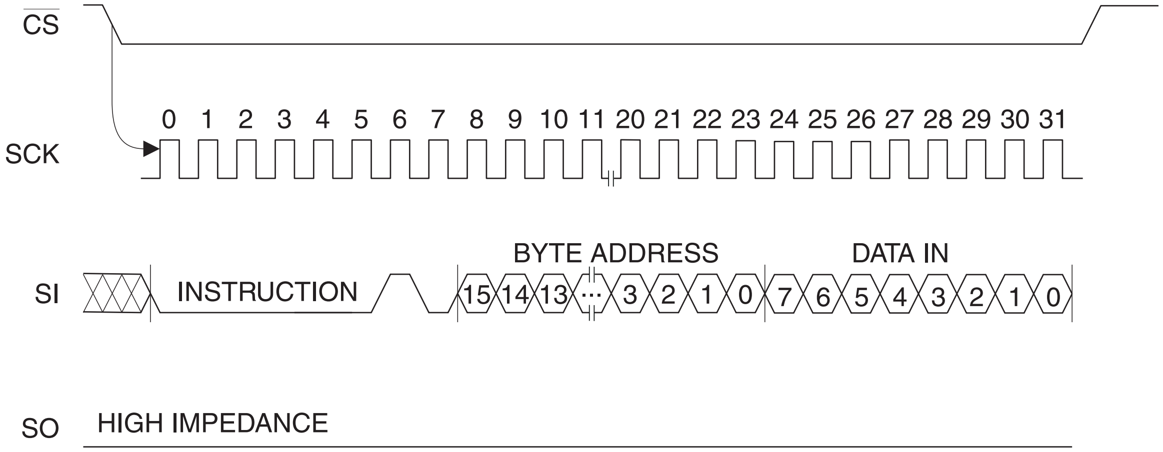
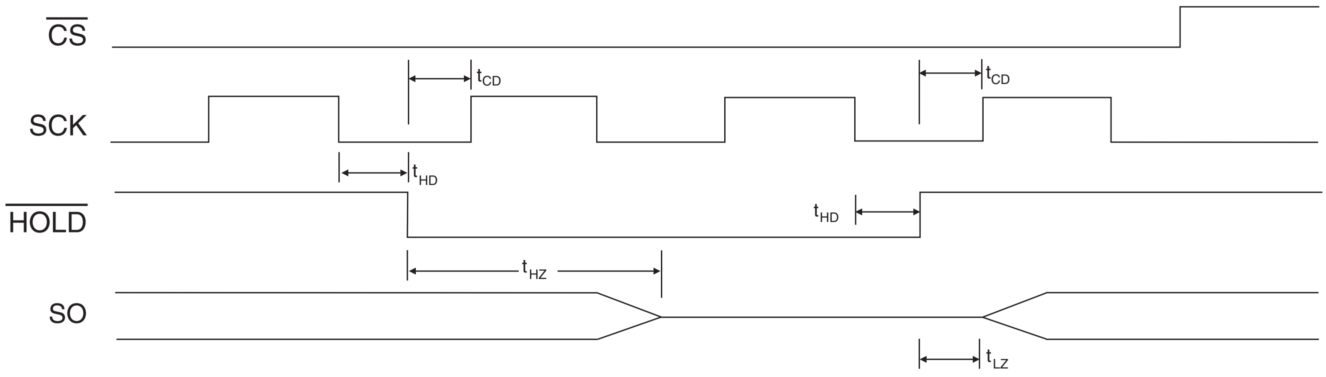


Figure 3-8. $\overline{\text{HOLD}}$ Timing



4. AT25080B Ordering Information

Ordering Code	Voltage	Package	Operation Range
AT25080B-PU (Bulk form only)	1.8	8P3	Lead-free/Halogen-free/ Industrial Temperature (–40 to 85°C)
AT25080BN-SH-B[(1)] (NiPdAu Lead Finish)	1.8	8S1	
AT25080BN-SH-T[(2)] (NiPdAu Lead Finish)	1.8	8S1	
AT25080B-TH-B[(1)] (NiPdAu Lead Finish)	1.8	8A2	
AT25080B-TH-T[(2)] (NiPdAu Lead Finish)	1.8	8A2	
AT25080BY6-YH-T[(2)] (NiPdAu Lead Finish)	1.8	8Y6	
AT25080BD3-DH-T[(2)]	1.8	8D3	
AT25080BU3-UU-T[(2)]	1.8	8U3-1	
AT25080B-W-11[(3)]	1.8	Die Sale	Industrial Temperature (–40 to 85°C)

Notes:
1. "B" denotes bulk.
2. "-T" deontes tape and reel. SOIC = 4K per reel. TSSOP, Ultra Thin Mini-MAP, SOT23, and dBGA2 = 5K per reel.
3. Available in waffle pack, tape and reel, and wafer form; order as SL788 for inkless wafer form. Bumped die available upon request. Please contact Serial Interface Marketing.

Package Type	
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8A2	8-lead, 4.4 mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)
8Y6	8-lead, 2.00 mm x 3.00 mm Body, 0.50 mm Pitch, Ultra Thin Mini-MAP, Dual No Lead Package (DFN), (MLP 2x3 mm)
8D3	8-lead, 1.8 mm x 2.2 mm Body, Ultra axLanda Grid Array (ULLGA)
8U3-1	8-ball, die Ball Grid Array Package (dBGA2)
Options	
–1.8	Low Voltage (1.8 to 5.5V)

5. AT25160B Ordering Information

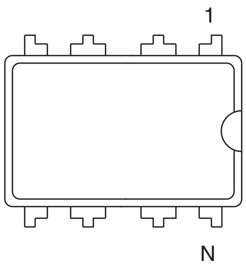
Ordering Code	Voltage	Package	Operation Range
AT25160B-PU (Bulk form only)	1.8	8P3	Lead-free/Halogen-free/ Industrial Temperature (–40 to 85°C)
AT25160BN-SH-B[(1)] (NiPdAu Lead Finish)	1.8	8S1	
AT25160BN-SH-T[(2)] (NiPdAu Lead Finish)	1.8	8S1	
AT25160B-TH-B[(1)] (NiPdAu Lead Finish)	1.8	8A2	
AT25160B-TH-T[(2)] (NiPdAu Lead Finish)	1.8	8A2	
AT25160BY6-YH-T[(2)] (NiPdAu Lead Finish)	1.8	8Y6	
AT25160BD3-DH-T[(2)]	1.8	8D3	
AT25160BU3-UU-T[(2)]	1.8	8U3-1	
AT25160B-W-11[(3)]	1.8	Die Sale	Industrial Temperature (–40 to 85°C)

Notes:
1. "B" denotes bulk.
2. "-T" deontes tape and reel. SOIC = 4K per reel. TSSOP, Ultra Thin Mini-MAP, SOT23, and dBGA2 = 5K per reel.
3. Available in tape and reel and wafer form; order as SL788 for inkless wafer form. Bumped die available upon request. Please contact Serial Interface Marketing.

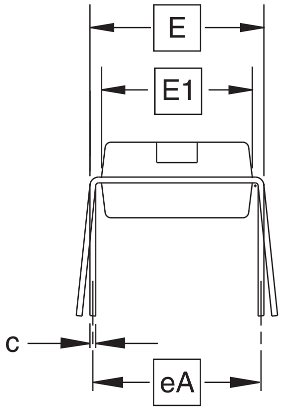
Package Type	
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8A2	8-lead, 4.4 mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)
8Y6	8-lead, 2.00 mm x 3.00 mm Body, 0.50 mm Pitch, Ultra Thin Mini-MAP, Dual No Lead Package (DFN), (MLP 2x3mm)
8D3	8-lead, 1.8 mm x 2.2 mm Body, Ultra axLanda Grid Array (ULLGA)
8U3-1	8-ball, die Ball Grid Array Package (dBGA2)
Options	
–1.8	Low Voltage (1.8 to 5.5V)

6. Packaging Information

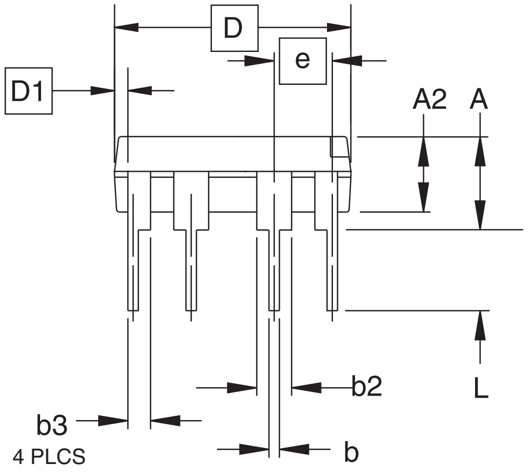
8P3 – PDIP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = inches)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	0.210	2
A2	0.115	0.130	0.195	
b	0.014	0.018	0.022	5
b2	0.045	0.060	0.070	6
b3	0.030	0.039	0.045	6
c	0.008	0.010	0.014	
D	0.355	0.365	0.400	3
D1	0.005	–	–	3
E	0.300	0.310	0.325	4
E1	0.240	0.250	0.280	3
e	0.100 BSC			
eA	0.300 BSC			4
L	0.115	0.130	0.150	2

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA, for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

01/09/02

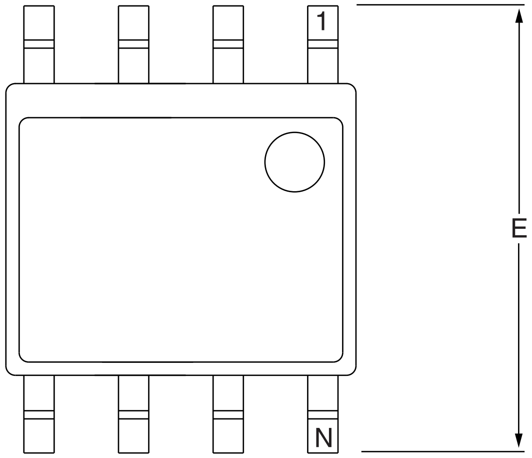
2325 Orchard Parkway
San Jose, CA 95131

TITLE
8P3, 8-lead, 0.300" Wide Body, Plastic Dual
In-line Package (PDIP)

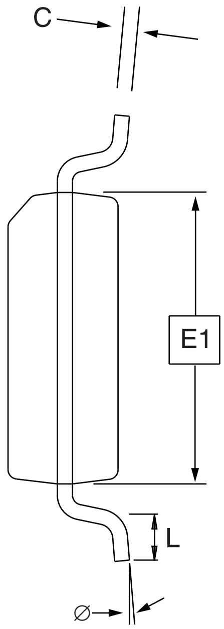
DRAWING NO.
8P3

REV.
B

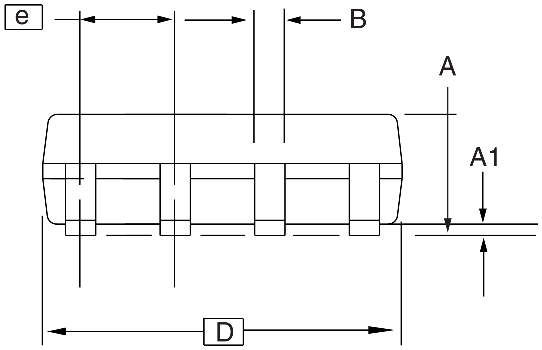
8S1 – JEDEC SOIC



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

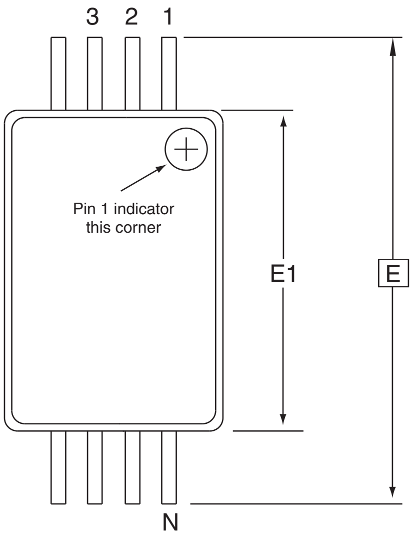
SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.00	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
∅	0°	–	8°	

Note: These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

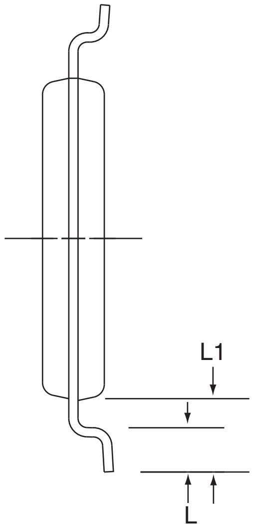
10/7/03

1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906	**TITLE** **8S1**, 8-lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**DRAWING NO.** 8S1	**REV.** B

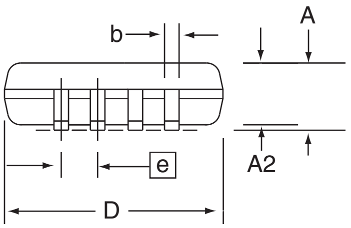
8A2 – TSSOP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

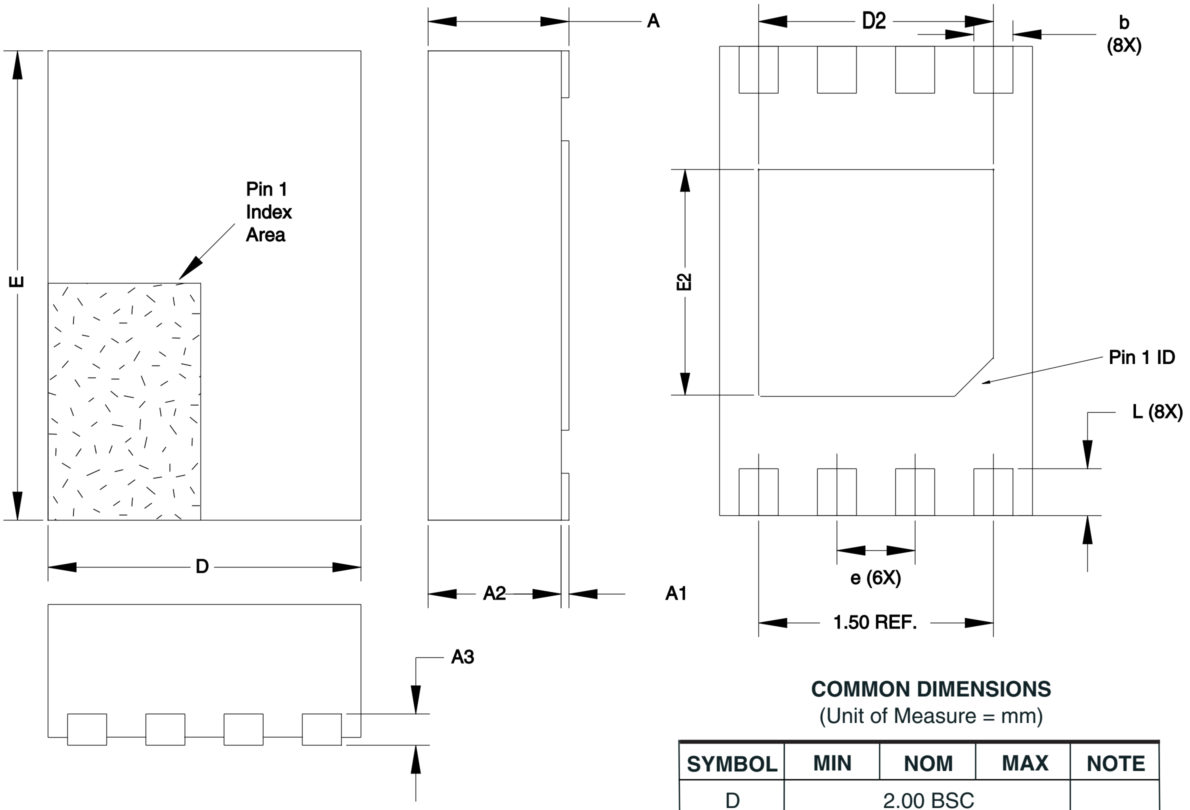
SYMBOL	MIN	NOM	MAX	NOTE
D	2.90	3.00	3.10	2, 5
E	6.40 BSC			
E1	4.30	4.40	4.50	3, 5
A	–	–	1.20	
A2	0.80	1.00	1.05	
b	0.19	–	0.30	4
e	0.65 BSC			
L	0.45	0.60	0.75	
L1	1.00 REF			

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm.
5. Dimension D and E1 to be determined at Datum Plane H.

5/30/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8A2**, 8-lead, 4.4 mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	8A2	B

8Y6 – Mini MAP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D		2.00 BSC		
E		3.00 BSC		
D2	1.40	1.50	1.60	
E2	-	-	1.40	
A	-	-	0.60	
A1	0.0	0.02	0.05	
A2	-	-	0.55	
A3		0.20 REF		
L	0.20	0.30	0.40	
e		0.50 BSC		
b	0.20	0.25	0.30	2

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-229, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.

8/26/05

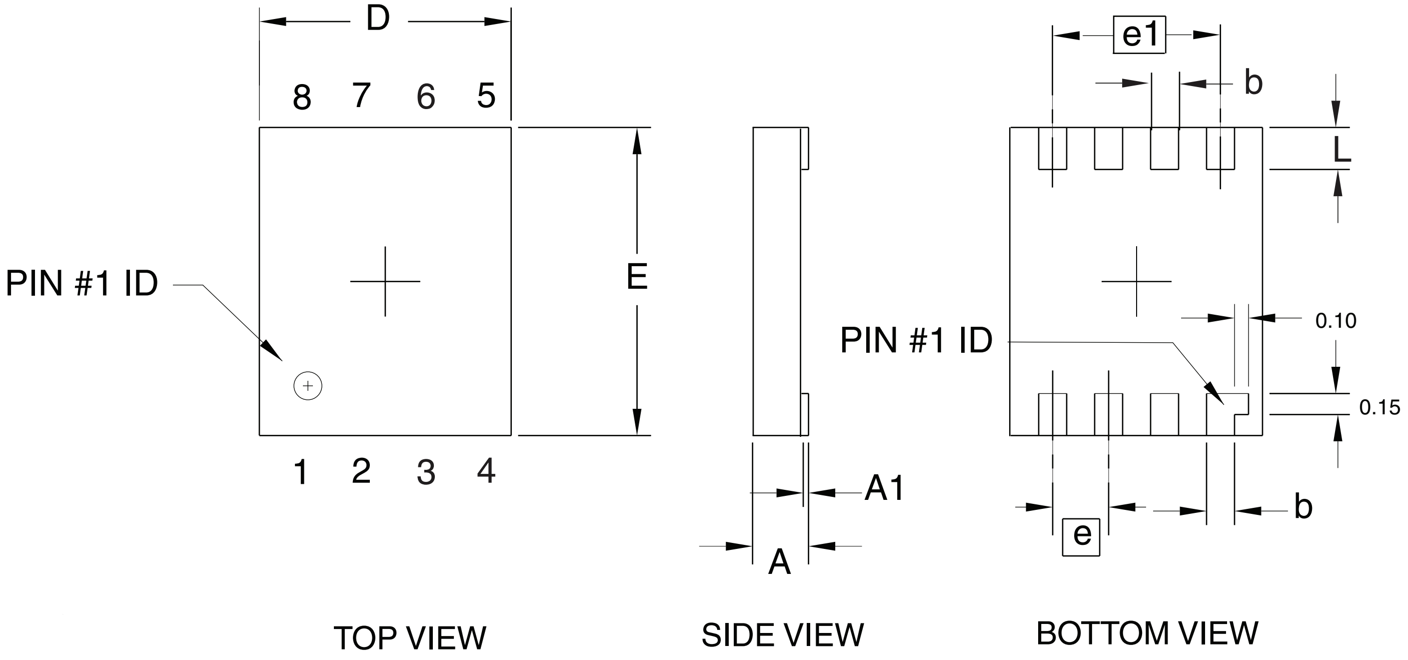
2325 Orchard Parkway
San Jose, CA 95131

TITLE
8Y6, 8-lead 2.0 x 3.0 mm Body, 0.50 mm Pitch, Utlra Thin Mini-Map, Dual No Lead Package (DFN) ,(MLP 2x3)

DRAWING NO. 8Y6

REV. C

8D3 - ULLGA



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	0.40	
A1	0.00	–	0.05	
D	1.70	1.80	1.90	
E	2.10	2.20	2.30	
b	0.15	0.20	0.25	
e		0.40 TYP		
e1		1.20 REF		
L	0.25	0.30	0.35	

11/15/05

	TITLE	DRAWING NO.	REV.
ATMEL 1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906	**8D3**, 8-lead (1.80 x 2.20 mm Body) Ultra Leadframe Land Grid Array (ULLGA) D3	8D3	0

7. Revision History

Lit No.	Date	Comments
5228B	7/2008	Changed ‘Endurance’ parameter on page 6
5228A	9/2007	Initial document release.