Features

- **Serial Peripheral Interface (SPI) Compatible**
- **Supports SPI Modes 0 (0,0) and 3 (1,1)**
- **Data Sheet Describes Mode 0 Operation**
- **Low-voltage and Standard-voltage Operation**
  - **1.8 (V_{cc} = 1.8V to 5.5V)**
- **20 MHz Clock Rate (5V)**
- **64-byte Page Mode and Byte Write Operation**
- **Block Write Protection**
  - **Protect 1/4, 1/2, or Entire Array**
- **Write Protect ($\overline{\text{WP}}$) Pin and Write Disable Instructions for Both Hardware and Software Data Protection**
- **Self-timed Write Cycle (5 ms Max)**
- **High-reliability**
  - **Endurance: 1 Million Write Cycles**
  - **Data Retention: >100 Years**
- **8-lead PDIP, 8-lead EIAJ SOIC, 8-lead JEDEC SOIC, 8-lead TSSOP, 8-ball dBGA2 and 8-lead Ultra Thin Mini MAP Packages**
- **Lead-free/Halogen-free**
- **Available in Automotive**
- **Die Sales: Wafer Form, Waffle Pack, and Bumped Die**

SPI Serial EEPROMS

128K (16,384 x 8)

256K (32,768 x 8)

AT25128B
AT25256B

Preliminary

Description

The AT25128B/256B provides 131,072/262,144 bits of serial electrically-erasable programmable read only memory (EEPROM) organized as 16,384/32,768 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The devices are available in space saving 8-lead PDIP, 8-lead EIAJ SOIC, 8-lead JEDEC SOIC, 8-lead TSSOP, 8-ball dBGA2 and 8-lead SAP packages. In addition, the entire family is available in 1.8V (1.8V to 5.5V).

The AT25128B/256B is enabled through the Chip Select pin ($\overline{\text{CS}}$) and accessed via a 3-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). All programming cycles are completely self-timed, and no separate Erase cycle is required before Write.

8593A–SEEPR–01/09

Figure 1. *Pin Configurations*

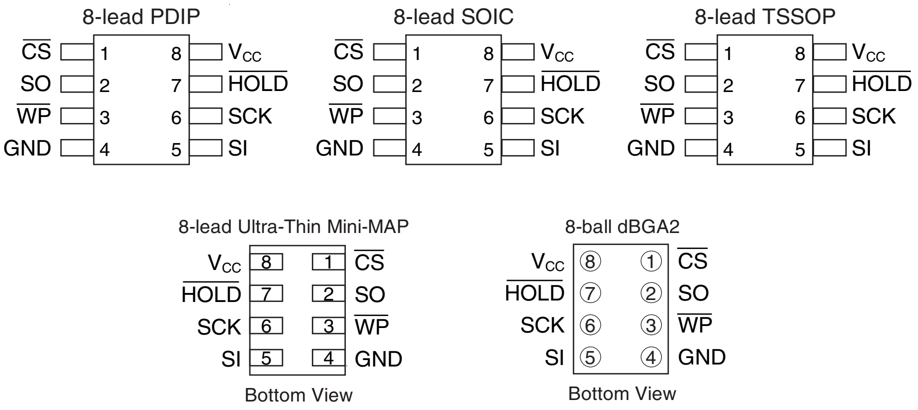


Table 1. *Pin Configurations*

Pin	Function
$\overline{\text{CS}}$	Chip Select
SCK	Serial Data Clock
SI	Serial Data Input
SO	Serial Data Output
GND	Ground
V_{cc}	Power Supply
$\overline{\text{WP}}$	Write Protect
$\overline{\text{HOLD}}$	Suspends Serial Input
NC	No Connect

Block Write protection is enabled by programming the status register with top ¼, top ½ or entire array of write protection. Separate Program Enable and Program Disable instructions are provided for additional data protection. Hardware data protection is provided via the $\overline{\text{WP}}$ pin to protect against inadvertent write attempts to the status register. The $\overline{\text{HOLD}}$ pin may be used to suspend any serial communication without resetting the serial sequence.

1. Absolute Maximum Ratings*

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to + 150°C
Voltage on Any Pin with Respect to Ground	–1.0 V +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 2. Block Diagram

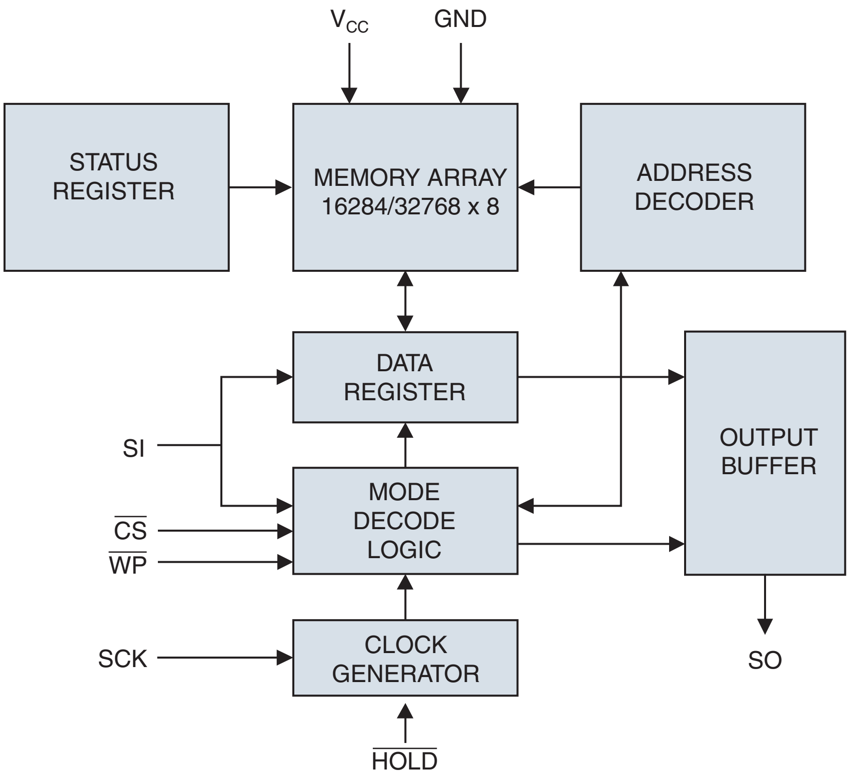


Table 2. Pin Capacitance [1]

Applicable over recommended operating range from $T_A = 25°C$, f = 1.0 MHz, $V_{CC} = +5.0V$ *(unless otherwise noted)*

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (SO)	8	pF	$V_{OUT} = 0V$
C_{IN}	Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	6	pF	$V_{IN} = 0V$

Note: 1. This parameter is characterized and is not 100% tested.

Table 3. DC Characteristics

Applicable over recommended operating range from $T_A = -40°C$ to +85°C, V_{CC} = +1.8V to +5.5V, V_{CC} = +1.8V to +5.5V(unless otherwise noted)

<table>
<tr><th>Symbol</th><th>Parameter</th><th colspan="2">Test Conditions</th><th>Min</th><th>Typ</th><th>Max</th><th>Units</th></tr>
<tr><td>V_{CC1}</td><td>Supply Voltage</td><td colspan="2"></td><td>1.8</td><td></td><td>5.5</td><td>V</td></tr>
<tr><td>V_{CC2}</td><td>Supply Voltage</td><td colspan="2"></td><td>2.5</td><td></td><td>5.5</td><td>V</td></tr>
<tr><td>V_{CC3}</td><td>Supply Voltage</td><td colspan="2"></td><td>4.5</td><td></td><td>5.5</td><td>V</td></tr>
<tr><td>I_{CC1}</td><td>Supply Current</td><td colspan="2">V_{CC} = 5.0V at 20 MHz, SO = Open, Read</td><td></td><td>9.0</td><td>10.0</td><td>mA</td></tr>
<tr><td>I_{CC2}</td><td>Supply Current</td><td colspan="2">V_{CC} = 5.0V at 10 MHz, SO = Open, Read, Write</td><td></td><td>5.0</td><td>7.0</td><td>mA</td></tr>
<tr><td>I_{CC3}</td><td>Supply Current</td><td colspan="2">V_{CC} = 5.0V at 1 MHz, SO = Open, Read, Write</td><td></td><td>2.2</td><td>3.5</td><td>mA</td></tr>
<tr><td>I_{SB1}</td><td>Standby Current</td><td colspan="2">V_{CC} = 1.8V, $\overline{CS} = V_{CC}$</td><td></td><td>0.2</td><td>3.0</td><td>µA</td></tr>
<tr><td>I_{SB2}</td><td>Standby Current</td><td colspan="2">V_{CC} = 2.7V, $\overline{CS} = V_{CC}$</td><td></td><td>0.5</td><td>3.0</td><td>µA</td></tr>
<tr><td>I_{SB3}</td><td>Standby Current</td><td colspan="2">V_{CC} = 5.0V, $\overline{CS} = V_{CC}$</td><td></td><td>2.0</td><td>5.0</td><td>µA</td></tr>
<tr><td>I_{IL}</td><td>Input Current</td><td colspan="2">V_{IN} = 0V to V_{CC}</td><td>−3.0</td><td></td><td>3.0</td><td>µA</td></tr>
<tr><td>I_{OL}</td><td>Output Leakage</td><td colspan="2">V_{IN} = 0V to V_{CC}, T_{AC} = 0°C to 70°C</td><td>−3.0</td><td></td><td>3.0</td><td>µA</td></tr>
<tr><td>$V_{IL}^{(1)}$</td><td>Input Low-voltage</td><td colspan="2"></td><td>−1.0</td><td></td><td>V_{CC} x 0.3</td><td>V</td></tr>
<tr><td>$V_{IH}^{(1)}$</td><td>Input High-voltage</td><td colspan="2"></td><td>V_{CC} x 0.7</td><td></td><td>V_{CC} + 0.5</td><td>V</td></tr>
<tr><td>V_{OL1}</td><td>Output Low-voltage</td><td rowspan="2">$3.6 \le V_{CC} \le 5.5V$</td><td>I_{OL} = 3.0 mA</td><td></td><td></td><td>0.4</td><td>V</td></tr>
<tr><td>V_{OH1}</td><td>Output High-voltage</td><td>I_{OH} = −1.6 mA</td><td>V_{CC} −0.8</td><td></td><td></td><td>V</td></tr>
<tr><td>V_{OL2}</td><td>Output Low-voltage</td><td rowspan="2">$1.8V \le V_{CC} \le 3.6V$</td><td>I_{OL} = 0.15 mA</td><td></td><td></td><td>0.2</td><td>V</td></tr>
<tr><td>V_{OH2}</td><td>Output High-voltage</td><td>I_{OH} = −100 µA</td><td>V_{CC} −0.2</td><td></td><td></td><td>V</td></tr>
</table>

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

Table 4. AC Characteristics

Applicable over recommended operating range from $T_A = -40°C$ to $+ 85°C$, V_{CC} = As Specified, CL = 1 TTL Gate and 30 pF *(unless otherwise noted)*

Symbol	Parameter	Voltage	Min	Max	Units
f_{SCK}	SCK Clock Frequency	4.5−5.5 2.5−5.5 1.8−5.5	0 0 0	20 10 5	MHz
t_{RI}	Input Rise Time	4.5−5.5 2.5−5.5 1.8−5.5		2 2 2	µs
t_{FI}	Input Fall Time	4.5−5.5 2.5−5.5 1.8−5.5		2 2 2	µs
t_{WH}	SCK High Time	4.5−5.5 2.5−5.5 1.8−5.5	20 40 80		ns
t_{WL}	SCK Low Time	4.5−5.5 2.5−5.5 1.8−5.5	20 40 80		ns
t_{CS}	$\overline{\text{CS}}$ High Time	4.5−5.5 2.5−5.5 1.8−5.5	100 100 200		ns
t_{CSS}	$\overline{\text{CS}}$ Setup Time	4.5−5.5 2.5−5.5 1.8−5.5	100 100 200		ns
t_{CSH}	$\overline{\text{CS}}$ Hold Time	4.5−5.5 2.5−5.5 1.8−5.5	100 100 200		ns
t_{SU}	Data In Setup Time	4.5−5.5 2.5−5.5 1.8−5.5	5 10 20		ns
t_H	Data In Hold Time	4.5−5.5 2.5−5.5 1.8−5.5	5 10 20		ns
t_{HD}	$\overline{\text{HOLD}}$ Setup Time	4.5−5.5 2.5−5.5 1.8−5.5	5 10 20		ns
t_{CD}	$\overline{\text{HOLD}}$ Hold Time	4.5−5.5 2.5−5.5 1.8−5.5	5 10 20		ns
t_V	Output Vaild	4.5−5.5 2.5−5.5 1.8−5.5	0 0 0	20 40 80	ns
t_{HO}	Output Hold Time	4.5−5.5 2.5−5.5 1.8−5.5	0 0 0		ns
t_{LZ}	$\overline{\text{HOLD}}$ to Output Low Z	4.5−5.5 2.5−5.5 1.8−5.5	0 0 0	25 50 100	ns

Symbol	Parameter	Voltage	Min	Max	Units
t_{HZ}	HOLD to Output High Z	4.5−5.5 2.5−5.5 1.8−5.5		25 50 100	ns
t_{DIS}	Output Disable Time	4.5−5.5 2.5−5.5 1.8−5.5		25 50 100	ns
t_{WC}	Write Cycle Time	4.5−5.5 2.5−5.5 1.8−5.5		5 5 5	ms
Endurance (1)	5.0V, 25°C, Page Mode		1M		Write Cycles

Note: 1. This parameter is characterized and is not 100% tested. Contact Atmel for further information.

2. Serial Interface Description

MASTER: The device that generates the serial clock.

SLAVE: Because the serial clock pin (SCK) is always an input, the AT25128B/256B always operates as a slave.

TRANSMITTER/RECEIVER: The AT25128B/256B has separate pins designated for data transmission (SO) and reception (SI).

MSB: The Most Significant Bit (MSB) is the first bit transmitted and received.

SERIAL OP-CODE: After the device is selected with CS going low, the first byte will be received. This byte contains the op-code that defines the operations to be performed.

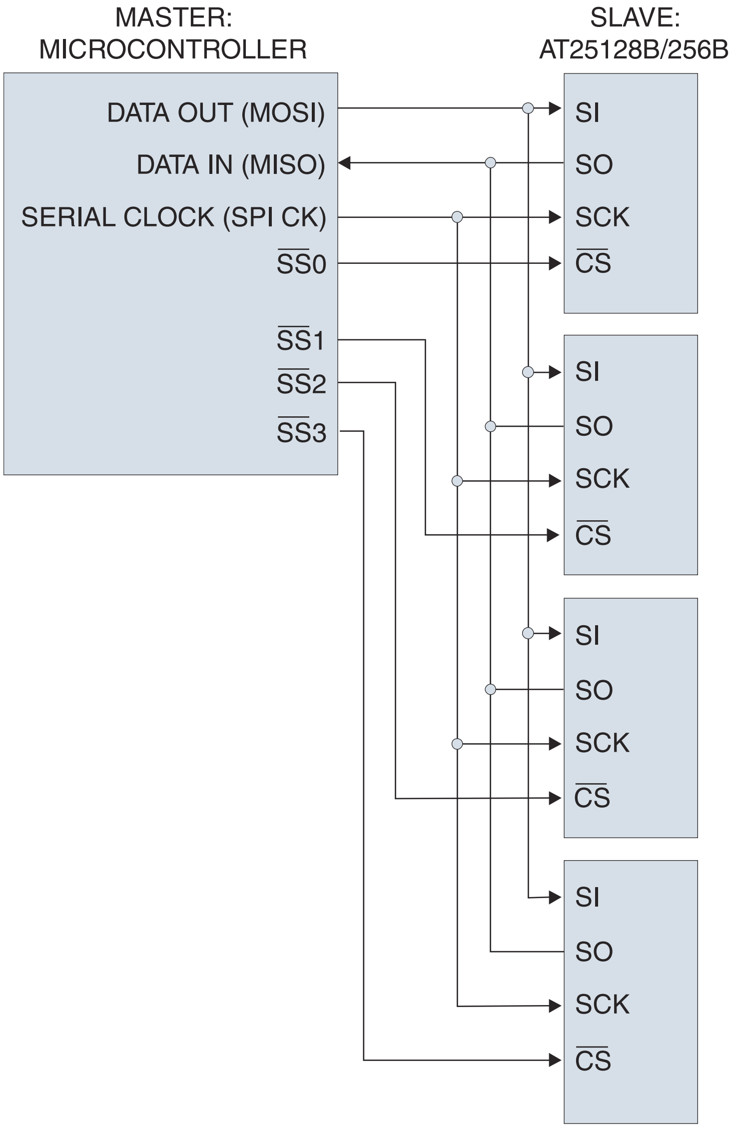
INVALID OP-CODE: If an invalid op-code is received, no data will be shifted into the AT25128B/256B, and the serial output pin (SO) will remain in a high impedance state until the falling edge of CS is detected again. This will reinitialize the serial communication.

CHIP SELECT: The AT25128B/256B is selected when the CS pin is low. When the device is not selected, data will not be accepted via the SI pin, and the serial output pin (SO) will remain in a high impedance state.

HOLD: The HOLD pin is used in conjunction with the CS pin to select the AT25128B/256B. When the device is selected and a serial sequence is underway, HOLD can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the HOLD pin must be brought low while the SCK pin is low. To resume serial communication, the HOLD pin is brought high while the SCK pin is low (SCK may still toggle during HOLD). Inputs to the SI pin will be ignored while the SO pin is in the high impedance state.

WRITE PROTECT: The write protect pin (WP) will allow normal read/write operations when held high. When the WP pin is brought low and WPEN bit is "1", all write operations to the status register are inhibited. WP going low while CS is still low will interrupt a write to the status register. If the internal write cycle has already been initiated, WP going low will have no effect on any write operation to the status register. The WP pin function is blocked when the WPEN bit in the status register is "0". This will allow the user to install the AT25128B/256B in a system with the WP pin tied to ground and still be able to write to the status register. All WP pin functions are enabled when the WPEN bit is set to "1".

Figure 3. *SPI Serial Interface*



3. Functional Description

The AT25128B/256B is designed to interface directly with the synchronous serial peripheral interface (SPI) of the 6800 type series of microcontrollers.

The AT25128B/256B utilizes an 8-bit instruction register. The list of instructions and their operation codes are contained in Figure 6. All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low $\overline{\text{CS}}$ transition.

Table 5. Instruction Set for the AT25128B/256B

Instruction Name	Instruction Format	Operation
WREN	0000 X110	Set Write Enable Latch
WRDI	0000 X100	Reset Write Enable Register
RDSR	0000 X101	Read Status Register
WRSR	0000 X001	Write Status Register
READ	0000 X011	Read Data from Memory Array
WRITE	0000 X 010	Write Data to Memory Array

WRITE ENABLE (WREN): The device will power-up in the write disable state when V_{CC} is applied. All programming instructions must therefore be preceded by a Write Enable instruction.

WRITE DISABLE (WRDI): To protect the device against inadvertent writes, the Write Disable instruction disables all programming modes. The WRDI instruction is independent of the status of the $\overline{\text{WP}}$ pin.

READ STATUS REGISTER (RDSR): The Read Status Register instruction provides access to the status register. The Ready/Busy and Write Enable status of the device can be determined by the RDSR instruction. Similarly, the Block Write Protection bits indicate the extent of protection employed. These bits are set by using the WRSR instruction.

Table 6. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN	X	X	X	BP1	BP0	WEN	$\overline{\text{RDY}}$

Table 7. Read Status Register Bit Definition

Bit	Definition
Bit 0 ($\overline{\text{RDY}}$)	Bit 0 = "0" ($\overline{\text{RDY}}$) indicates the device is ready. Bit 0 = "1" indicates the write cycle is in progress.
Bit 1 (WEN)	Bit 1 = 0 indicates the device is not write enabled. Bit 1 = "1" indicates the device is write enabled.
Bit 2 (BP0)	See Table 8 on page 9.
Bit 3 (BP1)	See Table 8 on page 9.
Bits 4 – 6 are 0s when device is not an internal write cycle.	
Bit 7 (WPEN)	See Table 9 on page 9.
Bits 0 – 7 are "1"s during an internal write cycle.	

WRITE STATUS REGISTER (WRSR): The WRSR instruction allows the user to select one of four levels of protection. The AT25128B/256B is divided into four array segments. Top quarter (1/4), top half (1/2), or all of the memory segments can be protected. Any of the data within any selected segment will therefore be read only. The block write protection levels and corresponding status register control bits are shown in Table 8.

The three bits, BP0, BP1, and WPEN are nonvolatile cells that have the same properties and functions as the regular memory cells (e.g. WREN, t_{WC}, RDSR).

Table 8. Block Write Protect Bits

Level	Status Register Bits		Array Addresses Protected	
	BP1	BP0	AT25128B	AT25256B
0	0	0	None	None
1 (1/4)	0	1	3000 – 3FFF	6000 – 7FFF
2 (1/2)	1	0	2000 – 3FFF	4000 – 7FFF
3 (All)	1	1	0000 – 3FFF	0000 – 7FFF

The WRSR instruction also allows the user to enable or disable the write protect ($\overline{\text{WP}}$) pin through the use of the write protect enable (WPEN) bit. Hardware write protection is enabled when the $\overline{\text{WP}}$ pin is low and the WPEN bit is “1”. Hardware write protection is disabled when either the $\overline{\text{WP}}$ pin is high or the WPEN bit is “0”. When the device is hardware write protected, writes to the Status Register, including the Block Protect bits and the WPEN bit, and the blockprotected sections in the memory array are disabled. Writes are only allowed to sections of the memory which are not block-protected.

NOTE: When the WPEN bit is hardware write protected, it cannot be changed back to “0”, as long as the$\overline{\text{WP}}$ pin is held low.

Table 9. WPEN Operation

WPEN	$\overline{\text{WP}}$	WEN	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writable	Writable

READ SEQUENCE (READ): Reading the AT25128B/256B via the SO pin requires the following sequence. After the $\overline{\text{CS}}$ line is pulled low to select a device, the Read op-code is transmitted via the SI line followed by the byte address to be read (Table 10 on page 10). Upon completion, any data on the SI line will be ignored. The data (D7 - D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the $\overline{\text{CS}}$ line should be driven high after the data comes out. The read sequence can be continued since the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached, the address counter will roll over to the lowest address allowing the entire memory to be read in one continuous read cycle.

WRITE SEQUENCE (WRITE): In order to program the AT25128B/256B, two separate instructions must be executed. First, the device *must be write enabled* via the Write Enable (WREN) Instruction. Then a Write instruction may be executed. Also, the address of the memory location(s) to be programmed must be outside the protected address field location selected by the Block Write Protection Level. During an internal write cycle, all commands will be ignored except the RDSR instruction.

A Write Instruction requires the following sequence. After the $\overline{CS}$ line is pulled low to select the device, the Write op-code is transmitted via the SI line followed by the byte address and the data (D7 - D0) to be programmed (Table 10). Programming will start after the $\overline{CS}$ pin is brought high. (The Low-to-High transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the D0 (LSB) data bit.

The Ready/Busy status of the device can be determined by initiating a Read Status Register (RDSR) Instruction. If Bit 0 = 1, the Write cycle is still in progress. If Bit 0 = 0, the Write cycle has ended. Only the Read Status Register instruction is enabled during the Write programming cycle.

The AT25128B/256B is capable of a 64-byte Page Write operation. After each byte of data is received, the six low order address bits are internally incremented by one; the high order bits of the address will remain constant. If more than 64 bytes of data are transmitted, the address counter will roll over and the previously written data will be overwritten. The AT25128B/256B is automatically returned to the write disable state at the completion of a Write cycle.

NOTE: If the device is not write enabled (WREN), the device will ignore the Write instruction and will return to the standby state, when $\overline{CS}$ is brought high. A new $\overline{CS}$ falling edge is required to re-initiate the serial communication.

Table 10. Address Key

Address	AT25128B	AT25256B
A_N	$A_{13} - A_0$	$A_{14} - A_0$
Don't Care Bits	$A_{15} - A_{14}$	A_{15}

4. Timing Diagram (for SPI Mode 0 (0,0)

Figure 4. Synchronous Data Timing

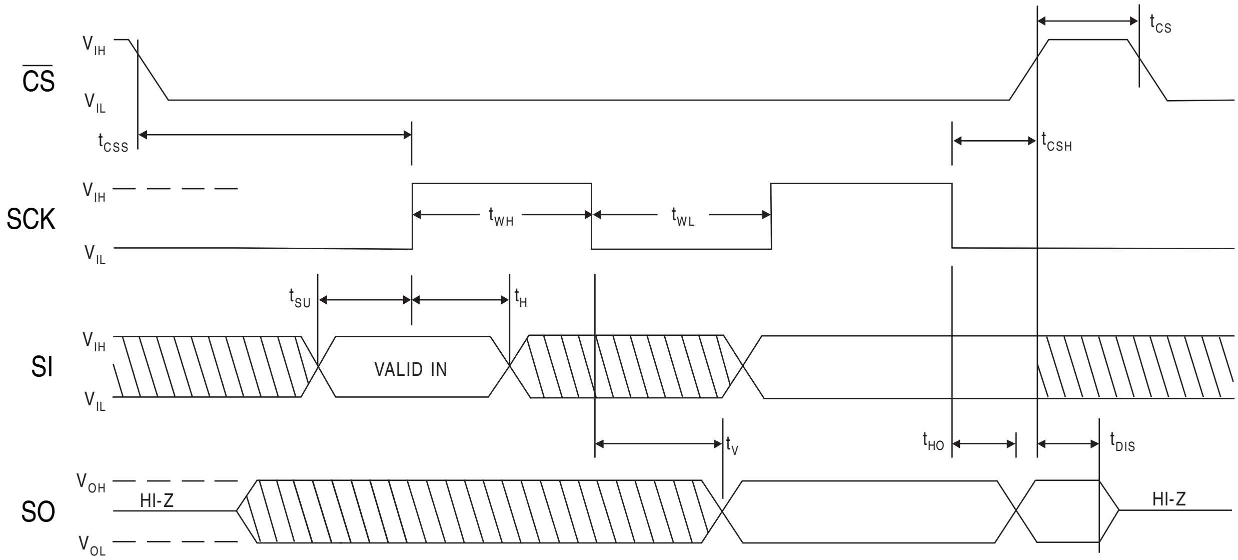


Figure 5. *WREN Timing*

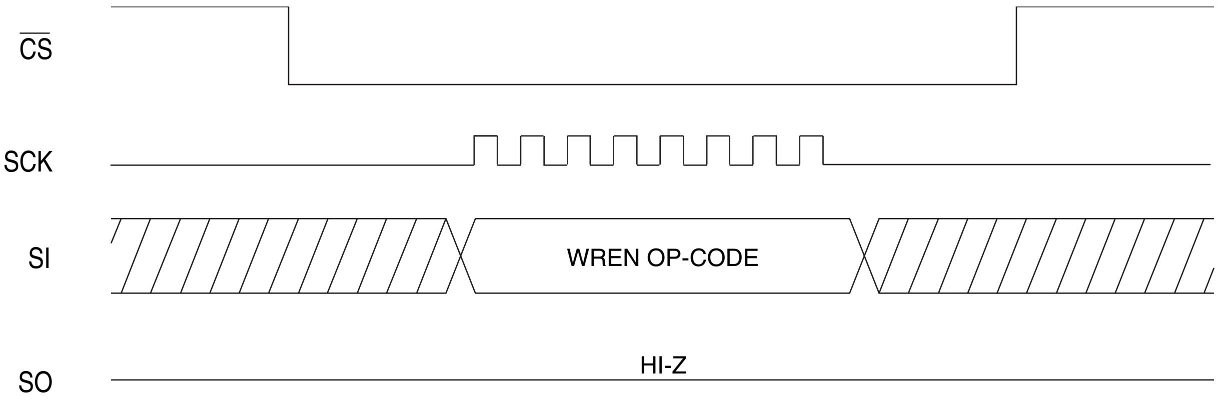


Figure 6. *WRDI Timing*

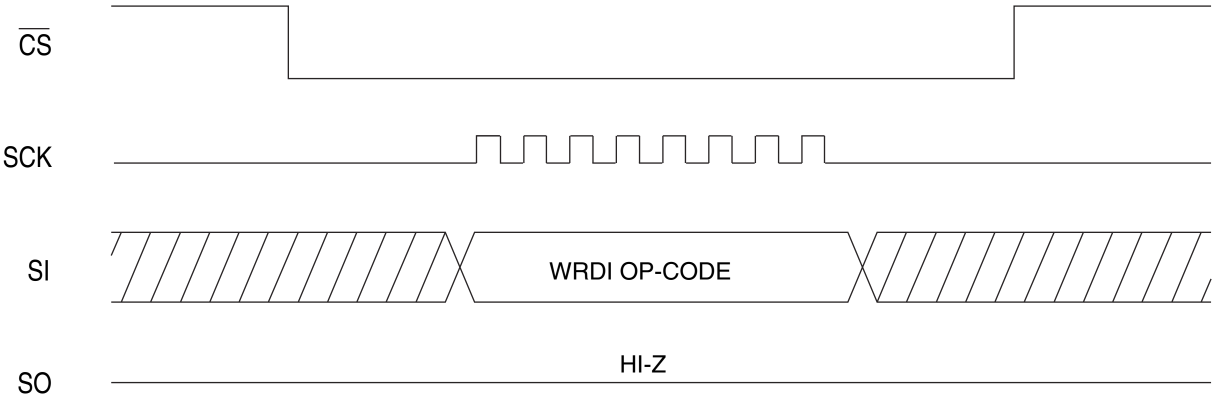


Figure 7. *RDSR Timing*

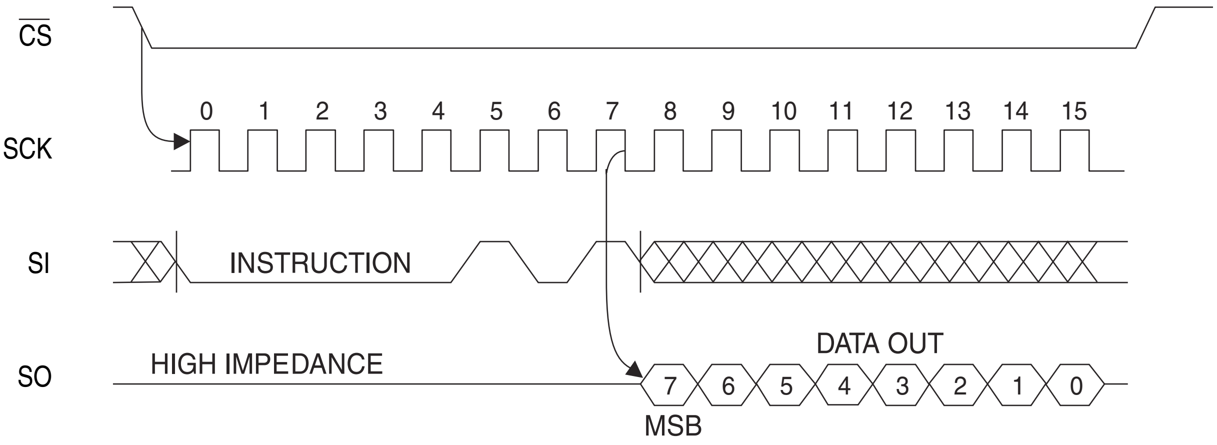


Figure 8. WRSR Timing

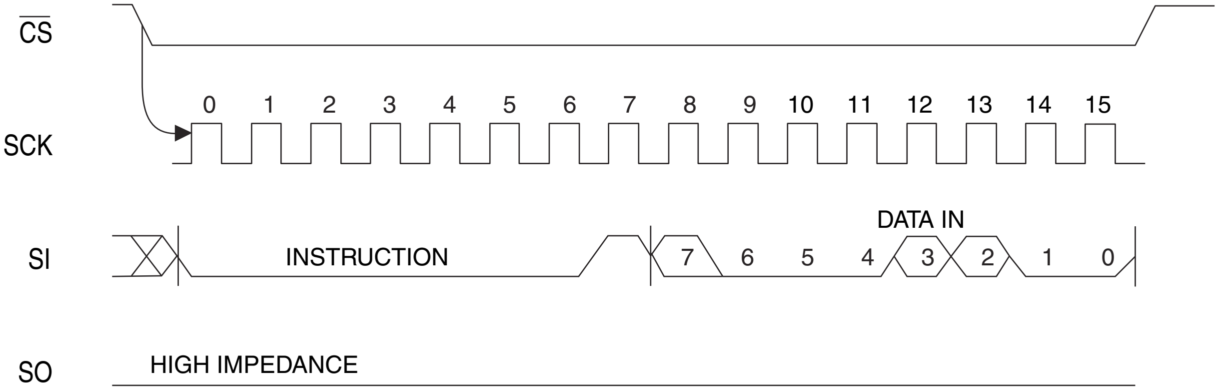


Figure 9. READ Timing

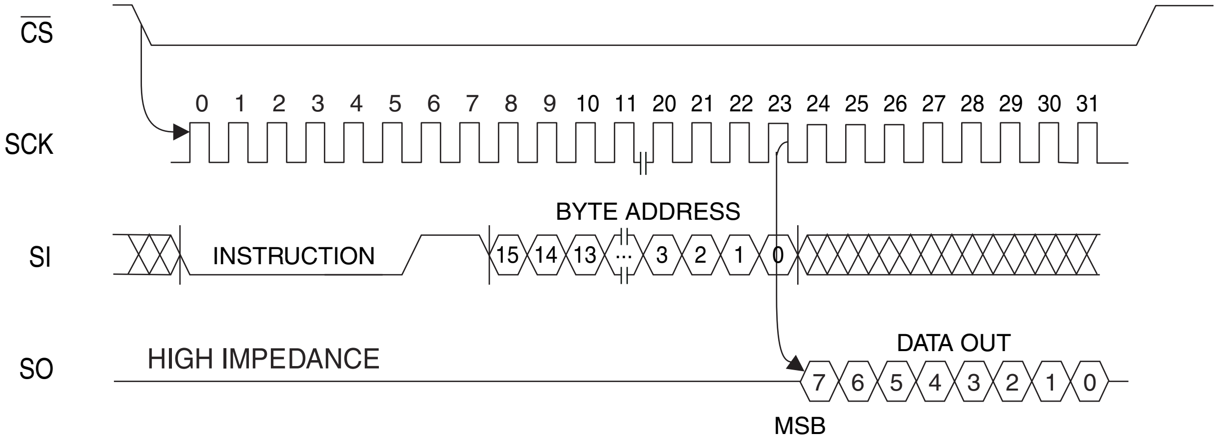


Figure 10. WRITE Timing

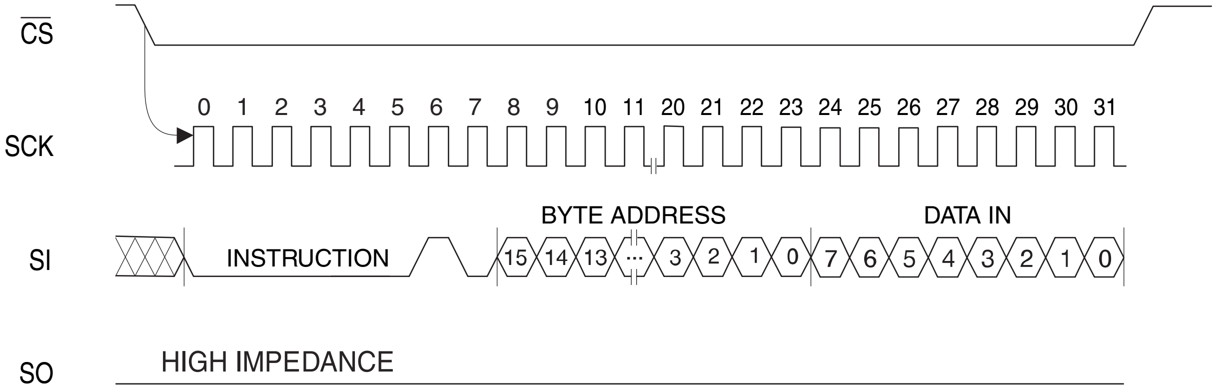
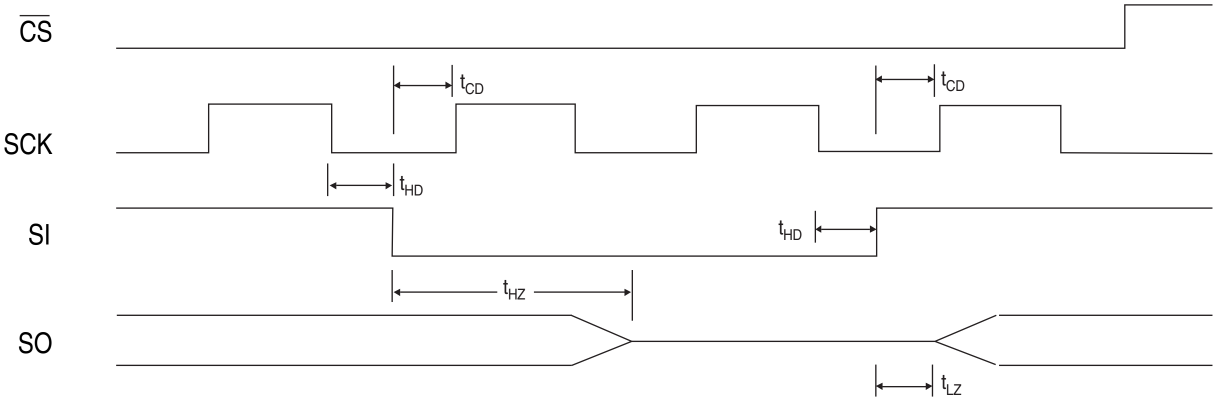


Figure 11. $\overline{\text{HOLD}}$ *Timing*



5. Package Ordering Information

AT25128B Ordering Information

Table 11. AT25128B Ordering Information

Ordering Code	Package	Voltage Range	Operation Range
AT25128B-PU(1) AT25128BN-SU(1) AT25128BW-SU(1) AT25128B-TU(1) AT25128BU2-UU(1) AT25128BY6-YH(1)	8P3 8S1 8S2 8A2 8U2-1 8Y6	1.8 1.8 1.8 1.8 1.8 1.8	Lead-free/Halogen-free/ Industrial Temperature (−40°C to 85°C)
AT25128B-W-11(2)	Die Sale	1.8	Industrial Temperature (−40°C to 85°C)

Notes: 1. "U" designates Green package + RoHS compliant.
2. Available in waffle pack and wafer form; order as SL788 for wafer form. Bumped die available upon request. Please Contact Serial Interface Marketing.

Package Type	
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
8S2	8-lead, 0.200" Wide, Plastic Gull Wing Small Outline Package (EIAJ SOIC)
8U2-1	8-ball, die Ball Grid Array Package (dBGA2)
8A2	8-lead, 4.40 mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)
8Y6	8-lead, 2.00 mm x 3.00 mm Body, 0.50 mm Pitch, Ultra Thin Mini-MAP, Dual No Lead Package (DFN), (MLP 2x3mm)

AT25256B Ordering Information

Table 12. AT25256B Ordering information

Ordering Code	Package	Voltage Range	Operation Range
AT25256B-PU(1) AT25256BN-SU(1) AT25256BW-SU(1) AT25256B-TU(1) AT25256BU2-UU(1) AT25256BY6-YH(1)	8P3 8S1 8S2 8A2 8U2-1 8Y6	1.8 1.8 1.8 1.8 1.8 1.8	Lead-free/Halogen-free/ Industrial Temperature (−40°C to 85°C)
AT25256B-W-11(2)	Die Sale	1.8	Industrial Temperature (−40°C to 85°C)

Notes: 1. “U” designates Green package + RoHS compliant.
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Package Type	
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
8S2	8-lead, 0.200” Wide, Plastic Gull Wing Small Outline Package (EIAJ SOIC)
8U2-1	8-ball, die Ball Grid Array Package (dBGA2)
8A2	8-lead, 4.40 mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)
8Y6	8-lead, 2.00 mm x 3.00 mm Body, 0.50 mm Pitch, Ultra Thin Mini-MAP, Dual No Lead Package (DFN), (MLP 2x3mm)

AT25128B Part Markings

AT25128BU2-UU-T 8U2-1 dBGA2

```
 TOP MARK
|---|---|---|---|
  5   D   B   U
|---|---|---|---|---|
  P   Y   M   X   X
|---|---|---|---|---|
  *  <--  Pin 1 Indicator

    P = Country of Origin
    Y = One Digit Year Code
    M = One Digit Month Code

    XX = TRACE CODE (ATMEL LOT
         NUMBERS TO CORRESPOND
         WITH TRACE CODE LOG BOOK)
          (e.g. XX = AA, AB...YZ, ZZ)

 Y = ONE DIGIT YEAR CODE
   4: 2004   7: 2007
   5: 2005   8: 2008
   6: 2006   9: 2009

 M = SEAL MONTH (USE ALPHA DESIGNATOR A-L)
 A = JANUARY
 B = FEBRUARY
  """""""
 J = OCTOBER
 K = NOVEMBER
 L = DECEMBER
```

AT25128BY6-YH-T 8Y6 Ultra Thin Mini-MAP

```
TOP MARK

|---|---|---|
  5   D   B
|---|---|---|
  H   1
|---|---|---|
  Y   X   X
|---|---|---|
  *
  |
 Pin 1 Indicator (Dot)

Y = YEAR OF ASSEMBLY

    XX = TRACE CODE (ATMEL LOT
         NUMBERS TO CORRESPOND
         WITH TRACE CODE LOG BOOK)
          (e.g. XX = AA, AB...YZ, ZZ)

Y = SEAL YEAR
 8: 2008   0: 2012
 9: 2007   1: 2013
 0: 2010   2: 2014
 1: 2011   3: 2015
```

AT25128B-PU 8P3 PDIP

```
                     Seal Year
TOP MARK              |  Seal Week
                      |   |   |
|---|---|---|---|---|---|---|---|
  A   T   M   L   U   Y   W   W
|---|---|---|---|---|---|---|---|
  5   D   B   1               @
|---|---|---|---|---|---|---|---|
     *   Lot Number
|---|---|---|---|---|---|---|---|
  |
 Pin 1 Indicator (Dot)

Y = SEAL YEAR          WW = SEAL WEEK WW = SEAL WEEK
 8: 2008   2: 2012      02 = Week 2  02 = Week 2
 9: 2009   3: 2013      04 = Week 4  04 = Week 4
 0: 2010   4: 2014      :: : :::: :   :: : :::: :
 1: 2011   5: 2015      52 = Week 52  :: : :::: ::
  50 = Week 50
  52 = Week 52

 @ = Country of Assembly
           No Bottom Mark
```

AT25128BN-SU-T/B 8S1 JEDEC SOIC
AT25128BW-SU-T/B 8S2 EIAJ SOIC

```
                      Seal Year
TOP MARK              |  Seal Week
                      |   |   |
|---|---|---|---|---|---|---|---|
  A   T   M   L   H   Y   W   W
|---|---|---|---|---|---|---|---|
  5   D   B   1               @
|---|---|---|---|---|---|---|---|
     *   Lot Number
|---|---|---|---|---|---|---|---|
  |
 Pin 1 Indicator (Dot)

Y = SEAL YEAR          WW = SEAL WEEK WW = SEAL WEEK
 8: 2008   2: 2012      02 = Week 2   02 = Week 2
 9: 2009   3: 2013      04 = Week 4   04 = Week 4
 0: 2010   4: 2014      :: : :::: :    :: : :::: :
 1: 2011   5: 2015      52 = Week 52   :: : :::: ::
  50 = Week 50
  52 = Week 52

 @ = Country of Assembly
           No Bottom Mark
```

AT25128B-TU-T/B 8A2 TSSOP

```
TOP MARK

 Pin 1 Indicator (Dot)
  |
     |---|---|---|---|---|---|
  *    A   T   H   Y   W   W
     |---|---|---|---|---|---|
       5   D   B   1       @
 |---|---|---|---|---|---|---|
    ATMEL LOT NUMBER
 |---|---|---|---|---|---|---|

Y = SEAL YEAR          WW = SEAL WEEK
 8: 2008   2: 2012      02 = Week 2
 9: 2009   3: 2013      04 = Week 4
 0: 2010   4: 2014      :: : :::: :
 1: 2011   5: 2015      52 = Week 52


  @ = Country of Assembly
           No Bottom Mark
```

AT25256B Part Markings

AT25256BU2-UU-T 8U2-1 dBGA2

```
 TOP MARK
|---|---|---|---|
  5   E   B   U
|---|---|---|---|---|
  P   Y   M   X   X
|---|---|---|---|---|
  *  <--  Pin 1 Indicator

    P = Country of Origin
    Y = One Digit Year Code
    M = One Digit Month Code

    XX = TRACE CODE (ATMEL LOT
         NUMBERS TO CORRESPOND
         WITH TRACE CODE LOG BOOK)
          (e.g. XX = AA, AB...YZ, ZZ)

 Y = ONE DIGIT YEAR CODE
   4: 2004   7: 2007
   5: 2005   8: 2008
   6: 2006   9: 2009

 M = SEAL MONTH (USE ALPHA DESIGNATOR A-L)
 A = JANUARY
 B = FEBRUARY
  """""""
 J = OCTOBER
 K = NOVEMBER
 L = DECEMBER
```

AT25256BY6-YH-T 8Y6 Ultra Thin Mini-MAP

```
TOP MARK

|---|---|---|
  5   E   B
|---|---|---|
  H   1
|---|---|---|
  Y   X   X
|---|---|---|
  *
  |
 Pin 1 Indicator (Dot)

Y = YEAR OF ASSEMBLY

    XX = TRACE CODE (ATMEL LOT
         NUMBERS TO CORRESPOND
         WITH TRACE CODE LOG BOOK)
          (e.g. XX = AA, AB...YZ, ZZ)

Y = SEAL YEAR
 8: 2008   0: 2012
 9: 2007   1: 2013
 0: 2010   2: 2014
 1: 2011   3: 2015
```

AT25256B-PU 8P3 PDIP

```
                     Seal Year
TOP MARK              |  Seal Week
                      |   |   |
|---|---|---|---|---|---|---|---|
  A   T   M   L   U   Y   W   W
|---|---|---|---|---|---|---|---|
  5   E   B   1               @
|---|---|---|---|---|---|---|---|
     *   Lot Number
|---|---|---|---|---|---|---|---|
  |
 Pin 1 Indicator (Dot)

Y = SEAL YEAR          WW = SEAL WEEK WW = SEAL WEEK
 8: 2008   2: 2012      02 = Week 2  02 = Week 2
 9: 2009   3: 2013      04 = Week 4  04 = Week 4
 0: 2010   4: 2014      :: : :::: :   :: : :::: :
 1: 2011   5: 2015      52 = Week 52  :: : :::: ::
  50 = Week 50
  52 = Week 52

 @ = Country of Assembly
           No Bottom Mark
```

AT25256BN-SU-T/B 8S1 JEDEC SOIC
AT25256BW-SU-T/B 8S2 EIAJ SOIC

```
                      Seal Year
TOP MARK              |  Seal Week
                      |   |   |
|---|---|---|---|---|---|---|---|
  A   T   M   L   H   Y   W   W
|---|---|---|---|---|---|---|---|
  5   E   B   1               @
|---|---|---|---|---|---|---|---|
     *   Lot Number
|---|---|---|---|---|---|---|---|
  |
 Pin 1 Indicator (Dot)

Y = SEAL YEAR          WW = SEAL WEEK WW = SEAL WEEK
 8: 2008   2: 2012      02 = Week 2  02 = Week 2
 9: 2009   3: 2013      04 = Week 4  04 = Week 4
 0: 2010   4: 2014      :: : :::: :   :: : :::: :
 1: 2011   5: 2015      52 = Week 52  :: : :::: ::
  50 = Week 50
  52 = Week 52

 @ = Country of Assembly
           No Bottom Mark
```

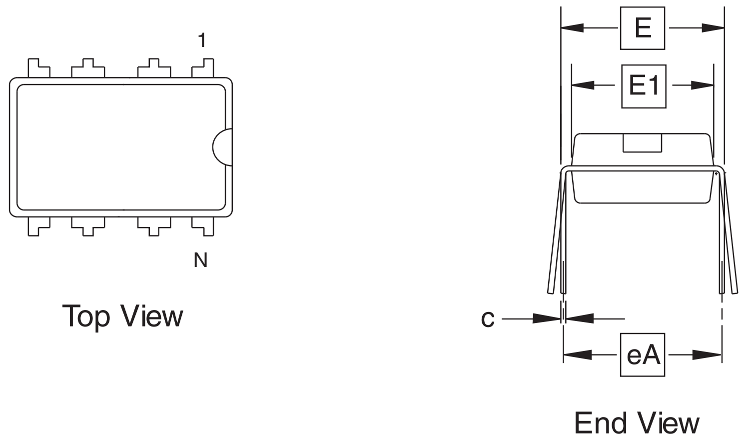
AT25256B-TU-T/B 8A2 TSSOP

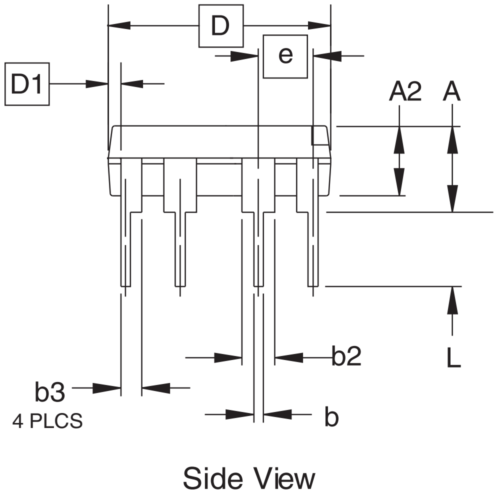
```
TOP MARK

 Pin 1 Indicator (Dot)
  |
     |---|---|---|---|---|---|
  *    A   T   H   Y   W   W
     |---|---|---|---|---|---|
       5   E   B   1       @
 |---|---|---|---|---|---|---|
    ATMEL LOT NUMBER
 |---|---|---|---|---|---|---|

Y = SEAL YEAR          WW = SEAL WEEK
 8: 2008   2: 2012      02 = Week 2
 9: 2009   3: 2013      04 = Week 4
 0: 2010   4: 2014      :: : :::: :
 1: 2011   5: 2015      52 = Week 52


  @ = Country of Assembly
           No Bottom Mark
```

6. Packaging Information

8P3 – PDIP

Figure 12. 8P3 – PDIP





COMMON DIMENSIONS
(Unit of Measure = inches)

SYMBOL	MIN	NOM	MAX	NOTE
A	•	•	0.210	2
A2	0.115	0.130	0.195	
b	0.014	0.018	0.022	5
b2	0.045	0.060	0.070	6
b3	0.030	0.039	0.045	6
c	0.008	0.010	0.014	
D	0.355	0.365	0.400	3
D1	0.005	•	•	3
E	0.300	0.310	0.325	4
E1	0.240	0.250	0.280	3
e	0.100 BSC			
eA	0.300 BSC			4
L	0.115	0.130	0.150	2

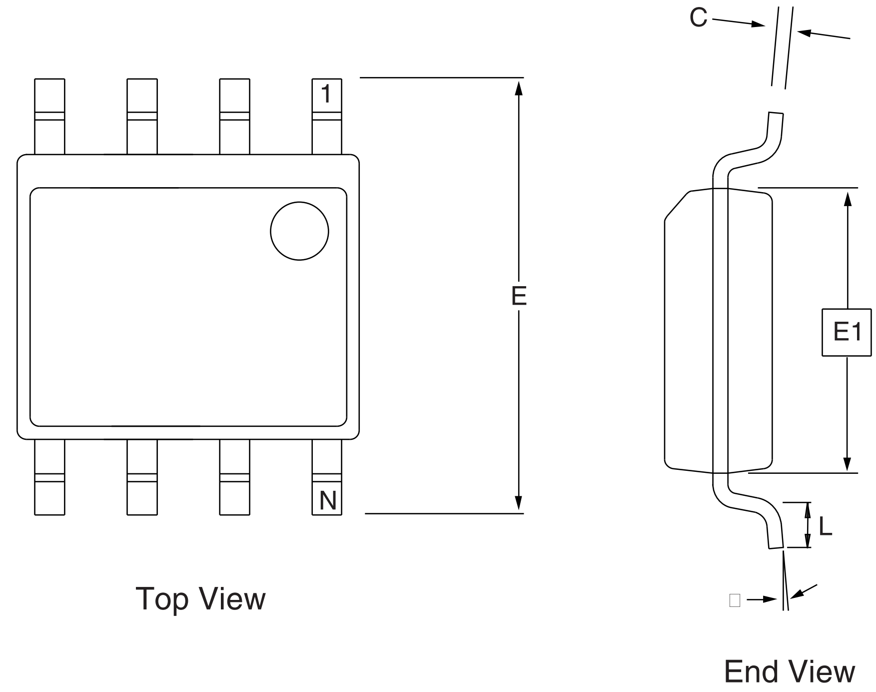
Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA, for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not • exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not • exceed 0.010 (0.25 mm).

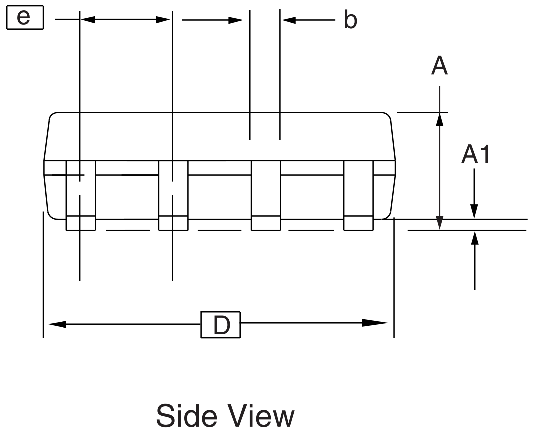
01/09/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8P3,** 8-lead, 0.300" Wide Body, Plastic Dual In-line Package (PDIP)	8P3	B

8S1 – JEDEC SOIC

Figure 13. 8S1 – JEDEC SOIC





COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
□	0˚	–	8˚	

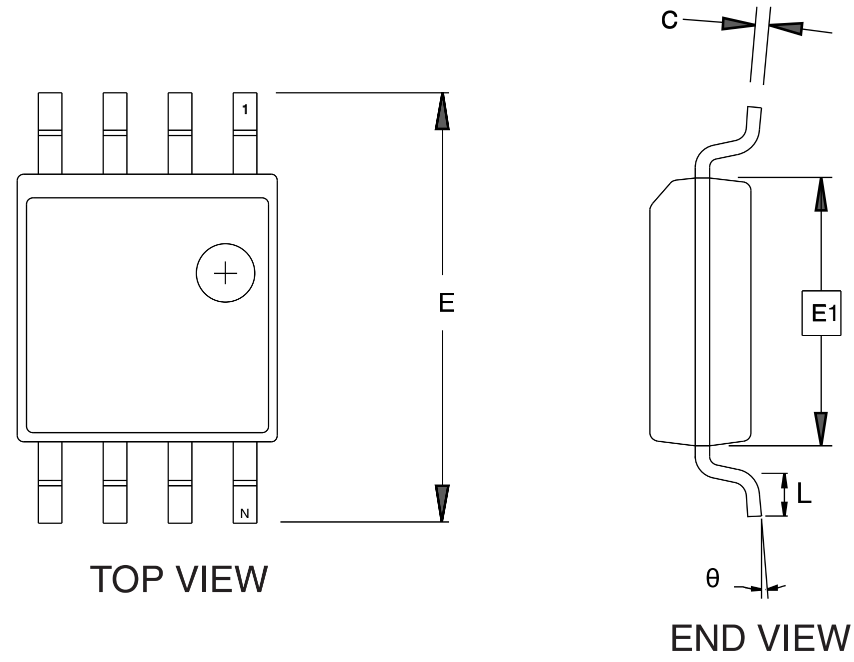
Note: These drawings are for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

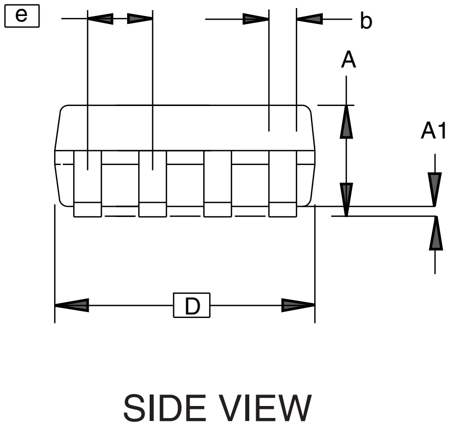
3/17/05

1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906	**TITLE** **8S1,** 8-lead (0.150" Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	**DRAWING NO.** 8S1	**REV.** C

8S2 – EIAJ SOIC

Figure 14. *8S2 – EIAJ SOIC*





COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.70		2.16	
A1	0.05		0.25	
b	0.35		0.48	5
C	0.15		0.35	5
D	5.13		5.35	
E1	5.18		5.40	2, 3
E	7.70		8.26	
L	0.51		0.85	
θ	0°		8°	
e	1.27 BSC			4

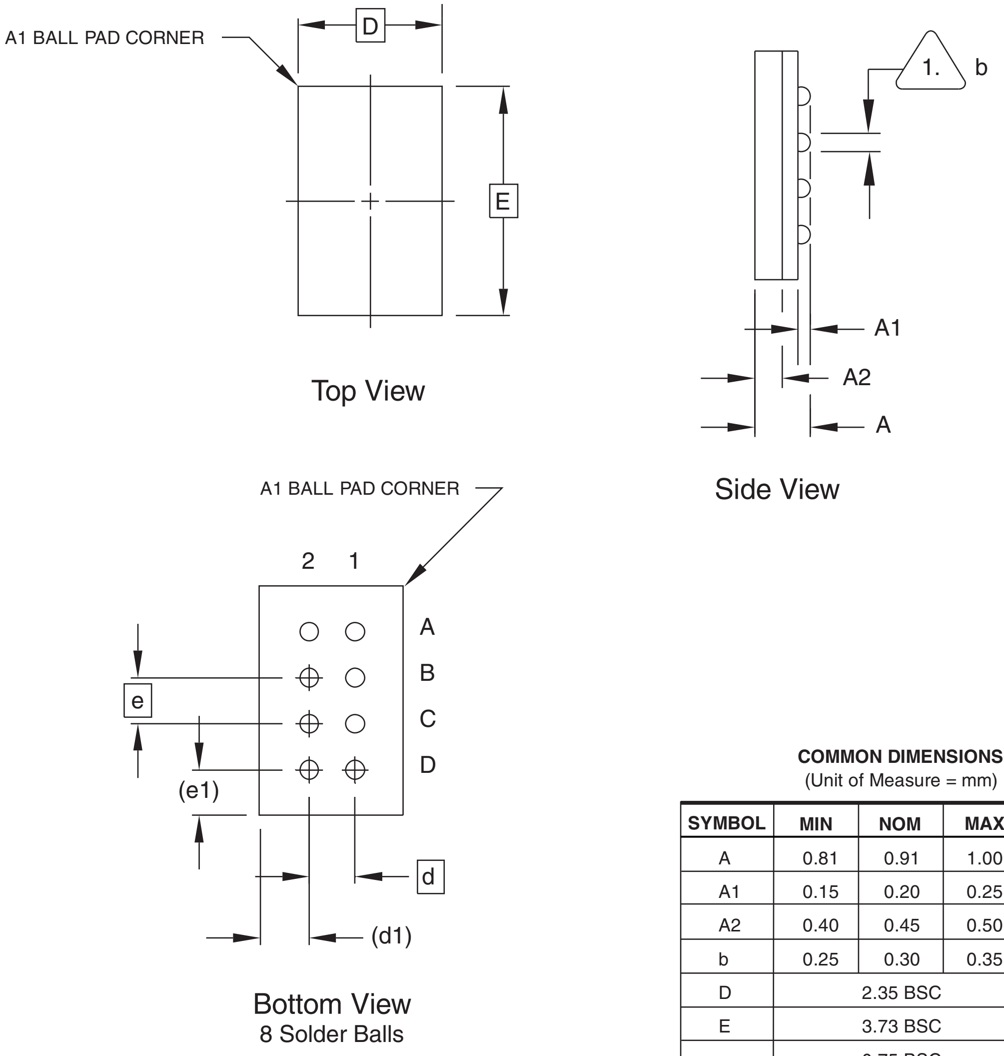
Notes:
1. This drawing is for general information only; refer to EIAJ Drawing EDR-7320 for additional information.
2. Mismatch of the upper and lower dies and resin burrs aren't included.
3. It is recommended that upper and lower cavities be equal. If they are different, the larger dimension shall be regarded.
4. Determines the true geometric position.
5. Values b,C apply to plated terminal. The standard thickness of the plating layer shall measure between 0.007 to .021 mm.

04/07/06

2325 Orchard Parkway San Jose, CA 95131	**TITLE** **8S2,** 8-lead, 0.209" Body, Plastic Small Outline Package (EIAJ)	**DRAWING NO.** 8S2	**REV.** D

8U2-1 – dBGA2

Figure 15. *8U2-1 – dBGA2*



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.81	0.91	1.00	
A1	0.15	0.20	0.25	
A2	0.40	0.45	0.50	
b	0.25	0.30	0.35	1
D		2.35 BSC		
E		3.73 BSC		
e		0.75 BSC		
e1		0.74 REF		
d		0.75 BSC		
d1		0.80 REF		

1. Dimension 'b' is measured at the maximum solder ball diameter.

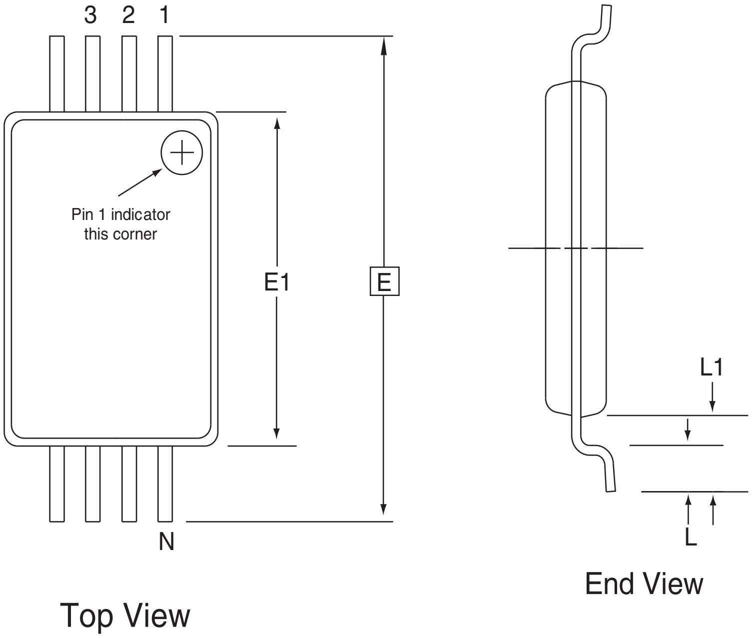
This drawing is for general information only.

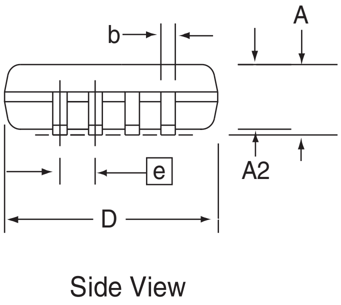
06/24/03

	TITLE	DRAWING NO.	REV.
1150 E. Cheyenne Mtn. Blvd. Colorado Springs, CO 80906	8U2-1, 8-ball, 2.35 x 3.73 mm Body, 0.75 mm pitch, Small Die Ball Grid Array Package (dBGA2)	PO8U2-1	A

8A2 – TSSOP

Figure 16. *8A2 – TSSOP*





COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D	2.90	3.00	3.10	2, 5
E	6.40 BSC			
E1	4.30	4.40	4.50	3, 5
A	–	–	1.20	
A2	0.80	1.00	1.05	
b	0.19	–	0.30	4
e	0.65 BSC			
L	0.45	0.60	0.75	
L1	1.00 RE3			

Notes:

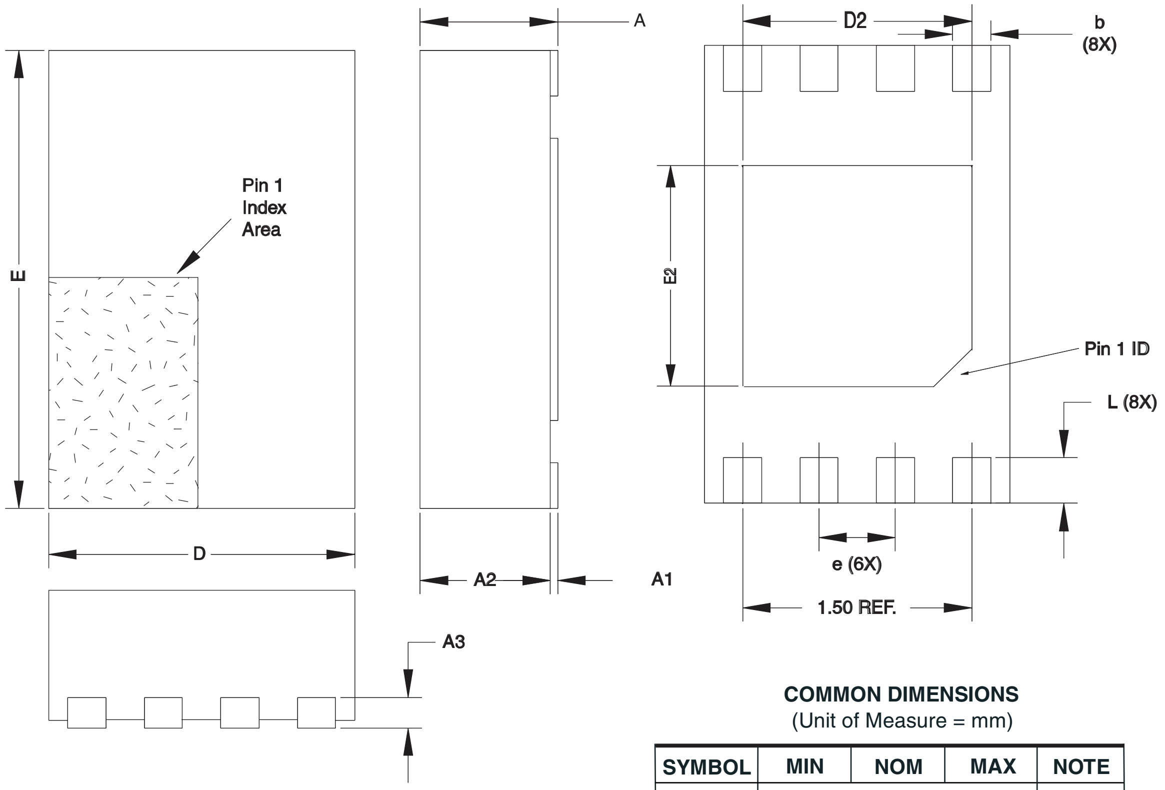
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07 mm .
5. Dimension D and E1 to be determined at Datum Plane H .

10/29/08

Package Drawing Contact:• packagedrawings@atmel.com	**TITLE** **8A2,** 8-lead, 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	**GPC** TNR	**DRAWING NO.** • 8A2	**REV.** C

8Y6 – Ultra Thin Mini-MAP

Figure 17. 8Y6 – Ultra Thin Mini-MAP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D		2.00 BSC		
E		3.00 BSC		
D2	1.40	1.50	1.60	
E2	-	-	1.40	
A	-	-	0.60	
A1	0.0	0.02	0.05	
A2	-	-	0.55	
A3		0.20 REF		
L	0.20	0.30	0.40	
e		0.50 BSC		
b	0.20	0.25	0.30	2

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-229, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.
3. Soldering the large thermal pad is optional, but not recommended. No electrical connection is accomplished to the device through this pad, so if soldered it should be tied to ground

11/21/08

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact:• packagedrawings@atmel.com	**8Y6, 8-lead**, 2.0x3.0 mm Body, 0.50 mm Pitch, UltraThin Mini-MAP, Dual No Lead Package (Sawn)(UDFN)	YNZ	8Y6	E

7. Revision History

Doc. Rev.	Date	Comments
8593A	01/2009	Initial document release.