Dual Single-Supply Audio Operational Amplifier

SSM2135*

FEATURES

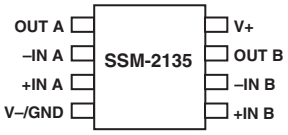
Excellent Sonic Characteristics
High Output Drive Capability
5.2 nV/√Hz Equivalent Input Noise @ 1 kHz
0.001% THD+N (V_O = 2.5 V p-p @ 1 kHz)
3.5 MHz Gain Bandwidth
Unity-Gain Stable
Low Cost

APPLICATIONS

Multimedia Audio Systems
Microphone Preamplifier
Headphone Driver
Differential Line Receiver
Balanced Line Driver
Audio ADC Input Buffer
Audio DAC I-V Converter and Filter
Pseudo-Ground Generator

PIN CONNECTIONS

8-Lead Narrow-Body SOIC
(S Suffix)



GENERAL DESCRIPTION

The SSM2135 Dual Audio Operational Amplifier permits excellent performance in portable or low power audio systems, with an operating supply range of +4 V to +36 V or ±2 V to ±18 V. The unity gain stable device has very low voltage noise of 4.7 nV/√Hz, and total harmonic distortion plus noise below 0.01% over normal signal levels and loads. Such characteristics are enhanced by wide output swing and load drive capability. A unique output stage* permits output swing approaching the rail under moderate load conditions. Under severe loading, the SSM2135 still maintains a wide output swing with ultralow distortion.

Particularly well suited for computer audio systems and portable digital audio units, the SSM2135 can perform preamplification, headphone and speaker driving, and balanced line driving and receiving. Additionally, the device is ideal for input signal conditioning in single-supply, sigma-delta, analog-to-digital converter subsystems such as the AD1878/AD1879.

The SSM2135 is available in an 8-lead plastic SOIC package and is guaranteed for operation over the extended industrial temperature range of –40°C to +85°C.

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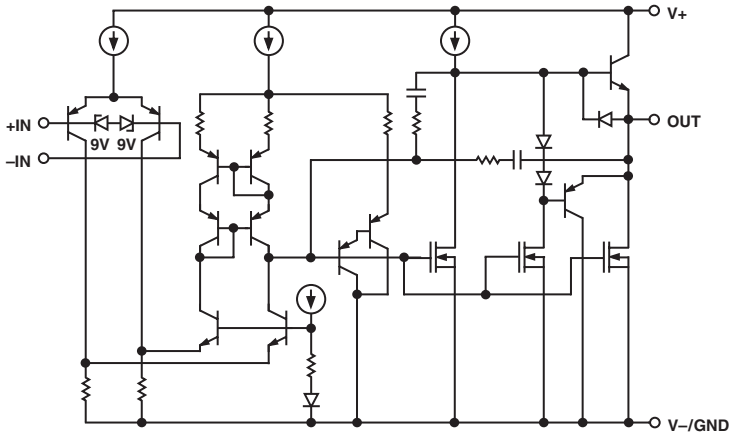
FUNCTIONAL BLOCK DIAGRAM



*Protected by U.S. Patent No. 5,146,181.

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SSM2135–SPECIFICATIONS

(V_S = 5 V, –40°C < T_A < +85°C, unless otherwise noted. Typical specifications apply at T_A = +25°C.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
AUDIO PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		5.2		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.5		pA/√Hz
Signal-To-Noise Ratio	SNR	20 Hz to 20 kHz, 0 dBu = 0.775 V rms		121		dBu
Headroom	HR	Clip Point = 1% THD+N, f = 1 kHz, R_L = 10 kΩ		5.3		dBu
Total Harmonic Distortion	THD+N	A_V = +1, V_O = 1 V p-p, f = 1 kHz, 80 kHz LPF				
		R_L = 10 kΩ		0.003		%
		R_L = 32 Ω		0.005		%
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ, T_A = 25°C	0.6	0.9		V/µs
Gain Bandwidth Product	GBW			3.5		MHz
Settling Time	t_S	To 0.1%, 2 V Step		5.8		µs
INPUT CHARACTERISTICS						
Input Voltage Range	V_{CM}		0		4.0	V
Input Offset Voltage	V_{OS}	V_{OUT} = 2 V		0.2	2.0	mV
Input Bias Current	I_B	V_{CM} = 0 V, V_{OUT} = 2 V		300	750	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V, V_{OUT} = 2 V			50	nA
Differential Input Impedance	Z_{IN}			4		MΩ
Common-Mode Rejection	CMR	0 V ≤ V_{CM} ≤ 4 V, f = dc	87	112		dB
Large Signal Voltage Gain	A_{VO}	0.01 V ≤ V_{OUT} ≤ 3.9 V, R_L = 600 Ω	2			V/µV
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	R_L = 100 kΩ	4.1			V
		R_L = 600 Ω	3.9			V
Output Voltage Swing Low	V_{OL}	R_L = 100 kΩ			3.5	mV
		R_L = 600 Ω			3.0	mV
Short Circuit Current Limit	I_{SC}			±30		mA
POWER SUPPLY						
Supply Voltage Range	V_S	Single Supply	4		36	V
		Dual Supply	±2		±18	V
Power Supply Rejection Ratio	PSRR	V_S = 4 V to 6 V, f = dc	90	120		dB
Supply Current	I_{SY}	V_{OUT} = 2.0 V, No Load				
		V_S = 5 V		2.8	6.0	mA
		V_S = ±18 V, V_{OUT} = 0 V, No Load		3.7	7.6	mA

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Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- Single Supply . . . . . 36 V
- Dual Supply . . . . . ±18 V

Input Voltage . . . . . $\pm V_S$
Differential Input Voltage . . . . . 10 V
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range . . . . . –65°C to +150°C
Operating Temperature Range . . . . . –40°C to +85°C
Junction Temperature Range (T_J) . . . . . –65°C to +150°C
Lead Temperature (Soldering, 60 sec) . . . . . 300°C

ESD RATINGS

883 (Human Body) Model . . . . . 1 kV
EIAJ Model . . . . . 175 V

THERMAL CHARACTERISTICS

Thermal Resistance*		
8-Lead SOIC	θ_{JA} θ_{JC}	158°C/W 43°C/W

*θ_{JA} is specified for worst case conditions, i.e., θ_{JA} is specified for device soldered in circuit board for SOIC package.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
SSM2135S	–40°C to +85°C	8-Lead SOIC	SOIC-8

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the SSM2135 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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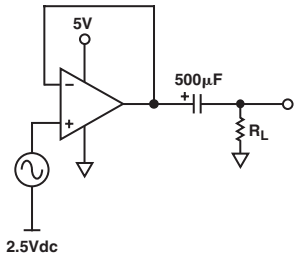
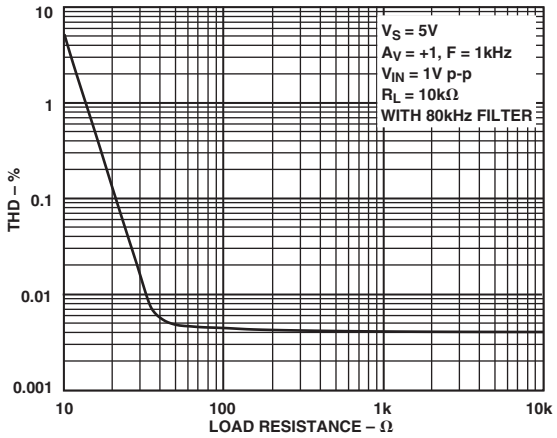
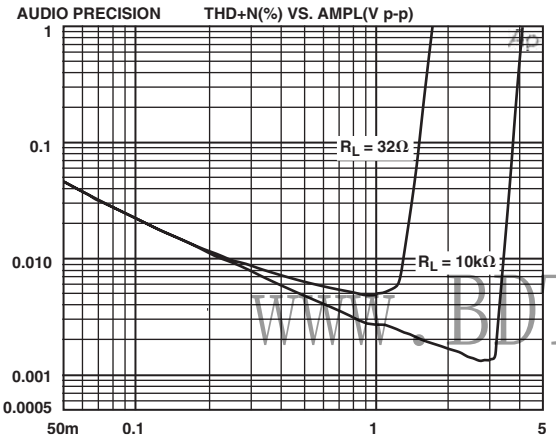
SSM2135–Typical Performance Characteristics



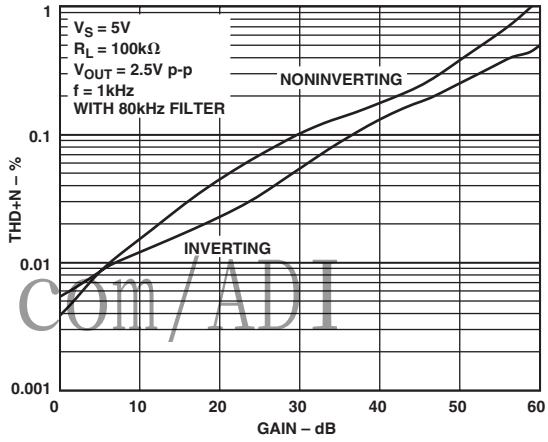
Test Circuit 1. Test Circuit for TPCs 1, 2, and 3



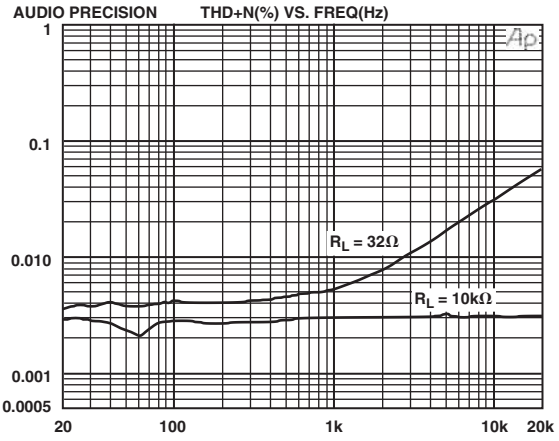
TPC 3. THD+N vs. Load (See Test Circuit)



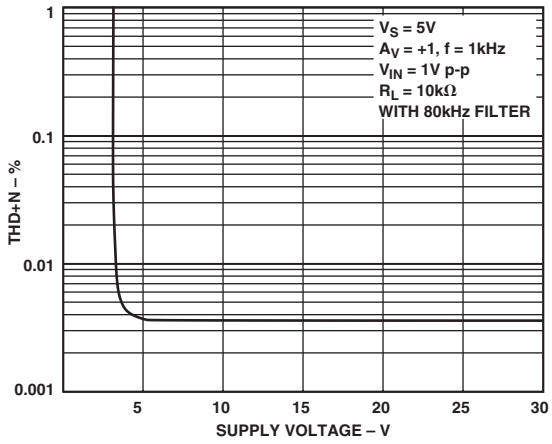
TPC 1. THD+N vs. Amplitude (See Test Circuit 1; A_V = +1, V_S = 5 V, f = 1 kHz, with 80 kHz Low-Pass Filter)



TPC 4. THD+N vs. Gain



TPC 2. THD+N vs. Frequency (See Test Circuit 1; A_V = +1, V_{IN} = 1 V p-p, with 80 kHz Low-Pass Filter)



TPC 5. THD+N vs. Supply Voltage

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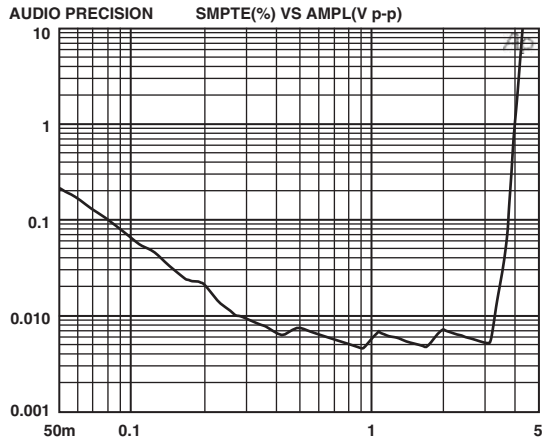
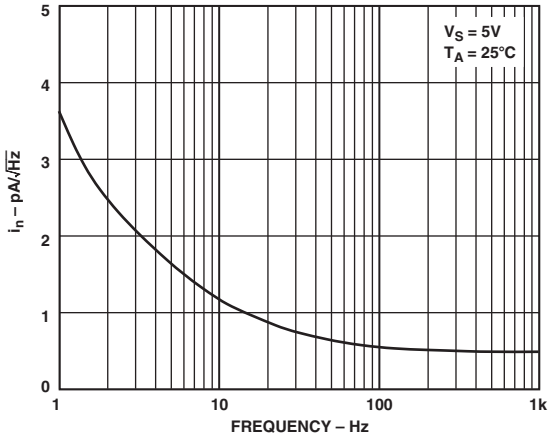
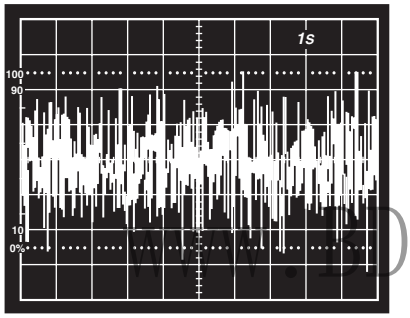


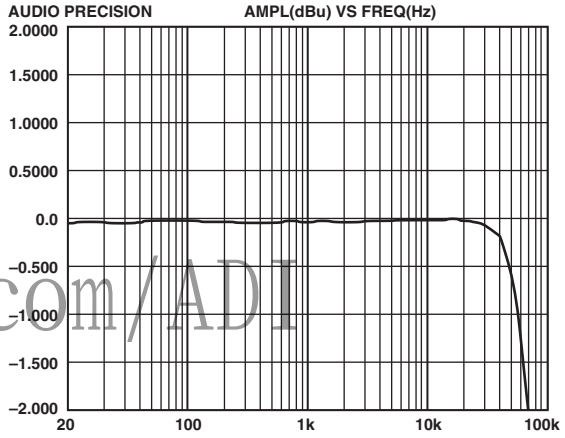
TPC 6. SMPTE Intermodulation Distortion (A_V = +1, V_S = 5 V, f = 1 kHz, R_L = 10 kΩ)



TPC 9. Current Noise Density vs. Frequency



TPC 7. Input Voltage Noise (20 nV/div)



TPC 10. Frequency Response (A_V = +1, V_S = 5 V, V_{IN} = 1 V p-p, R_L = 10 kΩ)

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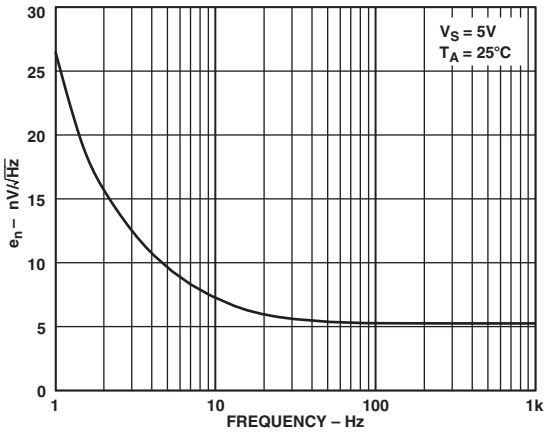
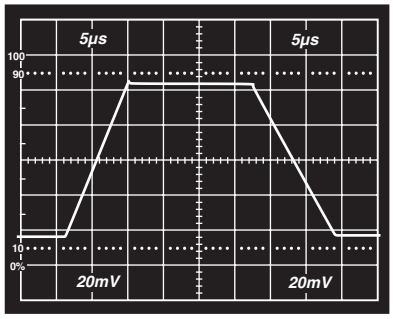
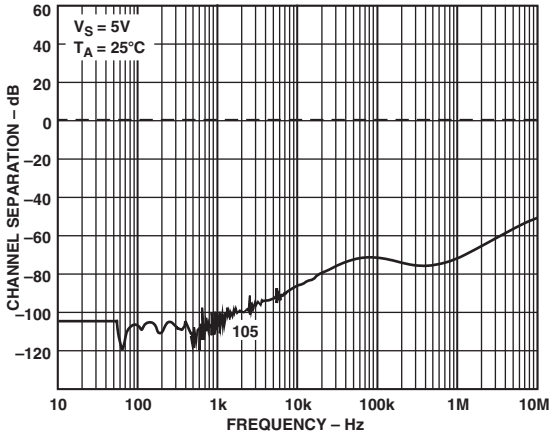


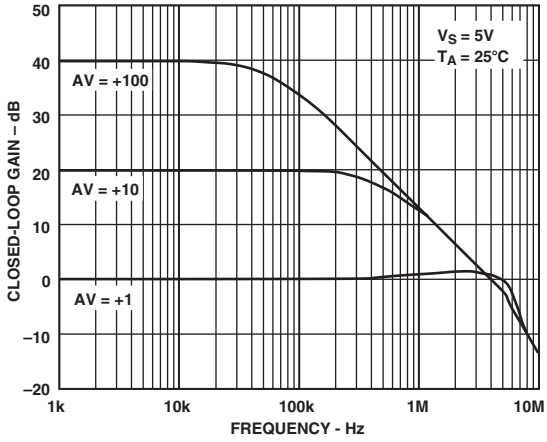
TPC 8. Voltage Noise Density vs. Frequency



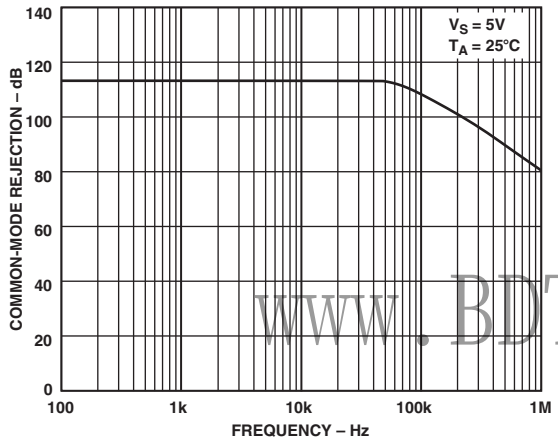
TPC 11. Square Wave Response (V_S = 5 V, A_V = +1, R_L = ∞)



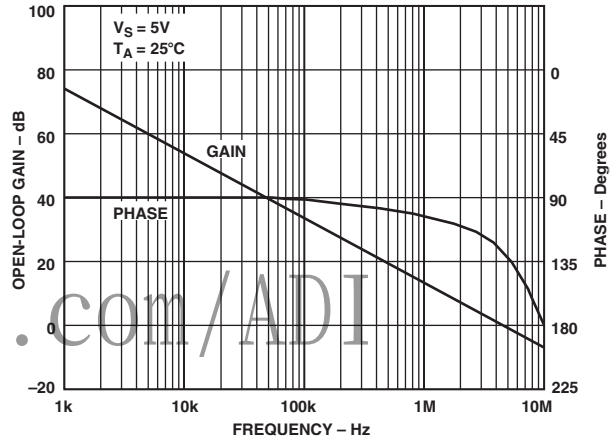
TPC 12. Crosstalk vs. Frequency (R_L = 10 kΩ)



TPC 15. Closed-Loop Gain vs. Frequency



TPC 13. Common-Mode Rejection vs. Frequency



TPC 16. Open-Loop Gain and Phase vs. Frequency

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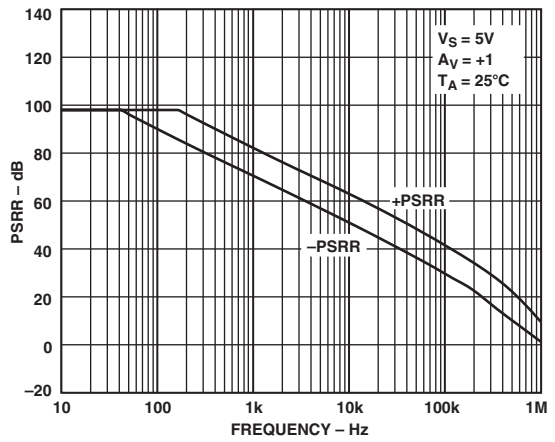
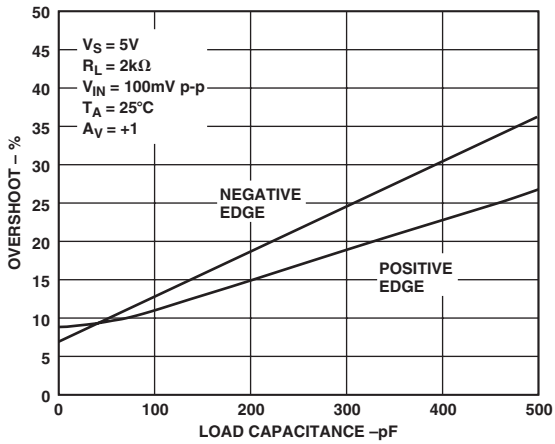
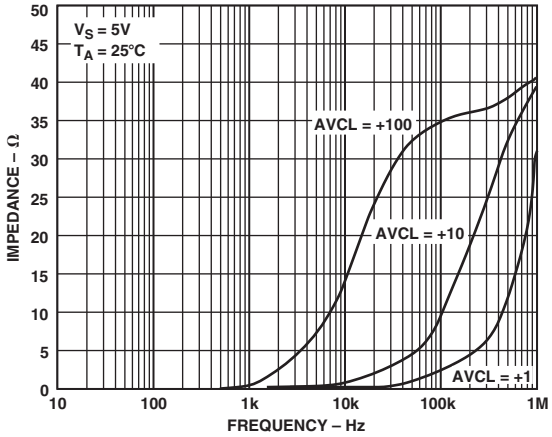


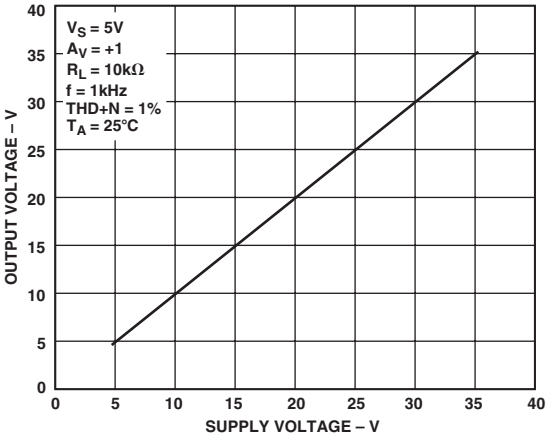
TPC 14. Power Supply Rejection vs. Frequency



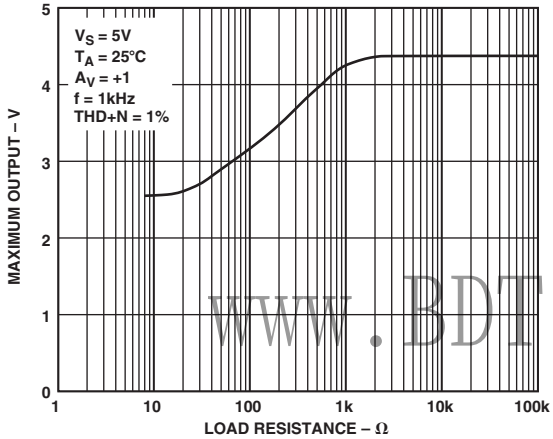
TPC 17. Small Signal Overshoot vs. Load Capacitance



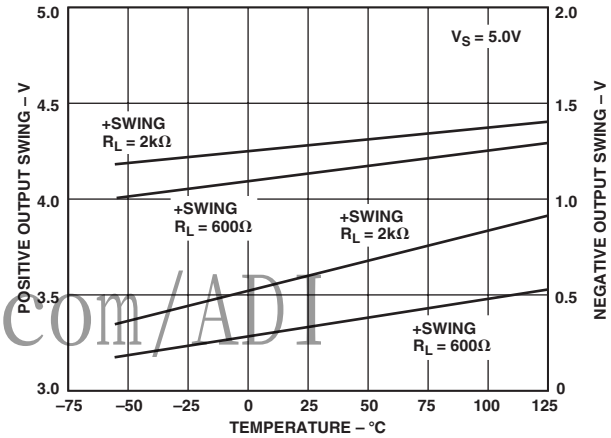
TPC 18. Output Impedance vs. Frequency



TPC 21. Output Swing vs. Supply Voltage



TPC 19. Maximum Output Voltage vs. Load Resistance



TPC 22. Output Swing vs. Temperature and Load

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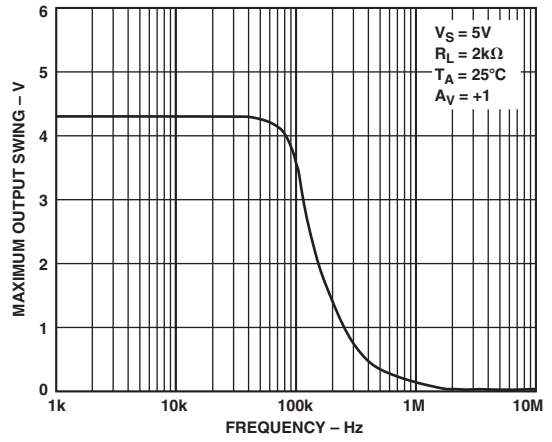
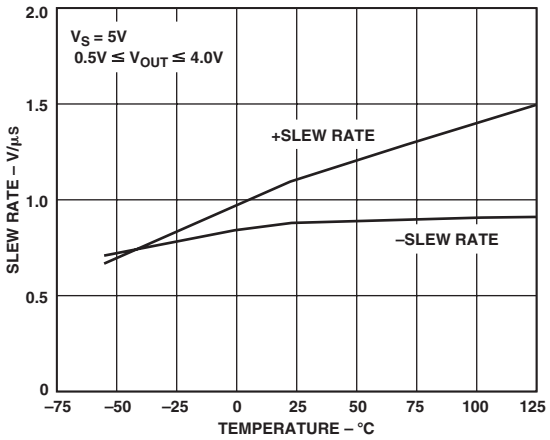
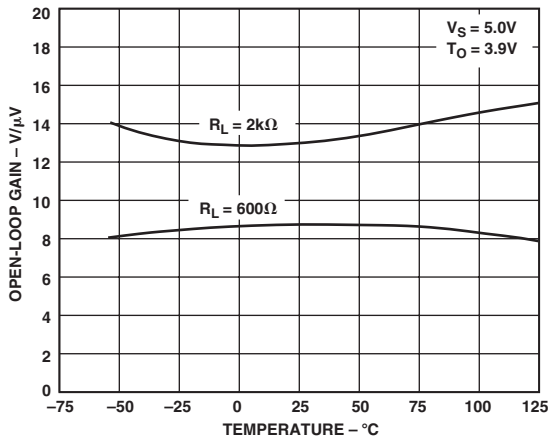


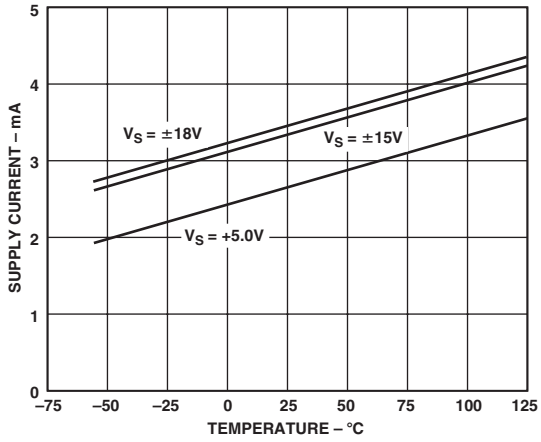
TPC 20. Maximum Output Swing vs. Frequency



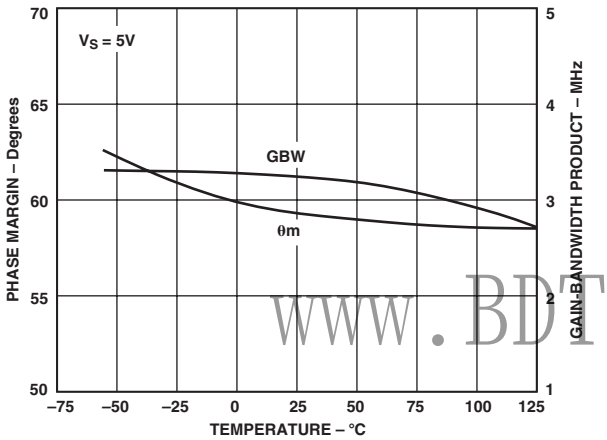
TPC 23. Slew Rate vs. Temperature



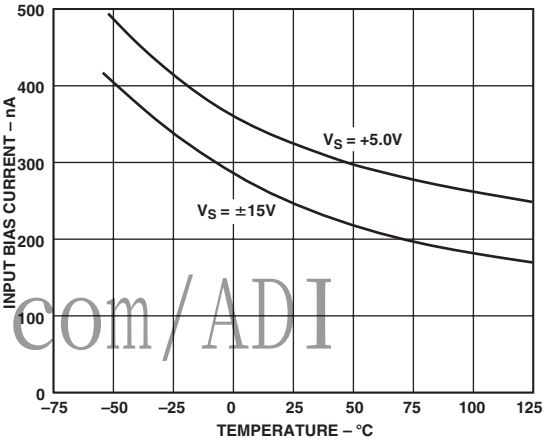
TPC 24. Open-Loop Gain vs. Temperature



TPC 26. Supply Current vs. Temperature



TPC 25. Gain Bandwidth Product and Phase Margin vs. Temperature



TPC 27. Input Bias Current vs. Temperature

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APPLICATION INFORMATION

The SSM2135 is a low voltage audio amplifier that has exceptionally low noise and excellent sonic quality even when driving loads as small as 25 Ω. Designed for single supply use, the SSM2135's inputs common-mode and output swing to 0 V. Thus with a supply voltage at 5 V, both the input and output will swing from 0 V to 4 V. Because of this, signal dynamic range can be optimized if the amplifier is biased to a 2 V reference rather than at half the supply voltage.

The SSM2135 is unity-gain stable, even when driving into a fair amount of capacitive load. Driving up to 500 pF does not cause any instability in the amplifier. However, overshoot in the frequency response increases slightly.

The SSM2135 makes an excellent output amplifier for 5 V only audio systems such as a multimedia workstation, a CD output amplifier, or an audio mixing system. The amplifier has large output swing even at this supply voltage because it is designed to swing to the negative rail. In addition, it easily drives load impedances as low as 25 Ω with low distortion.

The SSM2135 is fully protected from phase reversal for inputs going to the negative supply rail. However, internal ESD protection diodes will turn on when either input is forced more than 0.5 V below the negative rail. Under this condition, input current in excess of 2 mA may cause erratic output behavior, in which case a current limiting resistor should be included in the offending input if phase integrity is required with excessive input voltages. A 500 Ω or higher series input resistor will prevent phase inversion even with the input pulled 1 V below the negative supply.

"Hot" plugging the input to a signal generally does not present a problem for the SSM2135, assuming the signal does not have any voltage exceeding the device's supply voltage. If so, it is advisable to add a series input resistor to limit the current, as well as a Zener diode to clamp the input to a voltage no higher than the supply.

APPLICATION CIRCUITS

Low Noise Stereo Headphone Driver Amplifier

Figure 1 shows the SSM2135 used in a stereo headphone driver for multimedia applications with the AD1848, a 16-bit stereo codec. The SSM2135 is equally well suited for the serial-bused AD1849 stereo codec. The headphone's impedance can be as low as 25 Ω, which covers most commercially available high fidelity headphones. Although the amplifier can operate at up to ±18 V supply, it is just as efficient powered by a single 5 V. At this voltage, the amplifier has sufficient output drive to deliver distortion-free sound to a low impedance headphone.

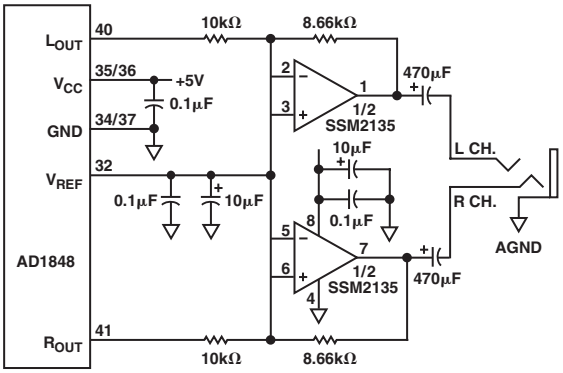

Figure 1. A Stereo Headphone Driver for Multimedia Sound Codec

Figure 2 shows the total harmonic distortion characteristics versus frequency driving into a 32 Ω load, which is a very typical impedance for a high quality stereo headphone. The SSM2135 has excellent power supply rejection, and as a result, is tolerant of poorly regulated supplies. However, for best sonic quality, the power supply should be well regulated and heavily bypassed to minimize supply modulation under heavy loads. A minimum of 10 µF bypass is recommended.

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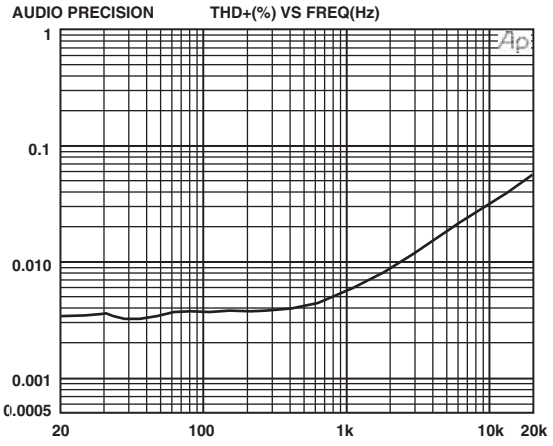

Figure 2. Headphone Driver THD+N vs. Frequency into a 32 Ω Load (V_S = 5 V, with 80 kHz Low-Pass Filter)

Low Noise Microphone Preamplifier

The SSM2135's 4.7 nV/√Hz input noise in conjunction with low distortion makes it an ideal device for amplifying low level signals such as those produced by microphones. Figure 3 illustrates a stereo microphone input circuit feeding a multimedia sound codec. As shown, the gain is set at 100 (40 dB), although it can be set to other gains depending on the microphone output levels. Figure 4 shows the preamplifier's harmonic distortion performance with 1 V rms output while operating from a single 5 V supply.

The SSM2135 is biased to 2.25 V by the V_{REF} pin of the AD1848 codec. The same voltage is buffered by the 2N4124 transistor to provide "phantom power" to the microphone. A typical electret condenser microphone with an impedance range of 100 Ω to 1 kΩ works well with the circuit. This power booster circuit may be omitted for dynamic microphone elements.

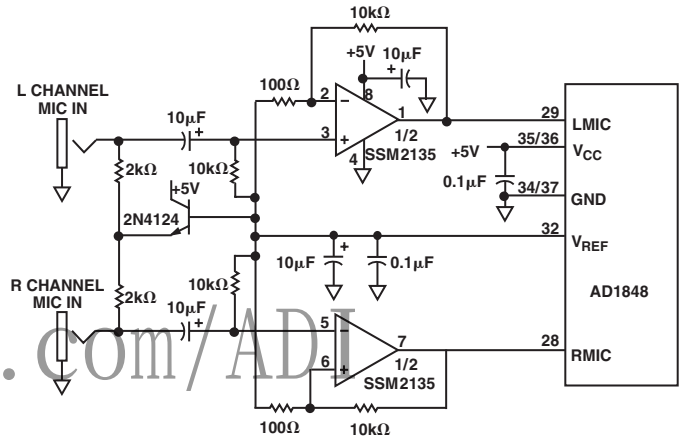

Figure 3. Low Noise Microphone Preamp for Multimedia Sound Codec

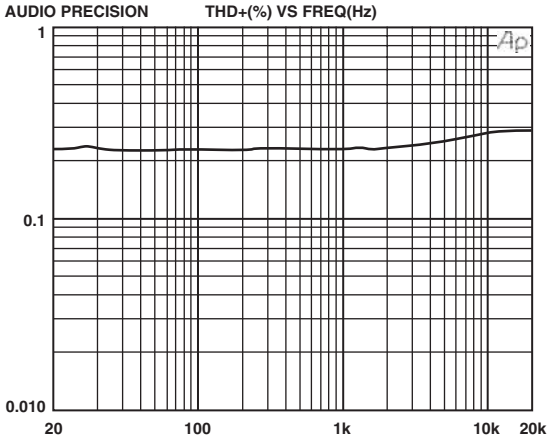

Figure 4. MIC Preamp THD+N Performance (V_S = 5 V, A_V = 40 dB, V_{OUT} = 1 V rms, with 80 kHz Low-Pass Filter)

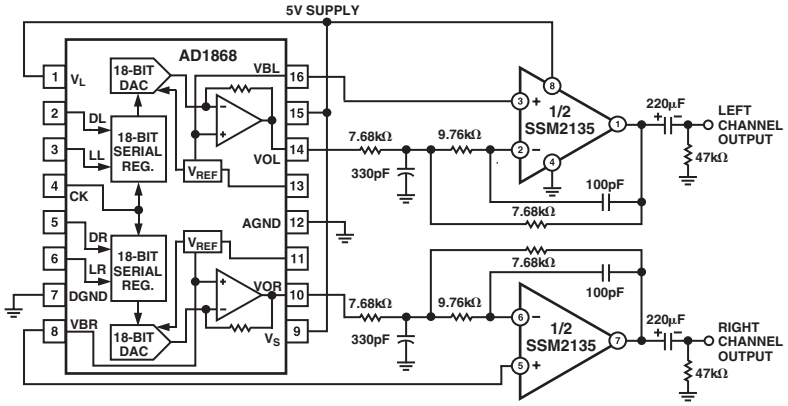

Figure 5. 5 V Stereo 18-Bit DAC

18-Bit Stereo CD-DAC Output Amplifier

The SSM2135 makes an ideal single-supply stereo output amplifier for audio D/A converters because of its low noise and distortion. Figure 5 shows the implementation of an 18-bit stereo DAC channel. The output amplifier also provides low-pass filtering for smoothing the oversampled audio signal. The filter's cutoff frequency is set at 22.5 kHz and has a maximally flat response from dc to 20 kHz.

As mentioned above, the amplifier's outputs can drive directly into a stereo headphone that has impedance as low as 25 Ω with no additional buffering required.

Single Supply Differential Line Driver

Signal distribution and routing is often required in audio systems, particularly portable digital audio equipment for professional applications. Figure 6 shows a single supply line driver circuit that has differential output. The bottom amplifier provides a 2 V dc bias for the differential amplifier in order to maximize the output swing range. The amplifier can output a maximum of 0.8 V rms signal with a 5 V supply. It is capable of driving into 600 Ω line termination at a reduced output amplitude.

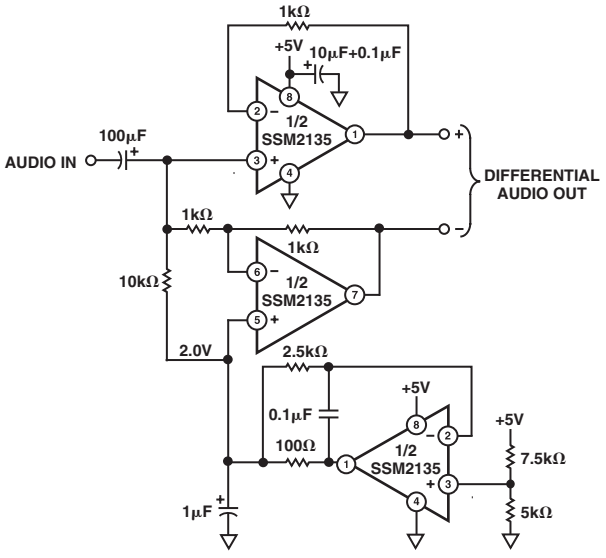

Figure 6. Single-Supply Differential Line Driver

Single-Supply Differential Line Receiver

Receiving a differential signal with minimum distortion is achieved using the circuit in Figure 7. Unlike a difference amplifier (a subtractor), the circuit has a true balanced input impedance regardless of input drive levels. That is, each input always presents a 20 kΩ impedance to the source. For best common-mode rejection performance, all resistors around the differential amplifier must be very well matched. Best results can be achieved using a 10 kΩ precision resistor network.

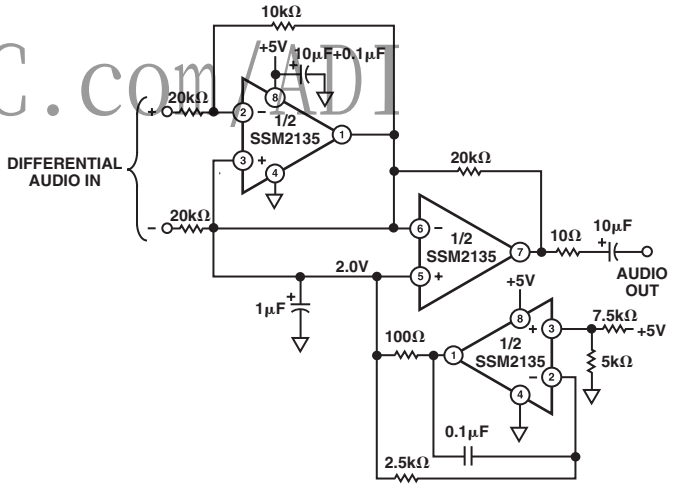

Figure 7. Single-Supply Balanced Differential Line Receiver

Pseudo-Reference Voltage Generator

For single-supply circuits, a reference voltage source is often required for biasing purposes or signal offsetting purposes. The circuit in Figure 8 provides a supply splitter function with low output impedance. The 1 µF output capacitor serves as a charge reservoir to handle a sudden surge in demand by the load as well as providing a low ac impedance to it. The 0.1 µF feedback capacitor compensates the amplifier in the presence of a heavy capacitive load, maintaining stability.

The output can source or sink up to 12 mA of current with a 5 V supply, limited only by the 100 Ω output resistor. Reducing the resistance will increase the output current capability. Alternatively, increasing the supply voltage to 12 V also improves the output drive to more than 25 mA.

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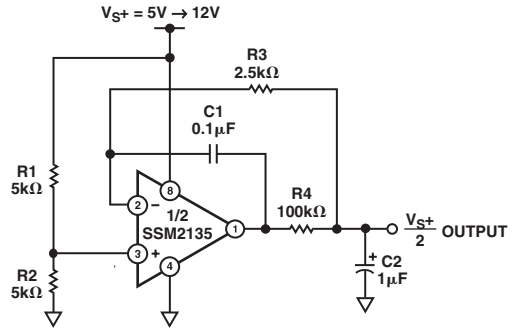

Figure 8. Pseudo-Reference Generator

Digital Volume Control Circuit

Working in conjunction with the AD7528/PM7528 dual 8-bit D/A converter, the SSM2135 makes an efficient audio attenuator, as shown in Figure 9. The circuit works off a single 5 V supply. The DACs are biased to a 2 V reference level, which is sufficient to keep the DACs' internal R-2R ladder switches operating properly. This voltage is also the optimal midpoint of the SSM2135's common-mode and output swing range. With the circuit as shown, the maximum input and output swing is 1.25 V rms. Total harmonic distortion measures a respectable 0.01% at 1 kHz and 0.1% at 20 kHz. The frequency response at any attenuation level is flat to 20 kHz.

Each DAC can be controlled independently via the 8-bit parallel data bus. The attenuation level is linearly controlled by the binary weighting of the digital data input. Total attenuation ranges from 0 dB to 48 dB.

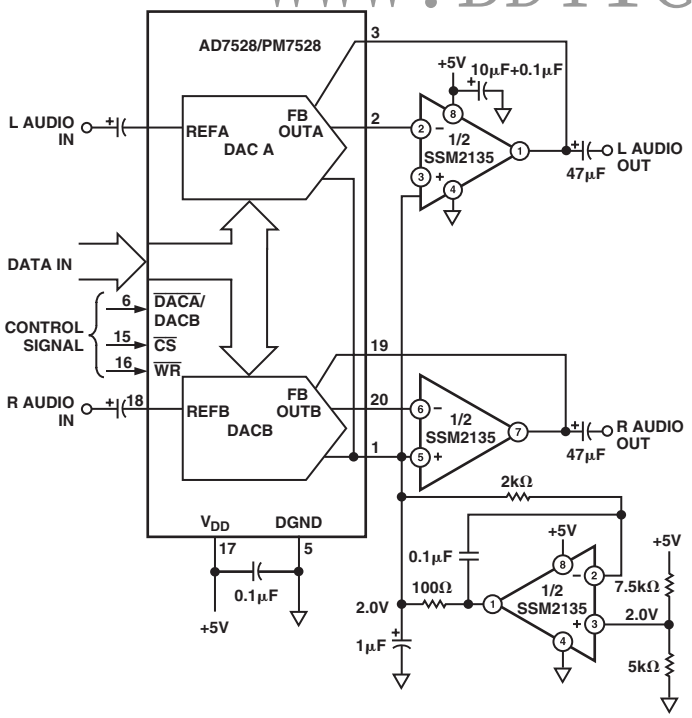

Figure 9. Digital Volume Control

Logarithmic Volume Control Circuit

Figure 10 shows a logarithmic version of the volume control function. Similar biasing is used. With an 8-bit bus, the AD7111 provides an 88.5 dB attenuation range. Each bit resolves a 0.375 dB attenuation. Refer to the AD7111 data sheet for attenuation levels for each input code.

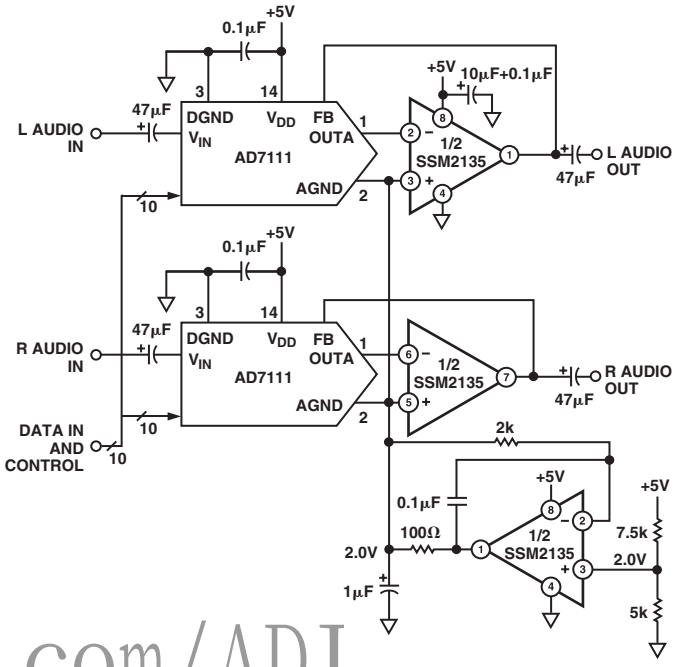

Figure 10. Single-Supply Logarithmic Volume Control

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SPICE MACROMODEL

```
*SSM2135 SPICE Macro-Model      9/92, Rev. A
*                               JCB/ADI
*Copyright 1993 by Analog Devices, Inc.
*
*Node Assignments
*
*                          Noninverting Input
*                          |    Inverting Input
*                          |    |    Positive Supply
*                          |    |    |    Negative Supply
*                          |    |    |    |    Output
*                          |    |    |    |    |
.SUBCKT SSM2135            3    2    7    4    6
*
* INPUT STAGE
R3      4     19    1.5E3
R4      4     20    1.5E3
C1      19    20    5.311E–12
I1      7     18    106E–6
IOS     2     3     25E–09
EOS     12    5     POLY(1)   51   4    25E–06   1
Q1      19    3     18        PNP1
Q2      20    12    18        PNP1
CIN     3     2     3E–12
D1      3     1     DY
D2      2     1     DY
EN      5     2     22        0    1
GN1     0     2     25        0    1E–5
GN2     0     3     28        0    1E–5
*
* VOLTAGE NOISE SOURCE WITH FLICKER NOISE
DN1     21    22    DEN
DN2     22    23    DEN
VN1     21    0     DC 2
VN2     0     23    DC 2
*
* CURRENT NOISE SOURCE WITH FLICKER NOISE
DN3     24    25    DIN
DN4     25    26    DIN
VN3     24    0     DC 2
VN4     0     26    DC 2
*
* SECOND CURRENT NOISE SOURCE
DN5     27    28    DIN
DN6     28    29    DIN
VN5     27    0     DC 2
VN6     0     29    DC 2
*
* GAIN STAGE & DOMINANT POLE AT .2000E+01 HZ
G2      34    36    19        20   2.65E–04
R7      34    36    39E+06
V3      35    4     DC        6
D4      36    35    DX
VB2     34    4     1.6
*
* SUPPLY/2 GENERATOR
ISY     7     4     0.2E–3
R10     7     60    40E+3
R11     60    4     40E+3
C3      60    0     1E–9
*
* CMRR STAGE & POLE AT 6 kHZ
ECM     50    4     POLY(2)   3    60   2    60   0    1.6  1.6
CCM     50    51    26.5E–12
RCM1    50    51    1E6
RCM2    51    4     1
*
*
OUTPUT STAGE
R12  37   36   1E3
R13  38   36   500
C4   37   6    20E–12
C5   38   39   20E–12
M1   39   36   4  4 MN L=9E–6 W=1000E–6 AD=15E–9 AS=15E–9
M2   45   36   4  4 MN L=9E–6 W=1000E–6 AD=15E–9 AS=15E–9
5    39   47   DX
D6   47   45   DX
Q3   39   40   41   QPA 8
VB   7    40   DC  0.861
R14  7    41   375
Q4   41   7    43   QNA 1
R17  7    43   15
Q5   43   39   6    QNA 20
Q6   46   45   6    QPA 20
R18  46   4    15
Q7   36   46   4    QNA 1
M3   6    36   4  4 MN L=9E–6 W=2000E–6 AD=30E–9 AS=30E–9
*
* NONLINEAR MODELS USED
*
.MODEL DX D (IS=1E–15)
.MODEL DY D (IS=1E–15 BV=7)
.MODEL PNP1 PNP (BF=220)
.MODEL DEN D(IS=1E–12 RS=1016 KF=3.278E–15 AF=1)
.MODEL DIN D(IS=1E–12 RS=100019 KF=4.173E–15 AF=1)
.MODEL QNA NPN(IS=1.19E–16 BF=253 VAF=193 VAR=15 RB=2.0E3
+ IRB=7.73E–6 RBM=132.8 RE=4 RC=209 CJE=2.1E–13 VJE=0.573
+ MJE =0.364 CJC=1.64E–13 VJC=0.534 MJC=0.5 CJS=1.37E–12
+ VJS=0.59 MJS=0.5 TF=0.43E–9 PTF=30)
.MODEL QPA PNP(IS=5.21E–17 BF=131 VAF=62 VAR=15 RB=1.52E3
+ IRB=1.67E 5–RBM=368.5 RE=6.31 RC=354.4 CJE=1.1E–13
+ VJE=0.745 MJE=0.33 CJC=2.37E–13 VJC=0.762 MJC=0.4
+ CJS=7.11E–13 VJS=0.45 MJS=0.412 TF=1.0E–9 PTF=30)
.MODEL MN NMOS(LEVEL=3 VTO=1.3 RS=0.3 RD=0.3 TOX=8.5E–8
+ LD=1.48E–6WD=1E–6 NSUB=1.53E16UO=650 DELTA= 10VMAX=2E5
+ XJ=1.75E–6 KAPPA=0.8 ETA=0.066 THETA=0.01TPG=1 CJ=2.9E–4
+ PB=0.837 MJ=0.407 CJSW=0.5E–9 MJSW=0.33)
*
.ENDS SSM-2135
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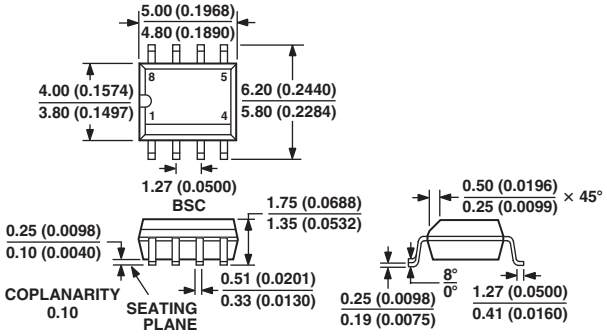
OUTLINE DIMENSIONS

8-Lead Standard Small Outline Package [SOIC]
Narrow Body
(R-8)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

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Revision History

Location	Page
2/03—Data Sheet changed from REV. D to REV. E.	
Removed 8-Lead Plastic DIP Package	Universal
Edits to THERMAL CHARACTERISTICS	3
Edits to ORDERING GUIDE	3
Updated OUTLINE DIMENSIONS	13

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